ITER Fast Plant System Controller Prototype Based on PXI Platform

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ITER Organization
Outline

- Project scope and requirements.
- FPSC HW elements.
- FPSC SW elements.
  - Applications running in the controller.
  - Data acquisition. FPSC control using EPICS PVs
  - Streaming/archiving applications
- Conclusions.
Project Scope and requirements

- ITER CODAC Design identifies two types of Plant System Controllers (PSC):
  - Slow PSC is based on industrial automation technology (control loops rates <1 kHz).
  - The Fast PSC is based on embedded technology with higher sampling rates and more stringent real-time requirements.

- Essentials requirements of FPSC:
  - Data acquisition and preprocessing
  - Interfacing with the networks (PON, TCN, SDN, streaming/archiving networks)
  - LINUX OS and EPICS IOC. System setup and operation using process variables.
  - COTS solutions.

- Developing a prototype FPSC targeting Data Acquisition for ITER IO
  - Two different form factors for the implementation:
    - ATCA based solution (IST)
    - PCIe based solution (CIEMAT/UPM)
  - A two steps approach: Alpha and Beta version.
ATCA form factor (IST/IPFN): Alpha version

CODAC
- HMI
- CODAC systems
- Central database

Fusion Experiment

Diagnostics
- PCIe bus extension
- Fast Plant System Controller

Actuators
- IO shelf
- Network cards

1588 Master clock
- Time Communication Network (TCN)

1588 switch

Synchronous Database Network (SDN)

Scientific Data Archiving (SDA)

High Performance Computers

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PXI form factor: alpha version

- Requirements
  - Hardware: COTS
  - Software: Linux RHEL 64 bits & EPICS

- Issues (2010)
  - The drivers (and device support) are not available under Linux 64 bits
    - Other people in charge of the development
    - Greatly complicated development to be finished in a limited time

- Solution for alpha version:
  - Labview Real Time based (to avoid third parties dependences, to test system capabilities and to learn about problems and gain experience for the beta version)
  - PXIe solution using:
    - National Instruments hardware (PXI chassis, timing modules, DAQ using FlexRIO and external controller)
    - LabVIEW RT Module applications running in the controller
    - LabVIEW FPGA for FlexRIO
    - LabVIEW EPICS IOC for real time target for supporting channel access.
    - Specific application developed running in external computers for streaming/archiving, data processing with GPUs, and monitoring using ITER CODAC Core System.
Development tools

PFSC
System Controller CPU

LabVIEW
Real-Time

NI 8353 RT

172.17.152.11

DEVELOPMENT HOST

MiniCODAC

172.17.152.40

Data Archiving servers

miniCODAC
PC Desktop

172.17.152.52

Real Time Controller

19

1U Chasis

NI 8353 RT

PXI Clk10

172.17.152.13

ETHERNET

NI PXI-7952R

ETHERNET

NI PXI-6682
NI PXI-6683

NI PXI-6653

172.17.152.13

Development tools

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FPSC software elements

Archiver Service

d1wave and event files

NFS

FPSC Labview RT

Archiver Service

Development System

Signal Generator

LabVIEW 2010

EPICS IOC

archiver

service

d1wave

and event

files

NFS

FPSC software elements

CODAC State Machine

CODAC IOC

IOC Log Service

Configuration Management

Archiving monitoring

Archive Viewer

Pulse Control

LabVIEW 2010

CODAC IOC

iodLog Service

Configuration Management

Archiving monitoring

Archive Viewer

Pulse Control

CODAC State Machine

CODAC IOC

iodLog Service

Configuration Management

Archiving monitoring

Archive Viewer

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china eu india japan korea russia usa
FPSC software elements

- Archiver Service
- Archiver Service
- d1wave and event files
- NFS
- EPICS IOC
- EPICS IOC
- EPICS IOC
- EPICS IOC
- EPICS IOC
- FPSC Labview RT
- FPSC GPU System
- CODAC State Machine
- CODAC IOC
- iocLog Service
- Configuration Management
- Archiving monitoring
- Pulse Control
- Signal Generator
- Development System

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FPSC applications running in NI8353 computer

- **LabVIEW Modules implemented:**
  - **CORE.** General queues management. Creation, destruction and state machine control.
  - **EPICS-IOC.** Channel access and PVs management.
  - **TCN.** Management of PXI6653 and PXI6682 for clock generation and event time-stamping.
    - PXI CLK 10MHz is in phase with PXI6682 IEEE1588 clock
  - **ACQ.** Data acquisition and selection.
  - **FPGADAC.** Data acquisition application for RIO devices with time-stamping. Also include a signal simulator (inside FPGA) for debugging purposes.
  - **EVT.** Event management. **SDN.** Implemented using NI-Time Triggered Variables
  - **RTP.** Real time processing. Basic algorithms. **RTPGPU.** GPU management.

![Diagram of Fast Plant System Controller: Alpha version DEMO](image-url)
Main features of FPSC software

- **ADQ parameters** are controlled & changed using PVs (also during the pulse):
  - Sampling rate and block size for FlexRIO device.
  - Decimation factor and modes (samples and blocks) for EPICS monitoring.
- **FPSC State machine control and status** using PVs: start/stop, memory used, CPU load, etc.
- **Acquired data** can be sent to streaming, monitoring with EPICS, real-time processing and GPU using «FANOUT PVs».
- **Preprocessing algorithms** can be dynamically selected using PVs.
FPSC software elements

Development System

Signal Generator

CODAC State Machine
CODAC IOC
iocLog Service
Configuration Management
Archiving monitoring

Pulse Control

Archiver Service

EPICS IOC

d1wave and event files

EPICS IOC

FPSC Labview RT

FPSC GPU System

EPICS IOC

FPSC software elements

FPGA

NFS

Archive Viewer

LabVIEW 2010

EPICS IOC

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GUI using EDM (EPICS), LOG and states machine

- Manual start/stop of FPSC
- Basic control of PVs during the pulse.
- Implementation of IocLog client in LabVIEW
- IOC with the pulse states machine and configuration management (XML files)
FPSC software elements

Development System

Signal Generator

CODAC State Machine
CODAC IOC
IOC Log Service
Configuration Management
Archiving monitoring

LabVIEW 2010

EPICS IOC

FPSC Labview RT

FPSC GPU System

d1wave and event files

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FPSC software elements

Archiver Service

FPSC software elements

Archiver Service

Archive Viewer

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Data sources can be assigned to data archivers

**netCDF** file is the fundamental storage unit

A file per data source (signal) and pulse

Two types of data are currently implemented: “d1wave” and “event”.

EPICS IOC currently used for monitoring
Archiving Viewer and monitoring

- “Online” and “Offline” mode
- On remote via NFS (Network File System)
- Time slice positioning
- Self Description data visualization
- Flexible plotter
  - Zooms
  - Export options
- Completely based on EPICS channel access
  - Every archiver implements its own EPICS IOC
- System variables:
  - CPU load
  - Memory Usage
- Archiving system performance
  - Receiving data rate per channel
  - Total received data rate
  - Storing data rate per channel
  - Total saved data rate
Conclusions

- Implementation of a basic FPSC devoted to data acquisition following essential ITER requirements:
  - “Intelligent data acquisition” using FPGA DAQ devices with IEEE-1588 time-stamping.
  - System DAQ parameters controlled by EPICS’ PVs (changed dynamically during the PULSE)
  - Streaming capabilities.
  - Preprocessing algorithms using local processor and GPU (controlled with EPICS PVs).
  - Integration with EPICS CODAC system (v1.1).
  - 100kS/s per channel with streaming, time-stamping, EPICS monitoring, and 2 channels preprocessing

- LabVIEW based tools (RT/FPGA) have been a good choice for quick prototyping in a short period of time (3 months).
  - Graphical oriented design simplifies: the definition of complex software models, the debugging of the different applications, and the test of complex hardware setups.
ITER Fast Plant System Controller
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Thank you for your attention!!

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