

## High Temperature Pulsed and DC Performance of AlInN/GaN HEMTs

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The AlGaN/GaN high-electron mobility transistors (HEMTs) have been considered as promising candidates for the next generation of high temperature, high frequency, high-power devices. The potential of GaN-based HEMTs may be improved using an AlInN barrier because of its better lattice match to GaN, resulting in higher sheet carrier densities without piezoelectric polarization [1]. This work has been focused on the study of AlInN HEMTs pulse and DC mode characterization at high temperature.

The devices were fabricated in III-V Labs [2]. Drain current ( $I_D$ ) and transconductance ( $g_m$ ) were measured from room temperature up to 500 K on devices with different geometry ( $L_G=250$  nm;  $W_G=2 \times 75$   $\mu\text{m}$ ,  $2 \times 100$   $\mu\text{m}$ , or  $8 \times 75$   $\mu\text{m}$ ). Pulsed  $V_{GS}$  measurements (gate lag) were done to evaluate the presence of trapping effects [3]. In addition, pulsed  $V_{DS}$  characterization was also carried out.

As with AlGaN-barrier HEMTs, the drain current of AlInN/GaN devices decreased at high temperature, due to reduction of the electron mobility and drift velocity [4]. However, unlike AlGaN barrier devices, these thermal effects on  $I_D$  and  $g_m$  values were not reversible (Fig. 1). This behaviour could be related to the increase of the gate leakage current. Gate lag measurements in Fig. 2 ( $\Delta V_{GS}=-6$  V, 1  $\mu\text{s}$  period up to DC) have shown the presence of traps, specially located either at the surface or in the barrier near the 2DEG [3]. On the other hand, pulsed  $V_{DS}$  measurements have shown an almost constant  $I_D$  independent of pulse width. In contrast, AlGaN/GaN HEMTs typically showed an increase in  $I_D$  as the duty cycle decreased. That increase in drain lag in AlInN/GaN HEMTs could correlate to the buffer trap density in our devices [3].

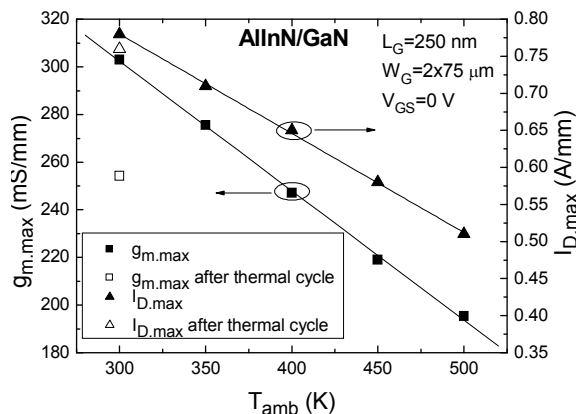


Figure 1. Trapping effects characterized by gate lag measurements.

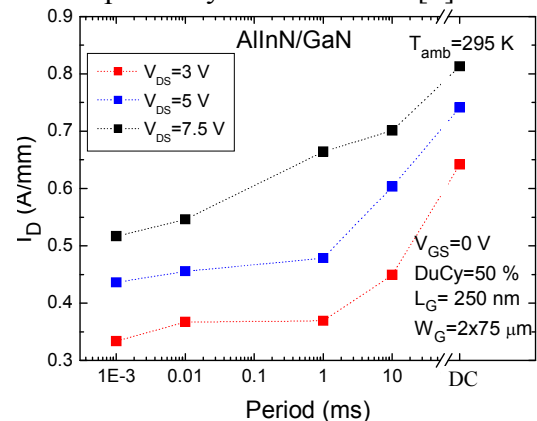


Figure 2. Gate lag measurements by means of  $V_{GS}$  pulsed characterization.

[1] F. Medjdoub, *et al.*, *IEEE Electr. Lett.*, Vol. 43, No. 5, pp. 71-72, March 2007.

[2] N. Sarazin, *et al.*, *IEEE Electr. Dev. Lett.*, Vol. 31, No. 1, pp. 11-13, January 2010

[3] A.P. Zhang, *et al.*, *Solid-State Electronics*, Vol 47, pp. 821-826, 2003.

[4] S. Martin-Horcajo, *et al.*, *WOCS DICE 2010*, May 2010

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