DIGITAL CHAOS ANALYSIS IN OPTICAL LOGIC STRUCTURES

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ABSTRACT

Digital chaotic behaviour in an Optically-Processing Element is analyzed. It was obtained as the result of processing two fixed train of bits. The process is performed with an Optically Programmable Logic Gate. Possible outputs, for some specific conditions of the circuit, are given. Digital chaotic behaviour is obtained, by using a feedback configuration. Different ways to analyze a digital chaotic signal are presented.

Keywords: Digital chaos, optical logic structures, optical chaos, Optically-Procesing Cell, Optical Computing.

1.- INTRODUCTION

Electronic circuits with chaotic behavior have been reported in the literature since the beginning of the Chaos Theory. After the well-known forced van der Pol oscillator, several other electronic families have shown different types of chaos being the most important the Chua's Circuit Family. Chua's circuit is regarded as a classical example of chaos for several reasons. First, it is the simplest autonomous circuit which can become chaotic. Second, it has been observed by computer simulation and verified by laboratory measurements. Finally, it has been the subject of several mathematical analyses and its chaotic nature has been rigorously proved. These facts give, according to M.J. Hasler[1], the only completely convincing evidence for chaotic behavior. As he points out, the chaotic behavior observed in the laboratory could be caused by some uncontrollable noise and computer simulations could be strongly distorted by the accumulation of round-off errors. Mathematical proofs cannot be refuted as such but a case can be made that a mathematical model of a circuit might fail to reproduce the behavior of the physical circuit itself. Hence, a concurrence of the three above mentioned results should be obtained in order to determine the existence of a real chaos.

Everyone of the above mentioned circuits have a common point: all of them are working in an analogical way being their outputs, as a consequence, analog signals. If a digital chaotic output is wanted, an analog-to-digital converter is needed and, hence, some additional circuitry has to appear in the system. It should be interesting to introduce new types of circuits showing direct digital chaotic outputs without any further modification. These type of circuits could be applied, for instance, in communications when some kind of random signal is required or in the case of sending information signals embedded in chaos. An example of this situation appears in [2].

Moreover, another point needs to be considered. It is the one related with the type of signals involved. Previous paragraphs have shown electronic circuits handling electric signals. It is obvious that if these circuits are to be employed in communications they should have to work with a type of signal equivalent to the one employed in the whole system. Optical communications are the first candidates to be the core of communications in the next future. Hence, photonic circuits should be needed to handle optical signals. A possible first approach to this problem is to convert electrical signals to optical, by conventional LEDs or LDs. This approach is, as a matter of fact, similar to the one adopted nowadays in Optical Communications where just the path from the emitter to the receiver is optical and the rest of the system is mainly electronic. But photonic circuits are going to be needed in the next years in some other areas, as switching, and some new concepts in this field have to be set down.

Optical circuits showing chaotic outputs are well-known since the beginning of the eighties. Several types of materials, devices and structures have been reported since then. Most of them are related with electro-optical bistable configurations, either

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hybrid or all-optical, with some delayed feedback. Under some circumstances, the output could become a chaotic one. A very good panoramic view of this area can be seen in[3].

A new approach is going to be reported in this paper. Because one of the main objectives of future Photonics is the possibility to have general purpose photonic integrated circuits, a multipurpose configuration should be required. This situation would give to Photonics the same character than Microelectronics has today. The configuration to be presented has been employed by us[4-8] to process two input binary signals being its two outputs logical functions of these inputs. The type of processing is related to the eight main Boolean Functions, namely, AND, OR, XOR, NAND, NOR, XNOR, ON and OFF. The programmable ability of these two outputs, as it has been described, allows the generation of several data-coding for optical data transmission. Moreover, a chaotic output has been obtained. In this paper, a computer simulation and some laboratory results are going to be reported as well as some mathematical justifications.

2.- OPTICAL CONFIGURATION OF THE OPTICALLY-PROGRAMMABLE DIGITAL CIRCUIT

The present optically-programmable digital circuit has been already reported[4-5] as a Programmable Logic Gate. A brief description on its working characteristics, as well as the way it has been practically implemented, will be summarized here. A major discussion that the reported previously, about the different possible devices to be employed and the transmission medium used for its physical implementation, will be presented in this work.

A block diagram of the circuit is show in Fig. 1. As it can be seen, the circuit is composed by two optical devices, P and Q, with a non-linear behaviour. The outputs of each one of them correspond to the two final outputs, O_1 and O_2, of the cell.

The possible inputs to the circuit are four. Two of them are input data, I_1 e I_2, and the other two, g and h, control signals. The way these four inputs are arranged inside the circuit, is also represented in Figure 1. The corresponding inputs to the non-linear devices, P and Q, are functions of these signals plus, in the case of the P device, one other signal coming from inside the own cell and obtained from the Q device output.

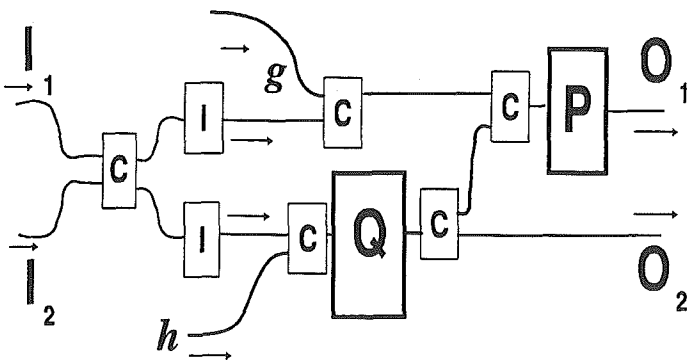

Fig. 1.- Basic configuration of the Optical Logic Structure. I: Isolators. C: Optical Couplers.

The practical implementation we have carried out of the processing element has been based on an optoelectronic configuration. Lines in Fig. 1 represent optical multimode fibers. The indicated blocks, placed in order to combine the corresponding signals, are conventional optical couplers. In this way, inputs arriving to the individual devices are multilevel signals. Isolators are added to eliminate backward signals and possible influences between P and Q. Working levels are:

$$I_P = (I_1 + I_2)/2 + g + O_2/2 \qquad (1)$$

for device P, and

$$I_Q = (I_1 + I_2)/2 + h \qquad (2)$$

for device Q. Output from device Q is divided into two equal intensity signals. One of them is one of the two final outputs and the other one becomes a part of the input to device P.

Therefore, the output of the P-device depends on the control signal g, plus one half of the output, O_2, of the Q-device. The output of the Q-device depends only on its control signal h. We understand as "output" the type of processing, or logical function, which executes each one of the devices on the two binary data inputs.

The characteristics of the non-linear devices are shown in Fig. 2. Device Q, corresponds to a thresholding or switching device, and device P is a multistate device, being the ideal response of this non-linear optical device the one represented in Fig. 2 with a dashed line. This response is similar to the one had by a SEED device. Because the input signal is a multilevel signal, as it can be seen from equations (1) - (2), the output depends on the relations between:

a) the level of a bit "1",

b) the level of the control signal, and

c) the level for switching from one state to another. This level is intrinsic to the employed device.

Some examples about how the possible outputs for each device can be obtained are given in[6].

Optical interconnections between elements are carried out by optical fibers. 1 x 2 couplers are the mixing signals elements. Because nonlinear all-optical devices, with enough high speed, were not available to us, non-linear devices **P** and **Q** were simulated by optoelectronic methods. Light coming to them was converted to an electrical signal and, by electronic circuitry, the nonlinear optical behaviour was simulated. The output of the circuit was again a light beam sent to the fiber. Multimode optical fibers have been employed and common LEDs have been used as light sources. No attempt was given to obtain high bit rates, but only the method validity.

Non-linear devices were carried out, experimentally, with an optoelectronic approximation. Their blocks diagram is shown in Fig. 3. Optical signal get a conventional photodiode and the resulting electrical signal is amplified to the adequate level. The resulting signal is electronically processed according to the type of function needed, an on-off for the Q-device and a SEED-like for the P. Finally, a third black-box corresponds to the new conversion from electrical to optical signal. Common LEDs were employed in this step. First and third blocks are identical for both devices. Just the central one, where the logic processing is done differs from P to Q.

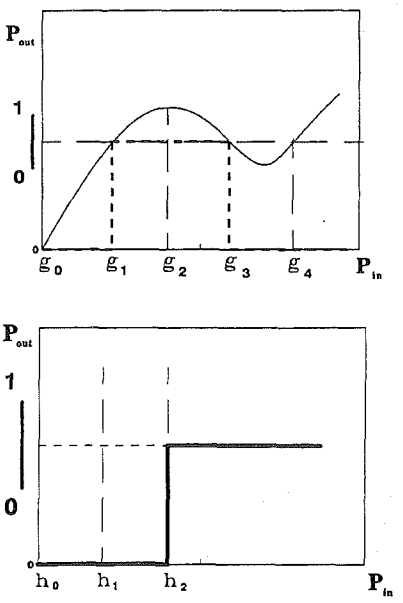

Fig. 2.- Behavior of SEED and On-Off devices.

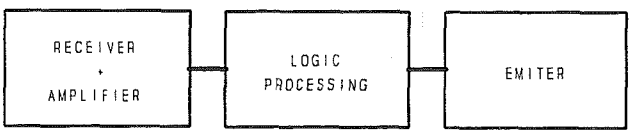

Fig. 3.- General diagram of the optoelectronic simulation for SEED and On-Off devices.

P device, according to the function has to perform, needs comparators in order to relate input signals to the P device with previously fixed values. Its electronic scheme is shown in Fig. 4. The four indicated comparators process the electrical input signal. Their reference levels are the decision levels adopted for P-device. Decision levels have to be adapted to the amplification level of the data electrical signal. The employed logic allows to discriminate the equality levels of input signal and decision level. Values of decision levels adopted are

$$d_0 = 0, \quad d_1 = \frac{P_1}{2}, \quad d_2 = \frac{3P_1}{2}, \quad d_3 = 2P_1 \qquad (3)$$

These values are, in some cases, the same ones than the bias or control levels. They are given by

$$g_0 = d_0, \quad g_1 = d_1, \quad g_2 = P_1, \quad g_3 = d_2, \quad g_4 = d_3 \qquad (4)$$

P_1 corresponds with an input power level of a bit "1".

Finally, this circuit combines output data from the comparators in order to obtain the processing binary result from P-device.

Q-device (Fig. 5) needs an easier circuit and a simple comparator is present. It just discriminates the levels of input signal corresponding to an output "0" or "1".

Moreover, most of the results to be reported here, have been obtained by computer simulation. It has been done with the MATLAB™ program and its SIMULINK™ application.

The value of a bit "1" at any of the two inputs of the cell, namely I_1 or I_2, has been considered as normalization value for the present simulation of the Optical-Programmable Logic Circuit. As changing parameters have been taken:

i) the decision levels of each device, d_Q and d_P, and

ii) both controls signals, *g* and *h*.

Moreover, we have considered five levels of decision at the P-device. They are equidistant, as it has been indicated in previous equations, with respect to the first one d_{P1}. However, there are just three input levels where the output is able to switch from one state to another. This fact is in good agreement with the real characteristics of the optical non-linear device considered, namely, a SEED.

In a practical situation, and as a first application of the structure, the decision levels for each device have well defined values. We have fixed them to $d_Q = 1$ and $d_{P1} = 0.5$. By changing both control signals, g and h, from 0 to 2.5, a total of fourteen pairs of logic functions can be obtained. They are summarized on Table I.

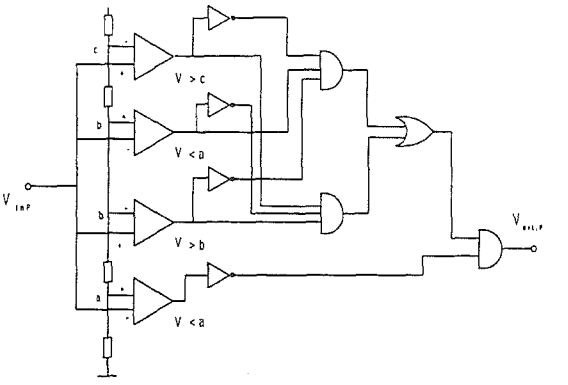

Fig. 4.- Electronic simulation of the SEED device.

Another way to work with this cell is the possibility to control the decision levels. These levels are intrinsic to each particular employed device. In our case, and by maintaining the same normalization as before, other different tables, equivalents to Table I, are possible to be obtained by changing these decision level values. In order to show a more general example, we will analyze and report just the results corresponding to the output, O_1. As it can be seen in Fig. 1, it is related to the more complex device P. A similar study can be done for the Q-device.

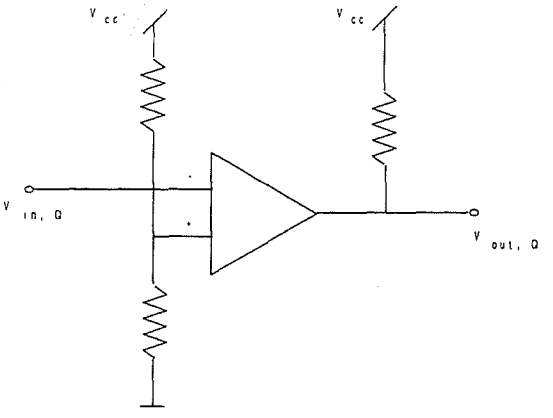

Fig. 5.- Electronic simulation for the On-Off device.

The behaviour of the O_1-output, for function OR at output O_2, is shown in Fig. 6 The axis represents, in ordinates, the power level of control signal *h* and, in x-axis, the power level of decision signal, d_{P1}.

As we can see, a large variety of logic functions are obtained in a very simple way. Moreover, a particular point needs to be pointed out. It concerns the extreme sensitivity of the output logic functions with respect to both control signals and decision levels. This fact is of a great importance for further considerations on the working conditions.It will be analyzed later.

Behavior of output O_2 is much easier than in O_1. The number of possible functions to be obtained from it is much smaller than from output O_1.

3 APPLICATION OF THE LOGICAL CIRCUIT AS LINE ENCODER FOR OPTICAL COMMUNICATIONS

Although the main objective of a logical circuit as the above analyzed one, was for Optical Computing, some other possibilities are open. Most of them are related with its application to other fields as Optical Communications. Two of the more important ones are the related with line encoding and with the generation of a periodic pulse sequence from a constant input. The first one will be presented in this paragraph.

In our work, the above mentioned structure has been able to perform Line Coding. As an example, biphase or Manchester encoding will be shown, but almost any two level block codes, of the *nBmB* type, can be obtained.

As it can be seen in Table I, one of the possible outputs through port O_1 is an XOR function of the two inputs. This gives us the possibility of obtaining a Manchester encoding in a very easy way. If the initial uncoded NRZ data stream is feed to input I_1 and a train of "0" and "1" alternated bits, with a value of period half of the previous one, goes to input I_2, the resulting output in O_1 is the requested biphase encoding. The experimental results obtained by us can be seen in[6].

TABLE I.- Possible output logic functions from the Optical Logic Structure.

Output optical signals -- ->	O_1	O_2	O_1	O_2	O_1	O_2
g_0	XOR	AND	XOR	OR	NAND	ON
g_1	NAND		NOR		NOR	
g_2	XNOR		XNOR		AND	
g_3	AND		OR		OR	
g_4	OR		OR		ON	
Control Optical Signals	h_0		h_1		h_2	

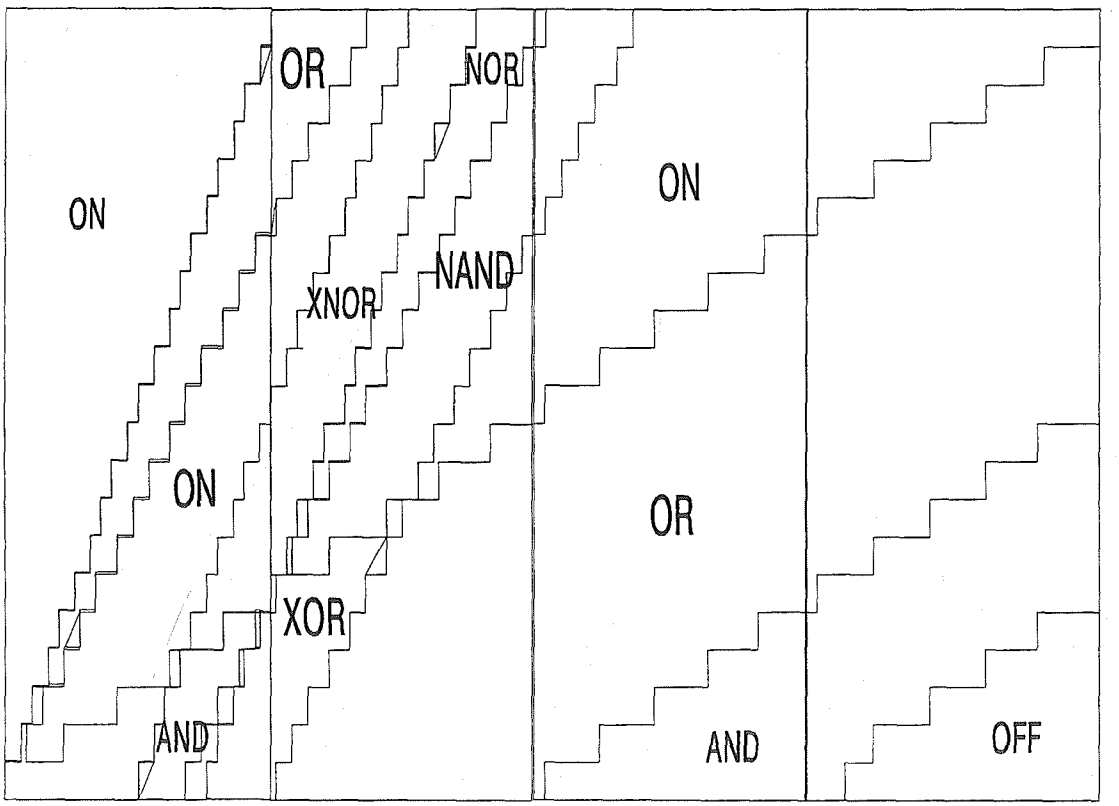

Fig. 6.- Behavior of the O1 output for an OR function at O2 output.

4.- PERIODIC AND CHAOTIC BEHAVIOUR

A non-linear behavior can be expected from the above reported cell, if some kind of feedback should be applied. Some examples of this type of behavior are given in references[9-10]. Although the present configuration has almost no points in common with the cases reported there, the presence of non-linear devices in the system gives some analogies with them.

In order to study the non-linear response of our circuit, some minor modifications are needed. The first one should be to introduce a feedback from one of the two possible outputs to one or both of the cell inputs. Moreover, according to previous studies in this field, the introduced feedback has to have some time delay. In the same way, because the results we are going to get will be obtained by computer simulation, another internal delay should be needed. It corresponds to the response time of the simulated nonlinear devices, **P** and **Q**.

In general, a periodic behaviour should be expected as the normal output of the system. But, under some conditions, this is not always true. The output, as we will show, is not periodic with some parameters values of the system.

If feedback is going to be applied to the system, two are the possibilities we have. They correspond with its two outputs, O_1 and O_2. Because the P-device output has more possible different functions, depending on its control signal (see Table I), than the Q-, we have adopted its output as signal feedback. Several were, again, the possibilities to feed this signal to the cell, because four are the possible inputs. The solution adopted was to go to the control input, *g*, of P-device. No other additional control signal is used. Fig. 8 shows the final circuit with feedback.

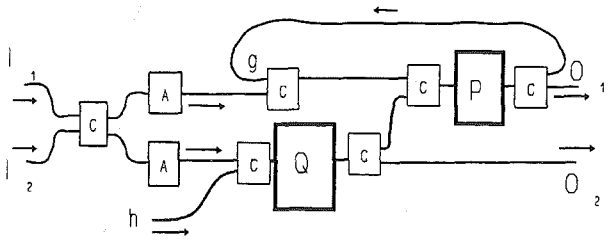

Fig. 7.- Optical Logic Structure with feedback.

The first analysis that we have performed, by simulation tools, considered null delay times. This situation has not an algebraic solution and no data were obtained. But results are strongly different if finite delay times, namely, internal and external delays are introduced.

According to previous studies[9-10], the situation with more probability to give a periodic or even chaotic solution is when internal delay time is shorter than the external one. In everyone of the studied cases, a regular train of pulses has been the input. The real input to the device P, before the feedback takes place, is a multilevel signal corresponding to the addition of the two inputs.

If the ratio between internal and external delay times is smaller than 1, we obtain a periodic situation. The period of this signal is strongly dependent on the ratio value. In the particular case, where external time delay is 200 and internal delays are 2, 4 and 12, obtained results are strings of 0's and 1's periodically repeated. Period goes from 70 to 280 time units as the ratio between delays get smaller. Frequency doubling have been obtained. This indicates a possible route to chaos. Some more details can be seen in[6].

Finally, we have made the internal response time equal to zero. Some output signals are given in Figs. 8 a-d. No indication of a possible periodic behaviour has been obtained for longer intervals of time. These results, because they have been achieved after a Period-Doubling Route, clearly indicate that a certain type of chaos is present.

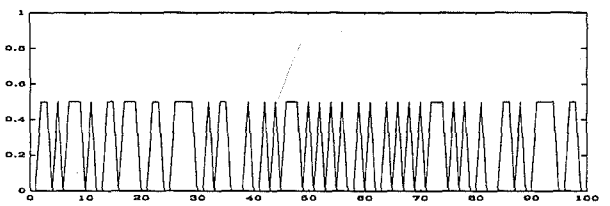

Figure 8.a

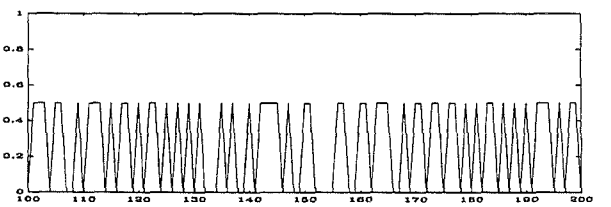

Figure 8.b

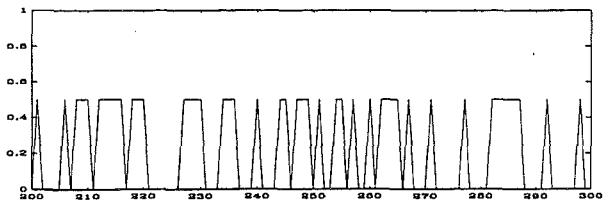

Figure 8.c

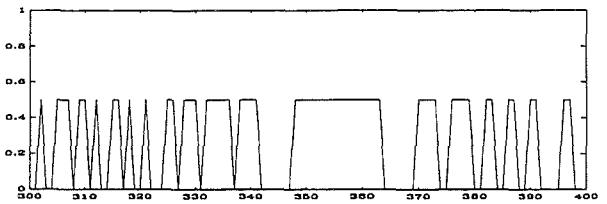

Figure 8.d

5.- ANALYSIS OF THE OBTAINED RESULTS

In order to characterize the obtained chaotic signal, conventional methods are difficult to be applied here. The above results constitute a Time Series from where a chaos measure should be obtained. But the correct phase-space representation is not possible to be grasped from these results in an straightforward way. We do not even know what the adequate phase-space variables are and it is not even known how many variables are needed to fully describe the dynamics of this particular system. There is fortunately a partial answer to this problem that has been applied successfully in a large number of experimental investigations. The basic idea is that if the fundamental phase-space variables are x and x', to study the evolution of the system numerically, x and x' have to be follow as functions of t. But since $x' = [x(t+\Delta t)-x(t)]/\Delta t$ in the limit as $\Delta t \to 0$, a knowledge of $x(t+\Delta t)$ is equivalent to a knowledge of x'. In other words, a knowledge of a trajectory of points $[x(t),x(t+\Delta t)]$ is equivalent to a knowledge of the trajectory of points $[x(t),x'(t)]$. As a consequence, a phase-space trajectory

$$x(t) = [x_1(t),x_2(t),...,x_n(t)] \tag{5}$$

is replaced by a trajectory in an artificial phase space with points given by

$$y(t) = [y(t),y(t+\Delta t),...,y(t+m\Delta)] \tag{6}$$

where y(t) is any one of the phase-space variables $x_i(t)$. Thus from a set of measurements of a single quantity y(t) we can construct a sequence of points in an artificial phase space

$$x(t) = [y(t),y(t+\Delta t),...,y(t+m\Delta t)] \tag{7}$$

$$x(t+\Delta t) = [y(t+\Delta t),...,y(t+(m+1)\Delta t)] \tag{8}$$

With the data we have, the first problem to solve is how to operate with our digital signal where just two values, "0" and "1", are present. If we adopt just this output as possible values for y, the resulting plot at the phase space should be concentrated on just four points, namely, (0,0), (0,1), (1,0) and (1,1). Almost no information could be obtained from it. Hence a new technique has to be implemented.

The first method we have adopted[7-8] is to group sets of four consecutive bits and to convert them to their corresponding hexadecimal values. Hence, a sequence of zeroes and ones is converted to a new string of hexadecimal values, namely, 0, 1, 2, ..., 15. For example, "0010" would be a "2", "1001" a "9" and "1110" a "14". The total number of data is divided by four, but

much more information can be obtained from them than with simple binary signals. A diagram, similar to the t_{i+1} versus t_i in analogue signals, can be drawn in this way. In the case of periodic signals, a closed configuration is obtained. But in the case of chaotic signals, no definite pattern would be obtained. This situation has been reported in [7-8].

A further point needs to be considered. It is the one concerning the justification that the preceding quantity, namely the hexadecimal sequence, represents the same behavior of the system than the previously obtained binary one. But this situation is equivalent to the reverse one: to convert a chaotic analog signal into a digital one. As it is well known from digital communications, any analog signal can be quantized and from this quantization to obtain a digital signal with the same properties than the initial analog one. In our present case, we have accomplished the opposite operation, namely, to convert a digital signal into an analog one with sixteen possible levels. And, according to digital communication signal processing, both representations are equivalent.

A second possible method to study this particular type of chaos is by the LZ Complexity Measure. Its basis is to extract a meaningful information from data that have every appearance of being random and determine a computable measure of their complexity. One of the main methods is the studied by Lempel and Ziv [11], LZ for brevity. It measures the number of distinct patterns that must be copied to reproduce a given string. The only computer operations considered in constructing a string are copying old patterns and inserting new ones. Briefly described, a string $S=s_1s_2...s_n$ is scanned from left to right, and a complexity counter c(S) is increased by one unit every time a new substring of consecutive digits is encountered in the scanning process. The resultant number c(S) is the complexity measure of the string S. According to [8], the minimum value for LZ complexity is c(S) = 2. Moreover, only relative values of c(S) are meaningful and in particular it is the comparison with the c(S) for a random string that is meaningful. Lempel and Ziv have shown that for a random string of length n, the LZ complexity is given by

$$b(n) = \frac{hn}{\log_K(n)} \tag{9}$$

where K denotes the number of elements in the alphabet, 2 in our digital signal, and h denotes the normalized source entropy

$$h = \frac{-1}{\lg N} \sum_{i=1}^{N} p_i \lg p_i \leq 1 \tag{10}$$

In our present case, each symbol from the alphabet, namely "0" and "1", is equally probable and hence

$$pi = 1/N \text{ and } h = 1.$$

In order to compare with the complexity for a random string, we have to compute

$$\lim_{n \to \infty} [c(S) / b(n)] \tag{11}$$

for a string with n elements. If the above ratio is less than 1, then we can conclude that this is due to a pattern formation in the string S.

As an example of the application of this method, let us consider an example to make the procedure clear. Consider S = 0100

(1) 0.

(2) $Q = 1, SQ = 0 \cdot 1, v(SQ\pi) = \{0\}$, *thus* $Q \notin v(SQ\pi)$.

(3) $Q = 0, SQ = 0.1.0\ v(SQ\pi) = \{0, 1, 01\}$ *thus* $Q \in v(SQ\pi)$

(4) $Q=00\ SQ=0.1.00\ v(SQ\pi)=\{0,1,01,10,010\}\ thus\ Q\notin v(SQ\pi)$

where the notation $S\pi$ denotes the string $s_1...s_{n-1}$, being n the length of sequence S, and S = QR denotes the concatenated string $q_1...q_m r_1...q_n$.

According to[11] S = 0.1.00. and thus the complexity is c(S) = 3

We have applied this method to the study of the two types of patterns obtained before, namely, periodic and chaotic. In every case we have taken strings with 2048 digits. Obtained results are summarized in Table II.

Table II.- LZ Complexity for Outputs at Fig. 8.

OUTPUT	n	b	c	c/b
Period 70	2048	186.2	33	0.17
Period 140			65	0.34
Period 280			129	0.68
Chaotic			175	0.94

As it can be seen, values much smaller than 1 are obtained for those outputs where a periodic pattern was present. On the contrary, a value very close to 1 appears for the chaotic solution. Values should be much more different if larger strings should have been taken.

Finally, the technique proposed by Singh and Joseph [12], of extracting quantitative information from a binary symbol sequence, has been applied too. In order to do that, we have first represented our symbol sequence as a string of 1's and -1's. These values are chosen so that the expected mean of a random sequence of equally likely symbols be zero. In our present case we have change 0's by -1's. An autocorrelation on such a symbol sequence is defined as

$$r(n) = \frac{1}{N}\sum_{k=1}^{N} u(k+n)u(k) \qquad (n = 0,1,2,....;\ N>n) \tag{12}$$

If the sequence is chaotic, the autocorrelation should have the property

$$r(n) \to 0 \quad \text{as} \quad n \to \infty \tag{13}$$

We have obtained this value just for the chaotic reported case. When some type of periodicity was present. a plot of autocorrelation versus time delay shows peaks with value 1 every 70, 140 or 280 time units.

6.- INFLUENCE OF THE NON-LINEAR DEVICES AND THEIR DECISION LEVELS ON THE CIRCUIT BEHAVIOR

Although the general behavior reported above is the result of devices properties plus the way they are interconnected, some words are needed to add concerning the characteristics of individual devices.

As it has been pointed out before, most of the cell behavior is due to the characteristics of the SEED-like device. Its output vs. input curve is similar, in some way, to the characteristic of the nonlinear resistor in the forced van der Pol oscillator[13]

$$f(i) = Ri_0\left\{-\frac{i}{i_0} + \frac{1}{3}\left(\frac{i}{i_0}\right)^3\right\} \tag{14}$$

because it can be written

$$i_{out} = i_{co} + A[i_{inp} + i_{ci}] + B[i_{inp} + i_{ci}]^3 \tag{15}$$

where A, B, i_{co} and i_{ci} are constants verifying

$$i_{co} + i_{ci}[A + Bi_{ci}^2] = 0 \tag{16}$$

Similarities stop here. Our present circuit is not as straightforward as the van der Pol oscillator is and no second-order differential equation is possible to write in order to get possible solutions. As a matter of fact, no straightforward differential equations are possible to be written down for it. Analogical solutions are not valid because we are working with digital signals. Moreover, the possible tools we have are just simple equations, similar to [1] and [2], plus decision level values set up in order to obtain a "1" or a "0".

But some conclusions can be obtained in a phenomenological way by correlation with the van del Pol oscillator. The main one corresponds to the region where the circuit is unstable. In the van der Pol case this region covers the segment from $-i_0$ to $+i_0$. In our present case this should be equivalent to the line going from the maximum to the minimum at the SEED characteristics. Those situations, when our cell is working at or near this region, should give a more complex behavior than in others. This implies that some care has to be taken there.

Two facts need to be considered at this point. The first one is that any real device has some variations in its performance with respect to ideal ones. Firstly, its characteristics may vary with time. This fact can come just from pure heating or from the input light level or from its wavelength. Second, some type of hysteresis may appear where just a simple line should be present. Third, input-output curves can change slightly from one component to another. If operating conditions have been fixed in a very tight form, the final behaviour can be very different from the expected one. Hence, some margin has to be given to both, experimental and simulated models.

As it has been shown, a very important point for the cell behaviour is the position where the decision level is placed[14]. According to it, a logic boolean function of the two inputs, namely a "0" or a "1", will be obtained. Figure 9 shows the case for P-device. Continuous line indicates the device real behaviour and possible variations. Dashed line shows the simulated one. If the adopted margin is wide, the output will remain stable although characteristics may change. This situation corresponds to a large hysteresis-like cycle in the simulation. But if the margin is thin, the output can vary with time. These variations will be larger when the cell is working in the non-linear situation. Very small changes in device properties could give rise, in this way, to large output changes. Hence, the situation of decision levels may affect, in a very strong manner, to the output and, hence, to global cell behavior. Similar phenomena can take place in the Q-device.

Although the above reasoning is purely phenomenological, it can give a first explanation of why a chaotic situation is obtained in our circuit. Some more work in necessary to be done in order to obtain a more detailed proof.

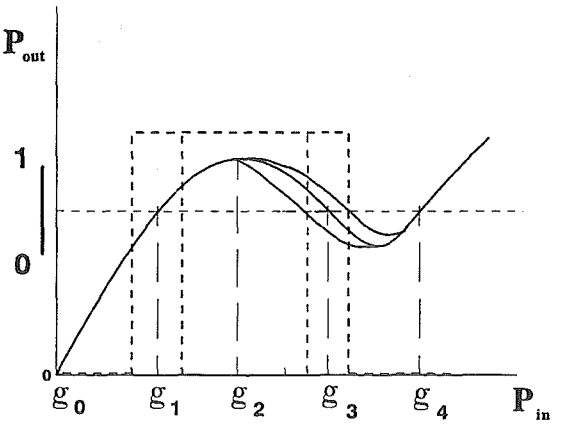

Fig. 9.- Behavior of the SEED device when an hysteresis cycle is present.

7.- CONCLUSIONS

A type of digital chaos has been reported. The basic structure is the same Optically Programmable Digital Cell, reported previously by us, as the main block for a possible optical computer. A feedback was applied and internal and external time delays considered.

Obtained results, both experimental and computer simulated, indicate that the same system is able to be employed as a random optical bits generator for use in Optical Communications. The obtained digital chaos has been studied from different view points. A phenomenological analysis is presented for the behavior of the individual nonlinear devices.

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