Temperature-dependent high-frequency performance of deep submicron AlGaN/GaN HEMTs

R. Cuerdo, Y. Pei, F. Recht, N. Fichtenbaum, S. Keller, S. P. Denbaars, F. Calle, and U. K. Mishra

Electrical and Computer Engineering Department, University of California Santa Barbara, 93106-9560, Santa Barbara, CA, USA

1 Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) are being used in monolithic microwave integrated circuits (MMIC) for power applications at X band and above for the last few years. They take advantage of some interesting properties of III-nitrides, such as their intense piezoelectric fields, high breakdown field and saturation velocity, and good thermal conductivity, to provide high power at increasing frequencies and harsh environments. To fully understand the HEMT performance from a thermal point of view, a complete characterization of the devices should be done over a wide range of temperatures. For high temperatures (HT), Lee and Webb reported a temperature dependent nonlinear model on a 0.35 μm gate length device from 300 K to 423 K. On the other hand, Nidhi has studied the impact of access resistance on HEMTs with high frequency performance for cryogenic temperatures. This work completes the study at low temperatures (LT) by means of extracting the small signal model from 300 K down to 100 K at every 50 K.

2 Experimental

Al_{0.33}Ga_{0.67}N/GaN HEMTs with 20 nm barriers were grown by metal-organic chemical vapour deposition (MOCVD) on SiC. A 0.6 nm AIN interlayer between the buffer and the barrier was used to improve the 2DEG transport properties. In order to achieve a non-alloyed low resistance ohmic contact (R_c ≈ 0.2 Ω·mm), Si ions were implanted into the source and drain regions and then activated by annealing the sample at ~1280 °C in a MOCVD system with a N_2 and NH_3 ambient. The sample was then passivated by SiN_x and a sacrificial Ge layer was deposited to decrease parasitic capacitances. Submicron gates were defined by e-beam lithography and dry-etched through the Ge and SiN_x layers. The gate region was treated by fluorine plasma for 10 minutes to decrease the gate leakage, and the AlGaN layer recessed by chlorine to improve the transconductance. Transistors have a gate length ~150 nm with gate-source spacing (L_{GS}) of 0.3 μm and drain-gate spacing (L_{DG}) of 1.1 μm. Gate widths are of 100 μm or 150 μm. The sheet carrier density (n_s) and Hall mobility (μ_H) were 1.1·10^{13} cm^{-2} and 2000 cm^2/V·s.
S-parameter measurements from 300 K to 100 K were carried out using a cryogenic high frequency probe station, composed of a liquid nitrogen cooled wafer stage and a heater to control the temperature. The station was connected to an Agilent PNA E8361A network analyzer for the RF measurements and to an Agilent 4155B parameter analyzer for the DC characterization. For the on wafer RF measurements from 1 GHz up to 40 GHz, the electrical reference plane was established by an “off-wafer” LRRM calibration at each temperature.

3 Results and discussion

Both drain cut-off current \( (I_{DSS}) \) and extrinsic transconductance \( (g_{m,\text{ext}}) \) increase around 30% from 300 K to 100 K as shown in Fig. 1, up to maximum values of 0.99 A/mm and 0.62 S/mm, respectively. This behaviour is related with the higher electron mobility in the 2DEG as devices are cooling, due to the reduction of the polar optical phonon scattering. This mechanism is dominant at 300 K, but becomes negligible as temperature decreases. At 100 K other types of scattering such as the alloy disorder are predominant with a temperature independent behaviour. Thus, the improvement in the HEMT performance saturates for \( T < 150 \text{ K} \).

The source resistance \( (R_s) \) has been extracted from specific DC measurements. For transistors with \( L_{GS} = 0.3 \ \mu m \) and \( L_{DS} = 1.1 \ \mu m \), \( R_s \) decreases from 0.49 \( \Omega \)·mm at 300 K to 0.35 \( \Omega \)·mm at 100 K as is shown in Fig. 2. Drain resistance \( (R_D) \) can be also calculated as the difference between the on-resistance \( (R_{on}) \) and \( R_s \), extracting \( R_{on} \) from the slope of the linear region in \( I_D \) vs \( V_{DS} \) curves at low \( V_{DS} \). For the same devices, \( R_D \) varies from 1.15 \( \Omega \)·mm at 300 K to 0.65 \( \Omega \)·mm at 100 K.

The measurements of the S-parameters allow the extraction of the current-gain \( (f_T) \) and power-gain \( (f_{\text{max}}) \) cut-off frequencies and the equivalent circuit parameters (ECPs). The \( f_T \) and \( f_{\text{max}} \) are estimated from \( |h_{21}|^2 \) and the unilateral power gain \( (U) \), respectively, assuming a 20 dB/decade linear decrease. As shown in Fig. 3, \( f_T \) increases ~16% from 300 K to 150 K, and stabilizes down to 100 K. The maximum of \( f_T \) occurs approximately at the same \( I_D \) for all temperatures under study. The \( f_{\text{max}} \) follows a similar evolution than \( f_T \), increasing ~21% from 129 GHz at 300 K to 156 GHz at 100 K. Both \( f_T \) and \( f_{\text{max}} \) increases are related with the improvement of the parasitic resistances \( (R_s \) and \( R_D) \) as devices are cooled.

The small signal model has been extracted and simulated at different bias by means of ADS software. The equivalent circuit used was proposed by Dambrine et al.

The extrinsic resistances \( R_s \) and \( R_D \) have been previously calculated, and \( R_g \) is set as 1/3 of the gate metal strip resistance. From pinched HEMT measurements, extrinsic capacitances \( C_{pg} \) and \( C_{pd} \) are obtained. The extrinsic inductions \( L_{pg} \) and \( L_d \) are calculated from cold measurements \( (V_{DS} = 0 \ \text{V} \) and \( V_{GS} = 2 \ \text{V} \) ). Next, the intrinsic circuit parameters are deduced following . The equivalent circuit is simulated and fitted to achieve a good agreement between model and measured characteristics, especially for frequencies between 1 to 20 GHz (see Fig. 4). Inductances and capacitances for the extrinsic circuit are supposed constant with temperature. Regarding the
4 Conclusion

Low temperature measurements allow the determination of the dominant limiting factors of the HEMT performance. From 300 K down to 100 K, \( R_s \) and \( R_D \) experience a clear decrease above 40%, which improves not only the DC performance (\( I_D \) and \( g_{\text{m,ext}} \)) but also \( f_I \) and \( f_{\text{max}} \).

Every 50 K the ECPs of several transistors have been extracted in an accurate way. Apart from the parasitic resistances behaviour, \( g_d \) shows a significant reduction at low temperatures. This fact suggests a better buffer isolation, as also confirmed by the decrease of leakage currents and by the better 2DEG confinement deduced from simulations. Other parameters (\( g_{\text{m,ext}}, \tau, C_{\text{gs}}, C_{\text{gd}} \)) from the small signal model seem to be rather constant with temperature for this type of deep gate transistors.

References

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