

# Ratio-Based Temperature-Sensing Technique Hardened Against Nanometer Process Variations

Pablo Ituero

and Marisa López-Vallejo

**Abstract**—This letter presents a temperature-sensing technique on the basis of the temperature dependency of MOSFET leakage currents. To mitigate the effects of process variation, the ratio of two different leakage current measurements is calculated. Simulations show that this ratio is robust to process spread. The resulting sensor is quite small—0.0016 mm<sup>2</sup> including an analog-to-digital conversion—and very energy efficient, consuming less than 640 pJ/conversion. After a two-point calibration, the accuracy in a range of 40 °C–110 °C is less than 1.5 °C, which makes the technique suitable for thermal management applications.

**Index Terms**—Leakage, process variations, ratio-based, sensor, temperature, time-to-digital.

## I. INTRODUCTION

**E**XACERBATED variability in nanometer CMOS jeopardizes yield, robustness, reliability and performance of current analog and digital systems. In this context, temperature is by itself a source of new variations—many aging process are tightly coupled with thermal gradients and stresses—but also a victim of the process uncertainties. Its dependence on power densities along with its relationship to leakage currents make it specially sensitive to all these issues. Therefore, the importance of dynamic thermal management (DTM) techniques with technology scaling has kept on increasing. However, it is not a simple task to design temperature sensors that fulfill the accuracy requirements imposed by DTM policies ( $\pm 1$  °C at throttle,  $\pm 5$  °C at 50 °C [1]) comprising a small area and power overhead under this scenario of device uncertainties. Process variations can affect the quality of the reference signal or that of the measurement in such a way that the accuracy of the sensor is completely ruined.

Most previous works in the literature on temperature sensors targeting DTM employ a time-to-digital (TDC) or a frequency-to-digital converter to perform the digitization as they suppose a smaller area and power-overhead than voltage- or current-based converters and also take a very robust reference which is the system clock. There have been several proposals to generate a temperature-dependent pulse width or frequency. In [2] we proposed a sensor in the 0.35  $\mu\text{m}$  node based on the temperature dependency of MOSFET leakage currents that had an area of 843  $\mu\text{m}^2$  (0.01 mm<sup>2</sup> including ADC)

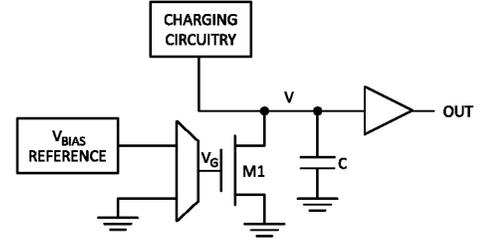


Fig. 1. Constituent blocks of the 65-nm thermal sensor.

and an energy of 0.21-13nJ with an accuracy 1.97 °C without calibration. A similar sensor, employed in the SX-9 supercomputer, has an area of 1225  $\mu\text{m}^2$  (without ADC) at the 65 nm node [3]. At the 32nm node, a sensor based on the leakage current of an SOI-CMOS diode has an area of 1000  $\mu\text{m}^2$  (with ADC) [4]. Also remarkable, in the field of BJT-based sensors—traditionally accuracy-oriented and too big for DTM—there has recently been proposed a small structure of 0.02 mm<sup>2</sup> (with ADC) at the 32nm node [1].

In this letter, we introduce a new leakage-current-based sensing technique that is robust to process variation. A sensor employing this mechanism has been implemented in a 65nm technology and its main features are the following. (1) Independent of most sources of process variations. (2) Ultra low energy per conversion of 48-640 pJ. (3) Area of 439,8  $\mu\text{m}^2$  (0.0016 mm<sup>2</sup> including ADC). (4) Inaccuracy of less than 1.5 °C considering process variations for a range of 40-110 °C.

## II. ANALYTICAL DESCRIPTION

Continuing with the fundamental idea of our previous work [2], our proposed technique is based upon the variations of the leakage currents with the temperature. Figure 1 shows the constituent blocks of the sensor that will help us explain its functioning. In our proposal we charge the capacitance  $C$  through a charging circuitry and measure the time it gets discharged mainly through the leakage currents of M1. More precisely, the sensor realizes the ratio of two measures: In the former the gate voltage of M1 is set to ground; in the latter the gate voltage is set to  $V_{BIAS}$ , where  $V_{BIAS}$  is a reference voltage different to 0V and below  $V_T$  so that M1 operates in the subthreshold regime.

Considering these premises, the expression of  $I_D$  of M1 as a function of the temperature,  $T$ , and the voltage between its drain and source,  $V$ , is the following:

$$I_D(T, V) = K_1 T^2 e^{\frac{1}{T} \left( \frac{V_G}{nk/q} - K_2 \right)} \left( 1 - e^{-\frac{V}{kT/q}} \right) \quad (1)$$

where  $K_1$  and  $K_2$  are technology parameters independent on the temperature,  $kT/q$  is the thermal voltage,  $n$  is

the transistor subthreshold swing coefficient and  $V_G$  is the gate-source voltage of transistor M1.

For a constant temperature, let us now calculate the discharge time of C through M1. Supposing that the charging circuitry charges the capacitor C to a voltage  $V_1$  and that the threshold of the output inverter is  $V_2$ , the sensor performs the following measure:

$$\begin{aligned} \Delta t_{V_1 \rightarrow V_2}(T) &= \frac{C}{K_1 T^2} \frac{kT}{q} e^{\frac{1}{T} \left( \frac{V_G}{nkT/q} - K_2 \right)} \left[ \ln \left( e^{\frac{V_1}{kT/q}} - 1 \right) - \ln \left( e^{\frac{V_2}{kT/q}} - 1 \right) \right]. \end{aligned} \quad (2)$$

Let us now see what happens when we perform the ratio of two measurements with different values of  $V_G$ :

$$\frac{\Delta t_{V_1 \rightarrow V_2}(T)|_{V_G=0}}{\Delta t_{V_1 \rightarrow V_2}(T)|_{V_G=V_{BIAS}}} = e^{\frac{V_{BIAS}}{nkT/q}}. \quad (3)$$

Which, when taking logarithms, yields the following expression:

$$\log \left[ \frac{\Delta t_{V_1 \rightarrow V_2}(T)|_{V_G=0}}{\Delta t_{V_1 \rightarrow V_2}(T)|_{V_G=V_{BIAS}}} \right] = \frac{V_{BIAS}}{nkT/q}. \quad (4)$$

As shown, this expression does not display any dependency on the size of the capacitor, the voltage the node is charged at, the threshold of the inverter or the device parameters of M1. This makes the sensor specially suitable to track the temperature on current nanometer technologies. The measurement displays linear sensitivity on  $V_{BIAS}$  whose robustness and characteristics, being such a small voltage, are one of the factors that will most impact the quality of the sensor. Supposing  $V_{BIAS} = 125$  mV, the sensitivity of the calculated  $T$  at 75 °C is 2.8 °C/mV. As explained in [3], this type of leakage-based sensors displays little dependence on Vdd variations. In this case the sensitivity on the supply comes through  $V_{BIAS}$ ; this value for each voltage reference circuit will display a certain dependency on the supply which will ultimately affect the calculated temperature.

### III. CHARACTERIZATION AND DISCUSSION

In order to prove the correctness of these equations, we have designed a sensor system as depicted in Fig. 1 employing a time-to-digital converter based on a logarithmic counter, as described in [2]. When laid out in a TSMC 65nm CMOS process, the sensor and voltage reference occupy an area of 440  $\mu\text{m}^2$ , which increases to 1568  $\mu\text{m}^2$  with the ADC. The simulations and layouts have been carried out in the Cadence™ environment. All the characterization results come from post place-and-route Monte Carlo simulations taking a distribution of 100 test circuits—representing different technology corners.

As expressed by equation 4, the sensor presents a transfer function that is directly proportional to the inverse of the temperature. For a limited range of temperatures this function can be approximated by a linear response, albeit a certain degree of curvature will always be present. Furthermore second and greater order effects not taken into account by our model would introduce a certain distortion. These limitations will be responsible for the inaccuracy of the sensor under nominal conditions. In order to provide a better approximation for the

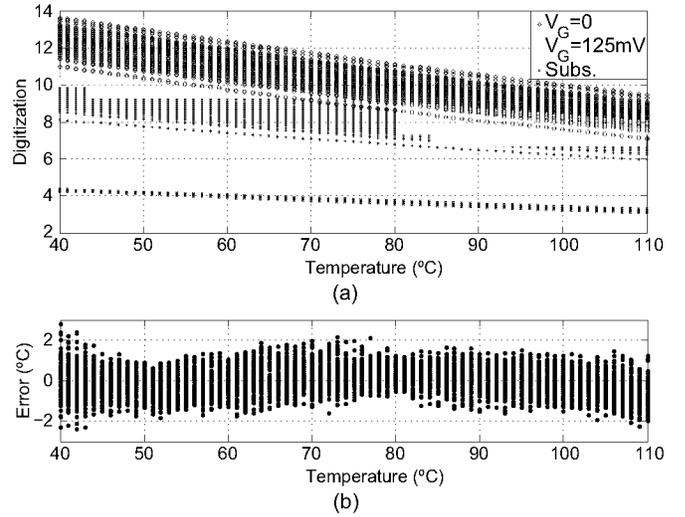


Fig. 2. Sensor response under the effects of process variability. (a) Digitization output. (b) Error distribution.

linear response, and considering the field of application of the monitor—on-chip thermal management—we restrict the range of temperatures to 40 – 110 °C.

The simulation results under nominal conditions yield a  $3\sigma$  inaccuracy of 0.96 °C, and a quantization error of  $\pm 0.20$  °C. The power has a variation from 3.16 to 0.239 nW (40–110 °C) and the energy ranges from 633 to 47.7 pJ from the minimum to the maximum temperature in the range as the length of the pulses varies and, thus, the logarithmic counter is active for different times.

Figs. 2(a)-(b) show the sensor's response in the presence of process variation. Figure 2(a) shows the digital signals output by the logarithmic counter for each of the measures along with the result of the subtraction. As shown there is a considerable spread in the digitized values of the measures due to process fluctuations, however when the subtraction is performed, the spread is greatly reduced, as expected from equation 4. Figure 2(b) shows the distributions of error for each temperature, once a two-point calibration has been performed. The  $3\sigma$  value of the error under these conditions is 1.18 °C. Compared to other temperature sensors reported in a recent survey [5], the sensor described in this letter exhibits significantly less area and energy consumption. These properties come along an accuracy and a resolution within the acceptable range for DTM policies.

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