

I. INTRODUCTION

The envelope amplifier (EA) that supplies the radiofrequency power amplifier (RFPA) in envelope tracking (ET) [1] or envelope elimination and restoration (EER) [2] technique has to accomplish several characteristics as large signal high bandwidth, high linearity, good quality of the transmitted signal and a high efficiency. A single stage converter has the advantage of a good linearity and bandwidth, but the switching frequency has to be highly increased to comply with the bandwidth requirements so the efficiency will drop and also the quality of the transmitted signal and the reliability will be degraded. Class E amplifiers can be a high efficiency single stage solution [3]-[4] even at high switching frequencies due to the zero voltage switching (ZVS) capability. However, ZVS is lost if duty cycle modulation is required, so it cannot be considered for this application where a high output voltage range is needed. Other solutions in the state of the art propose a hybrid solution consisting in a linear assisted converter, in a series [5] or parallel [6] combination of a switched DC-DC converter and a linear regulator. Those architectures provide a good trade-off between the above referred specifications but have the drawback of the increased complexity due to the additional stages of the converter. In this paper it is proposed a new solution for the envelope amplifier based on the single stage architecture which has the advantages of a high bandwidth and an output current ripple cancellation that allows a switching frequency reduction compared to the conventional buck converter, and therefore an increase in the efficiency and reliability. The solution is based in a new design for the synchronous rectifier buck converter with output current ripple cancellation circuit (RC buck converter). The specifications of this work comply with the frequency and power requirements of the envelope amplifier of the RFPA in applications as microsatellites or medium bandwidth communication services as satellite telephony of trunked radio systems. However, the solution presented in this paper is not limited to these specifications and can be applied to a buck converter for other applications.

II. NEW DESIGN FOR A BUCK CONVERTER WITH RIPPLE CANCELLATION CIRCUIT

Ripple cancellation technique is a well known solution to obtain, theoretically, output (or input) zero current ripple [7] [8]. By adding only some passive components, the performance of the converter can be improved without a high increase in the losses. In this work we will focus on the synchronous buck converter as shown in Figure 1, but this

![Figure 1. Schematic circuit of the synchronous buck converter with output current ripple cancellation circuit](image)
solution can be applied to several topologies [9], [10].

The aim is to achieve zero ripple \( i_2 \) by adjusting \( L_2 \) inductance value. State of the art design assumes a \( C_b \) capacitance high enough to ensure a DC blocking voltage on it, a N:1 turns ratio (N>1) for \( L_{1A} \) and \( L_{1B} \) (Figure 1) coupled inductors and a unique solution (1) for \( L_2 \) given \( L_{1A} \) and the coupled windings turn ratio \( N \) as shown in [5].

\[
L_2 = L_{1A} \cdot \frac{1}{N} \cdot \left(1 - \frac{1}{N}\right)
\]

With the previous considerations, the effect of the ripple cancellation technique is independent of the switching frequency, duty cycle or other parameters of the converter [5]. In Figure 2 and Figure 3 time domain and frequency domain simulations are shown for the conventional ripple cancellation circuit applied to a SR buck converter. \( i_1 \) and \( i_2 \) current ripples have the same amplitude and are 180° phase shifted so a no ripple \( i_1 \) is obtained. In Figure 3 it has been compared with the equivalent bandwidth buck converter in terms of attenuation of the output filter.

![Figure 2. Simulated buck converter with ripple cancellation circuit; steady-state operation](image)

![Figure 3. Output filter frequency domain (magnitude) comparison between the RC buck and the equivalent conventional buck (same resonant frequency)](image)

In this work it is presented an implementation of the current ripple cancellation technique for a synchronous buck converter where the focus is on increasing the large signal bandwidth without losing the output current ripple cancellation. This will allow a reduction of the \( f_{sw} \) for the same bandwidth and output voltage ripple than the conventional buck converter equivalent design. In order to increase the bandwidth, the passive components of the output filter should be reduced without degrading the output current ripple cancellation efficiency. A decrease in \( L_{1A} \) would imply a high current ripple in the circuit (despite it is cancelled in the output) which would generate additional losses so only a small reduction can be considered (increasing the maximum \( \Delta I_{pk-pk} \) specifications). The turns ratio \( N \) of the coupled windings has been considered high enough to allow a reduction in the \( L_2 \) inductance. The value of the capacitor \( C_b \) is the key parameter because, in principle, it can be reduced highly without big limitations regarding losses. The effect will be a voltage ripple on this capacitor, assumed sinusoidal, that will increase the \( i_2 \) current ripple and will have to be taken into account in the design of \( L_2 \).

### III. Dynamic Behavior Analysis of the Ripple Cancellation Buck Converter

The effect of the ripple cancellation technique in the new proposed design has been analyzed and simulated. It can be seen in Figure 4 the dynamic behavior and the high attenuation of the output voltage for a specific frequency range (centered in the \( \omega_{sw} \), 4MHz in this case).

![Figure 4. Magnitude and phase bode plots of \( d \) to \( V_0 \) for the conventional vs ripple cancellation buck converter](image)

It has been analyzed how the new design affects to the ripple cancellation and to the \( L_2 \) inductor value shown in (1). Equation (2), given in an implicit form for a better understanding, shows the new solution for the output current cancellation, obtained from the current ripple balance in the output of the converter. To obtain (2), the assumption of sinusoidal voltage ripple on the \( C_b \) capacitor of Figure 1 has been done. The duty cycle to output voltage transfer function bode plots corresponding to this design can be seen in Figure 4.

\[
\frac{1}{L_{1A}} + \frac{1}{N^2 \left( L_2 - \frac{\pi^2}{\omega^2 \cdot C_b} \right)} - \frac{1}{N \left( L_2 - \frac{\pi^2}{\omega^2 \cdot C_b} \right)} = 0
\]

Analyzing (2) it can be seen that the output current cancellation depends on more parameters, like \( C_b \), \( T \) and the duty cycle \( d \). By adjusting them properly, and once \( f_{sw} \) is set, there is a single value for \( L_2 \) that we can calculate with (2) to design a RC buck converter with higher bandwidth and therefore allow a reduction in the \( f_{sw} \) to bandwidth ratio. By reducing \( C_b \), it has been introduced a dependence on some parameters for the current ripple cancellation unlike the conventional design [5]. Ideally, no output capacitor will be needed, but to filter higher frequency spectral components a small capacitor \( C_o \) (with no effect in the resonance frequency of the converter) has been added. For variable duty cycle operation, it could be a problem the influence of \( d \) in the cancellation, but if the effect of the new term is limited by design, and considering that the specifications allow <1% of
output voltage ripple on the worst case and the small output capacitor, it has been demonstrated experimentally that on different operating points the efficiency of the current ripple cancellation will not be decreased.

![Image of sensitivity analysis](image1)

**Figure 5.** Sensitivity analysis of the proposed converter for L2 inductance variations (+10%). Magnitude bode plot of duty cycle to output voltage transfer function.

The sensitivity analysis of the ripple cancellation efficiency for L2, the most sensitive parameter for the ripple cancellation, can be seen in Figure 5, where it is also compared to the equivalent simulated conventional buck. The $R_d$ damping resistor, should be as small as possible as it decreases the ripple cancellation efficiency.

**IV. EXPERIMENTAL RESULTS**

The transfer function of $V_{sw}$ to $V_o$ (Figure 1) of the converter has been measured and modeled to validate the proposed design. The comparison is shown in Figures 6 and 7, where the $V_{sw}$ to $V_o$ transfer function of the conventional buck converter has been included to compare, for the same bandwidth and output voltage ripple attenuation, at the RC buck converter design point, the different $f_{sw}$ that have to be used for each converter, allowing a reduction from 12MHz to 4MHz for the RC buck converter as shown in Figure 6. It can be seen on Figures 6 and 7 that there is a good correspondence between them up to 30MHz, higher than the range of design. The simulated models include the parasitic components of the passive components, as the parasitic capacitances of the coupled inductors, obtained from measurements to achieve a good model to measurement correspondence.

![Image of experimental results](image2)

**Figure 6.** Comparison between measured and simulated transfer function $V_o/V_{sw}$ (magnitude) of the SR buck converter with ripple cancellation and the simulated equivalent design for the conventional buck converter.

First of all, a validation of the proposed converter has been done for $f_{sw}=4$MHz, $V_{in}=24$V and DC output voltage in a wide output voltage range to demonstrate zero output voltage ripple operation. A resistive load of 5Ω has been selected for all the tests. Figure 8 shows a photograph of the experimental prototype.

![Photograph of converter](image3)

**Figure 8.** Photograph of the ripple cancellation buck converter.

Figure 9 and 10 show $V_o$, $i_1$ and $i_2$ and low side drain-source voltage ($V_{ds,LS}$) for 0.5 and 0.3 duty cycle respectively. It can be seen that in both cases the current ripple of $i_1$ and $i_2$ are equal in magnitude and phase shifted 180° so current ripple cancellation and almost zero ripple $V_o$ are obtained.

![Main waveforms](image4)

**Figure 9.** Main waveforms of ripple cancellation buck converter for $f_{sw}=4$MHz, $V_{in}=24$V and $d=0.5$; $V_{ds}$ (10V/div), $V_o$ (2V/div), $i_1$ & $i_2$ (1A/div); 100ms/div.
The first issue can be solved by characterizing the output voltage for low duty cycles at different loads and compensating them using a digital control implementation.

The second issue can be considered a limitation of the buck converter for this type of application at low loads. With higher output currents this effect is decreased as the output capacitance of the MOSFET is discharged faster and therefore the contribution of the decreasing slope of \( V_{ds} \) to \( V_o \) is decreased. In a conventional point of load buck converter application, this limitation is almost overcome by the higher output loads.

For the proposed application, low duty cycles correspond to the lower output current operation points, as the load is considered resistive [11]. Due to the high switching frequency, in the range of MHz, as it can be seen in Figure 12, the falling slope of \( V_{ds} \), due to the slow output capacitance discharge of the low side MOSFET, can affect to the converter operation in two ways, both shown in Figure 13:

- Low accuracy of the output voltage for lower duty cycles due to the contribution of the \( V_{ds} \) discharging slope in the output voltage
- Limitation in the minimum output voltage of the converter
Figure 15. Experimental measurements of the conventional buck converter; Vo (2V/div); Io (500mA/div); 1μs/div

It can be seen the no output ripple for the RC buck converter compared to the noisy waveform of the conventional buck converter. In Figure 16 are also shown I1 and I2 currents for the RC buck converter and in Figure 17 the small ripple in V_Cb due to the reduction of its capacitance.

Figure 16. Experimental measurements of the buck converter with ripple cancellation circuit: 5V/div for Vo and 500mA/div for currents; 400ns/div

Figure 17. Experimental measurements of buck converter with the ripple cancellation circuit with sinusoidal output voltage (Vcb (5V/div); Ir (500mA/div); 1μs/div

Figure 18. Experimental measurements of the buck converter with the ripple cancellation circuit with a 64-QAM signal; Vo (2V/div); 20μs/div

As the main advantages of this converter are a high bandwidth and a high efficiency, this last characteristic has also been validated. The efficiency of the conventional buck converter switching at 12MHz and the efficiency of the SR buck converter with ripple cancellation circuit have been measured and compared for V_in of 10V, 15V and 20V, 50% of duty cycle and f_sw of 12MHz and 4MHz respectively.

<table>
<thead>
<tr>
<th>V_in (V)</th>
<th>Buck RC</th>
<th>Conventional buck</th>
<th>Efficiency difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td>82.45</td>
<td>66.5</td>
<td>15.95</td>
</tr>
<tr>
<td>15</td>
<td>86.3</td>
<td>73.9</td>
<td>12.4</td>
</tr>
<tr>
<td>20</td>
<td>87.8</td>
<td>75.3</td>
<td>12.5</td>
</tr>
</tbody>
</table>

As it can be seen, much higher efficiency is obtained for the proposed converter compared to the conventional buck converter for the same bandwidth.

V. CONCLUSIONS AND FUTURE WORK

It has been presented a design for SR buck converter with output current ripple cancellation circuit to obtain a high bandwidth with a reduced switching frequency compared to the conventional buck converter for an envelope amplifier application. As it has been demonstrated, the reduction of the switching frequency allows an increase in the efficiency and in the reliability of the converter, compared to other linear and high dissipative solutions for an envelope amplifier. The state of the art design of the ripple cancellation network has been compared with the proposed new design, where the ripple cancellation depends on several additional circuit parameters that can be optimized, allowing a f_sw reduction (validated a 12MHz to 4MHz reduction in this work). Experimental validation is provided showing the good performance of the converter for DC and for a sinusoidal output reference. Additionally it has been tested for a 64-QAM signal to validate the proposed converter for the envelope amplifier application. It has been compared experimentally the efficiency increase from 12.4% to 15.95% (10V_in to 20V_in) over the buck converter equivalent design. Future work will
consider the adaptation of this solution to higher $f_{sw}$ and bandwidth.