properly treated before nucleation (i.e. single domain structure formed by double steps in the absence of silicon oxide) this growth-mode minimizes the appearance of planar defects, which otherwise, might ruin the electrical behavior of the solar cell offering a defect-free template for the integration of the GaAsP graded buffer.

5.2. GaP on Si state-of-the-art

The nucleation of GaP on Si was widely studied in the past, regaining some importance recently [Dixit’06 Grassman’09b Lee’97 Narayanan’02a Németh’08 Soga’96 Takagi’98 Takano’09a Volz’11 Yamane’10]. The vast majority of the efforts of the different groups trying to materialize the strategy herein presented (i.e. the integration of III/V semiconductors on silicon by means of a GaP nucleation layer) have been directed towards the minimization and confinement of crystal defects in the structure. In this sense, high structural-quality nucleation layers have been reported, achieving promising results in the reduction of dislocation density and annihilation of APDs [Grassman’09b Lee’97 Németh’08 Soga’96 Sugo’88 Takano’10 Volz’11 Yamane’10].

Different approaches have been reported in the literature to be successful for obtaining a high quality two-dimensional GaP nucleation layer, though contradictory visions concerning the growth parameters have been given. The growth-mode (continuous or pulsed), the nucleation temperature, the pre-exposure precursor nature (V-group or III-group) or the V/III ratio are some examples of this discrepancy. Moreover, many groups have proven the beneficial effect of growing a homoepitaxial Si layer, using SiH₄ or SeH₆ as Si precursor, on top of the Si substrate to favor the nucleation of a defect-free GaP layer. This layer will bury any residual traces of contaminant such as carbon or oxygen, whose presence may ruin the quality of the III-V epitaxial layer. Moreover, due to the intentional doping of this layer, it will act as the silicon emitter of the bottom subcell (as an alternative to diffused emitters).

Starting with the nucleation mode, two alternatives exist: continuous mode, where group-V and group-III atoms are supplied at the same time for the GaP nucleation; or pulsed growth where atoms are alternatively introduced in the reactor chamber. Despite the structural and morphological quality of the III-V layer will be largely influenced by the growth-mode, promising results have been reported for both approaches. On the one hand, the pulsed growth-mode is based on the separate introduction of Ga and P atoms into the reactor chamber in an alternating sequence for guaranteeing a layer-by-layer coverage. This technique receives the name of migrated enhanced epitaxy (MEE) or atomic layer epitaxy (ALE) as it is applied in a
MBE or a MOVPE reactor, respectively. This type of growth precludes the formation of nucleation-related defects, such as antiphase domains, by eliminating adverse nucleation sites [Grassman'09b Takagi'98]. Accordingly, the resulting GaP layer growth by pulsed growth covers the silicon surface more uniformly compared to the continuous mode, preventing the formation of a 3D GaP layer [Grassman'09b Takagi'98]. The success of this technique lies in the combination of the pulsed growth with precursors which allow the use of low temperatures, resulting in sharp interfaces.

On the other hand, the continuous growth-mode approach is based on the introduction of both precursors on the reactor chamber at the same time. Nevertheless, as a result of the simultaneous introduction of both atoms from the very beginning of the process, the growth will proceed in a 3D island-type [Soga’94b]. Accordingly, in this approach, Si substrates are generally submitted to an initial flux of one of the precursors (either V-group or III-group) so the Si surface gets fully covered by P (or Ga) atoms. In this sense, the wetting of the GaP on silicon is highly increased, promoting the formation of a 2D nucleation layer [Soga’94b]. Despite both alternatives (i.e. P-pre-exposure and Ga pre-exposure) have been considered so far in the literature for the nucleation of GaP on Si, it has been reported that prolonged exposures of Si surfaces to TMGa will result in the appearance of pits in the substrate as a result of the Si being etched by the formation of Ga drops [Volz’11 Yamane’09]. In this sense, the amount of Ga deposited during the first monolayer has to be carefully controlled to avoid the formation of metal droplets. On the other hand, the pre-exposure of Si surfaces to PH₃ has been reported to produce excellent results [Soga’94b Takano’09a Yamane’09]; however, the use of large quantities of PH₃ has been shown to result in surface roughening (see section 4.3 in Chapter 4), which, in turns yields to island faceting and v-shaped pit formation [Soga’94b Takano’09a]. Accordingly, a trade-off between not too much PH₃ to avoid the roughening of the Si surface; but enough PH₃ to cover Si surface with P atoms for increasing the wetting of subsequent GaP has to be achieved. Moreover, the exposure of silicon substrates to an initial arsine (AsH₃) flow has been considered to circumvent the drawbacks encountered on the PH₃ pre-exposure [Kohama’88]. In this sense, the arsenic (As) resulting from the pyrolysis of arsine, will bond to the silicon surface atoms, forming very stable and strong Si-As bonds (stronger than Si-P), which, in turn, will favor the formation of a two-dimensional nucleation layer with a good crystalline quality [Kohama’88]. The advantage of this approach is that arsine does not attack silicon and consequently, the exposure of Si substrates to this precursor does not produce roughening. Nevertheless, not too much work has been done in this direction.
Regarding the nucleation temperature, two main approaches can be roughly defined: low temperature (450-600 °C), and high temperature approach (700-900 °C). On the one hand, low temperature growth processes have been extensively investigated over the last decades [Grassman'09b Kohama'88 Narayanan'02a Németh'08 Sugo'88 Takagi'98 Volz'11 Yamane'10 Yamane'09]. This type of growth is effective to obtain a smooth surface. Moreover, the use of low temperatures reduces the possibility of undesired cross-doping contamination (diffusion across the interface), the diffusion of impurities, and thermal mismatches [Volz'11]. Nonetheless, structural defects (such as stacking faults) appeared at the interface in most of the cases [Takano'09b].

On the other hand, nucleation at temperatures above 700 °C is believed to yield 3D growth as a result of P atoms desorption from the Si surface, degrading the crystal quality of the nucleation layer [Soga'94b Takano'09b]. However, some authors have reported high-quality and smooth GaP layers when using very high V/III ratios for temperatures up to 900 °C [Dixit'06 Lee'97 Soga'94b Takano'09b].

The use of low temperatures needs the use of a special P-precursor that can be thermally cracked at low temperatures, so an efficient pyrolysis is obtained for growing a stoichiometric GaP layer. In this sense, the use of phosphine is restricted as a result of the inefficient decomposition of this compound at low temperatures [Stringfellow'89]. Accordingly, Tertiarybutylphosphine (TBP), is generally used as the group-V precursor given its high cracking efficiency at low temperatures. Contrarily, the nucleation at high temperatures allows the use of PH₃ as the group-V precursor, since at high temperatures, the pyrolysis of phosphine is expected to be completed.

The election of a high V/III ratio (and more precisely, high P/Ga ratios) lies in the stability of the species to form a continuous layer under these conditions; contrarily to what happens at lower ratios, where the species are unstable and nucleate discretely. In the last case, unstable species migrate on the silicon surface, combining with the GaP islands, yielding to a 3D growth. Accordingly, the idea is to reduce the migration lengths of the GaP clusters to form a connecting layer between 3D islands. This reduction is achieved by either increasing the available P (i.e. by increasing the V/III ratio), the adsorption of P is enhanced, resulting in a continuous, 2D GaP nucleation on Si substrates), or by increasing the residence time of the source gas on the substrate (i.e. by increasing the gas pressure). In this sense, Figure 5.4, adapted from [Soga'93], evidences the dependence of the GaP/Si growth-mode with the V/III ratio at a constant pressure of 100 mbar (Figure 5.4.a) and as a function of the gas pressure (Figure 5.4.b).
To summarize, Table 5.I gathers the diverse alternatives reported for the successful integration of GaP on Si substrates. These approaches include continuous and pulsed growth modes; high and low temperature nucleation; or the exposure to different precursors before nucleation.

As it has been presented, there is a wide range of variables involved in the GaP/Si nucleation process, which have been reported to be successful in the integration of GaP on Si substrates under certain circumstances, depending on the MOVPE system. Accordingly, the idea of this chapter is to assess which is the most suitable approach (and the optimum conditions) to obtain a high quality GaP nucleation routine so it can be transferred to our MOVPE system respecting the major purpose of this thesis, which is the development of a simple and easy routine for the III-V/Si integration for its eventual transference to the PV industry. In this respect, the silicon homoepitaxial layer will not be considered in this approach, since it add some extra complication to the process, mainly due to the necessity of working with two different reactor chambers for avoiding cross-contamination. Consequently, the emitter of the proposed solar cell will be formed by P diffusion, as described by Chapter 3. In this case, the removal of the contaminants will be achieved by a proper chemical cleaning and a subsequent thermal annealing at high temperatures for promoting the step-doubling. Moreover, unlike many authors which consider TBP precursor for the nucleation of GaP layers at low temperatures, PH₅ will be used as the P-precursor for GaP nucleation regardless the temperature of the process, due to the absence of a TBP line in the actual configuration of our MOVPE system.
Table 5.1 GaP on Si nucleation state-of-the-art, considering different approaches in terms of nucleation temperature, growth-mode or the pre-exposure to a group-V or group-III precursor.

<table>
<thead>
<tr>
<th>Ref</th>
<th>Reactor</th>
<th>Growth-mode</th>
<th>Temperature</th>
<th>Pre-exposure precursor</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>MEE</td>
<td>Cont.</td>
</tr>
<tr>
<td>[Soga’94b]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Lee’97]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Dixit’06]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Takano’09a]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Kohama’88]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Sugo’88]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Németh’08]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Yamane’10]</td>
<td>MBE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Volz’11]</td>
<td>MOVPE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Takagi’98]</td>
<td>MBE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Narayanan’02a]</td>
<td>PCBE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Yamane’09]</td>
<td>MBE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[Grassman’09b]</td>
<td>MBE</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

5.3. GaP on Si Nucleation Studies

A first aspect to consider for obtaining a high quality epitaxy is the preparation of silicon substrates. This treatment involves, on the one hand, an exhaustive chemical cleaning for getting rid of the silicon oxide and other possible contaminants; and on the other hand, a thermal
treatment for promoting the step doubling of Si surfaces, obtaining in this way, a single-domain structure. Nonetheless, even working with a perfectly clean, oxide-free and a single-domain silicon surface, might be not enough for ensuring a high quality two dimensional growth. In this sense, not only a proper substrate preparation is required, but also an adequate nucleation routine. However, this epitaxial routine is not universal as shown in the previous section, but strongly depends on the reactor configuration, the MOVPE atmosphere, etc... As an example of this discrepancy, the ALE low-temperature strategy has been repeatedly reported in the literature [Grassman’09b Narayanan’02a] to be the most successful approach for obtaining a defect-free continuous GaP layer; nevertheless, other groups have been published that low temperature nucleation results in the formation of structural defects at the interface [Akiyama’84 Takano’09b]. Moreover, these groups reported excellent results on GaP nucleation layers based on the continuous growth-mode at high temperatures [Dixit’06 Lee’97 Soga’94b Takano’09a]. These differences can be extended to each parameter involved in the GaP nucleation routine (i.e. precursor nature for the pre-exposition of the silicon surface before nucleation, III/V ratio, GaP critical thickness, etc...). Accordingly, an extensive experimental study has been carried out for determining which are the best conditions for obtaining a high-quality GaP layer in our particular MOVPE system.

With the aim of evaluating the morphological and structural quality of the epitaxially grown samples, they have been individually characterized by means of different microscopic techniques. In this sense, most of the samples have been firstly characterized by Atomic Force Microscopy to have a broad idea of the surface morphology. This simple technique, which does not require specific sample preparation, gives us a first idea of the growth-mode (i.e. 2D or 3D growth), the surface roughness (in case a continuous layer has been deposited), or the island distribution (in case a 3D growth is obtained) along the surface. Complementary, Scanning Electron Microscopy (SEM) has been used for a more detailed characterization for certain samples. This technique, which is more complicated in terms of microscope manipulation, sample preparation or data analysis; allows us to analyze not only the surface from a top view scan, but also from a cross sectional analysis. This last characterization mode requires the use of an specific equipment; accordingly, only few samples where characterized by this method. Finally, Transmission Electron Microscopy (TEM), which apart from a detailed morphological characterization gives information about the structural quality of the nucleation layer by means of the cross-section high-resolution analysis, has been used occasionally in this thesis. This technique is time consuming, expensive, requires an extremely laborious sample preparation and the presence of a technician in charge of the microscope manipulation. These factors make
difficult to characterize all samples by this technique; accordingly, only the most relevant samples were selected for TEM characterization.

Based on the strategies described in Section 5.2, there is a wide range of possibilities for the GaP growth, involving the nucleation mode (i.e. continuous or pulsed), the pre-exposition of the wafer to group-V or group-III precursors, the nucleation temperature, the III/V ratio, etc... In this work, the growth-mode has been selected as the general criterion for classification. In this sense, experiments have been classified according to weather they have followed a continuous or a pulsed GaP growth. Within each section, the role of different parameters (temperature, V/III ratio, layer thickness) on the nucleation quality will be assessed.

5.3.1 Continuous growth-mode

The continuous growth-mode has been reported to be the most recurrent approach in the past for the nucleation of GaP on Si by epitaxial growth. Nonetheless, according to literature, this is a very heterogeneous technique. That is to say, to date, there is not a defined ubiquitous routine for obtaining a high quality GaP nucleation layer; on the contrary, results strongly depend on the MOVPE system. In this respect, what has been reported to be successful for obtaining a 2D layer in one case, might lead to a 3D island-type growth in a different MOVPE system.

In this approach, both precursors are introduced simultaneously into the reactor chamber; however, substrates are generally exposed to a short flux of one of the precursors (TMGa, PH₃ or AsH₃) for improving the wetting of the subsequent GaP layer, favoring in this way, the formation of a 2D nucleation layer. In this section, the three different approaches are discussed and the most convenient option for our system is assessed.

5.3.1.1. PH₃ pre-exposition

According to [Takano’09a], the exposure of Si substrates to PH₃ molecules is necessary for guaranteeing a high quality nucleation. By exposing Si to PH₃, the wetting of the GaP-Si is increased since the Si substrates gets fully covered by P dimmers, which rapidly capture the migrating specie (in our case Ga), favoring a 2D nucleation [Soga’94b]. On the contrary, when samples are not subjected to this pre-exposure, and thus, both precursors (i.e. TMGa and PH₃) are simultaneously introduced into the reactor chamber, the diffusion species migrate on the Si surface, due to the weak interaction between Si and P or Ga atoms [Soga’94b], nucleating following a 3D growth-type.
The beneficial effect of the P coverage of the Si surface for improving the GaP wetting has been reported either under high temperatures [Dixit’06 Lee’97 Soga’9b Takano’09b] or at low temperatures [Németh’08 Sugo’88 Takagi’98 Yamane’09]. Accordingly, both possibilities have been considered in this work for GaP/Si nucleation. Moreover, some additional parameters involved in the nucleation process have been swept to assess their impact on the nucleation quality. In this respect, Table 5.II lists the most relevant parameters involved in each step, establishing a sign criterion for their classification according to their magnitude.

Table 5.II Sign criterion used to identify samples exposed to phosphine before nucleation.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Time</strong> (min)</td>
<td>30</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>60</td>
<td>+</td>
</tr>
<tr>
<td><strong>Temp (°C)</strong></td>
<td>800</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>830</td>
<td>+</td>
</tr>
<tr>
<td><strong>Time</strong> (s)</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>550</td>
<td>-</td>
</tr>
<tr>
<td><strong>Temp (°C)</strong></td>
<td>600</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>650</td>
<td>++</td>
</tr>
<tr>
<td><strong>V (sccm)</strong></td>
<td>700</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>800</td>
<td>++</td>
</tr>
<tr>
<td><strong>Nucleation</strong></td>
<td>800</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>1200</td>
<td>++</td>
</tr>
<tr>
<td><strong>Time</strong> (s)</td>
<td>500</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>550</td>
<td>-</td>
</tr>
<tr>
<td><strong>Temp (°C)</strong></td>
<td>600</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>650</td>
<td>++</td>
</tr>
<tr>
<td><strong>V (sccm)</strong></td>
<td>700</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td>++</td>
</tr>
<tr>
<td><strong>III (sccm)</strong></td>
<td>800</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>++</td>
</tr>
<tr>
<td><strong>Anneal</strong></td>
<td>1.5</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>2.5</td>
<td>-</td>
</tr>
<tr>
<td><strong>Gas</strong></td>
<td>5</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>++</td>
</tr>
<tr>
<td><strong>Growth</strong></td>
<td>300</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>660</td>
<td>-</td>
</tr>
<tr>
<td><strong>Time</strong> (s)</td>
<td>720</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>780</td>
<td>++</td>
</tr>
<tr>
<td><strong>Temp (°C)</strong></td>
<td>300</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>600</td>
<td>-</td>
</tr>
<tr>
<td><strong>V (sccm)</strong></td>
<td>675</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td>++</td>
</tr>
<tr>
<td><strong>III (sccm)</strong></td>
<td>450</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>++</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>+</td>
</tr>
</tbody>
</table>

According to Table 5.II, parameters involved in sample preparation, GaP nucleation, subsequent anneal for recrystallization and the eventual GaP growth have been considered. Due to the big number of variables to sweep and targeting an easy evaluation of the role of each parameter on the general process, this section has been divided into four different parts, each of
one aimed to study the effect of a variable (or a group of them) included in one of these steps: 1) surface preparation, 2) GaP nucleation, 3) subsequent anneal and eventual GaP growth, and 4) finally, the last part of this section integrates all the information extracted from these experiments to develop an optimized routine for GaP nucleation.

### 5.3.1.1.a. Sample preparation

An important point which has been recurrently treated in this work is the preparation of Si substrates for guaranteeing a proper epitaxial growth. Apart from the chemical treatment, intended to get rid of oxide and other contaminants, the thermal preparation of Si wafers has been reported to be of special relevance for minimizing the appearance of planar defects (such as anti-phase domains). This preparation pursues the formation of a single-domain structure, which is believed to occur during the initial annealing of substrates at high temperature.

Table 5.3 III Description of the sample preparation and MOVPE routine followed by samples included in the first batch of experiments, where wafers have been exposure to phosphine before nucleation.

<table>
<thead>
<tr>
<th>5.3.a</th>
<th>5.3.b</th>
<th>5.3.c</th>
<th>5.3.d</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Cleaning</strong></td>
<td>-</td>
<td>HF</td>
<td>-</td>
</tr>
<tr>
<td><strong>Anneal</strong></td>
<td>Time</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>Temp</td>
<td>-</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>Gas</td>
<td>PH₃</td>
<td>H₂</td>
</tr>
<tr>
<td><strong>Pre-exposure</strong></td>
<td>Time</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Temp</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>V</td>
<td>+</td>
<td>+</td>
</tr>
<tr>
<td><strong>Nucleation</strong></td>
<td>Time</td>
<td>+++</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>Temp</td>
<td>++</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>V</td>
<td>++</td>
<td>+</td>
</tr>
<tr>
<td></td>
<td>III</td>
<td>+++</td>
<td>++</td>
</tr>
<tr>
<td><strong>AFM</strong></td>
<td>RMS (nm)</td>
<td>-</td>
<td>16.49</td>
</tr>
<tr>
<td></td>
<td>Skewness</td>
<td>-</td>
<td>-0.44</td>
</tr>
<tr>
<td></td>
<td>Kurtosis</td>
<td>-</td>
<td>2.87</td>
</tr>
</tbody>
</table>
All samples included in this experiment have been exposed to a long (30 min. to 60 min.) H₂ anneal for ensuring the adequate surface reconstruction (see section 2.4.2 in Chapter 2).

A first batch of experiments, intended to analyze the effect of the surface preparation on the GaP nucleation was carried out. The most relevant experiments have been included in Table 5.III, which summarizes the routine followed for each sample according to the established sign criterion. Moreover, Table 5.III includes the AFM characteristic parameters (RMS, skewness and kurtosis) for each sample with the aim of having a general idea of the surface morphology.

The necessity of performing a chemical cleaning before loading wafers into the reactor has been stated in Chapter 2; nevertheless, with the goal of giving a more enlightening vision of the chemical cleaning effect on the GaP nucleation quality, an initial nucleation experiment was carried out (sample 5.3.a). Due to the lack of experience of the group at this point on growing GaP nucleation layers, the growth conditions were selected according to the literature. An exhaustive TEM characterization of this sample was carried out for analyzing the growth-mode, the crystallographic and the morphological quality of the deposited material. Most relevant images have been included in Figure 5.5.

![Figure 5.5 Cross section TEM analysis of sample 5.3.a. a) General view of the island distribution; b) HR-TEM scan of the GaP/Si interface, revealing the presence of silicon oxide on it; c) detail of crystallographic defects encountered inside the islands.](image)

Leaving aside the poor quality of the GaP layer (Figure 5.5.a), which can be partially attributed to a non-appropriate nucleation routine, an amorphous layer located at the GaP/Si interface (Figure 5.5.b) can be perfectly identified. Such layer is characteristic of a native silicon oxide. It is worth noting at this point that the epitaxial integration of GaP on Si substrates consists on the growth of a crystalline GaP nucleation layer on a crystalline Si substrate. Needless to say that the presence of an amorphous material on top of the Si substrate is highly undesired, since it will ruin the epitaxial process. As a result of the presence of the oxide layer, a 3D growth, formed by
heterogeneous (in size and distribution) islands, occurs. A high density of defects (such as antiphase domains and staking faults) were found inside the islands [Narayanan'02a Narayanan'02b], as evidenced by Figure 5.5.c. Moreover, and related to the presence of the amorphous material, the GaP does not grow following the crystallographic pattern of the substrate, as it should occur when growing a metamorphic material by MOVPE.

At the beginning of this chapter it was claimed that the performance of a chemical cleaning before nucleation is necessary but not sufficient for guaranteeing a high quality growth. This fact can be confirmed by taking a look at sample 5.3.b (Figure 5.6), which followed an appropriate chemical cleaning (i.e. HF dip), but an island-type growth is still observed. This morphology can be explained by a non-adequate nucleation routine. Consequently, Si surface becomes covered by multiple islands, which in some cases coalesce, resulting into a semi continuous layer.

Figure 5.6 AFM topography scans of samples 5.3.b, 5.3.c, and 5.3.d, which have been exposed to phosphine before nucleation. The images in the left column are plain views and the images on the right are 3D representations of the same image. Moreover Z-scale has been included in the left most side. Note that sample 5.3.c has been plotted in a different Z-scale (500 nm) due to the height of the islands.
To further sustain the importance of performing a chemical cleaning before nucleation, and its effect on the nucleation mode, it is enlightening to compare AFM scans (Figure 5.6) of sample 5.3.b (cleaned) and sample 5.3.c (uncleaned), which suffered the same MOVPE routine, excluding the chemical cleaning. Despite neither of both present a high quality nucleation layer, the presence of silicon oxide on the GaP/Si interface in sample 5.3.c degrades the GaP quality, resulting in a heterogeneous 3D growth, consisting on isolated GaP islands which do not coalesce and with a height in the order of 4 times higher than the one measured on sample 5.3.b (even they have followed the same MOVPE routine).

For having a more precise idea of the growth-mode and for analyzing the crystallographic quality of the islands, sample 5.3.b was selected for a more detailed characterization by cross section TEM (Figure 5.7).

![Cross-section TEM characterization of sample 5.3.b](image)

Figure 5.7 a) Cross-section TEM characterization of sample 5.3.b, revealing the presence of island along the surface; b) High resolution TEM image of the GaP/Si interface to prove the absence of silicon oxide; c) Detail of a GaP island where different type of defects were revealed.

The presence of GaP islands distributed along the Si surface is now corroborated by TEM images (Figure 5.7.a). The islands are irregular in terms of height and length, as it was anticipated by AFM scans. The analysis of the GaP/Si interface by high resolution TEM (HR-TEM) confirms the absence of silicon oxide at the Si surface (Figure 5.7.b). Moreover, a continuation of the silicon crystallographic structure on the GaP islands is clearly observable. Finally, by looking in detail into a GaP island (Figure 5.7.c), it can be detected a big number of defects, which are generated at the GaP/Si interface and continue up to the top GaP surface. Accordingly, this sample is an example of a 3D growth-type, where islands exhibit poor crystallographic quality. Nevertheless, at this point we can unequivocally confirm that the cleaning procedure is enough to guarantee an oxide-free silicon surface.
A second aspect which has to be considered for sample preparation is the attainment of a smooth surface, so the III-V growth can occur under the best conditions. In this respect, in Chapter 3, it was confirmed that while the initial H₂ annealing promotes the formation of a smooth surface; the exposure of substrates to phosphine at high temperatures produces an important surface roughening due to Si dimmer displacement. In this respect, it was reported the beneficial effect of exposing wafers to an additional H₂ anneal at high temperatures, after the emitter formation, for reconstructing Si surfaces.

The effect of the surface roughness on the GaP nucleation mode can be easily assessed by comparing sample 5.3.b to sample 5.3.d. Both of them have followed the same nucleation routine; however, sample 5.3.d was annealed in the presence of phosphine prior to the nucleation step, to form the emitter. Significant differences can be observed by comparing the analysis parameters included in Table 5.III. In this sense, the resulting surface becomes rougher when a phosphine anneal is performed (samples 5.3.d). Moreover, by comparing AFM scans important differences in the morphology can be observed (Figure 5.6). It is clear that neither of both samples are grown following a layer-by-layer nucleation; however sample 5.3.d presents a rougher surface, showing a more abrupt profile. Note that, despite both samples have followed the same nucleation routine, with the same growth rate and nucleation time, the island height for sample 5.3.d is roughly twice the one measured for sample 5.3.b, indicating that GaP grows more vertically than horizontally (i.e. incoming GaP is accumulated on the already nucleated sites, rather than being deposited on naked areas).

According to these results, the importance of nucleating on a smooth Si surface is demonstrated. This fact supports the idea of exposing wafers to an additional H₂ anneal after the emitter formation to reconstruct the surface, so the roughness of the Si surface is brought back to values comparable to the one measured before the emitter formation. For simplicity, all nucleation experiments hereafter included have been done on inactive silicon substrates (i.e. no emitter and thus, no PH₃ exposure); however, these experiments could be eventually implemented on active silicon substrates since smooth surfaces can be easily obtained after the emitter formation as described in Chapter 4.

5.3.1.1.b. GaP nucleation

In the previous section it has been proven the necessity of performing a chemical cleaning before nucleation and the effect of the surface roughness on the GaP nucleation. Accordingly, this study allowed us to define a proper routine for sample preparation; so parameters within this step are no longer a variable of the process. Consequently, hereafter wafers will be cleaned
using a HF dip, and will be annealed under H$_2$ at 800 °C for 30 min. (the reason for reducing the annealing time is because 30 min. has been proven to be enough to guarantee the desired surface reconstruction).

Once a generic procedure for surface preparation has been established, we are going to focus on the GaP nucleation routine itself. Within this frame, a second batch of experiments was carried out with the aim of analyzing the effect of the temperature and the deposited thickness on the GaP nucleation quality. Table 5.IV lists the most relevant experiments within this batch, summarizing the MOVPE routine followed for each case as well as the characteristic AFM parameters. AFM scans of the most relevant samples are included in Figure 5.8. Z-scale is included in the left-side of each sample. Moreover, right column represents a 3D recreation of the topography scan.

Table 5.IV Sample preparation and MOVPE routine followed by samples included in the second batch of experiments.

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The role of the nucleation temperature on the growth-mode can be assessed by taking a look at the AFM parameters included in the bottom part of Table 5.IV. As expected, temperature plays a major role on the nucleation mode and the surface roughness; moving from an initial RMS of 3.14 nm for sample 5.4.a, which was nucleated at the lowest temperature (500 °C) up to 10.47 nm for the sample nucleated at the highest temperature (700 °C), including intermediate values, such as 8.06 nm for sample 5.4.c, which was nucleated at a moderate temperature (600 °C). Noticeably, as the temperature is higher (sample 5.4.e), the adatoms are more mobile on the surface. Consequently, once atoms are adsorbed on the surface, they will travel along it to
eventually find the most favorable nucleating sites. On the contrary, at low temperatures (sample 5.4.a), atoms will not have enough energy to travel long distances along the surface and thus, once an atom reaches the surface, it will be fixed in this particular site. This explanation is consistent with the morphology shown in AFM scans included in Figure 5.8. In accordance with this hypothesis, sample 5.4.a and 5.4.b show are more uniform distribution of islands, of different sizes and orientations. On the contrary, sample 5.4.e, which is nucleated at high temperature (700 °C), shows totally oriented features, nucleated on the step edges and grow parallel to this direction. To further sustain this explanation, samples have been also characterized by SEM. Resulting scans have been included in right-side of Figure 5.8.

Finally, sample 5.4.f was nucleated under the same conditions than sample 5.4.b (i.e. low temperature), but for a longer duration, which is manifested in a bigger size of the islands and a more covered surface, as clearly shown by SEM image (Figure 5.8). Moreover, tilted SEM images add some new information concerning the island size, height and distribution (Figure 5.9), distinguishing two main heights ranges: short islands (10-20 nm); and high islands (40-50 nm); both of them below the critical thickness.

![Figure 5.9 TEM and SEM characterization of sample 5.4.f. a) High resolution TEM image of the GaP/Si interface to prove the absence of silicon oxide; b) and c) TEM details of the GaP islands; d) and e) tilted SEM images of sample 5.4.f to show the island distribution along the Si surface and the different heights encountered on the sample.](image-url)
The HR-TEM analysis of this sample (Figure 5.9.a to c) confirms the island-type 3D growth—in accordance to AFM and SEM scans— with a multiple number of crystallographic defects in the GaP islands (Figure 5.9.b). These defects (staking faults), which are generated at the GaP/Si interface and propagate in the growth direction, result from an alteration of the normal stacking sequence of atoms, and are usually observed within islands before they coalesce [Narayanan'02b]. It is worth highlighting the occasional presence of small defect-free islands (Figure 5.9.a). These small nuclei are grown on top of a clean Si surface, without developing planar defects. Note that despite the initial anneal duration has been significantly reduced (30 min.), the analysis of the GaP/Si interface by HR-TEM clearly demonstrates the absence of silicon oxide on the surface (Figure 5.9.a).

In this study, a correlation between nucleation morphology and temperature has been established. Moreover, the evolution of the initial features with the nucleation duration has been evaluated. In summary, these routines show a 3D growth, formed by heterogeneous islands (in distribution, height and size), which present a poor crystallographic quality, confirmed by the presence of multiple defects (mainly stacking faults) which are originated at the GaP/Si interface and propagate along the island up to its top. Nonetheless, the use of lower temperatures results in a more homogeneous growth and a smoother surface; being preferred to the high temperature approach. In all cases, it has been observed a continuation of the Si crystallographic pattern on the GaP islands as a result of an epitaxial growth, occurring in the absence of oxide.

5.3.1.1.c. Subsequent anneal and eventual GaP growth

In agreement with previous explanations, the growth conditions must be selected to promote the formation of a layer-by-layer growth to obtain a smooth, 2D nucleation layer. Nevertheless, different approaches have been reported in literature to be successful in the formation of a 2D layer, following either a high- or a low-temperature approach; a high or a growth rate, etc... In practice, some conditions might be preferable; for example, low nucleation temperature and high nucleation rate are generally preferable, though their use might lead to the formation of a polycrystalline GaP layer. Nevertheless, it has been reported that if the GaP thickness is relatively thin, and just if this material covers all the Si surface, then the GaP can be re-crystallized by exposing samples to an additional annealing at high temperature [Yamane'10]; resulting in a 2D nucleation layer.

Accordingly, a third batch of experiments, aimed to analyze the effect of a high temperature annealing after the nucleation step on the GaP morphology, was carried out (Table 5.V).
Table 5.V Description of the sample preparation and MOVPE routine followed by samples included in the third batch of experiments, which considers an additional bake after nucleation for crystallization. AFM analysis parameters are also included.

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The main purpose of this anneal was to favor the migration of deposited atoms to homogenize the features already nucleated, promoting the island coalescence and thus, enhancing the formation of a continuous layer. The environment under which the annealing is performed (i.e. PH₃ or H₂) will affect the migration of the atoms, and hence, could impact the final morphology of the GaP. Consequently, both possibilities were considered (sample 5.5.a or 5.5.c and sample
5.5.b respectively). Once the different GaP nucleation layers were annealed, they were used as templates for a subsequent GaP growth at a higher temperature (samples 5.5.d, 5.5.e, and 5.5.f). The idea was to reproduce the two-step growth, which demonstrated excellent results on the integration of single-domain GaAs on Si substrates [Akiyama’84]. This two-step method was already used for GaP/Si integration [Németh’08 Sugo’88] and consists on the nucleation of a thin GaP layer (below the critical thickness) at low temperature, using low growth rates; then, temperature and growth rates are generally increased for the growth of a thicker GaP layer. Following this approach, sample 5.5.c was used as the base for growing a thicker GaP layer. This growth was done at high temperatures (sample 5.5.d); and at lower temperatures (sample 5.5.e) to assess the impact of this parameter on the GaP morphology.

Table 5.V lists the most relevant experiments within this batch, summarizing the MOVPE routine followed in each case, as well as the characteristic AFM parameters. Corresponding AFM scans are included in Figure 5.10. Z-scale is included in the left-side of each sample. Moreover, right column represents a 3D recreation of the topography scan.

An initial test for proving the effect of the anneal on reconstructing the GaP nucleation layer can be easily done by comparing sample 5.4.b (Figure 5.8), which was not annealed after GaP nucleation, with sample 5.5.a (annealing in PH3) and sample 5.5.b (annealing in H2). Far from improving the nucleation morphology, GaP features remain unchanged in the presence of phosphine at high temperatures (sample 5.5.a or sample 5.5.c) and, even worst, they are desorbed from the silicon surface, when annealed under hydrogen at high temperatures, resulting into a less covered surface (sample 5.5.b), as shown in Figure 5.10. As it generally occurs in a III-V MOVPE environment, in the absence of group-V overpressure (as is the case), the group-V element (i.e. P) tends to desorbs form the surface. In this scenario, Ga atoms could either diffuse towards the silicon or be re-evaporated. Consequently, if the annealing of the nucleation layer is performed in hydrogen (i.e. in the absence of group-V overpressure), this atmosphere will favor the desorption of the nucleated features, leading to a less covered surface, as it was demonstrated (Figure 5.10).

As a result of the annealing inefficiency on smoothing and homogenizing the GaP nuclei, the addition of a second growth step on the nucleated surfaces is not expected to favor the formation of a continuous nucleation layer. On the contrary, the growth of a new layer on an island-type surface will result into a more abrupt profile, aggravating the GaP morphology. This theory can be now confirmed by taking a look at AFM scans of sample 5.5.d and sample 5.5.e. In accordance with the previously discussed relationship between nucleation temperature and growth-mode, increasing the growth temperature implies a more heterogeneous growth (sample
5.5.d), where atoms deposit on already nucleated sites (energetically favorable places), promoting the divergence (in terms of height) between covered and non-covered sites (Figure 5.10).

Figure 5.10 AFM topography scans and SEM images of samples 5.5.a, 5.5.b, 5.5.d, 5.5.e, and 5.5.f which has been subjected to a PH₃ pre-exposure before nucleation. Images in the left column (which includes the Z-scale of the scan) are plain views; images on the center row are 3D representations of the same image; finally the right column corresponds to SEM plain view images.

To finally prove the inefficiency of the annealing on smoothing the initial GaP surface and to discard that this step has any benefits on the second growth step, it is useful to compare sample 5.5.e and sample 5.5.f, which have followed the same nucleation routine, excepting for the annealing step between GaP nucleation and growth. Despite an island-type growth is observed in both cases, sample 5.5.f shows the onset of island coalescence. Moreover, a substantial reduction of the GaP roughness is observed in the last sample (Table 5.V), indicating a more
uniform distribution of islands along the silicon surface, which can be also confirmed by SEM images included in Figure 5.11. Cross section SEM images confirm the presence of many islands, which in some cases coalesce. Two different height ranges were primarily identified (60 nm and 100 nm); being both of them below the critical thickness.

Figure 5.11 SEM characterization of sample 5.5, at different magnifications including height measurements by tilted SEM (a, b); and cross section SEM (c, d).

In summary, the beneficial effect of the high temperature annealing for GaP material re-crystallization can be discarded. The use of a high temperature anneal, in the absence of group-V overpressure, after nucleation leads to a reevaporation of the deposited material. Moreover, the beneficial effect of the two-step growth process under this particular nucleation conditions can also be discarded. That is to say, if a continuous 2D nucleation layer is not obtained during the nucleation process, the growth of a thicker GaP layer will not result in a 2D layer. On the contrary, the 3D growth will be exaggerated, favoring the divergence (in terms of GaP thickness) between covered and un-covered areas.
5.3.1.1.d. Optimization of the GaP nucleation routine

Finally, with the idea of marring up all the knowledge extracted from previous studies, a final set of experiments was carried out. Accordingly, after performing a chemical cleaning (HF dip); samples were annealed in hydrogen for 30 min. to promote the surface reconstruction and to guarantee a smooth Si surface for impending GaP growth (Table 5.VI).

Table 5.VI Description of the sample preparation and MOVPE routine followed by samples included in the fourth batch of experiments, where wafers were exposed to phosphine before nucleation. AFM analysis parameters are also included.

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This last batch focuses on the low temperature approach, since it proved to result in a more controllable and homogenous nucleation. The performance of an additional annealing after the first nucleation step was discarded as a result of its reported inefficiency. Nonetheless, some
samples were subjected to a two-step growth process (i.e. GaP nucleation + growth). The more important novelty of this strategy is the increase of the nucleation time (with respect to previous experiments) to check weather by increasing the GaP thickness at low temperatures, the morphology evolves towards a continuous GaP layer. The most relevant experiments of this last batch have been included in Table 5.VI, which summarizes the routine followed for each sample according to the established sign criterion. Moreover, Table 5.VI includes the AFM characteristic parameters (RMS, skewness and kurtosis) for each sample with the aim of having a general idea of the surface state. Corresponding AFM scans and SEM images have been summarized in Figure 5.12.

On the one hand, the role of the nucleation duration on the evolution of the morphology is evaluated. In this case, sample 5.6.a and sample 5.6.b used the same GaP nucleation routine, except for the nucleation time, being roughly twice longer for the latter. This increase does not turn into an improvement of the surface morphology; contrarily, a significantly increase of the sample roughness was observed for sample 5.6.b (Figure 5.12). This can be explained due to the high roughness measured just after the first nanometers of GaP deposited on the Si surface (sample 5.6.a), covering it uniformly but resulting into a 3D growth-mode. Following previous explanations, an increase of the nucleation time does not favor the smoothing of the surface when a 3D growth-mode is being observed; under those circumstances, the longer the nucleation duration, the higher the surface roughness.

According to the literature, the two-step growth technique has been reported to be successful for improving the crystallographic quality of the nucleation layer by reducing the GaP dislocation density. This was achieved by growing an initial thin (i.e. thinner than the critical thickness) GaP layer at low temperature, so a layer-by-layer nucleation is obtained. The total desired GaP thickness is obtained by the addition of a subsequent step at higher temperature. This growth does not longer present the problems related to the growth of a polar on a non-polar substrate, since the GaP is now grown on a defect-free GaP template. From previous experiments, we know that this two-step process is not effective when GaP has been nucleated following a heterogeneous island-type 3D growth. In those cases, the addition of the second step at higher temperatures will aggravate the morphology, obtaining a very rough morphology. Nevertheless, in the present scenario, a continuous (but very rough) nucleation layer was observed (sample 5.6.a); accordingly, the two-step approach was tested again under these circumstances. In this sense, sample 5.6.c and sample 5.6.d, which have followed a low temperature (i.e. 550 °C) nucleation routine, similar to the one reported in sample 5.6.a (except for the PH₃ partial pressure during pre-exposure), were subjected to a growth step at higher temperature (i.e. 675
°C). The main variable changed between samples 5.6.a and 5.6.d is the deposited thickness of the GaP (higher in 5.6.c) and the group-III partial pressure (higher in 5.6.d). According to the SEM images presented in Figure 5.12, the resulting surfaces have experienced a significant increase of the nuclei size (as compared to sample 5.6.a), forming a “more” continuous layer. Nonetheless, this nuclei increase has turned into a rougher surface (RMS roughly increased twofold).

Figure 5.12 AFM topography scans and SEM images of samples 5.6.a, 5.6.b, 5.6.c, and 5.6.d; which were subjected to a phosphine pre-exposure before nucleation. The images in the left column (which includes the Z-scale of the scan) are plain views; images on the centre row are 3D representations of the same image; finally the right column corresponds to SEM plain view images.

A more accurate characterization was carried out for sample 5.6.c by means of cross sectional SEM and TEM. The most relevant images have been included in Figure 5.13 and Figure 5.14, respectively. From cross-section SEM scans (Figure 5.13), it can be corroborated the presence of
a continuous GaP nucleation layer, resulting from the total coalescence of GaP nuclei. This characterization evidences the roughness of the GaP surface, as it was anticipated by AFM characterization.

![Figure 5.13 SEM analysis of sample 5.6c. a and b) Tilted SEM images of the samples at different magnitudes, proving the existence of a continue layer formed by the coalescence of islands; c and d) cross section SEM images at different magnifications, including some height measurements of the GaP layer.](image)

In addition, TEM characterization (Figure 5.13) reveals the presence of a high number of crystallographic defects within the GaP layer, originated as a result of the 3D growth-mode. The analysis of the GaP/Si interface confirms the absence of silicon oxide and the continuation of the silicon lattice on the GaP nucleation layer. Nonetheless, an important number of defects were found to be originated at the interface (Figure 5.13.c).

From this extended characterization it can be concluded that by the addition of a GaP growth step after the nucleation layer, the initial GaP features evolve towards a continuous layer. The resulting layer is homogeneous and it completely covers the Si surface. Nevertheless, it presents a non-negligible roughness (~13 nm) as a result of the 3D growth-mode (instead of a layer-by-layer growth). HR-TEM analysis (Figure 5.14.b) confirmed that the GaP presented a high number of stacking faults, degrading its crystallographic quality. Accordingly, it can be stated that if the first nucleated nanometers of GaP present a non-negligible roughness (as it is the
case), the subsequent GaP will grow aggravating this roughness, as observed in sample 5.6.c. Only when a smooth 2D GaP layer is initially nucleated on Si substrates, the addition of a second growth step, might result in the formation of a defect-free, 2D GaP layer, as it was reported in the literature.

![Image of TEM characterization](image)

**Figure 5.14 TEM** a) Cross-section TEM characterization of sample 5.6.c, revealing the presence of a continuous GaP layer, covering homogenously the Si surface; b) Zoom of the GaP layer for a more detailed view of the crystallographic defects which are originated at the interface and propagate vertically, reaching in some cases the top surface; c) High resolution TEM image of the GaP/Si interface to prove the absence of silicon oxide and the formation of SFs at the interface.

To sum up, the pre-exposure of Si samples to a short flush of PH₃ has resulted into interesting results. Regarding the morphological quality of nucleation layers, it can be concluded that when working under appropriate conditions, a continuous layer can be obtained from the total coalescence of GaP islands, presenting a moderate roughness. From the crystallographic point of view it can be stated that nucleation layers present a high density of defects, specially stacking faults, which, if not controlled, might ruin the crystal quality. According to these results, it could be considered that the formation of crystallographic defects, revealed in most of the samples, is associated to the absence of a Si homoepitaxial layer. From literature, it is well known that Si substrates are generally submitted to an initial step of homoepitaxy to guarantee a pristine surface. This epitaxial layer buries any traces of oxygen, carbon or any other contaminant remaining at the surface, favoring the formation of a continuous and defect-free nucleation layer. It is worth noting at this point that the idea of this thesis is to offer a simple and easy routine for the integration of III-V on Si substrates, avoiding the use of two separate MOVE reactors (which will be required in case of homoepitaxial growth). Consequently, in our purpose of avoiding the use of the Si homoepitaxial step for offering a simple routine, it might be assumed that the crystal quality of nucleated layers might be compromised.
5.3.1.2. TMGa pre-exposition

Different parameters have been tested at this point for assessing its impact on the nucleation process (i.e. temperature, V/III ratio, thickness, annealing nature...). These experiments were all framed on the continuous growth-mode approach and based on the pre-exposure of wafers to a short phosphine flux before nucleation. This approach was selected based on the widely reported benefits of phosphorous coverage on preparing the surface for subsequent growth. Nevertheless, as explained before, not only group-V exposure has been reported to be beneficial for GaP nucleation; but also group-III exposure. It is important to ensure that during the pre-exposure exactly one monolayer of Ga is deposited on the substrate. Excess Ga deposition would result in the formation of metal droplets and silicon etching. Following with previous studies, in this section we will explore two different approaches: low temperature nucleation regime (550 °C), and high temperature nucleation regime (700-800 °C). The goal of this division is to sweep the parameters to assess which one is the most advantageous approach for obtaining a two-dimensional defect-free GaP nucleation layer. With this objective and as in the previous section, the most relevant parameters implicated in each step have been listed in Table 5.VII; being classified according to their magnitude, following the established sign criterion.

Table 5.VII Sign criteria definition for samples exposed to TMGa before nucleation.

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<td>III (sccm)</td>
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<td>2.5</td>
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</tr>
</tbody>
</table>
5.3.1.2.a. Low temperature approach

The most relevant experiments included in the low-temperature approach have been summarized in Table 5.VIII. This table describes the routine followed for each sample according to the established sign criteria and the AFM characteristic parameters for each sample –extracted from AFM scans plotted in Figure 5.15– with the aim of having a first idea of the surface morphology.

Table 5.VIII Description of the sample preparation and MOVPE routine followed by samples included in the first batch of experiments, which has been pre-exposed to TMGa before nucleation. AFM analysis parameters have been also included.

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<td>Temp</td>
<td>-</td>
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</tr>
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<td>-</td>
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<td>Temp (°C)</td>
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Despite all samples are framed under the low-temperature nucleation approach, each one has been produced under specific conditions, differing from each other in one, or several parameters. As an example, the effect of the nucleation duration (i.e. GaP thickness) on the GaP morphology can be assessed by comparing the couples: sample 5.8.a vs. sample 5.8.b; and sample 5.8.d vs. sample 5.8.e (Figure 5.15). In both cases, the result of a longer growth is a
rougher surface, alike to what happened when samples were initially exposed to PH₃. Consequently, nucleated islands are not evolving towards a continuous layer over growth time. On the contrary, as nucleation gets longer, the difference between nucleated sites and GaP-free places gets more significant, increasing the roughness of the resulting layer.

Figure 5.15 AFM topography scans of samples 5.8.a, 5.8.b, 5.8.c, 5.8.f, and 5.8.g framed in the low-temperature nucleation approach, for samples that have been subjected to a TMGa pre-exposure before nucleation. Images in the left column are plain views and images on the left are 3D representations of the same image. Z-scale has been included in the left most side.
Separately, the effect of the V/III ratio on GaP morphology can be ascertained by comparing sample 5.8.b and sample 5.8.c, which are expected to present the same GaP thickness. In this sense, the increase in the group-III concentration (and thus in the growth rate) in sample 5.8.c was compensated by a proportional decrease of the nucleation time, yielding a roughly constant GaP thickness. The increase in group-III concentration will affect the size and the density of GaP features. Indeed, TMGa concentration will modulate the growth rate by changing the time needed to form a cluster for nucleation. In this respect, as the TMGa concentration increases, the time to produce a critical size for nucleation is reduced and thus, a reduction of the average island spacing is observed, producing a higher number of islands with a reduced size (sample 5.8.c).

A complementary study of the effect of the V/III ratio on GaP nucleation can be done by comparing sample 5.8.f and sample 5.8.g. In this case, both the group-III and group-V partial pressure were varied. In this sense, despite that a significantly higher V/III ratio is obtained for sample 5.8.g., GaP features measured in both cases are virtually identical, showing a very poor morphology. In this respect, we can conclude that when working under non-appropriate nucleation conditions, the V/III ratio will not have important repercussions on the final morphology; that is to say: the use of very high V/III ratios is a necessary condition, but not sufficient for guaranteeing a 2D nucleation. It is worth considering that samples 5.8.f and 5.8.g were subjected to a long TMGa pre-exposure (in the order of 15 times higher than the rest of the samples); meaning that the poor morphology might be related to the reported effect of the Ga etching Si surfaces.

For a better understanding of the low-temperature nucleation process, sample 5.8.a and sample 5.8.d were selected for a more detailed characterization, with the goal of analyzing the crystallographic quality of the nucleated GaP islands and the GaP/Si interface.

Initially, sample 5.8.a was analyzed by cross-section TEM (Figure 5.16). A general cross-section view of the sample reveals the presence of numerous islands (Figure 5.16.a), which tend to join to each other, turning into a semi-continuous layer. Nevertheless, isolated islands are also observed in this sample. By looking in more detail into one of the islands (Figure 5.16.b), the presence of numerous crystallographic defects is revealed. These defects (stacking faults) are originated at the GaP/Si interface and propagate until they reach the top surface. Moreover, other defects, namely dislocations, have been found in the areas where a continuous layer was present (Figure 5.16.c). On the other hand, sample 5.8.d has been analyzed by SEM and TEM. By taking a look at SEM images in Figure 5.17, it can be distinguished a 3D growth, formed by multitude of small islands, which coalesce forming a continuous, but heterogeneous layer. The
analysis of this sample by cross-section TEM (Figure 5.18) reveals the presence of a high density of crystallographic defects (SFs), which go from the GaP/Si interface to the top of the GaP layer (Figure 5.18.a).

Figure 5.16 Cross section TEM images of sample 5.8.a. a) General view of the GaP nucleated on the silicon substrate following a 3D growth (i.e. island-type), which in some cases coalescence forming a semi-continuous layer; b) detail of an isolated island, revealing the presence of a high number of crystallographic defects; c) detail of the semi-continuous layer resulted from the coalescence of islands. A huge number of defects are present in the layer.

Figure 5.17 SEM analysis of sample 5.8.d. SEM plain view (a) and tilted view (b) of the samples at different magnitudes, showing a continuous layer formed by the coalescence of islands.
Figure 5.18 TEM analysis of sample 5.8.d a) General view of sample 5.8.d where a continuous and very rough layer can be observed; b) a more detailed HR-TEM view of the GaP layer, to prove the presence of stacking faults from the interface to the top; c) HR-TEM image of the GaP/Si interface to prove the absence of silicon oxide and the origin of crystallographic defects.

According to this characterization it can be concluded that in our MOVPE reactor -where the injection of the exact amount of TMGa to form a single monolayer seems difficult to control-, the exposure of wafers to a group-III precursor at low temperatures, does not favor the GaP nucleation under optimum conditions. The formation of a continuous layer, resulted from island coalescence, has been occasionally observed. Nonetheless, as a result of the initial growth-mode (i.e. 3D), numerous defects have been observed, yielding a poor crystallographic quality.

5.3.1.2.b. High-temperature approach

In order to fully understand the GaP/Si nucleation process and to analyze the effect of the temperature, a batch of experiments based on the high temperature approach was carried out, being the most relevant experiments summarized in Table 5.IX. Moreover, most important AFM parameters (RMS, skewness and kurtosis) have been included in Table 5.IX.

By comparing sample 5.9.a and sample 5.9.c, the previous reported relation between nucleation temperature and island size can be reconfirmed. In this case, the nucleation of sample 5.9.a, which occurs at lower temperature, produces a higher density of smaller islands, than in the case of sample 5.9.c, which occurs at higher temperatures.

The role of the V/III ratio on favoring a 2D nucleation has been repeatedly reported in the literature. However, we have observed that the presence of a high V/III ratio is not a guarantee of a layer-by-layer growth; as it also depends on other nucleation parameters. In this respect, it is enlightening now, to compare sample 5.9.b with sample 5.9.c (Figure 5.19), which only differ on the V/III ratio. While sample 5.9.c presents an island-type growth formed by isolated islands; the analysis of sample 5.9.b reveals a homogenous base layer covering the silicon surface, resulted from a step-flow growth (typical from vicinal substrates). On top of this continuous base layer,
huge hillocks are selectively grown, probably coinciding with more favorable sites. The resulting surface is formed by a heterogeneous GaP layer, going from few nanometers-thick base layer, up to the order of microns for the tallest hillocks. These features resemble the typical SK growth-mode where, after a certain thickness, the initial wetting layer turns into a 3D growth, forming isolated islands, selectively grown on the continuous GaP layer. As it was previously described, this growth-mode usually occurs when growing materials with an important lattice mismatch, as a way to relax the stress. Nevertheless, in this case, both materials (i.e. GaP and Si) are almost lattice matched and consequently, their growth should not follow this growth-mode. Accordingly, it can be concluded that either the reported growth-mode is triggered by the presence of defects or contaminants on the surface of the silicon, prior to the GaP nucleation; or that, indeed, this growth does not correspond to a SK mode but to a combination of different growth modes, such as an initial FM mode followed by a 3D growth.

Table 5.9X Description of the sample preparation and MOVPE routine followed by samples exposed to TMGa before nucleation following the high-temperature approach. AFM analysis parameters have been also included.

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<td>Kurtosis</td>
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Figure 5.19 AFM topography scans of samples 5.9.a, 5.9.b, and 5.9.c framed in the high-temperature nucleation approach, which were subjected to a TMGa pre-exposure before nucleation. Images in the left column are plain views and images on the left are 3D representations of the same image. Moreover, Z-scale has been included in the left most side.

In order to have a better understanding of the nucleation process at high temperatures, sample 5.9.b has followed a more thorough characterization, by cross-section TEM analysis. Firstly, a more detailed AFM scan of the base layer is shown in Figure 5.20.b, showing what seems a typical step-flow nucleation. The presence of the already mentioned continuous wetting layer is corroborated by a general TEM cross section of the sample. In this scan (Figure 5.20.d), the hillocks grown on top of the base layer are not shown due to the reduced size of the TEM scan. Finally, the analysis of the GaP/Si interface reveals a silicon-oxide-free surface, where a GaP layer is grown continuing the Si lattice parameter. It is worth noting that along the area examined; only a single family of stacking faults (Figure 5.20.f) was encountered, revealing a high crystallographic quality. This can be explained by the uniform coverage of the silicon surface with a 2D GaP base layer.

To sum up, in this section the effect on the GaP nucleation morphology of exposing wafers to an initial short flux of TMGa has been explored. In this respect, two different approaches have been
considered: low-temperature and high-temperature nucleation. Despite the low-temperature nucleation has been reported to produce promising results on the GaP/Si integration when wafers are initially subjected to a short flux of PH₅ (Figure 5.13), the use of these low temperatures results in a typical 3D island-type growth when wafers are initially exposed to TMA. At best, island coalescence is observed, evolving to a continuous layer with a poor crystallographic quality. Nevertheless, the resulting surface is very rough and heterogeneous. On the other hand, the use of high temperatures for nucleation offers a more interesting alternative, reporting GaP layers with a seemingly crystalline quality. However, this approach presents important limitations related to the morphological quality of the nucleated layer. In this respect, the presence of the high hillocks on top of the continuous GaP base layer hinders its possible use for further III-V growth. Accordingly, at this moment this approach (i.e. the preexposure of wafers to a short flush of a group-III precursor before nucleation) is laid aside since it has been demonstrated not to be the best effective approach -in our particular MOVPE system- for ensuring a high-quality GaP nucleation.

![AFM and TEM images](Figure5.20.png)

Figure 5.20 AFM (a-c) and TEM (d-f) characterization of sample 5.9. a) AFM scan reveals the presence of very high mountains grown on a continuous GaP layer; b) the analysis of the background layer reveals a typical step-flow growth, resulting into a continuous GaP layer; d) A general cross-section TEM overview allow us to identify the presence of an heterogeneous (in terms of height) GaP layer. e) The analysis of the GaP/Si interface reveals an oxide-free surface and a continuation of the Si structure on the GaP layer. f) Along all the analyzed structure, only a single family of dislocations was found, meaning that despite the differences in height, the crystallographic quality of the GaPlayer is fairly good.
5.3.1.3. AsH₃ pre-exposition

As previously detailed, the idea of exposing Si surfaces to an initial short flux is based on favoring the wetting of the GaP on Si, to promote the nucleation of a high quality 2D GaP layer. In this sense, it has been considered so far the pre-exposition of surfaces to PH₃ and TMGa. Significant differences have been encountered between both, proving the effect of precursor on the nucleation quality. Nonetheless, in neither of both approaches it has been achieved a two dimensional defect-free GaP layer, though interesting results were obtained so far. It is important to highlight that in both cases, the exposure to precursors before nucleation has to be carefully controlled to avoid undesired side effects. In this sense, the prolonged exposure to TMGa could result in Si etching and metal droplets formation. On the other hand, the long exposure of Si surfaces to phosphine might result in surface roughening due to Si dimmer displacement. In both cases, these effects will have deleterious consequences on the nucleation of GaP.

Within this frame, the idea of exposing Si surfaces to a different group-III or group-V precursor arises. In this respect, AsH₃ is the most suitable candidate. The exposure of germanium to AsH₃ flux has been widely reported to have deleterious effects on the III-V growth quality due to the fact that AsH₃ etches germanium at high temperatures, turning into a roughness increase of the substrate [McMahon’01 Olson’98]. Moreover, it has been reported that AsH₃ precludes the formation of a single domain surface, causing faceting and step bunching [McMahon’01 Olson’98]. Nevertheless, the exposure of silicon wafers to AsH₃ has been reported to have the opposite effect. On the one hand, the bond formed by Si and arsenic –resulting from the arsine pyrolysis [Stringfellow’89] – is very stable and strong (even more than Si-P). In this respect, several authors reported that the exposure of Si to an AsH₃ preflow results into an As-stabilized surface. As a result of this surface configuration, the GaP/Si interfacial energy is reduced [Kohama’90 Kohama’88] and consequently, the formation of defects at the GaP/Si interface is hindered. Under these conditions, GaP nucleates following a continuous growth-mode, with a high crystalline quality [Hannappel’04 Kohama’90 Kohama’88 Soga’91a]. On the other hand, and unlike what happens with PH₃, AsH₃ has been reported to be innocuous to Si in moderate concentrations. Resulting surfaces remain flat with monolayer-high terraces covered with As dimmers and presenting a 2x1/1x2 configuration [Hannappel’04]. Nonetheless, other parameters such as the presence of surface contaminants, the annealing time or the nucleation temperature might also play a major role on the surface preparation.

Accordingly, the effect on GaP morphology of pre-exposing Si surfaces to an initial AsH₃ flow will be explored in this section. In accordance with previous studies, two different approaches
have been explored: low-temperature and high-temperature nucleation. Table 5.X summarizes all the parameters for each step; classifying them into one of the three possible categories according to their magnitude.

Table 5.X Sign criterion definition for samples exposed to AsH₃ before nucleation.

<table>
<thead>
<tr>
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<tbody>
<tr>
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<tr>
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<td>800</td>
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<td>800</td>
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<tr>
<td>V (sccm)</td>
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<td>450</td>
</tr>
<tr>
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<td></td>
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<tr>
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<tr>
<td>III (sccm)</td>
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<td>1.5</td>
<td>1.5</td>
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<tr>
<td>III (sccm)</td>
<td>1.5</td>
<td>1.5</td>
<td>1.5</td>
</tr>
</tbody>
</table>

As detailed in Table 5.X, not only the nucleation temperature, but also the pre-exposure conditions, or the GaP thickness, have been considered as variables for the nucleation process. In this respect, Table 5.XI lists the most relevant experiments developed within this frame, summarizing the routine followed for each sample according to the established sign criterion. Moreover, Table 5.XI includes the AFM characteristic parameters (extracted from AFM scans plotted in Figure 5.21) for each sample to have a broad idea of the surface state.

At a first sight, sample 5.11.a which was nucleated at low temperature, resembles sample 5.3.b, nucleated at low temperature too (slightly higher, though), which was pre-exposed to a PH₃ flux before nucleation. In this respect, the exposure to AsH₃ does not trigger any benefits with respect to the PH₃. Nevertheless, by taking a look at the AFM scans of the rest of the samples (Figure 5.21) it can be visualized a total different growth-mode to what we have reported so far.
On the one hand, sample 5.11.b and sample 5.11.d present a similar nucleation, tending to what seems a step-flow growth. The differences in morphology between them can be attributed to the additional growth-step included in sample 5.11.d, resulting in a longer growth. On the other hand, sample 5.11.c reveals a heterogeneous surface with a selective growth, where some steps grow quicker than others, resulting in a very rough and heterogeneous surface (RMS value of 85 nm).

Table 5.XI Description of the sample preparation and MOVPE routine followed by samples exposed to AsH₃ before nucleation. AFM analysis parameters have been also included.

<table>
<thead>
<tr>
<th></th>
<th>5.11.a</th>
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<td>H₂</td>
<td>H₂</td>
<td>H₂</td>
<td>H₂</td>
</tr>
<tr>
<td>Pre-exposure</td>
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<tr>
<td>Time</td>
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<td>-</td>
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<td>+</td>
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<tr>
<td>V</td>
<td>+</td>
<td>+</td>
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<td>Starting</td>
<td>V</td>
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</tr>
<tr>
<td>AFM</td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
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<td>34.62</td>
<td>85.88</td>
<td>23.98</td>
</tr>
<tr>
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<td>0.071</td>
<td>2.05</td>
<td>0.33</td>
</tr>
<tr>
<td>Kurtosis</td>
<td>3.07</td>
<td>2.85</td>
<td>9.95</td>
<td>2.56</td>
</tr>
</tbody>
</table>
Figure 5.21 AFM topography scans of sample 5.11.a, sample 5.11.b, sample 5.11.c and sample 5.11.d, which have been pre-exposed to AsH₃ before nucleation. Low temperature (sample 5.11.a) and high temperature (sample 5.11.b, 5.11.c and 5.11.d) regimes have been explored in this case. Images in the left column are plain views and images on the left are 3D representations of the same image. Z-scale has been included in the left most side. Note that sample 5.11.c is represented in a different Z-scale due to the height of the hillocks.

For a better understanding of the growth-mode occurring under these conditions, sample 5.11.b has followed a more deep characterization. A detailed SEM analysis, including tilted view (Figure 5.22.a and Figure 5.22.b) and cross-section (Figure 5.22.c and Figure 5.22.d) has been performed. This analysis confirms the presence of wave-shaped features following what
resemble a step-flow growth-mode. Cross-sectional SEM evidences the height-differences between two neighboring areas (Figure 5.22.c). Moreover, these scans reveal that GaP is growing with a certain tilt with respect to the Si substrate (Figure 5.22.c). Although further studies need to be done in this direction, it is believed that the inclination of the GaP features is directly related to the miscut of the substrates. In this respect, Figure 5.22.c includes estimations of the height and length of the features for calculating their angle of inclination with respect to the substrate. An angle of 6° approximately, coinciding with the miscut of our substrates, is obtained.

![Figure 5.22 SEM images of sample 5.11.b. General tilted view of sample surface, where step-flow growth can be easily perceived (a, b). Cross sectional SEM scans gives information about the thickness and the tilt of the GaP nucleation layer (c,d).](image)

A more detailed study by TEM reveals the presence of a continuous layer covering the total Si surface (Figure 5.23). In certain points, the hillocks grow wider, turning into an irregular surface, caused, probably, by the misorientation of the wafer. Despite this unevenness, the morphological quality of the layer is reasonable good. Moreover, the total absence of crystallographic defects on the whole layer (neither in the initial continuous layer, nor in the thicker parts of the layer), makes this approach the most promising alternative for GaP/Si growth, among the wide variety presented in this thesis, for the actual MOVPE configuration.
Figure 5.23 a) Cross-section TEM image of sample 5.11.b, revealing the presence of a continuous, but irregular, GaP layer; b) and c) High resolution TEM images of two separate sites to prove the absence of crystallographic defects along the continuous layer.

In order to fully prove the beneficial effect of this precursor (i.e. AsH₃) on providing a GaP layer free of crystallographic defects, sample 5.11.d has been also characterized by TEM. The most revealing images are included in Figure 5.24.

Figure 5.24 Cross-section TEM characterization of sample 5.11.d. a) A general view of the sample reveals the presence of an irregular, but continuous layer covering the silicon surface. b) and c) correspond to more detailed views of the GaP layer, confirming the absence of crystallographic defects within the layer; finally, d) HR-TEM of the GaP/Si interface, evidences the absence of silicon oxide and the continuation of the silicon lattice on the GaP layer without the occurrence of structural defects.
In agreement with results reported for sample 5.11.b, a 2D nucleation layer covering the silicon surface is observed in sample 5.11.d. In the same way, GaP features grow with a certain inclination (related to the miscut angle of the wafer) with respect to the silicon crystal. As a result of this growth, the resulting surface is heterogeneous; nonetheless, alike what happen in sample 5.11.b, the morphological quality of the layer is reasonably good and the crystallographic quality of the grown layer is excellent, with no defects revealed in this sample; confirming the effect of the AsH$_3$ pre-exposure on getting rid of APDs and dislocations. Nonetheless, the morphological quality requires further development to be used as a template for subsequent III-V integration.

Finally, it is worth examining sample 5.11.c, which presents important morphological differences, despite it has followed a nucleation routine similar to sample 5.11.d. While the growth of the nucleation layer on sample 5.11.d started with the group-V precursor (i.e. PH$_3$); group-III was selected for starting the growth in the case of sample 5.11.c. That is to say, after the AsH$_3$ pre-exposure, this precursor was switched off and immediately TMGa was introduced into the reactor chamber for a few seconds before PH$_3$ was switched on. As a result of this modification, the resulting surface presents a very poor morphology, where GaP selectively nucleates on the Si surface, observing a "vertical growth" at given sites rather than a general "horizontal growth". This means that initial GaP nuclei do not evolve towards a continuous layer by a step-flow growth, but instead, the incoming Ga and P adatoms deposit preferably on these nuclei, growing in height but not in area (note that the Z-scale for this sample had to be significantly increased).

To sum up, the effect of wafer pre-exposure to AsH$_3$ on the GaP nucleation process has been studied in this section. Despite not much work has been done within this frame, interesting results have been reported. On the one hand, GaP nucleation at low temperatures on AsH$_3$-exposed samples does not represent any advantage (in terms of GaP morphology or crystallographic quality) with respect to PH$_3$-exposed samples. On the contrary, GaP nucleation at high temperatures on AsH$_3$-exposed samples has resulted to be a very promising approach; reporting the best results, in terms of morphology and structural quality, obtained so far in this thesis. Future work will be directed to fully understand the effect of the Si wafer miscut on the GaP nucleation growth-mode and to improve the surface morphology to create a high quality template for subsequent III-V integration.
5.3.2 Pulsed growth-mode

As described in Section 5.2, two general alternatives exist for the growth of III-V semiconductors on Si substrates on a MOVPE environment: continuous and pulsed growth-mode. The differences between them basically lie in the mode in which precursor are introduced in the reactor chamber. The continuous growth-mode has been reported to produce good results on the integration of high quality GaP nucleation layers on Si substrates [Kohama’88 Lee’97 Soga’94b Sug’88]. Nevertheless, to date, there is not a universal routine for growing a high quality GaP nucleation layer; indeed, there is a wide controversy about the magnitude of different variables involved in the process. Moreover, results are dependent to the MOVPE system where samples are grown, being a non-easy reproducible technique. On the contrary, the use of the pulsed growth-mode has gained some importance in the last years [Grassman’09b Narayanan’02b Takagi’98 Yamane’09]. Unlike what happen with the continuous growth-mode, this approach has demonstrated to be highly reproducible and easily implemented disregarding the MOVPE system. The success of this technique lies in the combination of the pulsed growth with precursors which allow the use of low temperatures, resulting in sharp interfaces. Despite this technique has been mostly implemented on Molecular Beam Epitaxy (MBE) systems, its use has also been proved to produce good results on MOVPE reactors [Volz’11].

Table 5.XII Sign criterion definition for samples nuckrated under the pulsed-growth mechanism.

<table>
<thead>
<tr>
<th></th>
<th>Time (min)</th>
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<tbody>
<tr>
<td><strong>Annea</strong>l</td>
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<td></td>
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<tr>
<td><strong>Temp (°C)</strong></td>
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<tr>
<td><strong>N° cycles</strong></td>
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<td>50</td>
</tr>
<tr>
<td><strong>Temp (°C)</strong></td>
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<td></td>
<td></td>
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<tr>
<td><strong>V (sccm)</strong></td>
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<td>500</td>
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<td><strong>Continuous Growth</strong></td>
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<td></td>
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<tr>
<td><strong>V (sccm)</strong></td>
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<td>450</td>
<td></td>
</tr>
<tr>
<td><strong>III (sccm)</strong></td>
<td>2.5</td>
<td>5</td>
<td></td>
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</table>
Atomic Layer Epitaxy is based on the alternative introduction of precursors into the reactor chamber. The pulsed supply of atoms favors their mobility in a way that once atoms reach the surface, they can migrate promoting the formation of a monolayer before the other atom is injected [Narayanan'02a Takagi'98 Volz'11 Yamane'10]. One of the major advantages of this technique is that it allows the use of low temperatures for the nucleation. In this approach, TBP is generally used as the P-precursor, given its efficient pyrolysis at low temperatures; nevertheless, due to the absence of this line in our actual MOVPE configuration, PH₃ will be used as the P precursor.

Different parameters, such as the number of cycles, the V/III ratio or the addition of a second growth step, have been varied to assess their impact on the GaP morphology. Parameters implicated in each step have been listed and classified according to the sign criterion in Table 5.XII. Moreover, Table 5.XIII summarizes the most relevant experiments within this approach, as well as the most important parameters extracted from AFM analysis, included in Figure 5.25.

Table 5.XIII Description of the sample preparation and MOVPE routine followed by samples nucleated under the pulsed-growth mechanism. AFM analysis parameters have been also included.

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<td>H₂</td>
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<td>H₂</td>
<td>H₂</td>
<td>H₂</td>
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<td>0.39</td>
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<td>5.11</td>
<td>3.0</td>
<td>3.48</td>
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</table>
Figure 5.25 AFM topography scans of sample 5.13.a, sample 5.13.c, sample 5.13.d, and sample 5.13.e, which have been nucleated using the pulsed growth-mode. Images in the left column are plain views and the images on the left are 3D representations of the same image. Z-scale has been included in the left most side. Note that sample 5.13.a is represented in a significantly lower Z-scale as a result of the planar surface.

Initially sample 5.13.a and sample 5.13.b have been subjected to a single-step process, based on the pulsed growth-mode. The only difference between them is the number of cycles. The low values of roughness measured on these samples (Table 5.XIII) are surprising and are in good agreement with the soft surface shown in AFM scans included in Figure 5.25. Moreover, SEM scans of sample 5.13.a, included in Figure 5.26, confirm the smooth surface responsible for such low value of RMS. Nonetheless, the presence of GaP was corroborated by Energy-dispersive X-ray spectroscopy (EDX). The use of this technique allows us to obtain qualitative information about the surface composition of the sample. That is to say, the analysis of a certain area by EDX gives information about the elements which are present on that area, their distribution along the
surface and their relative concentration. In this respect, color plots included in the bottom row of Figure 5.26 (c, d and e) corresponds to SEM images where elements (i.e. Si, P and Ga respectively) have been selectively identified by means of EDX. According to this characterization it can be concluded that both elements (i.e. Ga and P) are present on the silicon surface. Given the low temperatures used for the growth (500 °C), it seems unequivocal that those elements do not come from the reactor walls (due to their partial desorption), but they come from the pyrolysis of the corresponding precursors (TMGa and PH3, respectively) at those temperatures. Nonetheless, given the short duration of the growth and thus, the reduced thickness of the deposited material (AFM scan of sample 5.13.a hardly differs from the one measured on an as-received sample), it cannot be fully assessed at this point whether both elements are deposited forming a monolayer, or separately distributed along the surface.

![Figure 5.26 SEM scans of sample 5.13.a at different magnifications. Top view (a) and tilted view (b) of the silicon surface where GaP has been grown at 500 °C by ALE for 30 cycles. EDX analysis of sample 5.13.a to verify the presence of Si (c), P (d) and Ga (e).](image)

The surface resulting from sample 5.13.a has been now used as a template for a subsequent step. At this point, the GaP growth was turned to the continuous mode; growing a thicker GaP layer at low temperature (sample 5.13.c). The resulting surface shows a combined growth, form predominantly by a step-flow along the (0-1-1) direction, occurring parallel to the step edges, and perpendicular to the flat of the wafer (Figure 5.3). Nevertheless, surface is not homogeneously covered by this GaP layer, detecting in some cases the absence of GaP (dark areas in AFM scan included in Figure 5.25). Moreover, sample 5.13.d, 5.13.e and 5.13.f have suffered this combined treatment consisting on an initial ALE growth at low temperature.
followed by a continuous-growth-mode at a slightly higher temperature (i.e. 550 °C). In those cases, the number of cycles during ALE has been increased (roughly duplicated), as compared to sample 5.13.c. In these experiments, parameters such as the V/III ratio or nucleation time have been varied to assess their impact on GaP evolution. As an example, the V/III ratio for sample 5.13.d and sample 5.13.e has been significantly increased (roughly by a factor of 4) as compared to sample 5.13.c. As a result of this variation, the resulting GaP presents a different morphology (Figure 5.25). Moreover, sample 5.13.e has been fabricated in a longer growth, as compared to sample 5.13.d; nevertheless, not important differences, apart from a rougher surface, can be easily perceived.

Sample 5.13.d has been characterized by SEM (Figure 5.27) and TEM (Figure 5.27) for a better understanding of the nucleation process. In this respect, Figure 5.27 summarizes the most relevant SEM images from the analysis of this sample. In this case, the morphology is similar to the one reported in sample 5.13.c; nonetheless, a more uniform coverage of GaP is observed in this case. Cross-section SEM images show a continuous, though very rough layer, which occasionally reaches a height up to 120 nm, exceeding the maximum critical thickness of the GaP layer.

Figure 5.27 SEM images of sample 5.13.d. General tilted view of sample surface, where step-flow growth can be perceived (a, b). Cross-sectional SEM images give information about the thickness of the GaP nucleation layer (c, d).
The presence of staking faults along the GaP layer has been confirmed by TEM (Figure 5.28.a, b) and HR-TEM (Figure 5.28.c). Accordingly, despite a continuous layer has been obtained by this growth-mode, the resulting layer presents a rather poor crystallographic quality, as a result of a very high density of defects.

Despite the GaP on Si integration has been mainly explored by the continuous growth-mode approach in this thesis –paying not much attention to pulsed growth-mode–, interesting results can be extracted in this section from the first contact to the ALE approach. While the mere use of the pulsed growth technique has been observed to be insufficient for growing a thick and homogeneous GaP layer (under the selected conditions), the addition of a second step, based on the continuous growth-mode approach, leads to the formation of a continuous layer. Nevertheless, the resulting nucleation layer presents a poor morphology (RMS close to 20 nm) and a moderate structural quality due the presence of a high density of crystallographic defects on this layer, which has been confirmed by TEM (Figure 5.28). Consequently, further work needs to be done within this frame with the aim of optimizing the ALE routine for improving the structural and morphological quality of the nucleation layer to obtain a high-quality and planar surface where III-V materials could be eventually integrated.

### 5.4. **Summary & Conclusions**

Along this chapter, different alternatives for the successful integration of a GaP nucleation layer on a Si substrate have been studied. The general idea of this study is to offer a **simple process for the III-V/Si integration** so it can be easily transferred to the PV industry. In this sense, we have explored the diverse (even contradictory) alternatives reported in the literature, to conform a simple yet successful integration of GaP on silicon substrates in our particular MOVPE
system. In this respect, the idea of growing an initial homoepitaxial layer, acting as the emitter of the bottom-cell, to favor the growth of III-V compounds was discarded due to the extra complexity of this process (related, on the one hand, to the necessity of two different reactor chambers to avoid cross-contamination; and, on the other hand, to the necessity of incorporating an additional line for a silicon precursor in our actual MOVPE system). Thereby, instead of using Si homoepitaxy, in our process the preparation of the substrates and the removal of contaminants will be attained by a proper chemical cleaning and a subsequent thermal annealing at high temperatures under H₂. It is worth noting that, according to literature, this Si homoepitaxial layer is intended to burn any traces of C, O, or any other contaminants which might ruin the quality of subsequent layers. Consequently, in our purpose of offering an easy and simple technique for III-V on Si integration, it might be assumed that the absence of the homoepitaxial step could have repercussions on the structural quality of the GaP.

Regarding the nucleation of GaP on Si, two general approaches have been initially considered: continuous growth-mode and pulsed growth-mode. On the one hand, the continuous growth-mode approach has reported to produce good results on obtaining a high-quality 2D nucleation layers. However, not a general routine has been, to date, established for this approach; on the contrary, a wide controversy about the magnitude of different variables (e.g. temperature, precursor for pre-exposure...) involved in the process has been reported. On the other hand, the pulsed growth-mode approach has received gaining attention in the last years, obtaining promising results in this direction. In this approach, a general routine which can be reproduced and easily transferred to any MOVPE system, if proper precursors (i.e. compatible with low temperatures) are employed, has been repeatedly reported. In this respect, giving the absence of the TBP line (P-precursor generally used for a low temperature nucleation) in the actual configuration of our MOVPE system and following our main premise (based on the process simplicity), PH₃ has been used as the P-precursor, disregarding the nucleation temperature.

Key points of each approach, and most enlighten TEM images, have been summarized in Table 5.XIV. In the light of these results we can conclude that not only a single technique is valid for a successful GaP/Si integration; on the contrary, most of the explored approaches have been resulted to be interesting in some way. Despite the many different alternatives suggested in this chapter, the one which has reported the best results (from a morphological and structural point of view), and so which will be considered as the starting point for future work, is the GaP nucleation at low temperatures under a continuous growth-mode, for samples which have been initially exposed to AsH₃. In this sense, future work will be directed 1) to promote the surface
smoothing, so the virtual substrate can be used as a template for further III-V growth, and 2) to evaluate the effect of the wafer miscut on the nucleation morphology.

Table 5.XIV Summary of the diverse approaches considered in this thesis for the epitaxial growth of GaP on Si substrates and the main results obtained for each case.

<table>
<thead>
<tr>
<th>CONTINUOUS MODE GROUP-V</th>
<th>LOW TEMPERATURE</th>
<th>HIGH TEMPERATURE</th>
</tr>
</thead>
</table>
| PH₃                     | • 3D nucleation with island coalescence forming a continuous layer.  
                          • Rough surface with a moderate morphological quality.  
                          • High density of crystal defects. |
| AsH₃                    | • 3D nucleation forming a semi-continuous layer.  
                          • Rough surface with a poor morphological quality.  
                          • Very poor structural quality with multitude of crystallographic defects. |
| TMGa                    | • 3D nucleation with island coalescence forming a continuous layer.  
                          • Rough surface with a poor morphological quality.  
                          • High density of crystal defects. |
|                         | • Continuous layer with a moderate morphological quality.  
                          • GaP growing tilted on Si surface.  
                          • Excellent crystallographic quality. |
| PULSED MODE             | • ALE process unaffordable for thick GaP layers.  
                          • ALE+ cont. growth: continuous layer with a moderate morphological quality.  
                          • Poor structural quality due to high defect density. |
| ALE                     | • Presence of high hillocks on top of a GaP wetting layer.  
                          • Very sharp morphology.  
                          • Seemly crystallographic quality. |
Table 5.XV Color classification of the different approaches regarding three different aspects: layer continuity, morphological quality and structural quality of the GaP nucleation layer. Color legend is plotted on the bottom.

<table>
<thead>
<tr>
<th></th>
<th>LOW TEMP.</th>
<th></th>
<th>HIGH TEMP.</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>PH₃</td>
<td>AsH₃</td>
<td>TMGa</td>
<td>PH₃</td>
</tr>
<tr>
<td><strong>Continuous-mode</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>Continuous-mode</strong></td>
</tr>
<tr>
<td><strong>ALE</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>ALE</strong></td>
</tr>
<tr>
<td>Continuity of the layer</td>
<td><img src="#" alt="Green" /></td>
<td><img src="#" alt="Yellow" /></td>
<td><img src="#" alt="Green" /></td>
<td><img src="#" alt="Green" /></td>
</tr>
<tr>
<td>Morphological quality</td>
<td><img src="#" alt="Yellow" /></td>
<td><img src="#" alt="Red" /></td>
<td><img src="#" alt="Red" /></td>
<td><img src="#" alt="Yellow" /></td>
</tr>
<tr>
<td>Structural quality</td>
<td><img src="#" alt="Red" /></td>
<td><img src="#" alt="Red" /></td>
<td><img src="#" alt="Yellow" /></td>
<td><img src="#" alt="Yellow" /></td>
</tr>
<tr>
<td><strong>Legend</strong></td>
<td><img src="#" alt="Good" /></td>
<td><img src="#" alt="Moderate" /></td>
<td><img src="#" alt="Poor" /></td>
<td><img src="#" alt="Good" /></td>
</tr>
</tbody>
</table>

Finally, Table 5.XV quantifies the quality of the different approaches, regarding three different aspects: 1) the continuity of the layer, given by the total/partial coalescence of 3D islands; 2) its morphological quality, homogeneity and roughness; and finally, 3) the structural quality of the GaP nucleation layer in terms of crystallographic defects. The color criterion is defined in the bottom of Table 5.XV.
6. PHOTOVOLTAIC BEHAVIOR OF THE BOTTOM CELL

The optimization of the bottom subcell has been repeatedly mentioned to be a key aspect for guaranteeing a highly efficient MJSC structure. This optimization involves several items; most of which have been faced in previous chapters. The preparation of Si substrates for subsequent epitaxial growth has been firstly discussed in Chapter 2. In this respect, an oxide-free surface has been proven to be obtained when wafers are submitted to a high-temperature anneal under H$_2$ [Döscher’11 Kunert’08]. Moreover, Chapter 3 and 4 have focused on the formation of the p-n junction and the reconstruction of the resulting surface, respectively. From that study it was proven that using a combined treatment consisting on a PH$_3$ exposure followed by a H$_2$ annealing, lead us to obtain an optimum emitter (shallow and highly doped) while preserving a high quality morphology for following heteroepitaxial growth. Nevertheless, a key aspect for the bottom subcell optimization, such as the attainment of good PV properties (i.e. sufficiently high minority carrier lifetime) in the base of the Si bottom subcell, has not been faced so far.

It is well established that the minority carrier lifetime in conventional PV silicon processing is not a constant material property but strongly depends on the thermal history and the environment where the sample was processed [Ulyashin’04]. This is a key issue since the bottom cell base minority carrier parameters will determine the PV performance of the bottom subcell in the tandem stack [Martin’13] and to a lesser extend it will limit the PV performance of the entire device. Therefore, it is important to fully characterize and understand the evolution of the bulk Si minority carrier lifetime during the fabrication process of III-V/Si MJSC structures. Accordingly, in this chapter, the influence of the MOVPE environment on the photovoltaic
properties (i.e. minority carrier lifetime) of the bottom subcell base during the different steps followed for the formation of a III-V/Si MJSC will be studied.

## 6.1. Minority Carrier Lifetime

When a photon is absorbed in a semiconductor, an electron from the valence band is excited and promoted to the conduction band; consequently, an electron/hole pair is generated. As a result of the concentration gradient existing in a p-n junction, the e/h⁺ pair is separated in a way that each charged particle diffuses to its corresponding contact (passing from minority to majority carriers). This collection has to be done before the particles recombine, so they can contribute to the photo current. Otherwise (i.e. if minority carriers are recombined before being collected), they will turn into recombination loses. The time a minority carrier can live before being recombined is called minority carrier lifetime and depends on the distance the particle can travel before it recombines and thus, on the existing recombination channels.

Accordingly, the effective minority carrier lifetime in a silicon wafer accounts for all the possible recombination channels, such as the recombination at the wafer surfaces or the recombination due to impurities in the bulk [Cuevas'04 Sinton'96a Sinton'96b]. On the one hand, the surface recombination is due to the presence of impurities or defects at the wafer surface. It is generally characterized by the surface recombination velocity (S_{ad}), rather than by the minority carrier lifetime. On the other hand, different recombination processes (schematically depicted in Figure 6.1) might coexist at the silicon wafer bulk:

- **Auger recombination** (τ_{Auger}): when a hole/electron pair is annihilated, the energy is transferred to a free particle (i.e. h⁺ or e'). It is the dominant mechanism at high injection levels. Its magnitude depends on the doping type, concentration and on the injection level.

- **Radiative recombination** (τ_{rad}): when the annihilation of a hole/electron pair involves the emission of a photon. It depends on the doping type, concentration, injection level and band structure of the material (direct vs. indirect). Being Si an indirect band gap semiconductor, this lifetime is generally much larger than the Auger contribution, so it is usually neglected.

- **Shockley-Read-Hall recombination** (τ_{SRH}): it is determined by the presence of impurities and defects (i.e. intermediate energy levels in the band gap) in the wafer bulk through which e/h⁺ pairs recombine usually emitting phonons.
Figure 6.1 Sketch of the three possible recombination processes in a Si wafer: a) Auger recombination: the energy released from the hole pair annihilation is transferred to another particle; b) Radiative recombination: the e/h pair annihilation yields a photon emission; c) SRH recombination: produced by the presence of an impurity or defect (characterized by its energy level, $E_D$) within the energy gap of the solar cell.

Accordingly, the bulk lifetime ($\tau_b$) can be expressed as a function of each individual contribution, following Equation 6.1:

$$\frac{1}{\tau_b} = \frac{1}{\tau_{\text{Auger}}} + \frac{1}{\tau_{\text{Red}}} + \frac{1}{\tau_{\text{SRH}}}$$

(Eq. 6.1)

Thus, effective lifetime ($\tau_{\text{eff}}$), which accounts for the bulk recombination and for the recombination at the surfaces, is generally expressed as a function of the wafer thickness ($W$) as follows:

$$\frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_b} + \frac{s_{\text{front}}}{W} + \frac{s_{\text{back}}}{W}$$

(Eq. 6.2)

Figure 6.2 [Kerr’02b] shows the contribution of each individual recombination mechanism to the effective lifetime as a function of the injection level ($\Delta n$). From this plot it can be seen how for injection levels up to $10^{15}$ cm$^3$ the effective lifetime is limited by SRH recombination, while Auger recombination becomes to be the dominant mechanism for high injection levels.

Figure 6.2 Contribution of the different recombination mechanisms to the effective lifetime as a function of the injection level [Kerr’02b].
### 6.1.1 Minority Carrier Lifetime Setup

The minority carrier lifetime was measured on wafers at room temperature (300 K) using the well-known photoconductance decay (PCD) technique with a Sinton WCT-120 tool (Figure 6.3) [Hofstetter’11]. This equipment measures the minority carrier lifetime via the wafer photoconductance variation [Sinton’96a], with a detection limit of 1 μs approximately, by two different modes, which might be selected depending on the wafer characteristics.

![Figure 6.3 Sketch of the WCT-120 tool using for measuring the minority carrier lifetime. The photoconductance is measured as a function of time and then converted into the excess carrier density (Δn). Depending on the measurement mode, the effective lifetime is directly calculated from Δn (QSS mode) or form its derivate with respect to time (Transient mode)](image)

When selecting the **quasi-steady state** (QSS) mode, the sample is subjected to a long, slowly-decaying pulse of light (i.e. the time constant of the flash is much longer than the carrier lifetime). In this sense, the generation and recombination rates are in balance since the excess carrier populations are always in steady-state. In this case, the sheet conductivity is continuously measured by a radio-frequency coil inductively coupled to the sample and the flash intensity is monitored by a calibrated light sensor. By using existing models for carrier mobilities as functions of doping and injection, and considering the initial (i.e. before illumination) dark sheet conductance, the sheet conductance can be converted into the excess carrier density (Δn) as a function of time. In the same way, the measured flash intensity can be converted into the generation rate (G) of electron/hole pairs as a function of time. Finally, the lifetime can be directly calculated for each excess carrier density, using the steady state condition (Equation 6.3):

\[ \Delta n = G \cdot \tau \]  
(Eq. 6.3)
The main disadvantage of this method is that it requires knowing the optical constants of the sample to estimate the amount of incident light which is absorbed in the sample. This procedure is only valid for low lifetime values ($\tau < 200 \mu s$).

When the transient mode is selected for measuring the carrier lifetime, the samples is subjected to a fast pulse of light, in a way that it returns to dark rapidly. Contrarily to the QSS mode, the sheet conductivity decay is measured as a function of time after the flash has finished and in the same way, it is converted to an average excess carrier density, as explained before. Finally, by taking the time derivative of the conductivity, the carrier lifetime can easily calculated for each carrier density, as indicated by Equation 6.4:

$$\tau = -\Delta n \cdot \left( \frac{\Delta n}{\Delta t} \right)^{-1} \quad \text{(Eq. 6.4)}$$

Contrarily to the QSS mode, the transient mode is preferable for high minority carrier lifetime ($\tau > 100 \mu s$). The reason for this is that carrier lifetimes longer than the flash turn-off time are required for having significant excess carrier density in the sample after the flash has decayed.

Generally, minority carrier lifetime values presented in this thesis are measured for an injection level of $10^5$ cm$^{-3}$; however, for low lifetime values (i.e. lower than 50 $\mu$s) the injection level was necessarily reduced to $10^4$ cm$^{-3}$.

### 6.1.2 Surface passivation

As explained before, the effective lifetime not only accounts for the bulk lifetime; but also for the recombination at the surfaces, which, in principle, should not be affected by the MOVPE environment. Accordingly, with the aim of quantitatively assessing the effect of the wafer processing and the MOVPE environment on the bulk minority carrier lifetime, it is mandatory to reduce the surface recombination so this parameter turns negligible as compared to the bulk lifetime contribution. Hence, the effective lifetime measured by the PCD corresponds to the bulk lifetime. In this sense, the lower the $S_{dss}$ the more accurate the determination of bulk lifetime will be [Page'03]. With the purpose of reducing the surface recombination and enabling an accurate bulk material minority carrier lifetime measurement, wafer surfaces were passivated before performing minority carrier lifetime measurements.

The passivation of silicon surfaces have been studied for decades [Aberle’01 Aberle’94 Chhabra’10 Grant’12 Gruenbaum’90 Horányi’93 Kerr’02a Mack’11 Matsumura’89 Okada’97 Page’03 Pollock’12 Schmidt’08 Solcansky’12 Stephens’94 Stephens’97 Takato’01 Takato’02 Thi’14

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Xiang-an’14 Yablonovitch’86]. In this sense, different alternatives have been proven to successfully passivate the surfaces, reducing significantly the effective recombination velocity.

**6.1.2.1. Surface passivation methods**

One of the most successful passivation technique so far reported is the formation of a silicon oxide by means of the thermal oxidation [Aberle’94 Kerr’02a Mack’11 Schmidt’08]. Despite the excellent effective recombination velocities achieved with this technique ($S_{ef}$ below 10 cm/s [Gruenbaum’90 Stephens’94]), it requires very high temperatures (1000 °C), which might affect the structural quality of the III-V/Si MJSC.

In this sense, low-temperature alternatives have been widely pursued and investigated. On the one hand, regarding dry-passivation methods, the most popular technique used so far consists in the deposition of a silicon nitride layer [Aberle’01 Matsumura’89 Okada’97 Thi’14]. Although this technique has been found to produce reproducible, stable, and high quality passivation layers, its implementation requires special equipment –i.e. a Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor–. Moreover, it is a time consuming and an expensive technique. On the other hand, wet-chemical passivation methods using a liquid or an organic material in a solvent, such as HF passivation, iodine-methanol or quinhydrone-methanol, have been extensively studied [Chhabra’10 Grant’12 Horányi’93 Stephens’97 Takato’02 Yablonovitch’86]. Apart from the already mentioned requisites (i.e. it must be stable over time and achieve a low recombination velocity), the use of wet-chemical passivation methods, must allow the measurement of wafers out of the solution. Consequently, the use of concentrated HF solutions is not recommended due to the danger involved in the manipulation of highly concentrated hydrofluoric acid solutions. Contrarily, the use of iodine or quinhydrone dissolved in methanol is safer and can be used to characterize wafers out of the solution by using simple a plastic bag to hold in the liquid. Despite both solutions have reported good results [Chhabra’10 Horányi’93 Stephens’97 Takato’02], it has been found that quinhydrone-methanol offers a more stable passivation and more reproducible results [Chhabra’10 Takato’01 Takato’02]. Accordingly, this is the preferable method in terms of simplicity, cost, and reproducibility and thus, it has been selected to be the passivation method for most of the samples presented in this thesis.

**6.1.2.2. Chemical cleaning and passivation**

Before passivating wafers, it is necessary to remove the diffused emitter formed in the Si wafers (in case there is one) or etch away the III-V layers grown on the Si substrate, to ensure that the
upper layers are not contributing to the effective lifetime; and so, that the effective lifetime corresponds to the bulk lifetime. Accordingly, for the samples treated under PH₃, the emitter was removed using a standard “etch-back solution”, consisting of HNO₃: HF: H₂O (1000:1:100). This etch was applied for 10 min. at 70 °C, removing approximately 1μm of silicon material, which is roughly a factor of 3 larger than the deepest diffusions measured on the samples. Samples which have been subjected to an epitaxial growth, were etched using an acidic etch (e.g. HCl HNO₃) to remove the epi-layers (homoepitaxial Si or heteroepitaxial III-Vs), followed by an "etch-back" to remove at least one micron of Si surface material from the entire wafer.

Once the emitter and the upper layers have been removed and the wafer surface is clean, samples are passivated using the previously described wet-chemical passivating agent. With this purpose, wafers were dipped for an hour in a 0.05M quinhydrone-methanol solution [Chhabra'10 Solcansky'12 Takato'02]. After this time, samples were removed from the solution and introduced in a hermetic plastic bag, where few milliliters of the solution are incorporated to prevent the wafer from drying.

6.2. MINORITY CARRIER LIFETIME EVOLUTION DURING THE P-N JUNCTION FORMATION

The formation and optimization of the p-n junction has been faced so far from the point of view of the emitter formation (in terms of doping and thickness) and the surface morphology reconstruction for subsequent III-V epitaxy. In this chapter it will be evaluated the impact of these processes on the PV performance of the bottom cell.

Wafer processing in conventional Si technology has been widely studied over the last 50 years [Green'03]. Typically, the formation of the p-n junction is based on the phosphorus diffusion gettering process (PDG), which consists of the formation of a phosphorus Si glass layer (PSG) on the wafer surface and subsequent P diffusion into the wafer [Green'03]. The PSG layer will act as a virtually infinite P source; therefore, the formation of the emitter will take place under supersaturation conditions. It has been demonstrated that the PSG and the highly doped surface layers effectively act as gettering centers, extracting metal impurities from the bulk material, and hence increasing the base layer bulk minority carrier lifetime [Caballero'05 Hofstetter'11 Kang'89 Khedher'05]. Another aspect to be considered in conventional Si processing is the impact of steps with a high thermal load performed in the absence of P (i.e. those that occur without gettering). An example of such a process would be oxidation; a widely used process in
high-efficiency Si technology typically performed at temperatures over 900 °C for durations in the range of hours [Glunz'01b]. Under these circumstances, it is widely accepted that the carrier lifetime mainly suffers a severe drop as a consequence of the activation of metallic (lifetimeo) impurities [Caballero'05]. This activation may result from either the dissolution of internal contaminants present (though inactive) in the as-received wafer or the diffusion of process-induced contaminants into the wafer during the high-temperature step. If the temperature is further increased to above 1000 °C, the generation of crystal defects may also degrade the minority carrier lifetime.

Having briefly summarized key situations in conventional Si processing technology, we can now focus on the MOVPE environment. In a MOVPE reactor, the formation of the p-n junction will be influenced by different factors. On the one hand, the environment will be remarkably different from that of conventional Si technology. In this case, Si wafers are treated in a chamber where several group-III and group-V species coexist in the presence of H₂ carrier gas, high temperatures, and organic radicals. Such an environment may have an unexpected impact on the concentration of deep recombination centers. Furthermore, heating in our MOVPE reactor is carried out using infrared (IR) lamps, which leads to the generation of radiation at significant levels during the process, and annealing under illumination has been demonstrated to produce a negative effect on lifetime since it favors the activation of B-O pairs [Glunz'01a]. On the other hand, wafer treatment required for forming a good bottom cell presents additional peculiarities. As previously explained, an initial wafer annealing at high temperatures will be needed for the surface preparation [Dösgwer'11 Kunert'08]. Furthermore, emitter formation will be achieved by the diffusion of P into the Si substrate under not-necessarily supersaturation conditions, this being the reason why the gettering effect of P might be minimized (in comparison with conventional technology). These two factors, will lead to notable differences in bottom cell PV properties with respect to conventional Si technology.

6.2.1 Silicon Substrate Preparation

In the initial stage of the MOVPE process, wafers are typically subjected to a high-temperature annealing under hydrogen atmosphere to prepare the surface for a high-quality III-V semiconductor epitaxy (oxide pyrolysis, double-step formation ...). This process implies working at high temperatures and the presence of hydrogen in the reactor atmosphere.

The role of the hydrogen on Si bulk lifetime has been widely studied in the past. In this sense, Graff and Pieper reported the detrimental effect of the hydrogen atmosphere on the minority
carrier lifetime of silicon as a consequence of the introduction of deep-level impurities into the material [Graff’80]. In the same way, Ulyashin et al. confirmed the introduction of lifetime killer centers by the presence of H₂, yielding to a reduction of the minority carrier lifetime [Ulyashin’04]. However, none of these studies contemplate a MOVPE environment; which, as explained before, differs significantly from the conventional silicon technology atmosphere.

With the aim of understanding the impact of the substrate preparation process on the minority carrier lifetime, wafers have been submitted to H₂ annealing under different conditions. In this sense, temperature, annealing time or reactor pressure have been varied for assessing the impact of each variable on the bulk lifetime (Table 6.1). Moreover, different wafer resistivity ranges (0.5-1.5 and 5-10 Ω-cm) have been tested (Table 6.1I). Following the substrate preparation process described in Chapter 2, wafers were chemically etched for removing the native silicon oxide and possible external contaminants before being loaded into the reactor.

<table>
<thead>
<tr>
<th>Wafer treatment</th>
<th>Δn (cm³)</th>
<th>τ (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-received</td>
<td>1·10⁵⁵</td>
<td>340</td>
</tr>
<tr>
<td>830 °C 900 mbar</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2 min.</td>
<td>1·10⁵⁵</td>
<td>60</td>
</tr>
<tr>
<td>60 min.</td>
<td>1·10⁴⁴</td>
<td>2</td>
</tr>
<tr>
<td>120 min.</td>
<td>1·10⁴⁴</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>30 min. 900 mbar</td>
<td></td>
<td></td>
</tr>
<tr>
<td>400 °C</td>
<td>1·10⁴⁴</td>
<td>41</td>
</tr>
<tr>
<td>800 °C</td>
<td>1·10⁴⁴</td>
<td>11</td>
</tr>
<tr>
<td>30 min. @ 800 °C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>150 mbar</td>
<td>1·10⁴⁴</td>
<td>7</td>
</tr>
<tr>
<td>900 mbar</td>
<td>1·10⁴⁴</td>
<td>11</td>
</tr>
</tbody>
</table>

Table 6.1 Minority carrier bulk lifetime of wafers annealed in H₂ under different conditions. An as-received wafer was included for comparison. The left column indicates the variable in each batch of experiments.

According to Table 6.1, a significant decrease in bulk minority carrier lifetime occurs during substrate annealing, aimed to prepare the surface for subsequent growth. This degradation process occurs very quickly (note that bulk lifetime is reduced by a factor of five after the first two minutes of annealing) and it continues dropping progressively, reaching values even lower
than the detection limit of the equipment. Unlike reactor pressure, which does not have a remarkable impact on lifetime degradation (at least for those annealing conditions), the annealing temperature seems to determine the degradation process kinetics. Nevertheless, a strong lifetime degradation (as-received lifetime is roughly reduced by a factor of 8) was observed even when a low temperature anneal (400 °C) was performed. Finally, lifetime degradation can be asserted not to be dependent of wafer doping, since the same results were obtained regardless of the wafer resistivity (Table 6.II). The differences in the as-received absolute lifetime values, though, are related to the different resistivity ranges (and consequently, doping levels).

Table 6.II Comparison of the minority carrier bulk lifetime measured on wafers annealed at 830 °C in H₂ for two different resistivity ranges. Values obtained from as-received wafers were also presented.

<table>
<thead>
<tr>
<th>Wafer treatment</th>
<th>Δn (cm⁻³)</th>
<th>τ (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>&gt;10Ω·cm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-received</td>
<td>1·10^{15}</td>
<td>340</td>
</tr>
<tr>
<td>60 min. @ 830 °C 900 mbar</td>
<td>1·10^{14}</td>
<td>2</td>
</tr>
<tr>
<td>120 min. @ 830 °C 900 mbar</td>
<td>1·10^{14}</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>0.5-1.5Ω·cm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-received</td>
<td>1·10^{15}</td>
<td>189</td>
</tr>
<tr>
<td>60 min. @ 830 °C 900 mbar</td>
<td>1·10^{14}</td>
<td>2</td>
</tr>
<tr>
<td>120 min. @ 830 °C 900 mbar</td>
<td>1·10^{14}</td>
<td>&lt; 1</td>
</tr>
</tbody>
</table>

Table 6.III Minority carrier lifetime for wafers annealed in hydrogen for 30 min. at 150 mbar in two different reactors.

<table>
<thead>
<tr>
<th>H₂ anneal</th>
<th>Reactor</th>
<th>Δn (cm⁻³)</th>
<th>τ (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-received</td>
<td>-</td>
<td>10^{15}</td>
<td>340</td>
</tr>
<tr>
<td>30 min. @ 800 °C 150 mbar</td>
<td>Horizontal</td>
<td>10^{14}</td>
<td>7</td>
</tr>
<tr>
<td>30 min. @ 800 °C 150 mbar</td>
<td>CCS</td>
<td>10^{14}</td>
<td>5</td>
</tr>
</tbody>
</table>
Nevertheless, in order to fully rule out the possibility of this degradation being a particular effect, caused by certain contamination present in our horizontal MOVPE reactor; some of the experiments were repeated in different installations. In this case, a close coupled showerhead (CCS) MOVPE reactor, located at The Ohio State University (OSU) was used. Results are presented in Table 6.III. These results prove that the lifetime degradation observed after the surface preparation reported in Table 6.I is neither the effect of a particular reactor condition nor configuration. On the contrary, lifetime degradation seems inherent to the MOVPE environment used for III-V growth (Table 6.III).

Accordingly, several possibilities were considered for explaining this behavior:

a. Light induced degradation, as a result of the activation of B-O pairs;

b. External contamination present at the wafer surface, which diffuses into the bulk at high temperatures (either present in the as-received wafer and not removed in the cleaning or introduced by the MOVPE environment);

c. Activation (i.e. unpassivation) of lifetime killing centers in the Si bulk (initially non-active in the bulk).

In this section, we will review each of these points to understand what is behind this lifetime degradation.

### 6.2.1.1. Light-induced degradation

The degradation of lifetime in Si wafers during illumination has been studied for decades [Caballero’05 Fischer’73 Glunz’01b Weizer’79]. Initially it was believed that this degradation was caused by the formation of certain metal-containing defect complexes. However, in 1997, Schmidt et al. proposed a complete defect reaction which did not involve metallic impurities [Schmidt’97]. This model was based on the formation of B-O pairs, which are metastable defects formed as a result of the binding of an interstitial boron to an interstitial oxygen atom (readily available in Cz-Si) during minority carrier injection. These defects become active in the presence of light and their amount is highly dependent on wafer doping (boron concentration), oxygen concentration, and thermal history of the sample [Glunz’01b]. When these pairs are activated, they act as deep recombination centers, significantly degrading the PV properties of the wafer. However, it was found that this process is reversible and thus, the lifetime can be recovered after annealing at low temperatures (300 °C). Accordingly, the processing of boron-doped Cz-Si wafers has to be optimized (in terms of temperature range, thermal load, and presence of light) to minimize the activation of B-O pairs since, when active, these defects act as very efficient
recombination centers, causing a significant degradation of the minority carrier lifetime [Glunz'01a].

With the aim of determining if the activation of the B-O pairs is the phenomenon responsible for the lifetime degradation, samples were submitted to the following stepwise process: 1) initially, samples were annealed under H₂ to trigger the lifetime degradation (light blue bar in Figure 6.4); 2) afterwards, samples were subjected to a light-soaking experiment, consisting in their exposure to an irradiance of 1000 W/m² in a conventional solar simulator for 24 hours (yellow bar in Figure 6.4) –this process has been reported to effectively activate B-O pairs [Caballero'05] –; 3) finally, samples were annealed at low temperature in a quartz tube furnace at 300 °C for one hour in total absence of light (dark blue bar in Figure 6.4). This process has been shown to be very effective to deactivate B-O pairs [Hashigami'03 Schmidt'02].

![Figure 6.4 Minority carrier bulk lifetime evolution: τ₀ represents the initial value of as-received wafers; τ₁ is the value measured after the MOVPE process; τ₂ is that measured after the light soaking test; and τ₃ is the lifetime measured after dark annealing.](image)

A sample annealed under H₂ for 60 min. at 830 °C (Table 6.1) was selected for performing the light-soaking experiment. The minority carrier lifetime was measured after each step, with τ₀ being the lifetime for the as-received wafer, τ₁ the minority carrier lifetime after the MOVPE process, τ₂ being that after the light degradation test, and τ₃ the lifetime after the low-temperature annealing in the dark. Average results of these experiments are summarized in Figure 6.4.

A strong degradation in lifetime is observed after the MOVPE process (τ₁), as expected. Light exposure (τ₂), which should activate inactive B-O pairs (if any) does not significantly affect the lifetime (the minor differences observed are likely related to the passivation quality); finally,
dark annealing ($\tau_i$), which should deactivate B-O pairs, does not significantly increase the minority carrier lifetime (in fact, they are virtually identical considering the uncertainty in the measurement). These findings suggest that lifetime degradation during the MOVPE process is not dominated by the activation of B-O pairs. Therefore, other defects or impurities must be behind the drop in lifetime.

In order to fully discard the activation of B-O pairs as the process behind the lifetime degradation, Gallium doped Cz Si wafers were tested. Accordingly, Si:Ga wafers were annealed in hydrogen at 830 °C for two different durations. Afterwards, they were compared with the results obtained for Si:B wafers subjected to the same annealing conditions (Table 6.IV).

<table>
<thead>
<tr>
<th>Treatment</th>
<th>$\Delta n$ (cm$^3$)</th>
<th>Si:B</th>
<th>Si:Ga</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-received</td>
<td>$10^{15}$</td>
<td>340</td>
<td>250</td>
</tr>
<tr>
<td>60 min. @830°C 900 mbar</td>
<td>$10^{14}$</td>
<td>2</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>120 min. @830°C 900 mbar</td>
<td>$10^{14}$</td>
<td>&lt; 1</td>
<td>&lt; 1</td>
</tr>
</tbody>
</table>

Despite the differences in the initial lifetime, the consequences of the H$_2$ annealing are the same regardless of the dopant used, measuring drastically reduced lifetimes after H$_2$ annealing. Accordingly, the activation of B-O pairs can be definitely discarded to be the phenomenon responsible for the lifetime degradation registered during the substrate preparation.

### 6.2.1.2. External contamination

It is well known that any metal contaminant initially present on a wafer surface will diffuse into the wafer’s bulk during a high temperature annealing, as a result of the thermal load. In this sense, the importance of a thorough wafer cleaning before subsequent thermal processing has been repeatedly reported in the literature [Dösch 11 Kunert 08]. In order to discard external contamination as the origin of the bulk lifetime degradation, the impact of the cleaning method on the minority carrier lifetime was assessed (Table 6.V). With this aim, wafers were cleaned using different chemical treatments. Afterwards, they were submitted to a hydrogen anneal.
Three different conventional cleaning methods [Kern’08 Kern’70], whose effectiveness on wafer cleaning was repeatedly reported, were tested:

a. Method A: diluted fluoryhydric acid

b. Method B: diluted fluoryhydric acid followed by a de-ionized water rinse

c. Method C: the standard RCA cleaning (described in Chapter 2)

d. Furthermore, a non-cleaned wafer was included for comparison.

As Table 6.5 evidences, no significant differences were observed on minority carrier lifetime despite the fact that different cleaning methods were used. Indeed, lifetimes are virtually identical considering the uncertainty of the equipment. Moreover, no difference was observed with respect to the non-cleaned wafer, meaning that the introduction of external impurities coming from a deficient wafer cleaning is not the main reason behind lifetime degradation observed during substrate preparation.

Table 6.5 Minority carrier lifetime of wafers cleaned following different routines. After cleaning, they were annealed in hydrogen for 30 min at 100 mbar.

<table>
<thead>
<tr>
<th>Cleaning</th>
<th>H₂ anneal</th>
<th>( \Delta n ) (\text{cm}^{-3})</th>
<th>( \tau ) (\text{µs})</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>As-received</td>
<td>( 10^{15} )</td>
<td>340</td>
</tr>
<tr>
<td>None</td>
<td>30 min. 830 °C</td>
<td>( 10^{14} )</td>
<td>9</td>
</tr>
<tr>
<td>Method A</td>
<td>30 min. 830 °C</td>
<td>( 10^{14} )</td>
<td>8</td>
</tr>
<tr>
<td>Method B</td>
<td>30 min. 830 °C</td>
<td>( 10^{14} )</td>
<td>6</td>
</tr>
<tr>
<td>Method C</td>
<td>30 min. 830 °C</td>
<td>( 10^{14} )</td>
<td>5</td>
</tr>
</tbody>
</table>

\subsection*{6.2.1.3. Activation of lifetime killing impurities}

The last possibility which was considered to be responsible for this degradation is the activation of lifetime killing impurities during the thermal process. These impurities could be either initially present in the wafer (though passivated) and be then activated (i.e. lose their passivation) during the MOVPE process, or they could come from the reactor atmosphere itself.

One example of recombination centers formed during the thermal anneal could be the formation of the well-known H-O complexes. For conventional silicon PV technology, it has
been reported that the presence of H$_2$ in p-type crystalline Si wafers is not desirable because of the introduction of lifetime killing centers by the formation of these complexes [Graff’80, Hara’95, Hatakeyama’97, Ulyashin’04]. On the one hand, it is known that Cz wafers contain a high concentration of defects (mainly oxygen), which could eventually associate to the hydrogen forming lifetime killing centers [Graff’80, Hara’95, Hatakeyama’97, Ulyashin’04]. On the contrary, Float zone wafers present an extremely low concentration of light impurities, such as carbon and oxygen. In this sense, it is expected that if the lifetime degradation process is trigged by these recombination centers (i.e. H-O complexes), then the use of Fz wafers should reduce significantly the drop in lifetime. Therefore, with the aim of ascertaining whether the activation of internal impurities is responsible for such degradation, Fz Si wafers were subjected to a H$_2$ anneal at high temperature. Resulting lifetime values were compared to the one measured on Cz wafer annealed under the same conditions (Table 6.VI).

Table 6.VI: Minority carrier lifetime comparison for Cz and Fz wafers annealed in H$_2$ for 30 min.

<table>
<thead>
<tr>
<th>Wafer treatment</th>
<th>(\Delta n (\text{cm}^{-3}))</th>
<th>(\tau (\mu\text{s}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cz wafers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-received</td>
<td>(1\times10^5)</td>
<td>340</td>
</tr>
<tr>
<td>30 min. @ 800 °C 150 mbar</td>
<td>(1\times10^4)</td>
<td>7</td>
</tr>
<tr>
<td>Fz wafers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>As-received</td>
<td>(1\times10^3)</td>
<td>449</td>
</tr>
<tr>
<td>30 min. @ 800 °C 150 mbar</td>
<td>(1\times10^4)</td>
<td>5</td>
</tr>
</tbody>
</table>

Despite the oxygen content on Fz wafers is expected to be negligible, their use yields an important lifetime degradation, similar to the one reported on Cz wafers (Table 6.VI). This behavior made us rule out the possibility of H-O complexes formation as the main responsible for this degradation. Nevertheless, the activation/formation of recombination centers can be triggered by other processes; for instance, they can be introduced from the MOVPE atmosphere. This possibility has been considered by studying the effect of the carrier gas influence onto the lifetime degradation. In this case, samples have been annealed under two different carrier gases (i.e. H$_2$ and N$_2$). The results of this experiment are summarized in Table 6.VII.

As it is shown in Table 6.VII, loosely the same values were measured after the annealing, regardless of the carrier gas; suggesting that H$_2$ does not have a determinant role in the degradation of electron lifetime in the p-silicon wafer. Moreover, these results serve to definitely
discard the hypothesis of the H-O complexes being responsible for such degradation, since even in the absence of hydrogen, lifetime is highly degraded.

Table 6.VII Minority carrier lifetime of wafers annealed for 30 min. at 900 mbar in different atmospheres. In this case, low-resistivity wafers (1-5 Ω·cm) were used.

<table>
<thead>
<tr>
<th>Treatment</th>
<th>Δn (cm⁻³)</th>
<th>τ(μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>As-received</td>
<td>10¹⁵</td>
<td>340</td>
</tr>
<tr>
<td>30 min. @830°C 900 mbar H₂</td>
<td>10¹⁴</td>
<td>11</td>
</tr>
<tr>
<td>30 min. @830°C 900 mbar N₂</td>
<td>10¹⁴</td>
<td>17</td>
</tr>
</tbody>
</table>

At this point, the possible formation of recombination centers during the thermal treatment can be confirmed not to be linked either to the formation of H-O complexes resulting from the presence of oxygen on the wafers; or to the introduction of impurities from the MOVPE atmosphere (carrier gas). Nevertheless, these are not the only possible mechanisms for triggering the formation of recombination centers. For instance, the formation of point defects or swirls during the thermal anneal might also have deleterious consequences on the minority carrier lifetime. Moreover, extrinsic lifetime killing impurities coming from the MOVPE environment (in general, not only from the carrier gas), might diffuse into the wafer bulk, turning into recombination centers after certain thermal load. Accordingly, the hypothesis of the lifetime degradation as a result of the formation of lifetime killing centers cannot be ruled out at this point.

In summary, the preparation of Si substrates for achieving an oxide-free and single domain structure has been found to have deleterious consequences on the minority carrier lifetime. Some possible causes behind this effect can excluded in the light of the experiments herein described, namely, B-O pairs, external contamination from a defective cleaning or carrier gas. With the aim of a better understanding of this phenomenon, the evolution of the bulk lifetime during the formation of the emitter will be studied.
6.2.2 Emitter formation

In conventional silicon technology, it has been demonstrated that the phosphorous-silicon glass (PSG) layer deposited on the wafer surface for acting as the P-source for the emitter formation, also works as a gettering center, extracting metal impurities from the bulk material, and hence increasing the base layer bulk minority carrier lifetime. On the other hand, in a MOVPE environment, the diffused emitter is formed under different circumstances. In this sense, wafers are exposed to high-temperature anneal under phosphine to enable the diffusion of P into the Si substrate, occurring in the absence of the PSG layer. This fact might have important consequences on limiting the gettering effect of phosphorous on extracting impurities.

This section aims to analyze the effect of the emitter formation in a MOVPE environment on the minority carrier lifetime. With this purpose, a wide variety of conditions (i.e. temperature, time exposure, PH$_3$ partial pressure...) were tested to assess the role of each parameter on the bulk lifetime. Firstly, the effect of the phosphine partial pressure on the minority carrier lifetime was analyzed. In this sense, wafers were annealed for 60 min. at 830 °C under different PH$_3$ partial pressures (Figure 6.5).

![Minority carrier bulk lifetime of P-diffused wafers after removing the emitter. Wafers were heated for 60 min. at 830 °C under different phosphine partial pressures. The average bulk lifetime of an as-received wafer is included (striped bar) for comparison. Minority carrier lifetime was calculated for an injection level of 10$^4$ cm$^{-3}$.

As shown in Figure 6.5, the improvement of minority carrier lifetime during the formation of the emitter is clear. The bulk lifetime increases as the PH$_3$ partial pressure does, reaching values close to those measured in as-received wafers, for the diffusions performed under the highest PH$_3$ partial pressure studied. This means that the drop in minority carrier lifetime occurring
during the anneal under H₂ used to prepare the Si wafer surface (Table 6.1) can be reversed, and suitable PV properties in the bottom cell base can be obtained.

Secondly, the effect on bulk lifetime of temperature and PH₃ annealing duration was assessed. With this aim, samples were annealed in phosphine at different temperatures (800 °C and 830 °C) for different times (5 min., 10 min., 20 min., 30 min. and 60 min.). In all cases, phosphine partial pressure remained constant and equal to 32.1 mbar as suggested in Figure 6.5.

Wafers were cleaned (according to above mentioned Method B) before being loaded into the MOVPE reactor. They were heated up in H₂ to the defined set point and, once the desired temperature was reached and stabilized, the PH₃ source was opened. With the aim of assessing the impact of the initial H₂ heating ramp (prior to the phosphine exposure) on minority carrier lifetime, a sample which was just heated up to the annealing temperature (in H₂) and cooled down afterwards, was also included for each temperature.

![Minority carrier lifetime vs Annealing Duration](image)

**Figure 6.6** Average minority carrier lifetime for Si wafers annealed under 32.1 mbar of PH₃ at 800 °C and 830 °C for different times. Lifetimes were calculated for an injection level of 10¹⁵ cm⁻³.

The average lifetime has been plotted in Figure 6.6, which shows the lifetime evolution as a function of PH₃ annealing conditions. The error bars represent the maximum and minimum values measured for each sample. The wide range of variation of the minority carrier lifetimes measured in the experiments is believed to be related to the surface passivation quality.

According to [Grivickas'89], the effective lifetime is related with the bulk lifetime and the effective surface recombination velocity –for S_{eff} lower than 10⁷ cm/s– following Equation 6.5.
\[ \frac{1}{\tau_{\text{eff}}} = \frac{1}{\tau_{b}} + \left[ \frac{W}{2S_{\text{eff}}} + \frac{1}{D} \left( \frac{W}{n} \right)^2 \right]^{-1} \] 

(Eq. 6.5)

Being \( D \) the diffusion coefficient for silicon (30 cm\(^2\)/s) and \( W \) de wafer thickness (275 \( \mu \)m).

Following Equation 6.5, the effective lifetime will be limited by the surface recombination velocity for samples with a very high bulk lifetime. On the contrary, it will be determined by the bulk lifetime for samples with an excellent passivation quality (i.e. very low \( S_{\text{eff}} \)). Figure 6.7 shows the contribution of minority carrier bulk lifetime and \( S_{\text{eff}} \) to the effective lifetime. It confirms the importance of having a low surface recombination velocity for measuring high effective lifetimes. Moreover, Figure 6.7 points out that wafers with high bulk lifetimes require an extremely good passivation (\( S_{\text{eff}} < 5 \) cm/s), to ensure that the effective lifetime measured corresponds to the bulk lifetime and it is not being limited by \( S_{\text{eff}} \). The fact that such low surface recombination velocity is needed for measuring the real bulk lifetime can explain the high variability of measurements shown in c.

According to literature, a wide range of SRV can be obtained depending on the passivating agent and the wafer specifications. For instance, \( S_{\text{eff}} \) values in the 20-50 cm/s range are usually reported for silicon nitride passivated surfaces; however, a record low \( S_{\text{eff}} \) of 4 cm/s were reported for a low-resistivity p-type Si wafer [Lauinger’96], reducing roughly in a factor of 10 the recombination velocity reported for SiO\(_2\) passivated surfaces. Typical values of \( S_{\text{eff}} \) for iodine/ethanol passivated surfaces are in the 10-50 cm/s range [Stephens’97]. Finally, typical values of about 10 cm/s were usually measured for quinhydrone/methanol passivated Si surfaces (the strategy used in this work); being the lowest \( S_{\text{eff}} \) reported 4.2 cm/s for a Fz Si wafer [Takato’03]. Therefore, a constant \( S_{\text{eff}} \) cannot be assumed for all the samples, since it will be deeply modulated by the surface preparation and the wafer properties. However, it seems reasonable to expect a \( S_{\text{eff}} \) in the range of 1-20 cm/s for our quinhydrone/methanol passivated surfaces (shown as a gray stripe in Figure 6.7).

With the aim of assessing the real impact of the surface passivation quality on measured (i.e. effective) lifetime, we have compared the bulk lifetime, corresponding to each average effective lifetime shown in Figure 6.6, for two different values of \( S_{\text{eff}} \) (within the expected range) according to Equation 6.5. Results are summarized in Figure 6.8. Despite \( S_{\text{eff}} \) is low in both cases (< 20 cm/s); a big discrepancy between \( \tau_{\text{eff}} \) and \( \tau_0 \) is observed. In this way, only when having an extremely good passivation (\( S_{\text{eff}} = 1 \) cm/s), the effective lifetime will correspond to the bulk lifetime. Otherwise (when having slightly higher, but still low, \( S_{\text{eff}} \)) the surface recombination limits the effective lifetime, and hence, the gap between \( \tau_0 \) and \( \tau_{\text{eff}} \) increases, measuring much...
lower $\tau_{\text{eff}}$. This fact can thereby explain the big variability in measurements depicted in Figure 6.6. In this sense, for a wafer with a certain $\tau_{\infty}$ only when a perfectly cleaned surface is obtained, an excellent passivation quality is achieved and thus, a $\tau_{\text{eff}}$ close to the $\tau_{\infty}$ is measured (highest level of the error bars included in Figure 6.6). On the contrary, when surfaces are not perfectly passivated (because of a poorer cleaning or non-uniform passivation), then $S_{\text{eff}}$ begins to limit the effective lifetime, measuring lower $\tau_{\text{eff}}$ (lowest level of the error bars in Figure 6.6) for the same $\tau_{\infty}$.

![Figure 6.7 Effective lifetime for a 275 µm thick Si wafer as a function of bulk lifetime and surface recombination velocity. A gray stripe, which corresponds to the expected range of $S_{\text{eff}}$ using quinhydrone/methanol solution as the passivating agent, has been also included.](image)

With such wide variation ranges (which are the result of small changes in the processing of the samples) we have concluded that we cannot accurately and repeatedly determine lifetimes above 350 µs. In other words, for measured lifetimes below 350 µs, we can be sure that they are close to the real bulk lifetime. For measured lifetimes above the 350 µs limit, we are limited by surface recombination velocity and the effective lifetime is just a lower limit for the bulk lifetime.

In summary, we have reported the effect of the emitter formation (by P diffusion) on the minority carrier lifetime (Figure 6.6) in a MOVPE environment. After heating up the wafer to the annealing temperature (in the absence of phosphine), the initial lifetime (340 µs) is roughly reduced by a factor of 3 (see leftmost bars of both temperatures in Figure 6.6); corroborating the effect shown in Table 6.1. Nevertheless, despite the initial degradation during the heating up of the wafer, lifetime can be recovered during the emitter formation, as it is shown in Figure 6.6.
Chapter 6
Photovoltaic behavior of the bottom cell

The impact on annealing duration and temperature has been assessed. However, it is complicated to quantify this improvement, since results will be deeply affected by small (i.e. highly uncontrollable) changes in the surface passivation quality that will limit our precision to assess the real bulk lifetime. Nevertheless, in the worst cases, lifetime was recovered to the initial value of the as-received wafer; while in the best cases, values larger than 1 ms were measured.

![Figure 6.8 Compass of bulk lifetime, calculated from average effective lifetimes reported in Figure 6.6 for 800 °C, for two different surface recombination velocities.](image)

The lifetime recovery has been linked so far to the gettering effect of P on extracting impurities, alike to what happens in conventional PV Si technology. The pyrolysis of PH₃ at high temperatures will supply important quantities of P but; nonetheless it also will provide some atomic hydrogen. This element is an extremely fast interstitial diffuser in Si [Bracht'00], capable of penetrating deep (or entirely through) the wafer at the process conditions employed during the emitter formation. The role of atomic H as a passivating agent has been widely reported in the literature [Ammerlaan'04 Hallam'13 Karzel'13 Kazmerski'87 McLean'06 Pearton'92 Ulyashin'04]. For example, the suppression of swirl defect formation by hydrogen doping has been reported by several authors [Ciszek'73 Wang'91]. Moreover, its effect on neutralizing recombination centers in Si has been well studied. Karzel et al. demonstrated the beneficial effect of the hydrogenation (by means of atomic H) on the improvement of the average effective bulk minority carrier lifetime on multicrystalline silicon [Karzel'13]. Similarly, Ulyashin et al. reported the improvement of the lifetime by the passivation of dangling bonds within structural defects [Ulyashin'04]. Moreover, it has been reported that hydrogenation of metallic impurities in Si wafers can yield a significant reduction in associated traps states, with reported reductions
for interstitial Fe by a factor of 5 [McLean’06] and for Zn up to roughly two orders of magnitude [Ammerlaan’04 Stolz’89]. Finally, Ammerlaan [Ammerlaan’04] and Stolz et al. [Stolz’89] reported the passivation of both acceptors (B, Al, Ga, Be, Zn…) and donors (P, As, Sb…) by the formation of stable acceptor-hydrogen (or donor-hydrogen) complexes. Therefore, it is very likely that, regardless of the specific source of the lifetime degradation, atomic H can act as an effective passivating agent, yielding an effective lifetime recovery.

Therefore two possible explanations for the lifetime recovery can be sustained at this point: the gettering effect of the P on extracting impurities (as it happens in conventional PV Si technology); or the passivation of the already activated recombination centers by atomic hydrogen. Further steps will serve to clarify this point.

### 6.2.3 Silicon surface reconstruction

Although the formation of the emitter by P diffusion can produce excellent lifetimes in the base and optimum emitter properties in the Si subcell; we have demonstrated that the effect of long PH₃ exposures at temperatures ranging from 800-875 °C will lead to an important degradation of the surface morphology. Of course, a degraded surface morphology will have deleterious repercussions on the quality of the subsequent epitaxial III-V layers. In this sense, we have also proven that using a combined treatment consisting on PH₃ exposure (Step 1) followed by a H₂ annealing (Step 2), lead us to obtain an optimum emitter (shallow and highly doped) while recovering surface morphology to acceptably low RMS values.

Previously, we have reported that the initial degraded lifetime (observed during the surface preparation) can be recovered during the emitter formation, achieving lifetimes even higher than the as-received values. Nevertheless, the additional H₂ anneal intended to reconstruct the surface morphology, might vary the Si bulk lifetime. Accordingly, the impact of this combined treatment on the minority carrier lifetime has been assessed at this point. With this aim, a lifetime comparison between wafers annealed in PH₃ (samples 6.1, 6.3 and 6.7) and wafers subjected to the combined treatment (as described in Chapter 4) is presented in Figure 6.9. The annealing conditions for each sample have been summarized in Table 6.VIII.
Table 6.VIII Description of the MOVPE routine followed by Samples 1 to 8, where wafers were first annealed under hydrogen mixed with 32.1 mbar of PH₃ and then annealed under pure H₂.

<table>
<thead>
<tr>
<th></th>
<th>6.1</th>
<th>6.2</th>
<th>6.3</th>
<th>6.4</th>
<th>6.5</th>
<th>6.6</th>
<th>6.7</th>
<th>6.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>800</td>
<td>800</td>
<td>830</td>
<td>830</td>
<td>830</td>
<td>830</td>
<td>875</td>
<td>875</td>
</tr>
<tr>
<td>Time (min)</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>30</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>PH₃ (mbar)</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
<td>32.1</td>
</tr>
<tr>
<td>Step 2</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Temp (°C)</td>
<td>-</td>
<td>830</td>
<td>-</td>
<td>830</td>
<td>830</td>
<td>875</td>
<td>-</td>
<td>875</td>
</tr>
<tr>
<td>Time (min)</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>20</td>
<td>60</td>
<td>60</td>
<td>-</td>
<td>60</td>
</tr>
<tr>
<td>PH₃ (mbar)</td>
<td>-</td>
<td>0</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>-</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 6.9 Minority carrier lifetime for samples summarized in Table 6.VIII. Solid bars correspond to samples annealed under PH₃ (lifetimes correspond to an injection level of 10¹⁵ cm⁻³). Samples submitted to the combined treatment were represented as dashed bars (injection level of 10¹⁴ cm⁻³).

Although bulk lifetime reaches high values after PH₃ exposure (solid bars in Figure 6.9), it gradually degrades after the second step in H₂ (dashed bars). This degradation is deeply modulated by the H₂ annealing conditions; becoming more important as the temperature increases and the annealing duration becomes longer. In this case, the degradation of lifetime is
unequivocal since the effective values measured are too low to be affected by surface passivation. This phenomenon limits the use of H₂ anneals to recover the morphology of the silicon surface and underlines the importance of gaining more insight into the processes behind minority carrier lifetime degradation.

What this result suggests is that the role of PH₃ in recovering lifetime is not related to a classic P gettering process as occurs in conventional Si PV technology. In other words, the preferential segregation of the lifetime killing impurity/defect that is responsible for minority carrier lifetime degradation to the highly P-doped region seems unlikely. This is because the highly P-doped region is still there during Step 2 (i.e. H₂ anneal), the high temperatures (to promote fast diffusion of impurities) are still there too, but the minority carrier lifetime degrades indicating that the lifetime killing impurity (or level) is re-introduced (or re-activated) in the bulk. In the light of these result, two different mechanisms have been suggested to explain this behavior.

**Mechanism 1:** The initial treatment under H₂ at high temperatures introduces an extrinsic lifetime-killing impurity coming from the reactor. During the PH₃ anneal, this impurity is either extracted with the help of the P surface coverage or passivated somehow with atomic H, coming from the pyrolysis of PH₃. The first process (extraction by P) seems unlikely since Figure 6.9 indicates that this process is extremely fast (in 5 minutes the lifetime seems to be recovered). More in agreement with such high speed would be a passivation process of the lifetime killing impurity based on the diffusion of atomic H into the silicon lattice. Once PH₃ flow is interrupted whilst high temperatures are still maintained, this passivation is gradually lost or new amounts of the impurity are introduced in the wafer.

**Mechanism 2:** The treatment under H₂ at high temperatures leads to the formation of thermally generated defects (swirls, point defects ...), which eventually become recombination centers by themselves or by interacting with some pre-existing intrinsic impurity, such as oxygen. During the PH₃ anneal, these recombination centers are either extracted with the help of the P diffusion process or passivated with atomic H. As in the previous case, due to the speed of this process, the passivation process based on the diffusion of atomic H into the silicon lattice is the most realistic option. Once PH₃ flow is interrupted, this passivation is lost and hence, new recombination centers are formed in the wafer, degrading again the lifetime.

In summary, the impact of the MOVPE environment on the minority carrier lifetime during the optimization of the Si bottom subcell, for its eventual integration on a III-V/Si MJSC has been analyzed so far. Firstly, we have studied the effect on the minority carrier lifetimes of the H₂ anneals at high temperature used for surface preparation. An important degradation of minority
carrier lifetime during the thermal treatment has been observed. The reproducibility of these results has been proven by repeating the most relevant experiments in two different MOVPE reactors. The exact cause behind this phenomenon remains unclear; however, some progress has been made so far to understand the process behind this degradation. On the one hand, it has been demonstrated that this degradation is not produced by a defective cleaning process prior to loading the samples in the MOVPE reactor, ruling out the introduction of an external contaminant (coming from a poorly cleaned wafer surface) as the possible cause behind lifetime degradation. On the other hand, we have discarded the sole effect of the hydrogen carrier gas on activating lifetime killing centers (as occurs in conventional Si technology with O-H pairs), since the same degradation was observed when N₂ was used as the carrier gas. In this sense, two different mechanisms based on 1) the introduction of extrinsic lifetime-killing impurities; 2) defect formation during the thermal treatment, are being considered as the possible mechanisms governing the lifetime degradation.

It has been also reported that the degraded minority carrier lifetime can be recovered during the exposure to a PH₃ atmosphere for the emitter formation. The extent of this recovery is difficult to assess since the impact of low (but not negligible) surface recombination velocities impedes an accurate determination of high bulk minority carrier lifetimes. Although the mechanisms governing this phenomenon have not been fully understood yet, it seems that phosphorus gettering cannot be the mechanism behind lifetime recovery. On the contrary, the passivation of recombination centers by atomic hydrogen, resulting from phosphine pyrolysis, is considered at this point to be the most likely explanation for the lifetime recovery.

Finally, we have assessed the impact on the minority carrier lifetime of an additional H₂ annealing after PH₃ exposure for emitter formation. The goal of this new annealing is to recover surface morphology (degraded during PH₃ exposure) and ensure a smooth surface for subsequent III-V growth. This experiment reveals that, once the phosphine supply was interrupted, the degradation of minority carrier lifetime starts again just as occurred in the initial H₂ anneal. This degradation is believed to be related to a loss of the passivation provided by H (since once the PH₃ is interrupted, the H supplied is not available any more), which turns into a re-activation of the recombination centers.
6.3. Minority Carrier Lifetime Evolution During Epitaxial Growth

Hitherto, the minority carrier lifetime evolution during the formation and optimization of the bottom subcell has been evaluated. Nevertheless, subsequent processing during the epitaxial growth might also affect the minority carrier lifetime. Indeed, different ambient environments can be present during the growth of the III-V/Si structure within a MOVPE reactor. In the previous section, the impact of the p-n junction formation on the PV performance of the solar cell was assessed. In that case, the emitter of the bottom cell was formed in a manner more aligned with traditional Si solar cell fabrication methods, such as phosphorus diffusion into a p-type wafer. Nonetheless, an alternative to this method consist on the emitter formation by the homoepitaxial growth of n-type Si on a p-type substrate [Grassman’14 Grassman’13b]. As previously reported, the election of this alternative is based on the reported necessity of growing a Si homoepitaxial layer to create a defect-free nucleation layer so that subsequent ideal GaAsP graded buffers can successfully occur. Despite high quality III-V layers have been successfully integrated on silicon substrates with a homoepitaxial emitter; the impact of these steps on the Si bulk lifetime has not been explored. With the purpose of studying the effect of these environments on the PV performance of the solar cell, a scientific collaboration was established with the Ohio State University (OSU), which has demonstrated to have a wide experience on the growth of III-V/Si solar cells. In this collaboration, the group headed by Professor Ringel at the Department of Electrical and Computer Engineering and the Institute for Material Research developed the III-V/Si structures, carrying out the optimization of the epitaxial routines and their structural characterization. These structures were used afterwards to study the effect of the III-V growth routines on the minority carrier lifetime, which was carried out by the UPM group.

To visualize the evolution of minority carrier lifetime in the Si wafer throughout the growth process, a wide set of samples were grown, with interruptions at one of four different points in the process: (1) homoepitaxial emitter, (2) homoepitaxial emitter + Atomic Layer Epitaxy (ALE) GaP nucleation layer, (3) homoepitaxial emitter + ALE GaP nucleation layer + GaP “bulk” layer, (4) homoepitaxial emitter + ALE GaP nucleation layer + GaP “bulk” layer + GaAsP1-x buffer. All of these steps are directed towards the development of the III-V/Si metamorphic structure depicted in Figure 1.5.a. The structures were grown on an Aixtron 3×2 close-coupled showerhead MOCVD system, located at the Ohio State University. Unless otherwise specified,
the substrates used were p-type (B-doped, 1 – 5 Ω-cm) float-zone Si (100) wafers, intentionally misoriented 6° towards <011>.

To track the evolution of the bulk Si minority carrier lifetime throughout the growth process, multiple samples were produced ending at the four different process phases described above. Before performing minority carrier lifetime measurements, all epitaxial material was removed via etching in a HCl: HNO3 solution. Moreover at least 1 μm of Si surface material was stripped away for ensuring a cleaned surface. The etched sample was then passivated in a 0.05M quinhydrone-methanol solution bath, as detailed before.

### 6.3.1 Epitaxial Emitter Growth

As previously discussed, in this section we will consider homoepitaxially grown emitters for the formation of the Si subcell. This approach is the one selected by the OSU group for the emitter formation since it also serves to bury any residual surface contamination, namely carbon, which can lead to non-ideal GaP nucleation. This step is conducted at 760 °C using a dilute SiH₄ source (typically used for n-type doping of III-V compounds), and with a growth rate of around ~5 Å/min.

Table 6.IX presents the bulk Si lifetime data after the first phase of the process (i.e. homoepitaxial growth of the emitter) with data from the as-received wafer included for comparison. Two different layer thickness, and thus growth times, were considered: 20 nm (40 min.) and 90 nm (180 min.).

Table 6.IX Evolution of average minority carrier lifetime for Fz Si wafers after the emitter formation by homoepitaxial growth. The emitter has been chemically removed for measuring the bulk lifetime. An as-received Fz wafer has been included for comparison.

<table>
<thead>
<tr>
<th>Treatment</th>
<th>Δn (cm⁻³)</th>
<th>τ (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Fz Si as-received</td>
<td>10¹⁵</td>
<td>432</td>
</tr>
<tr>
<td>Homoepitaxial emitter of ~20 nm (40 min.)</td>
<td>10¹⁴</td>
<td>6</td>
</tr>
<tr>
<td>Homoepitaxial emitter of ~90 nm (180 min.)</td>
<td>10¹⁴</td>
<td>1</td>
</tr>
</tbody>
</table>
According to Table 6.IX a massive degradation of more than two orders of magnitude of the minority carrier lifetime appears to occur over the course of the homoepitaxial Si emitter growth. Given that a lifetime reduction from 432 µs to only 6 µs was observed for even the relatively short growth period (40 min, 20 nm), the degradation process clearly occurs quite rapidly. An additional 140 min. (70 nm) growth reduces the lifetime further to 1 µs. However, since this is actually the lower detection limit for the instrument being used, it is is possible that the actual lifetime of the 90 nm emitter sample is even lower. Regardless of the final result, the low lifetime values observed in both cases are clearly detrimental to photovoltaic performance.

For the interpretation of this evolution, it is enlightening to compare this process with the process followed to prepare the silicon surfaces for subsequent epitaxial growth in a MOVPE environment (Table 6.I). The main analogy that can be extracted from this comparison is the similar degradation observed on both approaches. Indeed, if we neglect the small contribution of SiH₄ to the process atmosphere, the homoepitaxial growth of the emitter is a step very similar to an annealing under H₂ in a MOVPE environment, which has been reported to produce a rapid degradation of the lifetime (Table 6.I). From that study it was possible to eliminate a few potential degradation mechanisms, including: (1) wafer treatment (cleaning) prior to loading into the MOVPE reactor; (2) wafer type –Cz Si:B versus Fz Si:B versus Cz Si:Ga from different suppliers; or (3) carrier gas –H₂ versus N₂. In the light of the results here presented, and in accordance with previous results, two potential mechanisms were considered: introduction of lifetime-killing extrinsic (in-diffused) impurities from within the MOVPE reactor or formation of thermally-generated defects, which eventually become recombination centers.

An important feature of an extrinsic diffusion mechanism is that any such impurity should show a decreasing concentration with depth into the wafer, provided that the diffusivity is not such that the diffusion front can extend through the entire wafer thickness. High impurity/defect concentrations near the wafer surfaces can produce an effective bulk lifetime reduction, similar to that seen with high surface recombination velocities [Martin’13]. Therefore, if the lifetime degradation observed here is the result of some in-diffused impurity species, then removal of sufficient material from the wafer surfaces (where the concentration of the impurity would be highest) should result in an effective bulk lifetime recovery.

Table 6.X presents the results of just such an experiment where a chemical etch (CH₃COOH:HNO₃:HF) was used to remove approximately 20 µm of surface material from lifetime-degraded Si wafers, with a comparison of pre- and post-etch minority carrier lifetimes, τᵣ and τᵣ₀ respectively. Prior to etching, the p-type Fz-Si wafers were submitted to different
lifetime-killing high-temperature (830 °C) anneals in H₂ ambient of either 2 min. or 30 min., as well as different pre-anneal treatments (HF oxide etching vs. no chemical treatment). As seen in Table 6.X, the degraded bulk minority carrier lifetimes were found to remain virtually unchanged after etching, if not even slightly lower, suggesting that lifetime degradation is indeed a bulk effect rather than a surface induced effect. The minor differences (i.e. slightly lower post-etch values) may be related to the passivation quality, which could be to some extent impacted by the increased surface roughness resulting from the deep etch, but such effects are expected to be very small.

Table 6.X Minority carrier lifetime comparison before (a) and after (g) etching the silicon wafer. The estimated removed thickness from each side of the wafer, Δt, is included in the last column.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Cleaning</th>
<th>Treatment</th>
<th>τ₀ (μs)</th>
<th>τ₁ (μs)</th>
<th>Δt/substrate (μm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>HF</td>
<td>2 min. 830°C 100 mbar H₂</td>
<td>60</td>
<td>54</td>
<td>22.5</td>
</tr>
<tr>
<td>B</td>
<td>HF</td>
<td>30 min. 830°C 100 mbar H₂</td>
<td>5</td>
<td>5</td>
<td>26</td>
</tr>
<tr>
<td>C</td>
<td>None</td>
<td>30 min. 830°C 100 mbar H₂</td>
<td>9</td>
<td>7</td>
<td>23</td>
</tr>
</tbody>
</table>

Zinc was suggested to be a possible candidate for such extrinsic lifetime killing impurity associated to the MOVPE environment [García-Tabarés’14]. Zn was considered as the most likely option, since it is a typical p-type dopant in III-V semiconductors, and thus traces could be present in many MOCVD environments. Zn is also a fast-moving impurity with strong lifetime-killing effects in Si at concentrations as low as 10¹⁵ cm⁻³ capable of ruining minority carrier lifetime [Coletti’11], making it difficult to detect via standard methods like SIMS. Accordingly, in order to verify these results, the diffusion profiles of Zn, for the conditions shown in Table 6.X, were calculated using a simple Fickian diffusion model and are presented in Figure 6.10. A Zn-in-Si diffusivity (at 830°C) of 4×10⁹ cm²/sec [Bracht’00] and a constant surface impurity concentration (C₀) were used. It has been reported that, under some circumstances, the diffusion of Zn in Si deviates from the complementary error function (erfc) profile and follows a kick-out diffusion profile [Grünebaum’91]. However, according to the same work, the erfc profile always represents the most intense diffusion for wafer thicknesses below 500 μm. As such, a Zn erfc profile should then establish a working upper-limit “worst case” scenario for the situation under consideration here; and thus, the calculated final impurity
concentrations ($C_i$) given in Figure 6.10 will be higher than if they were calculated by a kick-out diffusion profile.

![Image of diffusion profile and SRH lifetime plots](image)

(a) Calculated diffusion profiles of Zn in Si for annealing times and temperatures as applied to samples A and B (C) described in Table 6.X. An arbitrary constant surface impurity concentration ($C_s$) was considered. The data points indicate the anticipated final surface impurity concentration ($C_f^*$) after performing the chemical etch for each sample from Table 2 ($i = A, B, C$). (b) Evolution of the Si Shockley-Read-Hall recombination lifetime as a function of the Zn concentration according to [Coletti’11]. The final concentration ($C_f^*$) calculated from $t_\mu$, and the initial concentration ($C_i^*$) expected to be in the order of 50 times higher than $C_f^*$ according to Figure 6.10a for Sample A, which showed the largest potential change in impurity concentration have been plotted to quantify the variation in terms minority carrier lifetime ($t_\mu$ vs $t_\pi$). According to this model, $t_\mu$ should be in the range of 1 $\mu$s; being significantly lower than the actual value (60 $\mu$s).

According to the calculated diffusion profiles in Figure 6.10, samples B and C, which underwent long, high-temperature anneals, yield post-etch near-surface impurity concentrations, $C_f^B$ and $C_f^C$, respectively, of about half the starting concentration. Since the impact of such a relatively small concentration change on the SRH recombination lifetime is also relatively small, as indicated by Figure 6.10b, the results from samples B and C are effectively inconclusive. That is, either the starting concentration was high enough to yield the observed degradation and the long, high-temperature anneals have resulted in a very deep penetration and thus relatively flat profile, or the extrinsic diffusion mechanism does not explain the results altogether. Regardless, neither can be concluded based on these samples alone. Sample A, on the other hand, which received a considerably shorter anneal, is much more telling. The calculated impurity concentration, $C_i^A$ (22.5 $\mu$m deep), is reduced by nearly 50× compared to the initial surface concentration (Figure 6.10a), which should induce an approximately equally large change in SRH lifetime [Coletti’11], as evidenced in Figure 6.10b, making sample A the more sensitive test case. However, the lack of change in measured lifetime between the pre- and post-etched measurements (i.e. $t_\mu = t_\pi$) indicates that there is no depth dependence, but rather suggests a
fully homogeneous distribution of lifetime-killing defects (i.e. $C_v = C_0$). Therefore, this result most likely eliminates the extrinsic diffused impurity mechanism as being the source of lifetime degradation.

Of course, it is worth noting that there are indeed even faster diffusing impurity species, such as Cu, Ni, and Fe [Bracht’00], that could potentially yield a sufficiently flat diffusion profile, even for the short anneal of sample A, such that the $\sim 20 \mu$m etch depth would not be expected to produce a significant change in lifetime. However, given the environment in the MOCVD reactor, such materials are extremely unlikely to be present in any significant or sufficient concentrations to impact lifetime. Testing for the characteristic injection-dependent lifetime fingerprint of Fe [Macdonald’04], the most likely species of any of these (given the presence of stainless steel in the construction of the MOCVD system), indicated that it was indeed not present. Moreover, it was also found that annealing the Fz-Si at 700°C for 60 min in UHV, which was equally absent of these elements (i.e. within an idle MBE chamber at $\sim 2 \times 10^{10}$ Torr chamber pressure), also resulted in a similar degradation of the minority carrier lifetime, to a value of 8 $\mu$s.

Taken together, these results strongly indicate against an in-diffused impurity mechanism as the cause of the observed lifetime degradation. Instead, the more likely mechanism is that the thermal treatments experienced by these samples are leading to the formation of either extrinsic or intrinsic defects [Susii’99]. Examples of extrinsic defects are the formation of complexes with low pre-existing concentrations of C (such as thermal donors) or extended defects (such as the well-known swirls); while point defects (e.g. in-diffused vacancies) are examples for intrinsic defects. In this sense, different works have been published reporting the formation of these defects and their deleterious effect on the minority carrier lifetime. As an example, the formation of oxide precipitates during thermal treatment is accompanied by the nucleation of extended lattice defects, which become recombination centers when attracting impurities present in the wafer bulk [Susii’99]. On the other hand, extended defects can be produced as a result of the mechanical stress during the thermal process. In this sense, Wang et al. [Wang’88] reported that the formation of swirl defects is conditioned by the cooling rate of the sample after being submitted to a high temperature annealing. In this respect, they stated that slow cooling rates ($\sim 1 ^\circ$C/sec) for a dislocation-free, swirl-free crystal is critical for obtaining high minority carrier lifetimes, avoiding the formation of lattice micro-defects related to fast cooling rates [Wang’88]. Moreover, the agglomeration of intrinsic defects might result in the formation of swirls, which can act as nucleation centers for oxygen precipitation, degrading the minority carrier lifetime [Susii’99]. In a different study, Usami et al. [Usami’77] reported a correlation
between lifetime degradation and formation of vacancies and V-O complex defects on swirls-containing crystals. On the contrary, lifetime degradation in swirls-free crystals was related to the formation of tiny defects, dispersed along the crystal, generated during the crystal growth as a result of the suppression of swirl defect generation [Usami’77]. In all cases, these defects act as recombination centers producing the lifetime degradation.

Separately, Graff and Pieper [Graff’80] explained the variation in lifetime observed at room temperature after specimens were quenched from high temperature by assuming reactions between impurities and intrinsic defects, or just as a result of intrinsic defects which acts as recombination centers. One example of this are vacancies, which become frozen-in during quenching and can react with residual impurities present on interstitial sites, yielding recombination centers. Moreover, vacancies can also act as recombination centers themselves [Graff’80].

Heating and cooling rates of no more than 1°C/sec were employed for this work, which should allow for sufficient thermal equilibrium and prevention of excessive defect freeze-in. However, unlike in conventional diffusion-based cell production, where optimized emitter and/or back surface field formation processes provide beneficial defect gettering, these epitaxial structures received no such treatment. Therefore, the degradation observed here would be anomalous mainly due to the fact that it is not being automatically mitigated by the cell formation process. Future epitaxial process development should be able to take this issue into account.

### 6.3.2 GaP Nucleation Layer and GaAsP Buffer Layer

Right after the growth of the homoepitaxial emitter, the epitaxial growth of the III-V structure takes place. To this end, after Si homoepitaxy, substrates were then quenched to 450 °C to start the next step in the process, namely, the growth of the GaP nucleation layer (Step 3.a in Table 6.XI). Atomic layer epitaxy technique was used to nucleate GaP. After a sufficient thickness (5-6 nm) of GaP is grown, the substrate temperature was increased to 550 °C and normal (i.e. non pulsed) epitaxial growth was carried out in order to complete the GaP epitaxial layer up to about 250 nm (Step 3.b in Table 6.XI). For this purpose, tertiarybutylphosphine (TBP) and triethylgallium (TEGa) were used as P and Ga sources, respectively. The fourth (and final), step of the process in this study is the growth of step-graded metamorphic GaAsP_{1-y} buffer layers at 725°C, terminating at a composition of GaAs_{0.8}P_{0.2}. For the present study, the total buffer thickness (including a thick terminal composition cap layer) was 3.2 μm with an aggressive grading rate of 1% misfit per μm and total growth time of 110 min. In this case, trimethylgallium
(TMGa) was the Ga source, while pure arsine (AsH₃) and phosphine (PH₃) were used as the group-V precursors. The impact of these steps, as sampled at the various stages, on the minority carrier lifetime was assessed. Results are summarized in Table 6.XI.

Table 6.XI  Average minority carrier lifetime for Fz Si wafers after III-V heteroepitaxy. All epitaxial material and some wafer surface material have been removed for measuring the bulk lifetime. An as-received Fz wafer was included for comparison.

<table>
<thead>
<tr>
<th>Phase</th>
<th>Treatment</th>
<th>Δn (cm⁻³)</th>
<th>τ (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Fz Si as-received</td>
<td>10¹⁵</td>
<td>432</td>
</tr>
<tr>
<td>2</td>
<td>Homoepitaxial emitter of ~90 nm</td>
<td>10¹⁴</td>
<td>1</td>
</tr>
<tr>
<td>3.a</td>
<td>Homoepitaxial emitter + 5-6 nm ALE GaP</td>
<td>10¹⁴</td>
<td>25</td>
</tr>
<tr>
<td>3.b</td>
<td>Homoepitaxial emitter + 250 nm GaP</td>
<td>10¹⁵</td>
<td>72</td>
</tr>
<tr>
<td>4</td>
<td>Homoepitaxial emitter + 250 nm GaP + 3.2 µm GaAsP</td>
<td>10¹⁵</td>
<td>467</td>
</tr>
</tbody>
</table>

The key result in Table 6.XI is that, while the Si homoepitaxy was found to yield a drastic lifetime reduction, it was found that the III-V epitaxy (Phases 3 and 4) does exactly the opposite, providing an equally drastic overall lifetime recovery. Nonetheless, the observed recovery process is less straightforward. After Phase 3.a, the GaP nucleation step, the lifetime increased by approximately an order of magnitude, to about 30 µs, despite the very short duration (2.5 min.), low-temperature (450 °C) GaP ALE process. Continued “bulk” GaP MOVPE growth for 30 min. at 550 °C (Phase 3.b) provides about another twofold improvement. The most substantial and remarkable Si lifetime recovery back to its as-received value or beyond, occurs in Phase 4, the long (110 min.), high-temperature (725 °C) GaAs₀.₆P₀.₄ buffer growth.

These results indicate that the MOVPE growth methodology used to create ideal GaAsP/Si solar cell structures from the viewpoint of structural defect reduction – specifically, the elimination of nucleation-related extended defects (APDs, stacking faults, twins) – has a substantial and dynamic impact on the minority carrier lifetime within the Si substrate. It is fortuitous that the sequential effects as a function of the four deposition phases outlined above return the Si lifetime to at least its starting value. Therefore, it is of utmost importance to fully understand the nature of both the degradation and recovery mechanisms, as well as to elucidate and predict the
impact on device performance as a result of growth conditions and methods, in order to better design future processes.

![Figure 6.11 Evolution of average Si bulk minority carrier lifetime (top row) during the production sequence of a III-V/Si hybrid MJSC at OSU; (bottom row) during the formation of the emitter by P diffusion at UPM.](image)

For the interpretation of this evolution, it is enlightening to compare this process (visually sketched in the top row of Figure 6.11) with the process followed to create the emitter of the Si subcell via diffusion in a MOVPE reactor (bottom row of Figure 6.11). Apart from the already commented degradation during Phase 2 of both approaches (homoepitaxial emitter growth and surface preparation annealing, respectively), a recovery of minority carrier lifetime in the Si wafer is measured in both cases in Phase 3; in one case associated to the growth of the GaP nucleation layer and in the other case associated to the P diffusion from PH₃. In both cases P-precurors are introduced in the reactor chamber, which suggests that the recovery is somehow linked to annealing/growth under P-based precursors, which in addition to P also provide significant quantities of atomic H, though it is noteworthy that the magnitude of the recovery for the epitaxial case is still an order of magnitude lower than that of the diffusion case. In this sense, it is worth mentioning that while the emitter formation (Phase 3 in bottom row) demonstrated significant levels of P in-diffusion due to the high (≥ 800°C) annealing temperatures, thereby likely offering some degree of defect gettering, no significant P diffusion is found for the lower temperature epitaxial GaP/Si case [Grassman’14]. Interestingly, a small
amount of group-V species was found to incorporate via background doping during the homoepitaxial Si growth, providing direct evidence that their presence alone is insufficient to yield lifetime recovery. Thus, during the GaP nucleation (Phase 3 in upper row), it is believed that the recombination center passivation occurs by means of atomic H, which would rapidly diffuse into the sample.

Additionally, the differing extents of recovery—approximately an order of magnitude through Phases 3.a and 3.b, and another order of magnitude through Phase 4—and its dependence upon the identities of precursor species, strengthen the role of atomic hydrogen on recovering lifetime. In this sense, Phases 3.a and 3.b utilized TEGa and TBP as the Ga and P precursors, respectively, which should provide some degree of available atomic H [Li’89], while Phase 4 utilized TMGa [Jacko’63] and PH_{3}/AsH_{3} [Stringfellow’89], which should provide substantially more, especially at the higher (725°C) growth temperature. Although the SiH_{4} should also be expected to yield some passivating atomic H during the homoepitaxial growth in Phase 2, the combination of process temperature (760°C) and pressure (150 mbar) actually favors the formation of H_{2} [Cavallotti’01]. Dissociation of H_{2} itself, without some catalyzing or reactive species, at those temperatures has been reported to be insignificant [Jones’99].

To further investigate the likelihood of an atomic H passivation mechanism, a final set of experiments were conducted, the results of which are presented in Table 6.XII. Here, 250 nm GaP-on-Si wafers were produced following Phases 2-3, as described previously, cleaved up into pieces, and subjected to a range of anneals (without growth) within the MOCVD reactor under different precursor ambient (PH_{3} and AsH_{3}) and temperatures (from 550 to 725 °C). In this sense, by increasing the annealing temperature, a more effective pyrolysis of the corresponding hydride is expected, and consequently higher doses of H will be available. The as-grown material (i.e. unannealed) is denoted as sample B. In this case, Si substrates used were high-quality Czochralski (Cz) wafers, with the same nominal doping and resistivity, as well as a similar as-received minority carrier lifetime (sample A), as the float-zone wafers used in the prior measurements. Note that the Phase 3 lifetime measured in sample B here is also similar to that seen for the Fz results shown in Table 6.XI.

The item of note is the result observed for Sample C, which received a 90 min. 725°C anneal in PH_{3}. This anneal was found to provide more than an order of magnitude increase in the lifetime, yielding a recovery back to (and even slightly higher than) the as-received value for the Cz substrate, similar to that seen with the Fz-Si after Phase 4 growth (see Figure 6.11). First, this sample, along with Samples A and B, suggest no impact of the wafer type (Cz versus Fz) on the lifetime degradation and the recovery mechanisms for this process. Second, and more
importantly, this result supports the conclusion of H-passivation as the source of lifetime recovery. As noted above, previous investigation of potential P diffusion into Si across the GaP/Si interface via annealing under these same conditions (725°C, PH₃/H₂ ambient, 120 min.) revealed to appreciable diffusion profile, as measured by SIMS [Grassman’14] leaving H-passivation as the only likely contender.

Table 6.XII Average minority carrier lifetime for Cz Si wafers after III-V heteroepitaxy. All epitaxial material and some wafer surface material have been removed for measuring the bulk lifetime. An as-received Cz wafer was included for comparison.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Temperature (°C)</th>
<th>Time (min.)</th>
<th>Precursor species</th>
<th>Δn (cm⁻³)</th>
<th>τ (μs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>10^{15}</td>
<td>444</td>
</tr>
<tr>
<td>B</td>
<td>550</td>
<td>30</td>
<td>H₂,TBP, TEGa</td>
<td>10^{14}</td>
<td>40</td>
</tr>
<tr>
<td>C</td>
<td>725</td>
<td>90</td>
<td>H₂, PH₃</td>
<td>10^{15}</td>
<td>475</td>
</tr>
<tr>
<td>D</td>
<td>650</td>
<td>90</td>
<td>H₂, PH₃</td>
<td>10^{15}</td>
<td>165</td>
</tr>
<tr>
<td>E</td>
<td>650</td>
<td>90</td>
<td>H₂, AsH₃</td>
<td>10^{15}</td>
<td>336</td>
</tr>
<tr>
<td>F</td>
<td>600</td>
<td>90</td>
<td>H₂, AsH₃</td>
<td>10^{15}</td>
<td>370</td>
</tr>
<tr>
<td>G</td>
<td>550</td>
<td>90</td>
<td>H₂, AsH₃</td>
<td>10^{15}</td>
<td>279</td>
</tr>
</tbody>
</table>

Consistent with the hypothesis of lifetime recovery due to atomic H passivation and reduced pyrolysis kinetics of the group-V hydrides at lower temperatures (thus yielding a lower dose of atomic H), is the fact that when decreasing the PH₃ annealing temperature from 725°C to 650°C (Sample D) the degree of lifetime recovery is also reduced, down to 165 μs, only about 4× greater than the initial (Sample B) value. Elucidation of whether this PH₃-based recovery is limited by a lack of available atomic H or the result of the lower temperature is not possible due to the limited range of PH₃ flows available in the MOCVD reactor used for this work. Therefore, to further examine this effect, an AsH₃ anneal under identical conditions, Sample E (650°C, 90 min.), was also performed. The AsH₃ anneal resulted in a ~8× increase in lifetime over the initial value, double which observed under PH₃ (Sample D). In fact, a similar degree of recovery was observed for AsH₃ based anneals all the way down to 550°C. At such lower temperatures the
likelihood of any group-V diffusion into the Si is effectively eliminated, further supporting the H-passivation mechanism.

The difference in magnitude of recovery observed for the two different species at 650°C is worth some examination. Since these anneals were completed at the same temperature, the difference suggests that the passivation is not limited by temperature but rather the availability of atomic H, which is likely related to the relative pyrolysis kinetics and/or thermodynamics of the two hydride species. That is, AsH₃ dissociates at the surface more readily than PH₅ [Stringfellow’89] due to its reduced molecular bond strength; AsH₃ (H₂As-H) has a significantly lower bond dissociation energy (for removal of the first H), 3.31 eV, versus that of PH₅ (H₂P-H), 3.64 eV [Luo’14-]. Based on a simple thermal Boltzmann analysis, this would suggest a difference in atomic H supply from the two hydride species of two to three orders of magnitude for the range of annealing temperatures examined here, reasonably consistent with the difference in lifetime recovery observed for the AsH₃ (Sample E) versus the PH₅ (Sample D) annealing at 650°C. This same analysis also suggests a strong temperature dependency for the supply of atomic H, and thus lifetime recovery, which would be consistent with the behavior observed for the PH₅ annealing at 725°C and 650°C. Of course, such a simplistic analysis ignores the more complex chemical realities in such a reactive system –for example, the detailed reaction pathways on the GaP and GaAs₉P₁₋ surfaces of interest (as opposed to mere thermal “cracking”) will strongly impact the actual reaction/dissociation kinetics— as evidenced by the relative lack of temperature dependence of the AsH₃ anneals (Samples E – G). It is also worth noting that a weak trend in the AsH₃ could exist, but is obscured by small errors in the lifetime measurement due to, for example, the quality of the quinhydrone surface passivation, although care was taken to ensure that all samples received identical preparation. Of note is the fact that the AsH₃ anneals were found to cause the GaP surface to roughen significantly, which was not observed for PH₅ or even pure H₂ annealing and is presumably due to As-P displacement. The roughening effect was also found to track with increasing annealing temperatures; 725°C AsH₃ annealing effectively resulted in the complete decomposition of the GaP film (thus its lack of inclusion here). As such, it may be possible that the excess strain in the GaP had some secondary impact on the underlying Si.

Finally, while H-passivation is effective for yielding a recovered lifetime, the question of longevity and stability deserves some attention. In this respect, although the passivation offered by atomic H has been reported to be indefinitely stable at lower temperatures [Pearson’91], it is important to highlight that if the H supply is interrupted and the temperature is still high enough to break the associated bonds, dehydrogenation can occur [Karzel’13], and lifetime will
be again degraded. Accordingly, post-growth device processing must be designed and carried out using a limited thermal budget in order to avoid the depassivation of the recombination center defects. It is fortuitous, then, that the typical thermal budget for III-V based device processing is generally low enough (≤ 450°C) to satisfy this requirement. Accordingly, the passivation of the atomic H is expected to remain stable during III-V/Si solar cell processing and application.

In summary, the evolution of the Si bulk lifetime during key phases in the fabrication of a III-V-on-Si epitaxial structure has been analyzed. A two order of magnitude reduction in bulk Si lifetime, followed by a complete recovery, was observed to result from the sequential growth of a Si homoepitaxial layer, GaP nucleation layer, GaP bulk growth and graded GaAsP in an all-MOCVD process that has been previously shown to achieve total elimination of nucleation-related extended defects in GaAsP/GaP/Si solar cell structures. A stepwise reduction and recovery mode was identified. Systematic etch experiments confirm this phenomenon to be a bulk and not a surface effect, since lifetime degradation has been observed to be independent of the wafer depth. Consequently, an extrinsic diffused impurity mechanism has been discarded as being the source of lifetime degradation. Accordingly, the primary source for degradation, which occurs during the Si epitaxy, is attributed to the formation of a homogeneous and deep distribution of crystalline defects, such as swirls, point defects or complexes with typical pre-existing atoms of C and/or O. On the other hand, partial recovery during GaP epitaxy appears to be consistent with limited H passivation upon exposure to TPB at 450-550 °C, but the presence of both AsH₃ and PH₃ at higher temperatures (which implies greater concentrations of atomic hydrogen) accelerate the passivation and lifetime recovery to the as-received value, suggesting that diffused atomic H is passivating the lifetime-killing defects. This mechanism is reinforced by the annealing of GaP/Si samples at different temperatures in the presence of AsH₃. From this study it was observed an increasing lifetime recovery with the annealing temperature, coinciding with a higher availability of atomic hydrogen from the cracking of the group-V precursor.

**6.4. MINORITY CARRIER LIFETIME IMPACT ON SOLAR CELL PERFORMANCE**

Along this chapter it has been demonstrated that the minority carrier lifetime, far from begin a constant material property, is highly modulated by the MOVPE environment. In this sense, important oscillations of this parameter have been observed during the different steps involved
on the development of III-V/Si metamorphic structure. Moreover, it has been reported that minority carrier lifetime of the bottom cell base will not only affect the PV behavior of the lower cell; but also might compromise the behavior of the whole device. Accordingly, it is important to quantify the impact of this parameter on solar cell performance for establishing a criterion to determine whether or not the solar cell performance will be limited by the bulk lifetime. In this respect, one might expect that the extremely low lifetimes reported after certain steps (e.g. the Si surface preparation, the homoepitaxial emitter growth, or the surface reconstruction after emitter formation) have deleterious consequences on the solar cell performance. Nevertheless, it is difficult to establish a bulk lifetime benchmark, below which the solar cell performance is compromised by this parameter; that is to say, to assess whether the lifetime values obtained after the different steps involved in the epitaxial growth of the structure are high enough to guarantee a high quality bottom cell PV performance.

With the purpose of quantitatively assessing how does the electrical performance of a bottom cell (working in a III-V/Si MJSC) vary with the reported minority carrier lifetime evolution, we have simulated its short circuit current density ($J_{sc}$), open circuit voltage ($V_{oc}$) and fill factor (FF) at 1 sun (AM1.5D) as a function of the Si bulk lifetime. On the Si bottom cell, the GaP nucleation and GaAs$_x$P$_{1-x}$ compositionally-graded buffer layers have been included. As we will focus on the bottom cell performance, the tunnel junction has not been simulated in this work and the top cell has been simplified to its optical equivalent: a 2.5 μm thick GaAs$_{0.7}$P$_{0.3}$ layer. The aim of simulating the complete multilayer structure is to account for the complex optical behavior of the nucleation, buffer and top-cell upper layers, rather than simply applying a cut-off wavelength to the spectrum.

**6.4.1 P-N JUNCTION OPTIMIZATION**

The impact of the MOVPE environment on the minority carrier lifetime during the formation and optimization of the Si bottom subcell have been analyzed in the first part of this chapter. It has been reported that the initially degraded minority carrier lifetime (as a result of the H$_2$ annealing aimed to prepare de surface) can be recovered during the exposure to a PH$_3$ atmosphere for the emitter formation. However, it has been revealed that the despite an additional H$_2$ annealing after PH$_3$ exposure is crucial for recovering the surface morphology (degraded during PH$_3$ exposure) and ensuring a smooth surface for subsequent III-V growth,

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14 Numerical simulations done by Dr. Diego Martín.
the minority carrier lifetime is degraded during this process just as occurred in the initial H₂ anneal.

To fully assess the role of this process (i.e. Si bottom cell formation) on the solar cell performance, we have simulated the PV behavior of different bottom cells working in a GaAsP/GaP/Si solar cell under 1 sun AM1.5D illumination. With this purpose, bottom cells formed following the routines described in Table 6.VIII were simulated. To do so, firstly it has been estimated the emitter depth and the doping for each sample (Table 6.XIII) following the simulation model described in Chapter 4. According to this model, an extra injection of defects is considered for samples 1 to 6 (as a result of the morphology degradation). Moreover, the group-V memory effect was considered for the two-step annealed samples. These simulations have been done assuming a 300 μm thick base with a doping level of Nₐ = 2x10¹⁵ cm⁻³. In order to achieve a better assessment of the minority carrier lifetime impact on the bottom cell PV performance, a moderately recombining GaP/Si interface –Interface recombination velocity (IRV)=10⁴ cm/s– and a BSF was assumed for these simulations.

Table 6.XIII Simulation of silicon subcell parameters for samples included in Table 6.VIII.

<table>
<thead>
<tr>
<th></th>
<th>6.1</th>
<th>6.2</th>
<th>6.3</th>
<th>6.4</th>
<th>6.5</th>
<th>6.6</th>
<th>6.7</th>
<th>6.8</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depth (nm)</td>
<td>88-</td>
<td>100-</td>
<td>95-</td>
<td>114-</td>
<td>122-</td>
<td>149-</td>
<td>44-</td>
<td>96-</td>
</tr>
<tr>
<td></td>
<td>93</td>
<td>107</td>
<td>100</td>
<td>133</td>
<td>126</td>
<td>155</td>
<td>47</td>
<td>103</td>
</tr>
<tr>
<td>Doping×10¹⁵(cm⁻³)</td>
<td>2.78</td>
<td>1.47</td>
<td>3.97</td>
<td>2.02</td>
<td>1.56</td>
<td>0.93</td>
<td>5.31</td>
<td>0.49</td>
</tr>
<tr>
<td>Lifetime (μs)</td>
<td>584</td>
<td>8</td>
<td>949</td>
<td>6</td>
<td>3</td>
<td>1</td>
<td>87</td>
<td>1</td>
</tr>
<tr>
<td>Jsc (mA/cm²)</td>
<td>13.9</td>
<td>12.0</td>
<td>13.9</td>
<td>11.7</td>
<td>11.0</td>
<td>9.8</td>
<td>13.6</td>
<td>9.8</td>
</tr>
<tr>
<td>Voc (V)</td>
<td>614</td>
<td>508</td>
<td>625</td>
<td>503</td>
<td>492</td>
<td>475</td>
<td>562</td>
<td>475</td>
</tr>
<tr>
<td>FF (%)</td>
<td>81.3</td>
<td>80.0</td>
<td>81.4</td>
<td>79.9</td>
<td>79.4</td>
<td>78.7</td>
<td>81.2</td>
<td>78.7</td>
</tr>
</tbody>
</table>

According to TCAD simulations, when moderate recombination velocities were considered (by adding a BSF and reducing the recombination velocity at the GaP/Si interface), the cell performance shifted to being bulk recombination limited, making the lifetime degradation discussed herein a key component for yielding high-performance cells.
Despite the reported benefits of the two-step process on the surface reconstruction after the emitter formation (Chapter 4), leading to the formation of emitters with optimum properties, the lifetime degradation observed after this combined process turns into a reduction of the PV quality of the solar cells, obtaining performance metrics significantly lower than the initial value (i.e. just after the P diffusion). Consequently, given the degradation observed after morphology recovery, the growth of the III-V part of the structure should be designed to provide sufficient hydrogen passivation to recover the lifetime.

6.4.2 III-V EPITAXIAL GROWTH

In the second part of this chapter it has been studied the evolution of the minority carrier lifetime during the epitaxial growth of the Si emitter and the subsequent III-V layers. The formation of the p-n junction by homoepitaxial growth has been found to produce a substantial degradation of the bulk lifetime. Then the growth of GaP slowly starts to recover the lifetime. Finally, the growth of the GaAs₅P₁₋₅ step-graded buffer totally recovers the minority carrier lifetime to a value similar to that of the as-received Fz wafer. With the aim of quantifying the effect of these processes on the bottom cell PV performance, and to evaluate whether the minority carrier lifetime evolution during the epitaxial growth process turns into PV gains or losses, we have calculated the short circuit current density, open circuit voltage and fill factor of a silicon subcell with a variable lifetime (taken from Table 6.XI) under 1 sun AM1.5D illumination in a GaAsP/GaP/Si structure. In this case, a Si epitaxially-grown emitter of 90 nm with a doping concentration of N_D=10¹⁸ cm⁻³ and a 300 μm-thick base were considered.

![Figure 6.12 False color maps for solar cell parameters as a function of base doping and minority carrier (electron) lifetime for the “lower-limit” scenario for the bottom subcell (i.e. no BSF and GaP/Si IRV of 10⁶ cm/s). (a) Short circuit current density (JSC); (b) Open circuit voltage (VOC); (c) Fill Factor (FF).](image)

For a better assessment of the minority carrier lifetime effect on the electrical parameters of the Si bottom cell, two possible scenarios were considered. Firstly, a “lower-limit” scenario was
simulated where surfaces with high interface recombination velocity – i.e. no BSF and a GaP/Si interface recombination velocity of 10⁷ cm/s – were considered. Contour plots for this simulation series are presented in Figure 6.12. Correspondingly, Table 6.XIV shows the evolution of Si bulk lifetime during the growth of the III-V structure and its simulated impact on the bottom cell performance for this scenario.

Table 6.XIV Bottom subcell electrical parameters for a base doping level of 2·10¹⁵ cm⁻³ and a variable bulk lifetime (taken from the second column), according to the simulations plotted in Figure 6.12.

<table>
<thead>
<tr>
<th>Step</th>
<th>(\tau_b) (μs)</th>
<th>(J_{SC}) (mA/cm²)</th>
<th>(V_{OC}) (mV)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.0</td>
<td>10.2</td>
<td>475</td>
<td>78.7</td>
</tr>
<tr>
<td>3.a</td>
<td>25</td>
<td>12.0</td>
<td>512</td>
<td>80.3</td>
</tr>
<tr>
<td>3.b</td>
<td>72</td>
<td>12.6</td>
<td>517</td>
<td>80.5</td>
</tr>
<tr>
<td>4</td>
<td>467</td>
<td>12.6</td>
<td>519</td>
<td>80.6</td>
</tr>
</tbody>
</table>

As expected, the results presented in Figure 6.12 and Table 6.XIV show that the degradation in bulk minority carrier lifetime that occurs during the growth of the homoepitaxial Si emitter causes a deleterious effect on all of the performance metrics of the Si bottom cell, being of particular relevance the very low \(V_{OC}\) and the \(J_{SC}\), which will limit the performance of the entire MJ device. These results are in good agreement with the ones reported in previous the subsection (i.e. surface reconstruction after the emitter formation by P diffusion). The partial recovery that takes place during the growth of the GaP nucleation layer improves the situation, which then stays virtually unchanged after the growth of the GaAsP buffer. This lack of significant improvement of \(J_{SC}\), \(V_{OC}\) and FF, despite the fact that minority carrier lifetime improves by a factor 8, is a direct result of the lack of efficient passivation of both the front and back Si surfaces. As evidenced by Figure 6.12, where all subplots have large areas of constant performance (i.e. uniform color) for lifetimes above ~20 μs and a wide range of base doping values, the design of a careful process to recover (or maintain) bulk lifetime to the level of as-received wafers does not necessarily pay back in the form of higher efficiencies if the surface/interface recombination velocities are too high.

Figure 6.13 presents simulated results from a more optimistic scenario. In this case, better surfaces were considered via the introduction of a full-area BSF (1 μm thick and doped at a
theoretically ideal $N_A = 10^{20}$ cm$^{-3}$) and reducing the GaP/Si IRV down to $10^6$ cm/s. For the purpose of comparison, the emitter doping and thickness are the same as in the previous simulations (Figure 6.13, Table 6.XV). Accordingly, Table 6.XV presents the performance metrics of the Si bottom cell for the same lifetime values under the optimistic scenario.

![Figure 6.13 False color maps for solar cell parameters as a function of base doping and minority carrier (electron) lifetime for an optimistic scenario for the bottom subcell (i.e. good BSF and GaP/Si IRV of 10$^6$ cm/s). (a) Short circuit current density; (b) Open circuit voltage; (c) Fill Factor.](image)

Table 6.XV Bottom subcell electrical parameters for a base doping level of 2·10$^5$ cm$^{-3}$, according to simulations plotted in Figure 6.13

<table>
<thead>
<tr>
<th>Step</th>
<th>$n_0$ ($\mu$s)</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>$V_{OC}$ (mV)</th>
<th>FF (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.0</td>
<td>10.19</td>
<td>475</td>
<td>78.75</td>
</tr>
<tr>
<td>3.a</td>
<td>25</td>
<td>13.02</td>
<td>531</td>
<td>80.68</td>
</tr>
<tr>
<td>3.b</td>
<td>72</td>
<td>13.94</td>
<td>558</td>
<td>81.13</td>
</tr>
<tr>
<td>4</td>
<td>467</td>
<td>14.27</td>
<td>610</td>
<td>81.19</td>
</tr>
</tbody>
</table>

Figure 6.13 and Table 6.XV show that moving to the new scenario not only implies a significant improvement of the electrical parameters (as a result of having lower recombination losses at the surfaces), but it also implies that $J_{SC}$ and $V_{OC}$ are no longer controlled by the recombination at the surfaces, but rather by the minority carrier lifetime in the Si bulk. Accordingly, unlike in the pessimistic scenario, any processes contributing to a larger recovery of such minority carrier lifetime would produce the corresponding increase in the PV parameters of the solar cells. As an example, Table 6.XV evidences that the increase of the bulk lifetime that is produced during the
growth of the GaAsP buffer layer in our samples (i.e. moving from 72 μs to 467 μs) is shown to have a deep impact on the bottom cell electrical performance, especially on its V_{OC}.

However, it is important to highlight that despite the evolution of bulk lifetime along the different phases involved in the growth of the III-V/Si structure has reported to deeply affect the performance metrics of the silicon bottom cell (Figure 6.13), the improvement of the J_{sc} with the minority carrier lifetime is only guaranteed until a certain point; that is to say, there is a lifetime value (100 μs approx.) beyond which an increase on lifetime does not pay back in an improvement of the short circuit current. Consequently, the increase of the lifetime beyond this point does not leave much room for improvement of the solar cell performance. In this sense, we can confirm that the minority carrier lifetimes obtained after the growth of the GaAsP graded buffers are sufficiently high for obtaining a high quality solar cell. Increasing this value will not have important repercussions on the solar cell PV behavior when having a moderate recombination velocity at the GaP/Si interface.

### 6.5. Summary and Conclusions

In this chapter, we have analyzed the impact of the MOVPE environment on the minority carrier lifetime during key steps in the production of a III-V on Si epitaxial structure. Particularly, the impact of two main processes has been analyzed: 1) the formation and optimization of the Si bottom subcell; and 2) the epitaxial growth of the III-V structure.

Initially, the evolution of the minority carrier lifetime during the formation of the Si bottom subcell has been assessed. This process consists of three different stages, which have been separately analyzed. Firstly, the surfaces deoxidation and their preparation for step-doubling have been reported to have detrimental effects on the PV properties of the bottom subcell. Although several mechanism were initially postulated for explaining this behavior, it was demonstrated that the lifetime degradation is neither a result of a defective cleaning process (prior to loading samples into the reactor); nor due to the effect of the carrier gas (i.e. H₂). On the contrary, it was suggested a mechanism based on the formation of recombination centers during the wafer annealing. These centers can either come from point defects and swirls, formed during the thermal treatment, and which can interact with initially present impurities; or they can be formed as a result of the introduction of extrinsic impurities from the MOVPE environment itself. Secondly, the formation of the emitter by P diffusion has been reported to bring back lifetime to initial values. During this step, high amounts of P and atomic hydrogen
will be present in the reactor as a result of phosphine pyrolysis. Accordingly, two possible mechanism were suggested for this lifetime recovery process: the gettering effect of P on extracting the impurities (as it happens in conventional Si technology); or the effect of atomic hydrogen on passivating recombination centers. Finally, the surface morphology recovery process drastically bring lifetimes down, turning into important PV loses. This observation suggest that the role of PH$_3$ in recovering lifetime is not related to a classic P diffusion-gettering process, since the lifetime recovery mechanism should not be reversible as long as the highly P-doped region remains on the surface (as it is this case, and still a significant lifetime drop is observed). On the contrary, the hypothesis of the atomic H acting as a passivating agent of recombination centers becomes the most likely explanation. In this sense, when PH$_3$ supply is interrupted and temperatures are still high enough, the passivation provided by the atomic hydrogen is lost and consequently, lifetime drops.

On the other hand, the evolution of the Si bulk lifetime during some key steps in the production of a III-V on Si epitaxial structure has been analyzed. In particular, the impact of multiple steps in the overall process have been studied: 1) the formation of the emitter by a different alternative (i.e. homoepitaxial Si emitter growth); 2) growth of the first layers of GaP; 3) growth of bulk GaP nucleation layer; and 4) growth of the GaAsP step-graded buffer. Firstly, a severe degradation of the Si bulk lifetime has been observed after p-n junction formation by homoepitaxial growth with silane. The growth of homoepitaxial Si emitter layers as thin as 20 nm has shown to degrade the minority carrier lifetime from the initial 445 μs down to around 6 μs. Thicker emitters (~90 nm) produce lifetimes at or below the detection limit of our PCD equipment (~1 μs). The subsequent growth of the GaP nucleation layer partially recovers the minority carrier lifetime. Finally, the growth of the GaAsP step-graded buffer layer yields full recovery of the minority carrier lifetime to a value virtually equal to that of the as-received Fz wafer. Accordingly, the minority carrier lifetime suffers a reversible degradation–recovery process during the epitaxial growth of the solar cell. On the one hand, it was suggested that the lifetime degradation (observed in Step 2) is related to the activation of recombination centers, in the same way that happens during the initial surface preparation. Although the origin of those recombination centers is still under investigation, it has been discarded that the mechanism governing the lifetime degradation is related to any phenomenon which implies the existence of a gradient between the surface and the wafer bulk (such as the formation of surface defects or the diffusion on impurities) since the lifetime degradation has been found to be independent to wafer depth and consequently, the introduction of an extrinsic impurity present in the MOVPE environment was discarded. The most likely explanation for this behavior is the formation of point defects or swirls during the annealing which eventually become recombination centers.
On the other hand, the lifetime recovery observed in subsequent phases is believed to be related to the passivation of those centers by means of atomic hydrogen, generated through the pyrolysis of precursor species during the growth of GaP and GaAsP, similarly to what happens during the emitter formation by P diffusion. This mechanism is reinforced by the annealing of GaP/Si samples at different temperatures in the presence of AsH₃. In this study an increased lifetime recovery with annealing temperature was observed, coinciding with a higher availability of H from the cracking of the group-V precursor.

In order to assess the importance of having a high minority carrier base lifetime in the overall photovoltaic performance of the associated Si bottom cell, TCAD simulations, as a function of the Si bulk lifetime, were performed. When high recombination velocities were considered at the cell surfaces (“lower-limit” scenario), the enhancement of the minority carrier lifetime beyond 20 μs provided no performance improvement, since the excessive surface recombination was the limiting factor. However, when moderate recombination velocities were considered (by adding a BSF and reducing the IRV at the GaP/Si interface), the cell performance shifted to being bulk recombination limited, making the lifetime recovery discussed herein a key component for yielding high-performance cells. Nonetheless, there is a critical lifetime value above which lifetime doesn’t pay back in a $J_{sc}$ increase. Accordingly, it was reported that the PV properties of the bottom cell after the growth of the GaAsP graded buffer are in the optimum range for guaranteeing a high-quality MJSC.

In summary, it was observed that minority carrier lifetime of the Si substrates evolves during the processes needed to manufacture a hybrid III-V/Si MJSC. Such evolution may imply processes with deleterious effects on the lifetime that, if not recovered, will have a detrimental impact on the Si bottom cell performance. Therefore, designing processes that promote the recovery of the lifetime during the growth of the III-V structure is a must to support the production of high-performance multijunction III-V/Si solar cells. However, if the minimization of recombination losses at Si interfaces is not addressed, any gain in minority carrier lifetime may not translate into any improvement of the solar cell performance.
7. **Summary & Future Work**

7.1. **Summary & Conclusions**

Dual-junction solar cells formed by a GaAsP or GaInP top cell and a Si bottom cell seem to be excellent candidates for the integration of III-V materials on Si substrates. The combination of these materials offers promising results based on: 1) the reduced costs resulting from the use of cheap substrates (i.e. Si) and, 2) due to the high theoretical efficiencies achievable with the use of MJSCs based on III-V semiconductors.

Within the many existing alternatives for the integration of III-V semiconductors on Si substrates, this thesis has been based on the metamorphic approach for the development of GaAsP/Si dual-junction solar cells. The idea is to offer a simple MOVPE routine, which can be easily transferred to PV industry in the near future. To this end, it is highly pursued that the whole process is carried out in a single MOVPE reactor, avoiding the use of different equipment, offering an economic and easy-to-implement technology.

In the last years, many groups have been focused on the development of GaAsP/Si metamorphic dual-junction solar cells, similar to the one here described. Despite the vast majority of the literature published in this field is focused on the upper layers of the structure (i.e. the growth of
a high quality nucleation layer and a graded buffer layer, minimizing the appearance of crystal defects), this thesis has focused on the optimization of the lower part of the structure, which indeed will be of important relevance in the global performance of the solar cell.

Accordingly, in this thesis we have tackled challenges associated to the Si bottom cell formation, related to the preparation of the Si substrates for epitaxial growth; the formation of an optimized emitter while preserving the silicon surface for subsequent growth; and finally, to the attainment of good photovoltaic properties in the bottom cell base during the MOVPE process. In addition to the optimization of the bottom cell, an extensive study concerning III-V on Si nucleation for developing a high quality GaP nucleation layer, which acts as the passivating layer of the silicon bottom cell and serves as the base for the subsequent III-V structure, has been presented in this thesis.

The preparation of Si (100) substrates has been found to be a key aspect for obtaining a high-quality surface where III-V semiconductors can be eventually integrated. In this thesis, we initially reviewed the preparation routine of silicon substrates required to obtain an oxide-free and single-domain structure, for favoring the growth of a high-quality III-V structure. Firstly, a chemical cleaning, aimed to get rid of any possible contaminants and to eliminate the native silicon oxide was performed on silicon substrates. As a result of this study, a HF-based cleaning procedure has been selected as the preferable method due to its effectiveness, simplicity and reduced cost. Secondly, a thermal treatment aimed to get rid of any residual traces of silicon oxide (if any) and favor the surface reconstruction of silicon substrates, to obtain a single-domain structure has been performed. According to literature, this step generally occurs at temperatures higher than 1000 °C, making its use unaffordable due to the impossibility of reaching such temperatures on our particular MOVPE system. In this thesis it has been presented a lower temperature (i.e. 800 °C) alternative to the conventional method for the silicon surface preparation (i.e. surface deoxidation and step doubling). After a proper chemical cleaning of silicon surfaces, the annealing of silicon substrates to temperatures up to 800-830 °C is sufficient to ensure a perfectly clean single-domain Si structure.

One of the first points to be addressed on the development of the bottom subcell is the formation of the p-n junction. This step not only implies the creation of the emitter itself, but also, to guarantee a high quality surface after its formation. In this respect, a wide study regarding the formation of the emitter by different alternatives was carried out. As a result of these studies, it has been found that shallow (<0.25 microns) and highly doped (>10¹⁹ cm⁻³) emitters are optimum designs for the emitter of the silicon sub-cell when working in a III-V/Si DJSC. Moreover, diffused emitters are potentially the best option since their electrical
performance has been found to be independent of the GaP/Si interface recombination velocity. Moreover, the simplicity of this technique, together with the possibility of being easily transferred to the industry make this approach the most attractive alternative for the emitter formation in our particular MOVPE reactor. However, the use of this alternative presents an important drawback: the roughening of Si surfaces as a result of the long PH$_3$ exposures at temperatures ranging from 800-875 °C which, if not controlled, will ruin the quality of subsequent epitaxial layers. Accordingly, a comprehensive study to determine, and quantify, the effect of the phosphine on the silicon surface morphology has been presented in this thesis. From this study, it has been described that the use of a combined treatment, consisting on a two-step anneal where samples are submitted to a high temperature anneal in hydrogen after the phosphine exposure, leads to obtain optimum emitter designs (thin and highly doped) and Si surfaces with a sub-nanometer roughness. Moreover, a P-in-Si diffusion model has been developed, accounting for the effect of the surface roughness on the diffusion process (i.e. extra injection of point defects) to offer a theoretical model capable of simulating the phosphorous diffusion and reproduce experimental profiles.

After the formation of the p-n junction and the subsequent reconstruction of the silicon surface, the next step in the development of the III-V/Si DJSC is the growth of the GaP nucleation layer. Different approaches have been reported in the literature to be successful for obtaining a high quality two-dimensional GaP nucleation layer, though contradictory visions concerning the growth parameters have been reported. The idea of this study is to offer a simply process for the III-V/Si integration so it can be easily transferred to the PV industry. In this sense, we have explored the diverse (even contradictory) alternatives reported in the literature, to offer a simple successful integration of GaP on silicon substrates in our particular MOVPE system.

Two general approaches have been initially considered: continuous growth-mode and pulsed growth-mode. In the light of the results we can conclude that not only a single technique is valid for a successful GaP/Si integration; since most of the explored approaches has been resulted to be interesting in some way. However, the best results have been reported for the continuous growth-mode approach. This can be related to the actual configuration of our MOVPE reactor and to the absence of precursors suitable for working at low temperatures (such as TBP), required for the pulsed growth-mode.

Moreover, different alternatives, regarding the precursors employed for the pre-exposure of Si wafers before nucleation, have been considered in this thesis. In this sense, the most interesting results have been achieved for samples which have been pre-exposed to a group-V precursor (i.e. PH$_3$ or AsH$_3$). Samples which have been initially exposed to PH$_3$ present a continuous layer
resulted from the total coalescence of multiple islands, covering uniformly the silicon surface but with a non-depreciable roughness. However, the structural quality of these samples is still poor, given the high number of crystal defects (mainly SFs) measured within the GaP nucleation layer. It is important to notice that the presence of these crystallographic defects could be linked to the MOVPE technology used in this thesis, which obviates the use of the Si homoeпитaxy step (normally used for burying any traces of C, O or other contaminants) for avoiding the use of two different reactors; with the aim of offering an easy routine for III-V on Si integration. On the other hand, samples which have been pre-exposed to AsH₃ have been found to be the ones exhibiting the best structural quality, since not a single dislocation, or SFs have been observed in those samples. In this case, GaP grow with a certain inclination (related to the miscut angle of the wafer) with respect to the Si crystal. Consequently, the resulting morphology is irregular, and thus need to be improved for further growth. In this sense, future work will be directed to optimize the nucleation routines with the aim of improving the structural and morphological quality of the nucleation layer so they can be used as templates for subsequent III-V integration.

Finally, the last (but not less important) point which has been treated in this thesis is the **PV behavior of the bottom cell base**. This is a key feature since the bottom cell base minority carrier parameters will determine the PV performance of the bottom sub-cell in a tandem stack and, to a lesser extent, might compromise the PV behavior of the entire device. It is well established that the minority carrier lifetime in conventional PV silicon processing is not a constant material property but depends strongly on the thermal history and the environment where the sample was processed. Accordingly, a strong influence of the MOVPE environment on this parameter has been reported. Results about minority carrier lifetime evolution in the MOVPE processing of silicon substrates for III/V-on-Si photovoltaics have been presented for the first time. Particularly, two general processes have been considered: the formation of the Si bottom subcell and the epitaxial growth of the III-V structure.

Initially, the evolution of the minority carrier lifetime during the formation of the Si bottom subcell suggests a step-wise mechanism. Firstly, the surfaces deoxidation and their preparation for step-doubling have been reported to have detrimental effects on the PV properties of the bottom subcell. A mechanism based on the formation of recombination centers during the wafer annealing was suggested. Secondly, the formation of the emitter by P diffusion has been reported to bring the lifetime back to initial values. During this step high amounts of P and atomic hydrogen are present in the reactor as a result of phosphine pyrolysis. Finally, the morphology recovery process (i.e. H₂ anneal after emitter formation) drastically brings lifetimes down again, turning into important PV loses. This observation suggests that the role of PH₃ in
recovering lifetime is not related to a classic P diffusion-gettering process, since this mechanism should not be reversible as long as the highly P-doped region remains on the surface.

Regarding the epitaxial growth process, a two order of magnitude reduction in p-type Si lifetime during Si homoepitaxy, followed by a complete recovery over the course of subsequent III-V heteroepitaxy, was observed. On the one hand, it was suggested that the lifetime is related to the activation of recombination centers, equal to what happen during Si surface preparation. Although the nature of those recombination centers is still under investigation, the most likely explanation for this behavior is the formation of point defects or swirls during the annealing which eventually becomes recombination centers. On the other hand, the step-wise lifetime recovery observed in subsequent phases is believed to be related to the passivation of those centers by means of atomic hydrogen, generated through the pyrolysis of precursor species during the growth of GaP and GaAsP, similarly to what happens during the emitter formation by P diffusion. In summary, it was observed that minority carrier lifetime of the Si substrates evolves during the processes needed to manufacture a hybrid III-V/Si MJSC. Such evolution may imply processes with deleterious effects on the lifetime that, if not recovered, will have a detrimental impact on the Si bottom cell performance.

### 7.2. Future Work

The intention of this thesis was not to manufacture a super-high efficiency solar cell but to lay the technological foundations that would enable the integration of high-efficiency photovoltaic devices (III-V multi-junction solar cells) on low cost substrates.

The work presented in this thesis has been mainly focused on the optimization of the bottom part of the structure, paying special attention to the Si bottom subcell for harnessing its full PV potential, whilst the complexity of the technology is kept low. Accordingly, the natural continuation of this work, will focus on the development of the upper layers of the structure, handling the problems associated with the material growth and crystallographic defect confinement for developing a high-quality III-V on Si structure. On the one hand, and based on the reported progress on the GaP nucleation studies, future activities will be directed towards the optimization of the nucleation routine, starting from the most successful approaches reported in this thesis, for obtaining a high quality GaP nucleation layer from the point of view of the morphology and the structural quality. On the other hand, it is expected to face the challenges associated to the growth of the GaAsP graded buffer layer to continue with the
development of the III-V structure. In this respect, and with the aim of working in parallel to the development of a high quality GaP nucleation layer, GaP or GaAs substrates will be used as templates to suppress the problems associated to the growth of a polar material on a non-polar substrate.

In addition to the development of the III-V on Si structure, future activities will be framed on a second research line, which aims to go a step further and moving from the actual conception of the III-V/Si structure (i.e. from the point of view of the material) to consider it as an electronic device. In this respect, virtually no attention has been paid in the literature to optimize the processing of III-V/Si devices. Typically, the few implementations of these devices reported so far have used processing strategies of III-V solar cells. However, in order develop highly efficient III-V/Si solar cells; the processing of the devices must be done in a way that the potential of the Si cell is fully exploited.

The development of an advanced design for the Si cell is, consequently, a must to ensure a high quality bottom cell. This advanced design implies to carry out a processing more aligned with conventional Si PV technology, which considers diverse alternatives for improving the bottom cell PV performance. As an example, the importance of incorporating a back surface field or more elaborated backside passivation strategies on the Si bottom cell –a key step in conventional Si technology– has been already demonstrated in Chapter 6. Aluminum BSF layers are typically formed by the annealing of the Al (back metal) at temperatures significantly higher than the Si-Al eutectic. As a result of the high temperatures required (800 °C approx.), the Al diffuses into the Si, forming a highly doped region (p+). The presence of this region has mainly two repercussions on the solar cell performance: on the one hand, it improves the quality of the semiconductor-metal contact, reducing the contact resistance; and on the other hand, as a result of the band bending formed by the highly doped region, an electric field directed towards the back contact is created, decreasing electron recombination at the back surface. As indicated, the effect of the BSF on the bottom cell performance parameters (J<sub>SC</sub>, V<sub>OC</sub> and FF) was previously assessed in Chapter 6, where the evolution of these parameters as a function of the silicon bulk lifetime was studied for a bottom cell structure with (Figure 6.13) and without a BSF layer (Figure 6.12). From that study it was observed that the presence of the BSF on the device not only yields a significant improvement of the electrical parameters (as a result of reduced recombination losses at the surfaces), but also releases J<sub>SC</sub> and V<sub>OC</sub> from being limited by the recombination at the surfaces, becoming instead limited by the minority carrier lifetime in the Si bulk (Table 6.XV). In this respect, unlike what happens in the more recombining structure
(Table 6.XIV), any processes contributing to a recovery of minority carrier lifetime would produce the corresponding increase in the PV performance of the Si bottom cell.

Moreover, Figure 7.1 [Martin'13] shows how the inclusion of the BSF layer greatly improves the minority carrier collection for the Si bottom cell, thus increasing IQE in all the wavelength range (due to the low absorption of the Si-cell emitter). The greater the BSF doping, the higher the electric field, keeping minority carriers away from high-recombining rear contact, especially for long wavelengths, which are absorbed closer to that rear contact. Accordingly, the presence of the BSF is highly recommended to ensure a high quality bottom cell performance.

![Image of IQE comparison](image)

**Figure 7.1 IQE comparison for a bottom cell without (red) and with BSF layer (blue, green) for different doping levels [Martin'13].**

Obtaining high efficiency III-V/Si MJSC needs the application of device manufacturing processes and architectures that exploit material potential to its limits. In these respect, and given the vast experience in manufacturing both Si and III-V solar cells, it could be argued that the best manufacturing process would be a conventional III-V processing for the front side and a conventional Si processing for the rear side of the III-V/Si MJSC. However, this solution is far for optimum since some common technological steps involved in conventional Si solar cell processing are not suitable since they might be harmful for some parts of the III-V structure. In particular, the key limitation of the process is the inadequacy to use high temperatures for long times once the epitaxial deposition of III-V materials has taken place on the Si substrate, since III-V buffer layers and tunnel junctions would be noticeably degraded if exposed to high thermal loads, and the minority carrier lifetime could be impacted as discussed in Chapter 6. This fact hampers the use of conventional well-established processes of the Si PV industry (Al-
BSF, thermal oxide passivation, fired contacts...) once the structures have the III-V epitaxy. Therefore, the development of a hybrid technology which guarantees a high quality structure and which is compatible with both families of materials (i.e. Si and III-V semiconductors) needs to be developed. In this sense, the focus should be put on the rear-processing of the Si subcell since the front processing of the III-V part –considering conventional III-V process steps– involves room- or low-temperature process which should have no impact on the bottom cell.

In this sense, the goal is to develop a hybrid technology which guarantees a high quality structure and which is compatible with both materials (i.e. Si and III-V semiconductors) in terms of chemical etchings, AR coating deposition and the electric contact formation. Such processes need to be optimized to get the most of the potential of the structure developed, considering the limitations associated to the coexistence of III-V and silicon materials in the structure. In this respect, this research line will be based on exploring different strategies for the III-V/Si solar cell processing, to obtain a high quality passivation of the rear silicon surface, which is key to reach high efficiency, without exposing the III-V part to high thermal loads. Accordingly, low temperature BSF/point contacts for the Si subcell will be pursued to emulate the back processing of conventional Si structures in a process compatible with the III-V part of the structure. Two different approaches are proposed to this end: a) formation of the BSF prior to the epitaxial process; b) rear surface processing after the epitaxial growth.

### 7.2.1 Pre-epitaxy processing of the rear surface

The point of this strategy is to avoid high thermal loads on the III-V part of the structure by carrying out some of the high temperature processes involved in the Si rear surface processing before the epitaxial growth. After, the rear passivated wafers have to be conditioned for epitaxy and loaded into the MOVPE reactor for III-V growth. The fact that the processing is realized before epitaxy takes place makes that the rear passivation to be performed must be compatible with the succeeding epi-ready treatment of the front silicon surface and must withstand the MOVPE process without significant degradation in passivation quality. Moreover, it might not affect the MOVPE process itself. This means that both in-diffusion of species participating in the MOVPE into the Si rear surface and out-diffusion of atoms from the Si rear side have to be avoided or minimized.

According to these requirements, the proposed process for this strategy is the one called "High temperature passivated emitter rear totally diffused" (HT-PERT). This process aims the formation of a full back surface BSF. Both aluminum and boron could be considered as
candidate materials. After the formation of the BSF the remains of Al/B should be etched and
the backside of the wafer should be encapsulated with SiN$_x$ to avoid in- and out-diffusion during
the MOCVD growth. The thermal load during the epitaxy will have to be accounted for in order
to optimize the BSF diffusion profile.

### 7.2.2 Post-epitaxy processing of the rear surface

In this approach, the processing of the structure is performed after the III-V epitaxy.
Accordingly the quest for low temperature alternatives is mandatory for preserving the quality
of the III-V layers. In this respect, three possibilities (schematically depicted in Figure 7.2) are
proposed for solar cell processing with regard to reduce the thermal budget:

- A first alternative is to implement a silicon bottom subcell using a low temperature
  passivated emitter and rear totally diffused structure (LT-PERT). This essentially
  represents what has been simulated in Figure 7.1. The formation of a full back surface BSF
  would be achieved using a fast firing processes at medium temperatures (<700°C) based
  on rapid thermal annealing (RTA). Candidate materials for this process include Al, Ga
  and In. Back side processing will be completed by forming the back contact using Al
  evaporation followed by a low temperature annealing or RTA (Figure 7.2.a).

- A second alternative is to implement a silicon bottom subcell using a low temperature
  passivated emitter and rear cell structure (LT-PERC). Here rear passivation is attained by
  the formation of an AlO$_x$/SiN$_x$ dielectric passivating stack, which is carried out using
  PECVD at temperatures below 350°C. Back side processing will be completed using Al
  evaporation followed by a laser process to form locally fired point contacts (Figure 7.2.b).

- A third approach aims to implement a silicon bottom subcell using a heterojunction with
  intrinsic thin layer structure (HIT). Here PECVD is again used to deposit a-Si:H
  passivating layers in a HIT-like rear processing. This step will be completed by forming
  the back contact using Al evaporation followed by a low temperature annealing or RTA
  (Figure 7.2.c).

Theoretical simulations have been carried out\textsuperscript{15} for analyzing which of the three described
structures will result in a better photovoltaic performance. In this respect, Figure 7.3 shows
Internal Quantum Efficiency (IQE) simulated for the standard (not passivated) structure,

\textsuperscript{15} Simulations done by Dr. Diego Martín
together with the three alternatives, using 2D numerical simulation with SILVACO ATLAS. It can be seen how the low-doped shallow BSF present at the LT-PERT shows a limited improvement in the cut-off region. LT-PERC and HIT-like schemes are much more efficient.

![Schematic of the suggested structures framed under the post-epitaxy processing](image)

**Figure 7.2** Schematic of the suggested structures framed under the post-epitaxy processing. a) LT-PERC structure where the back surface is fully covered by an Al-BSF; b) LT-PERC structure, with local contacts; and c) HIT-like structure.

![IQE comparison](image)

**Figure 7.3** IQE comparison of the standard Si-bottom structure and the three suggested rear-passivation schemes.

Moreover, the performance metrics (short circuit current, open circuit voltage and fill factor) for the three structures have been calculated for a solar cell performance at 1 sun under AM1.5D spectrum and compared to a standard solar cell structure (Table 7.1).
Table 7.1 Comparison of performance metrics for the three different structures under 1-sun AM1.5D illumination

<table>
<thead>
<tr>
<th>Alternative</th>
<th>$J_{SC}$ (mA/cm$^2$)</th>
<th>$V_{OC}$ (mV)</th>
<th>$FF$ (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard</td>
<td>12.3</td>
<td>522</td>
<td>80.8</td>
</tr>
<tr>
<td>LT-PERT</td>
<td>12.9</td>
<td>535</td>
<td>81.1</td>
</tr>
<tr>
<td>LT-PERC</td>
<td>14.6</td>
<td>557</td>
<td>80.5</td>
</tr>
<tr>
<td>HIT</td>
<td>14.9</td>
<td>628</td>
<td>79.6</td>
</tr>
</tbody>
</table>

Preliminary simulations show that the LT-PERC approach works better than the low-doped shallow BSF present at the LT-PERT. Further enhancement is attained with the HIT-like scheme: $J_{SC}$ near 15 mA/cm$^2$ and $V_{OC}$ as high as 628 mV are expected, as a result of the excellent passivating properties of this approach. Future work will be directed towards the experimental implementation and characterization of these structures to offer an advanced design for the processing of III-V/Si structures.
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