Multiphase Current Controlled Buck Converter with Energy Recycling Output Impedance Correction Circuit (OICC): Adaptive Voltage Positioning (AVP) and Dynamic Voltage Scaling (DVS) application

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Abstract—Modern microprocessors impose strict specifications on Voltage Regulating Modules (VRMs) with advanced features such as Dynamic Voltage Scaling (DVS) and Adaptive Voltage Positioning (AVP). In this study the Output Impedance Correction Circuit (OICC) concept is employed as an additional energy path in a Multiphase synchronous buck converter in a manner that, during the load steps transients, the output capacitor of 150 µF is virtually increased to 2.1 mF, thus improving the response under AVP operation. On the other hand, during the output voltage reference step, the OICC is inactive, facilitating DVS operation and reducing the current stress on the switches and the inductors. Furthermore, the proposed solution is compared with a reference converter with 2.1 mF output capacitor, for both AVP and DVS operations. The OICC is implemented as a Synchronous Buck Converter with Peak Current Mode Control (PCMC), having smaller penalty on the system efficiency comparing with Linear Regulator (LR) implementation.

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

In Voltage Regulation Module (VRM) applications, it is well known that the main driver in designing the output filter stage is the output impedance of the system due to the strict specifications imposed by the load [1], [2]. In addition, advance features, such as Dynamic Voltage Scaling (DVS) and Adaptive Voltage Positioning (AVP), impose opposite trends on the output capacitor design: for load steps, big capacitor is favorable, while for the output voltage reference step, smaller capacitor is favorable. Therefore, the ongoing research trend is directed to improve the dynamic response of the VRM while reducing the size of the output capacitor by means of either improving the controller [3]-[8], or by introducing an additional energy path to compensate the charge perturbation of the output capacitor [9]-[22].

The dynamic behavior of the system with a linear control (Voltage mode control, VMC, Peak Current Mode Control, PCMC,...) is limited by the converter switching frequency. The reduction of the output capacitor can be achieved by increasing the switching frequency of the converter, thus increasing the bandwidth of the system. The drawback of this approach is that the system efficiency is penalized due to increased switching losses and RMS currents. In order to achieve both the output capacitor reduction and high system efficiency, while satisfying strict dynamic specifications, a Multiphase converter system is adopted as a standard for VRM applications [3]. In order to ensure the current sharing among the phases, the multiphase converter is usually implemented with current mode control.

The second possibility to reduce the output capacitor is to introduce an additional energy path to compensate the charge unbalance of the output capacitor [9]-[22], consequently reducing the transient time and output voltage deviation. Doing so, during the steady-state operation the system has high efficiency because the main low-bandwidth converter is designed to operate at moderate switching frequency, whereas the dynamic behavior is determined by the high-bandwidth auxiliary energy path, during the load-step transients. The auxiliary energy path can be implemented as a resistive path ([9], [10]), as a Linear regulator, LR, ([11]-[13], [19], [20]), or as a switching converter ([14]-[18], [21], [22]). The first two implementations provide faster response, at the expense of increasing losses during the transient. On the other hand, the switching converter implementation presents lower bandwidth, limited by the auxiliary converter switching frequency, though it produces smaller losses compared to the two previous implementations.

The Output Impedance Correction Circuit (OICC) concept, employed in this study, has been presented in [19] and analyzed in detail in [20], while the concept is extended to multiphase solutions in [21] and analyzed in detail in [22]. This solution utilizes an additional energy path, provided by the OICC, so that the auxiliary current, injected/extracted through this path is controlled to have n-1 times higher value than the output capacitor current with appropriate directions. Doing so, the OICC creates an equivalent n times bigger virtual capacitor at the output, thus reducing the output impedance for AVP operation. On the other hand, for DVS operation, the OICC remains inactive, thus the output voltage step is performed with smaller, nominal capacitor. In order to measure the output
transient routine. At the same time, in order to maintain the transients, thus reducing the output impedance by the same factor. The system is composed of the Multiphase Buck converter, which can be dynamically modified, the OICC (green - power stage, purple - current measurement) behaving like a controlled current source CCS and the system control (red). The control block allows the OICC to inject/extract the current only in certain states of the transient routine. At the same time, in order to maintain the stability of the system, the control modifies the main converter regulator.

During the steady-state, the OICC is inactive; all the energy is transferred through the Multiphase buck converter and it is behaving like a voltage source, while the system control is sensing the output capacitor current in order to initialize the transient routine when a load step occurs. In this manner, by sensing the output capacitor current, the system reacts nearly instantaneously to any load perturbation, since the output capacitor current is the fastest variable in the system that detects this perturbation. When the load step occurs, the OICC is activated and the output impedance correction starts. The system controller, implemented as a state machine in Fig. 2, is triggered by the output capacitor current and the system changes to the Active state. In this state, the OICC is providing n-1 times more current than the output capacitor, thus reducing the amount of charge extracted/injected from/to the output capacitor. As a result, the voltage perturbation is smaller. On the other hand, when the output-voltage reference step occurs, the OICC is not activated and the DVS operation is performed with small capacitor.

III. AVP-PCMC MAIN BUCK CONVERTER REGULATOR IMPLEMENTATION: THE OICC IMPACT

In order to achieve AVP behavior, various strategies can be applied to design the main converter regulator [5]. In CMC controlled converter, the simplest implementation is that the regulator generates the inductor current reference proportionally to the output voltage error, creating specified output voltage drop. Doing so, the error is not canceled, leaving more room for the voltage deviation under the load steps. In the proposed solution, the converter behaves like hybrid system with two different control-to-output transfer functions, $v_{OUT}(s)/v_{ref}$ depending on the state of the system: Idle or Active state. In order to have desired behavior, the regulator needs to be implemented in that manner to achieve the same load-line resistance $R_L$ in both states. In following analysis this issue is addressed.

A. Stability analysis

The small signal behavior of the system can be modeled for both states as presented in Fig. 3. During the Idle state (Fig. 3a), the OICC is inactive and the output capacitor is the nominal, thus the transfer function from the inductor current reference, $i_{L_{Ref}}$ to the output voltage, $v_{OUT}$ is

$$G_{iL_{Ref}}v_{OUT} = \frac{v_{OUT}}{i_{L_{Ref}}} = N_{ph}Z_{Cont} = \frac{N_{ph}}{k_L} \frac{1}{sC_{OUT}}$$

where $N_{ph}$ is the number of the phases of the multiphase buck converter, $k_L$ is inductor current gain and $Z_{Cont}$ is the impedance of the output capacitor. On the other hand, during the Active state (Fig. 3b), the OICC is active and the OICC subsystem affects the converter transfer function. In order to ensure stability of the OICC subsystem, its open-loop gain needs to be limited and, assuming unity gain of the capacitor current estimator $k_C$ and $k_{CCS}$, it is

$$L_{OICC} = F(s) = \frac{v_{OUT}(s)}{v_{CCS}(s)} = \frac{n-1}{s}$$

where $n$ is the number of phases.
where $n$ is the multiplication factor and $f_{OICC}$ is the OICC corner frequency, a frequency up to which the OICC has constant gain $n-1$. The bandwidth of the OICC subsystem, $BW_{OICC}$, is $(n-1)f_{OICC}$. During the Active state, the impedance of the equivalent virtual output capacitor, $Z_{Cout}^{EQ}$, is defined by

$$Z_{Cout}^{EQ} = \frac{Z_{Cout}}{1 + \frac{s}{2\pi f_{OICC}}}$$

(3)

The OICC reduces the impedance of the output capacitor by factor $n$ in a frequency range below the OICC corner frequency and, since it needs to be bigger than the main converter bandwidth $BW$ [22], in the frequency range of interest, the converter model presented in Fig. 3b is valid. The converter transfer function during the Active state is

$$G_{Active}^{def_{out}} = \frac{\bar{v}_{OUT}}{\bar{v}_{ref}} = \frac{Np}{k_{ll}} Z_{Cout}^{EQ} = \frac{Np}{k_{ll}} \frac{1}{s^{1/n} C_{OUT}}$$

(4)

The closed loop output impedance is the system is affected by the open loop gain of the converter during both states defined by

$$L_{Idle} = R(s) G_{Idle}^{def_{out}}$$

$$L_{Active} = R(s) G_{Active}^{def_{out}}$$

(5)

where $R(s)$ and $R'(s)$ are regulators for Idle and Active state, respectively. Finally, the closed loop output impedance of the system is defined by

$$Z_{Idle}^{def_{OUT}} = \frac{Z_{Cout}}{1 + R(s) G_{Idle}^{def_{out}}}$$

$$Z_{Active}^{def_{OUT}} = \frac{Z_{Cout}^{EQ}}{1 + R'(s) G_{Active}^{def_{out}}}$$

(6)

In order to achieve AVP behavior, as seen in (6), the output impedance depends on the regulator design, so both regulators need to create the same load-line resistance, $R_{LL}$. Assuming that the open loop output impedance during the Idle state has higher value than $R_{LL}$, $Z_{Cout}^{jwBW} > R_{LL}$, while during the Active state has lower value $Z_{Cout}^{EQ} < R_{LL}$. The regulators are defined by

$$R(s) = \frac{k_{ll}}{Np R_{LL}} \left(1 + \frac{s}{z}\right)$$

and

$$R'(s) = \frac{k_{ll}}{Np R_{LL}} \left(1 + \frac{s}{p}\right)$$

(7)

where $z$ is a zero of the regulator transfer function and $p$ is a pole. Closing the control loop, (7) can be introduced into (6) and desired low frequency output impedance is achieved:

$$Z_{Idle}^{def_{OUT}} = \frac{R_{LL} \left(1 + \frac{s}{p}\right)}{1 + \frac{s}{z}}$$

$$Z_{Active}^{def_{OUT}} = \frac{R_{LL} \left(1 + \frac{s}{z}\right)}{1 + \frac{s}{p}}$$

(8)

The amplitude characteristics of the output capacitor and closed loop output impedance are presented in Fig. 4 (Idle state: blue, Active state: red), while the output voltage time response of the closed loop system is presented in Fig. 5. It can be seen from Fig. 4a) that the closed loop output impedance $Z_{OUT}$ has bigger value at the bandwidth frequency $BW$, causing an undershoot of the output voltage as presented in Fig. 5 (blue). The bandwidth frequency $BW$ is limited due to the switching frequency or large signal stability constraints. On the other hand, during the Active state (Fig. 4b), the output impedance $Z_{OUT}^{def_{Idle}}$ is defined by a first order transfer function with a dominant pole at the new bandwidth $BW'$. The bandwidth $BW'$ is defined by $1/(2\pi R_{LL} \cdot C_{OUT})$. The time-domain output voltage response has an exponential transition to a new value as shown in Fig. 5 (red). Furthermore, in Fig. 4 normalized amplitude characteristics of both regulators, $R(s)$ and $R'(s)$, are presented. It can be seen that, below the bandwidth frequency, the output impedance is defined by inverse the regulator transfer function, while above the bandwidth, it is defined by the output capacitor impedance: physical capacitor during Idle state and virtual capacitor during Active state.

For the presented case, the open-loop gain characteristics for both states are presented in Fig. 6. During Idle state (blue), the bandwidth of the system is nominal, $BW$, while the phase margin PM is 80°. Desired phase margin is achieved by positioning the pole and zero, $p$ and $z$, of the regulator transfer function $R(s)$, having in mind that the zero should be as higher as possible since it becomes pole in closed loop output impedance during the Idle state (8) and it affects the time domain response [24].

On the other hand, the open-loop gain, shown in Fig. 6 (red), is defined as a first order system in the frequency range below the OICC corner frequency, $f_{OICC}$. Therefore, the bandwidth of the main converter $BW'$ is defined by the load-line resistance and the capacitance of the virtual capacitor and it is $1/(2\pi R_{LL} \cdot C_{OUT})$. Further, since it is a first order system, the phase margin is 90° if the OICC corner frequency is sufficiently high. Fig. 6 shows the impact on the open-loop
The AVP operation of the converter system is defined by the regulator implementation, as presented above. Since the converter transfer function is different during Idle and Active states, in order to maintain the same open-loop characteristic, the regulator needs to be modified as defined by (7). Possible analog implementation is presented in Fig. 7a).

The regulator is implemented as inverting amplifier, with an additional analog multiplexer (AMux) and a switch (Sw). Both additional components are controlled by the system controller (red in Fig. 1). During Idle state, the control signal Modify is low, thus the analog multiplexer is in position 0 and the switch is open. Doing so, series impedance of the resistor $R_s$ and the capacitor $C_s$ is connected in to the feedback branch of the amplifier as presented in Fig. 7b). The regulator transfer function is

$$R(s) = \frac{R_s}{R_0} \frac{1 + sC_sR_s}{1 + sC_s(R_s + R_i)}$$  \hspace{1cm} (9)$$

Comparing both regulator transfer functions given by (7) and (9), regulator components can be calculated from

$$\frac{k_{ll}}{N_{ph}R_{LL}} = \frac{R_i}{R_0}, \quad z = \frac{1}{C_sR_s}, \quad p = \frac{1}{C_s(R_s + R_i)}$$  \hspace{1cm} (10)$$

On the other hand, during Active state, Modify signal is high, connecting the analog multiplexer to position 1 and closing the switch, thus configuring the amplifier as presented in Fig. 7c). As it can be seen, the feedback branch is composed only of the resistor $R_i$, defining the regulator transfer function as

$$R'(s) = \frac{R_i}{R_0}$$  \hspace{1cm} (11)$$

Once again, comparing both regulator transfer functions given by (7) and (11) and the component relations given in (10), it can be seen that needed regulator is achieved.
Moreover, by configuring the AMux to position 1 and closing the switch Sw, the capacitor $C_S$ is connected to two ideal voltage sources, $V_{REF}$ and the output of the operational amplifier, $V_{op}$, achieving that its dynamic does not influence the system and that its voltage is equal to the voltage of the feedback resistor $R_S$. Doing so, upon reconnecting the $R_SC_S$ branch in to the feedback of the amplifier (going back to Idle state), the capacitor $C_S$ is charged to correct voltage and the current of the $R_SC_S$ branch is equal to zero. If this would not be the case, the $R_SC_S$ branch current would affect $R_1$ current as step deviation since the current trough $R_0$ is constant and defined by the difference between the reference $V_{REF}$ and the output voltage $V_{OUT}$. The step deviation of $R_1$ current would create a step of the main converter inductor current reference and the system would enter into a settling transient.

IV. SYNCHRONOUS PCMC BUCK OICC IMPLEMENTATION

The OICC implementation is presented in Fig. 8. The OICC subsystem is composed of non-invasive current estimator (purple) implemented as a simple transimpedance amplifier with the difference that, instead of using the OICC, it has 15 MOSFETs and designed to have load-line resistance of 10 $\Omega$ and the same main converter power stage with a difference in the output capacitor implementation. The first prototype, Low_C OUT, has the output capacitor of 140 $\mu$F and it utilizes the OICC in order to improve the dynamic behavior. The OICC has been implemented as a Synchronous Buck converter with PCMC which has multiplication factor of 15 and the OICC corner frequency $f_{OICC}$ at 50 kHz and the bandwidth $BW_{OICC}$ a 700 kHz.

V. EXPERIMENTAL RESULTS

In order to demonstrate and compare the dynamic behavior of proposed OICC system and a traditional design, two prototypes, Low_C OUT and High_C OUT, have been designed and built with the specifications given in TABLE I. Both prototypes are design to have load-line resistance of 10 $\Omega$ and the same main converter power stage with a difference in the output capacitor implementation. The first prototype, Low_C OUT, has the output capacitor of 140 $\mu$F and it utilizes the OICC in order to improve the dynamic behavior.

$V_{IN}$

$V_{OUT}$

$R_L$

$V_{ref}$ per Phase

$BW_{main}$

I. per Phase

$C_OU T$

MOSFETs

Driver

Low_C OUT Pr.

High_C OUT Pr.

$V_{IN}$

5 V

5 V

$V_{OUT}$

1.5 V

1.5 V

$R_L$

10 m$\Omega$

10 m$\Omega$

$V_{ref}$ per Phase

150 kHz

150 kHz

$BW_{main}$

8 kHz

8 kHz

I. per Phase

2 $\mu$H

2 $\mu$H

$C_OU T$

Ceramic: 3 x 47 $\mu$F

OSCON: 2 x 560 $\mu$F

MOSFETs

SI4866HDY

FDMS7620S

Driver

ISL6605

ISL6605

In order to demonstrate and compare the dynamic behavior of proposed OICC system and a traditional design, two prototypes, Low_C OUT and High_C OUT, have been designed and built with the specifications given in TABLE I. The results of the experiments for Low_C OUT Prototype are presented in Fig. 9 with the OICC and in Fig. 10 without the OICC. In Fig. 9 can be seen that when the load step ($i_{OUT}$, green) is detected, the OICC is activated and it starts to inject the auxiliary current $i_{aux}$, pink) to reduce the output voltage deviation ($V_{OUT}$, blue). The output voltage has smooth transition from 1.5 V (no load value) to 1.42 V (reduced by 80 mV = $R_0$ $\Delta i_{aux}$). Also, in the output voltage, it can be seen high switching frequency ripple generated by the OICC. The whole transient lasts 50 $\mu$s. On the other hand, the Low_C OUT Prototype behavior without the OICC is presented in Fig. 10, where it is shown that the output voltage has an undershoot of 380 mV while the transient lasts 160 $\mu$s, although the system have the similar bandwidth during both...
Idle and Active states. The long transient is caused by the additional dynamic in the regulator, or more precise, the zero $z$ of the regulator transfer function $R(s)$ defined by (7). The regulator zero, upon closing the control loop, becomes dominant pole in the output impedance during Idle state and it defines the length of the transient [24]. In Fig. 10, the currents of both phases are presented ($i_L^1$, yellow and $i_L^2$, pink) and it can be seen that the current sharing is achieved. The results of the experiments for High_COUT Prototype are presented in Fig. 11 where it is shown that the output voltage $v_{OUT}$ (blue) has the same dynamic behavior as in the case of the Low_COUT Prototype with the OICC presented in Fig. 9: the voltage has a smooth transition from 1.5 V to 1.42 V, while the transient lasts 50 $\mu$s. Comparing Fig. 9 and Fig. 11, it can be concluded that the OICC concept achieves to create virtual capacitor of 2.1 mF as the one used in High_COUT Prototype.

Both prototypes have been tested for DVS operation by tracking the output voltage reference step from 1.1 V to 1.5 V and the results are presented in Fig. 12 for Low_COUT Prototype without the OICC and Fig. 13 for High_COUT Prototype. In the case of Low_COUT Prototype, the OICC is intentionally not activated since the perturbation comes from the controller and the converter operates with small output capacitor (150 $\mu$F) needing small amount of charge to change the output voltage. In Fig. 12 it can be seen that the peak of the inductor currents is increased by only 2 A. In the case of High_COUT Prototype, the output capacitor is 2.1 mF, thus the peak of the inductor currents is increased by 24 A for the same reference step. This imposes additional stress to the switches and the design criteria needs to consider the peak of the current defined by the full load current (10 A per phase) plus the increase of the peak value to perform maximal reference step (24 A per phase for High_COUT Prototype or 2 A for Low_COUT Prototype). Furthermore, additional losses are generated due to the increased RSM currents.

In order to quantify the impact of the output capacitor on the efficiency during the DVS operation, two prototypes have been compared in terms of static and dynamic power losses. Fig. 14 presents generated power losses in steady-state operation of the two prototypes. Fig. 14a) shows power losses dependence on the output voltage variation under no load conditions (Low_COUT: blue, circles; High_COUT: red, squares) and with 10 A output current (Low_COUT: green, diamonds; High_COUT: pink, triangles), while Fig. 14b) shows losses dependence on the output current with 1.5 V output voltage (Low_COUT: blue, circles; High_COUT: red, squares). As it can be seen, both prototypes have the same behavior under light load conditions, generating 537 mW of power losses with 0 A load current and 1.5 V output voltage. As the output current increases (Fig. 14b), the power losses dependency curves starts to separate due to the slight difference of the power path resistance. At the load current of 10 A Low_COUT Prototype generates 2.843 W of losses, while High_COUT Prototype generates 2.738 W of losses, having the losses difference of 105 mW, which is a difference of 0.7% of the converter efficiency. On the other hand, varying the output voltage in the range from 1.1 V to 1.5 V, the power losses have small increment since the load current is the same in all considered cases; for Low_COUT Prototype the increment of the losses at 0 A load current is
with 1.1V and 1.5V output voltages, presented in Fig. 14a), the losses corresponds to the average value of the static losses bandwidth of the main converter. Fig. 15a) shows generated performed periodically creating the output voltage reference $V_{\text{ref}}$ measured and presented in Fig. 15. The experiments have been Prototype the increment of the losses at OA load current is seen that, at low frequency, both systems are generating similar power losses comparison. Further, the dynamic characteristics as a function of the frequency of the output voltage reference steps have been measured and presented in Fig. 15. The experiments have been performed periodically creating the output voltage reference steps from 1.1V to 1.5V and back to 1.1V with the duty cycle of 50%, while the frequency of the reference has been swept from 100 Hz up to 25 kHz. The upper limit is imposed by the bandwidth of the main converter. Fig. 15a) shows generated average losses of the converter, calculated as the difference of average total input power and average output power. It can be seen that, at low frequency, both systems are generating similar losses under the same conditions: 493 mW with 0A output current and 2.688 W with 10 A output current. These values of the losses corresponds to the average value of the static losses with 1.1V and 1.5V output voltages, presented in Fig. 14a), since the transient is negligible compared to the period. As the frequency increases, the transient becomes comparable to the period of the reference steps, resulting that the losses for High_COUT Prototype have peak of 7.65W and 15.4W for 0A and 10A output current, respectively, while in the case of Low_COUT Prototype the peaks are 320 mW for both cases. These big differences in the losses are caused by higher RMS currents of the High_COUT Prototype. Fig. 15b) presents the
difference of the losses of both prototypes under the same conditions, showing that the peak of added losses are 6.92W for 0A output current and 12.45 W for 10 A output current.

VI. CONCLUSIONS

In this study the Output Impedance Correction Circuit (OICC) concept is extended to AVP Multiphase Current Controlled Buck converter with PCMC and compared with a system which has n times bigger output capacitor. Two 2-phase Buck converter systems with PCMC have been designed, one with the OICC system, which has multiplication factor 15 and another with 15 times bigger capacitor. Both systems exhibit the same dynamic behavior under the resistive load steps of 8 A, thus implying that the reduction of the output capacitor by factor 15 can be applied (from 2.1 mF to 140 mF). The output capacitor increase is achieved by injecting auxiliary current at the output node which is proportional to the estimated capacitor current, obtained by using a simple and easily feasible transimpedance amplifier.

Furthermore, both prototypes have been tested for DVS operation, demonstrating that the OICC approach facilitates the implementation since the switches and the inductors operate with smaller RMS currents. This is achieved by not activating the OICC subsystem during the DVS transient, thus operating with smaller output capacitor. As demonstrated in experiments, an increase of the peak value of the inductor current is 2 A per phase for the OICC design, while for the converter with 2.1 mF, the increase of the peak value is 24 A per phase. Due to the lower RMS currents generated during DVS operation, the OICC concept also improves the efficiency of the system. It has been demonstrated that the increment of the losses, due to the big capacitor employment, goes as high as 6.92W for 0A output current and 12.45 W for 10 A output current.

REFERENCES