DC/DC CONVERTER FOR AIRCRAFT APPLICATIONS: DESIGN SPACE FOR INTERLEAVED TRIANGULAR FULL BRIDGE TOPOLOGY

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July 2016
I dedicate this work to my family. They have always supported me in whatever I do.

“Nunca dejes de creer”
I very much appreciate the assistance provided by my cotutor Yann Bouvier and my tutor Pedro Alou. Their help has been crucial for realizing this project.
SUMMARY
**SUMMARY**

The goal of this project is the analysis and design of a DC/DC converter for aircraft applications. This converter is part of the output of an isolated rectifier unit for the distribution of electric power inside the airplane.

This work is part of the research effort done by the Center of Industrial Electronics in Universidad Politécnica de Madrid (CEI-UPM), in the More Electric Aircraft (MEA) topic.

The system works as a rectifier of the current obtained at the turbines, the generator of the plane. A three-phased current flows to a device for eliminating the electronic interference (EMI). Then, a buck rectifier reduces the current, and finally a DC/DC converter adjusts its input voltage to the voltage at the load.

The objective of this project is designing an efficient and lightweight DC/DC converter in order to reduce fuel consumption on the plane. Its input voltage come from the rectifier. Output voltage is 28V as it is nowadays integrated in most planes. It is formed by active elements (switches and control) and by passive elements (transformer and bridge):

The specifications of the DC/DC converter are gathered together in the following table:

<table>
<thead>
<tr>
<th>Specification</th>
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</tr>
</thead>
<tbody>
<tr>
<td>Rated output power</td>
<td>$P_{\text{rated}}$</td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{\text{in}}$</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{\text{out}}$</td>
</tr>
<tr>
<td>Temperature range</td>
<td>$T$</td>
</tr>
<tr>
<td></td>
<td>-55ºC to +85ºC</td>
</tr>
</tbody>
</table>

The topology chosen is full-bridge as isolation is needed and transformer is simpler than in half-bridges. Inside full-bridge, there are different possibilities: phase shifted, dual active bridge, resonant dual active bridge and triangular full bridge.

The Triangular Full-Bridge is the chosen topology because the soft switches on both bridges at the primary and the secondary, and it only needs one magnetizing component, which gives the leakage needed for obtaining the triangular wave form. Due to the high ripple on this current, high capacitance is needed at the output. This capacitance can cover a big volume, being a disadvantage for this topology.

It is mandatory to avoid Continuous Current Mode (CCM) and always operate with Discontinuous Current Mode (DCM), as behavior control of the converter...
changes and less hard-switchings are required. **ZCS** is achieved on most switches and less losses and noise on output are produced.

Anyway, there are some disadvantages that must be considered:

- **High number of transistors**: The main disadvantage of a full-bridge topology is that it needs minimum eight transistors. Because of this the total voltage drop in transistors duplicates of that in case of center-tap rectifiers, if both sides of the transformer are connected as rectifiers. Losses are increased and conversion efficiency is somewhat reduced.

- **High RMS currents**: The RMS current is the equivalent steady DC value which gives the same effect and therefore the same losses on transformer and transistors, as they have internal resistances.

Another disadvantage of high RMS current is high ripple, that leads to high capacitance on the output. With interleaving ripples can be compensated and capacitance can be smaller.

There are three different states per cycle on current waveform. The Dead state allows to have ZCS.

Different types of power semiconductor switches are designed for functioning in diverse conditions. Voltage, current and switching frequency of the application are the parameters that need to be considered for electing the right switch.

Increasing frequency allows the transformer to be smaller. As converter's layout depends on the size of the transformer and specifications establish that it is needed a high power density. Therefore, a high frequency is obligatory.

MOSFET is the technology that best fits these exigencies. Some IGBTs are also good solutions. There are different kinds of MOSFETs depending on their material: Silicon MOSFETs are the traditionally used; Silicon Carbide MOSFETs are good for preforming with high voltages and high power, Gallium Nitride MOSFETs are excellent for high frequencies.
Interleaving consists in producing a multiphase current thanks to various converters connected in parallel. There are as many phases as converters. The main advantage is that every converter handles less power so current peaks are lower.

In this application, interleaving helps to take advantage of the leakage inductance of the transformer. With a single converter, for most turn ratios it is mandatory to add another external inductance to the circuit. This is a big disadvantage as it would force to operate with specifications that would not produce the less losses possible, or to place an external inductance that would drop power density.

In order to evaluate the efficiency of this converter, a proper calculation of losses in the devices as well as in the transformer is required. As it was explained before, the design and optimization of the transformer is out of the aim of this work so it will not be calculated. However, the optimized design is going to take into account some of the restrictions on the transformer design and the integration of the magnetizing components needed to achieve a good power density.

The parameters regarded for the design space are:

- Frequency
- Inductance
- Turns ratio of the transformer.
- Number of devices in parallel (Primary and secondary)
- Diodes or MOSFET in secondary
- Number of Parallel converters
- Stability
- Maximum current on devices

Primary bridge MOSFETs operate with 400V, therefore the best materials are Silicon and Silicon Carbide. It is possible to discriminate two types of MOSFET side:

- High side has switching, conduction and reverse recovery losses. Consequently, the number of MOSFET in parallel per side and the MOSFET employed are determined by the configuration that reaches the lower losses.
- Low side only has conduction losses. For that reason, the MOSFET chosen is the one with less $R_{DS}$ at temperature of operation. Also a high number of MOSFET per side is desired.

Secondary bridge performs with 28V, for that reason GaN MOSFETs and diodes can be taken into account as alternatives to Silicon and Silicon Carbide MOSFETs. Secondary side mainly has conduction losses. Therefore, the same configuration selection as in low MOSFETs in primary is applicable.
An important fact to take into account is that devices have to be able to endure the current that flows through them without breaking.

With low frequencies, the time demanded for reaching the current peak that delivers on output the correct power is bigger than in high frequencies. Consequently, slope is smaller and inductance bigger in low frequencies than in high frequencies.

But with more converters, different turn ratios produce different waveforms at the output, and consequently ripple changes as well. Ripple drops and capacitance thus is not forced to be that big. Its size changes with turn ratio as well. However, there are some turn ratios where adding more converters ripple increases.

Losses in transformer are reduced by ZVS. But, in order to achieve zero voltage, some magnetizing current is required. As a consequence, on dead state there is no zero current and ZCS on MOSFETs is not achieved. Therefore, switching losses increase in configurations where high magnetizing current is needed.
There are three possible configurations for the multiphase converter:

<table>
<thead>
<tr>
<th>FIRST CONFIGURATION</th>
<th>FREQ (kHz)</th>
<th>TURN RATIO</th>
<th>PAR-CONV</th>
<th>Nº CAP</th>
<th>MAG. CUR.*</th>
<th>EFFICIENCY</th>
<th>LOSSES (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>5:1</td>
<td>6</td>
<td>1</td>
<td>1.4A</td>
<td>0.971</td>
<td>305</td>
<td></td>
</tr>
</tbody>
</table>

Table 2 First configuration.

<table>
<thead>
<tr>
<th>SECOND CONFIGURATION</th>
<th>FREQ (kHz)</th>
<th>TURN RATIO</th>
<th>PAR-CONV</th>
<th>Nº CAP</th>
<th>MAG. CUR.*</th>
<th>EFFICIENCY</th>
<th>LOSSES (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100</td>
<td>7:1</td>
<td>4</td>
<td>1</td>
<td>1A</td>
<td>0.976</td>
<td>240</td>
<td></td>
</tr>
</tbody>
</table>

Table 3 Second configuration.

<table>
<thead>
<tr>
<th>THIRD CONFIGURATION</th>
<th>FREQ (kHz)</th>
<th>TURN RATIO</th>
<th>PAR-CONV</th>
<th>Nº CAP</th>
<th>MAG. CUR.*</th>
<th>EFFICIENCY</th>
<th>LOSSES (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>200</td>
<td>8:1</td>
<td>6</td>
<td>1</td>
<td>1.7A</td>
<td>0.971</td>
<td>295</td>
<td></td>
</tr>
</tbody>
</table>

Table 4 Third configuration.

*Minimum needed

It is not possible to determine which is the best solution. Future research lines on the transformer will allow to choose the configuration with lower volume, weight and losses.

**KEY WORDS**

- CONVERTER
- TRIANGULAR FULL-BRIDGE
- TRANSFORMER
- MOSFET
- CAPACITOR
- INDUCTANCE
- INTERLEAVING OF PARALLEL CONVERTERS
- TURN RATIO
- ZCS
- ZVS

**UNESCO CODE**

- 3306.01 DIRECT CURRENT POWER UTILIZATION
- 3306.05 INSULATED CONDUCTORS
- 3307.14 SEMI-CONDUCTOR DEVICES
- 3307.19 TRANSISTORS
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INTRODUCTION
1. INTRODUCTION

The goal of this project is the analysis and design of a DC/DC converter for aircraft application, based on full-bridge topology. This converter is part of the output of an isolated rectifier unit for the distribution of electric power inside the airplane.

This work is part of the research effort done by the Center of Industrial Electronics in Universidad Politécnica de Madrid (CEI-UPM), in the More Electric Aircraft (MEA) topic.

There is a strong tendency in aircraft designs towards a More Electric aircraft (MEA). This concept is the consequence of the substitution of pneumatic, mechanic and hydraulic equipment by electrical equipment. This increase in electric loads inside the aircrafts causes the need for bigger and more efficient power supply solutions.

The aviation industry is investigating how to reduce emissions without a cost in efficiency. Most part of the development is based on reducing weight, which leads to a reduced fuel consumption. Recent ideas are trying to integrate on planes high-voltage direct current (HVDC), a highly efficient alternative for transmitting large amounts of electricity. A conventional aircraft grid has a main bus voltage of 115V AC with frequencies from 360 to 800 Hz, and 28V as output voltage. These new ideas are planning to incorporate a 270V DC voltage level. [1] [2]

The system works as a rectifier of the current obtained at the turbines, the generator of the plane. A three-phased current flows to a device for eliminating the electronic interference (EMI). Then, a buck rectifier reduces the current, and finally a DC/DC converter adjusts its input voltage to the voltage at the load.

![Figure 6 Simplified block diagram of the system](image)

The objective of this project is designing an efficient and lightweight DC/DC converter in order to reduce fuel consumption on the plane. Its input voltage come from the rectifier. Despite the benefits of 270V DC, output voltage is 28V as it is nowadays integrated in most planes. It is formed by active elements (switches and control) and by passive elements (transformer and bridge):

The specifications of the DC/DC converter are gathered together in the following table:

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated output power</td>
<td>$P_{\text{rated}}$ 10kW</td>
</tr>
<tr>
<td>Input voltage</td>
<td>$V_{\text{in}}$ 400V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>$V_{\text{out}}$ 28V</td>
</tr>
<tr>
<td>Temperature range</td>
<td>$T$ -55°C to +85°C</td>
</tr>
</tbody>
</table>

Table 5 Specification Table
Isolated DC/DC converters have a separation between the input and output terminal, allowing them to have high isolation voltage properties. These converters are advantageous for negative or positive grounds, as for floating ground. Dissimilar to non-isolated converters, they have the capacity to block noise and interference. This enables them to provide a cleaner DC source. Moreover, they are generally safer. The transformer is the element that causes isolation. [3]

As this DC/DC converter works with high voltages, it is isolated. There are two basic types of isolated converters:

- **Flyback converter**: In this topology, the transformer is forced to have a big size as it stores energy and it is not demagnetized. Losses on the transformer consequently are high.

  ![Figure 7 Flyback converter](image)

- **Forward Converter**: The transformer does not demagnetize either and therefore it is complex as well.

  ![Figure 8 Forward Converter](image)

The full bridge configuration is typically used at power levels of 750 W or greater. At lower power levels, topologies as the forward converter are chosen because of their lower parts count. [4]

These topologies do not have the best efficiency possible for this application, as none of them demagnetizes the transformer. Half-bridge and full-bridge topologies are more complex converters, but they do demagnetize the transformer.
• Half-bridge Converter: This topology only allows to demagnetize in half of the hysteresis curve of the transformer.

![Half-bridge Converter with Voltage Doubler at Secondary](image)

*Figure 9 Half-bridge Converter with Voltage Doubler at Secondary*

![Hysteresis Curve](image)

*Figure 10 Hysteresis Curve*
• Full-bridge Converter: In this case, transform magnetizes and demagnetizes through the whole hysteresis curve.

![Figure 11 Full-bridge Converter with Doubler at Secondary](image)

In terms of rectification efficiency, the full-wave rectifier doubles the half-wave rectifier. Ripple in output voltage is lower and has a bigger frequency compared with the half-wave rectifier, so it requires a simpler filter. Losses in transformer are also lower. Full-bridge topologies take more advantage from the transformer, allowing it to have a smaller size.

<table>
<thead>
<tr>
<th>Primary Bridge - Half-Bridge compared to Full-Bridge</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{me}$</td>
</tr>
<tr>
<td>× 2</td>
</tr>
</tbody>
</table>

**Figure 12 Comparison between the half-bridge and the full-bridge switching circuits.** [5]

Full-bridge topology is chosen as transformer can be simpler. Inside full-bridge, there are different possibilities: phase shifted, dual active bridge, resonant dual active bridge and triangular full bridge: [6]

• The Full-bridge Phase-Shifted converter is a robust converter with high density power, but switching losses in MOSFETs in primary are too high.

• The Dual Active Bridge topology allows a bidirectional converter through two sets of full bridges. But in this applications it is not necessary. Switches control is also difficult and it adds complicity in the design.

• The Resonant Dual Active Bridge is a type of Dual Active Bridge that attenuates switching losses. It has ZCS in all switches with the detriment of a more complex control. Its disadvantage is that the output voltage can not be controlled, it is always proportional to the input voltage.

• The Triangular Current Waveform Full-Bridge is a topology that uses an inductance, ideally the leakage inductance of the transformer, to reach a triangular waveform that allows ZCS in the primary switches. It can also minimize the reverse recovery effect on the secondary bridge.

The topology chosen is the Triangular Full-Bridge because the soft switches on both bridges at the primary and the secondary, and it only needs one magnetic component, which gives the leakage needed for obtaining the triangular wave form.
Due to the high ripple on this current, high capacitance is needed at the output. This capacitance can cover a big volume, being a drawback for this topology.

There are different possibilities for rectifying voltage in the secondary of the transformer:

- **Voltage Doubler**: Its main disadvantage is complexity and losses on transformer, that has two terminals in secondary. On the other hand, it only has two diodes.

- **Current Doubler**: Apparently this design would be the best, as it gives on output two currents. But losses on inductances and their volume are great disadvantages.

- **Full-bridge**: The topology chosen in the secondary is full-bridge, as its transformer is simple and this design is not voluminous.
The converter has to fulfill the avionics derating. Topics such as efficiency, parallel operation, input and output protection, thermal, electrical stress, immunity to conducted noise and reliability considerations need to be taken into account. [7]

It is mandatory to avoid Continuous Current Mode (CCM) and always operate with Discontinuous Current Mode (DCM), as behavior control of the converter changes and less hard-switchings are required. Less noise on the output is produced as well.

With a better efficiency, a smaller thermal impedance evacuates the heat produced. This helps to reduce the volume and therefore the power density, very important for aircrafts applications because the converter occupies the less possible. losses have to be studied at the different temperatures reached. In interleaving, as the number of converters increases, although efficiency increases as well, density power reduces and it is needed to find the equilibrium. [8]

Even thought MOSFETs are chosen to stand electrical stress, power-supply failure takes on significant importance in DC/DC converter. An adequate input and output protection in the system reduces these problems.

The noise behavior of MOSFET devices can basically be divided in two noise sources: thermal noise and flicker (1/f) noise. The quality, the number of defects and the material of the device determine this level of noise. [9]

However, in Aircrafts applications the intrinsic noise from space-quantization effects can not be underestimated, being able to cause the destruction of some MOSFETs or alter the control system. [10]

Nowadays Silicon Carbide is the best material possible as it is more resistant to space noise than Silicon. In the future, Gallium Nitride will be probably another good option, but it is still developing.

There were two options for the control of the converter. One possibility was working with closed loop. The input voltage, which comes from the previous rectifier state, would vary in a certain range and the control of the converter would modify the duty cycle in order to obtain the output wanted, 28V. But after weighing up how simple it would be, it has been decided that the rectifier will give the same output voltage so the converter’s control is in opened loop.

There are basically two types of transformer losses, and they can not be undervalued. They are the copper losses, that vary according to the internal resistance presented by the windings, and the iron losses, appeared in the core of the transformer and are caused by alterations in the flux. Both types, beside the leakage inductance, depend on the geometry of the transformer, the materials, the frequency, etc. The design of the transformer absorbs the same amount of work as the design of the converter. That is why this assignment focuses on the converter. However, results deliver the turn ratio and the frequency demanded in order to acquire the best point of operation of the converter. [11]
METHODOLOGY
METHODOLOGY

This section is to facilitate the design of a converter and selection of the best parameters that best fit specifications. The ultimate design objective is to achieve the best performance with the lower losses possible.

The following diagram is an explanation of all design steps of any DC/DC converter.
The topology chosen depends on the specifications required. For example, some topologies have a better performance with high power and others with low power. Having chosen one, different parameters have to be changed in order to optimize the converter: devices, inductance, capacitance, etc.

Once the best configuration are found, the correct magnetizing current is needed in order to have zero voltage switching on transformer.
TOPOLOGY
2. TOPOLOGY

2.1. TRIANGULAR CURRENT WAVEFORM FULL-BRIDGE

The Triangular current waveform full-bridge is a topology that uses an inductance to achieve a triangular current waveform and has ZCS in the primary switches. The leakage inductance of the transformer can be used. It also minimizes the reverse recovery effect on the secondary bridge. [12]

The topology is composed of two bridges, a primary active bridge, and a typically passive secondary bridge. This secondary bridge can be substituted by an active bridge for losses optimization, as it is going to be explained in Optimization section. The two bridges are connected by a transformer and an inductor in series.

The main advantages of this topology are the following:

- Soft transitions: This topology of full-bridge converter works in discontinuous conduction mode DCM, therefore all of the transitions in primary side except one per leg and cycle are done with ZCS. Additionally, zero voltage switching can also be achieved with the magnetizing current.
- Magnetizing integration: The full-bridge topology needs a single magnetic component and a single core, that confers the leakage inductance demanded.
- Easy control: The management of MOSFETs and their duty cycle of several parallel converters can be easily realized with Peak Current Mode Control, making sure of running in a stable range of duty cycle. With a single converter this range is larger.

Figure 17 Schematic of the triangular current full-bridge

Anyway, there are some disadvantages that must be considered:

- High number of transistors: The main disadvantage of a full-bridge topology is that it needs minimum eight transistors. Because of this the total voltage drop in
transistors duplicates of that in case of center-tap rectifiers, if both sides of the transformer are connected as rectifiers. Losses are increased and conversion efficiency is somewhat reduced.

- High RMS currents: The RMS current is the equivalent steady DC value which gives the same effect and therefore the same losses on transformer and transistors, as they have internal resistances. Another inconvenience of high RMS current is the high ripple, which leads to a higher capacitance value for the output. With interleaving ripples can be compensated and capacitance can be smaller.

### 2.2. PRINCIPLE OF OPERATION

In Figure 18 appears the current of the transformer secondary and its voltage. First Powering state, on d1, S1 and S4 switches are turned ON. The input voltage is applied to the primary of the transformer and the output voltage to the secondary. The current ascends linearly due to the leakage inductance of the transformer. In secondary side, diodes D5 and D8 are conducting the output current. The slope of the current can be calculated with the following equation.

\[
\Delta I_t = \frac{(n \cdot V_{in} - V_{out})}{L_t}
\]  

(1)

First freewheeling state, on d2, S1 is turned OFF and after an inactive-time S2 is turned ON. The current circulates through the parallel diode D2 and S4. The voltage assigned to the primary is zero and the output voltage in the secondary side, so the current declines linearly and the slope is calculated with this equation.

\[
\Delta I_t = \frac{-V_{out}}{L_t}
\]

(2)

![Figure 18 Transformer current and voltage waveforms, and switching states on a cycle](image)

First dead state, on d3, the current has finally fallen into zero. A small sinusoidal current expected by the resonance of the leakage inductance and diode parasitic capacitance can be discerned during this break time.
Second powering state, on d4, S3 and S2 are turned ON. The current drops to negative values. This period is equivalent to d11 period. In the secondary side, D6 and D7 are conducting the output current.

Second freewheeling state, on d5, S3 is turned OFF and S2 is turned ON, the current circulates through D4 and S2.

Second waiting state, on d6, the current in the transformer is zero and the next switching cycle can initiate.

To achieve ZCS in the primary MOSFETs, it is fundamental to avoid continuous conduction. This can be done with an accurate control of the leakage inductance of the transformer. The equations (1) and (2) define the slopes for the triangle waveform. The input voltage $V_{IN}$, the turn’s ratio $n$ and the leakage inductance $L_d$ are critical parameters in the design of this topology.

In order to avoid continuous conduction, it can be settled the dead time, $d_3$, and in function of this parameter, calculate the rest of the variables. Then, Powering time, $d_1$, can be obtained as shows equation (2)

$$d_1 = \frac{V_{OUT} \cdot (1 - d_3)}{n \cdot V_{IN}}$$

The next step is calculating the Free-Wheeling time, $d_2$. The cycle’s period is divided into two half periods, where each one has one Powering, one Free-Wheeling, and one Dead-Time state. As a result, the addition of $d_1$, $d_2$ and $d_3$ results the unit, and are the same as $d_4$, $d_5$ and $d_6$, respectively. Accordingly with this explanation, $d_2$ can be calculated as follows equation (4):

$$d_2 = 1 - d_1 - d_3$$

The knowledge of the time spent in every state allows to find the leakage inductance that fits the slopes demanded for fulfilling these times.

$$L_t = \frac{(n \cdot V_{IN} - V_{OUT}) \cdot d_1^2 + V_{OUT} \cdot d_2^2}{2 \cdot I_{AVG} \cdot f_s}$$
where $I_{AVG2}$ is the average current at the output and $f_s$ is the frequency of half period.

Equation (5) is acquired equalizing the area confined by the current waveform and the area that would confine the average current. That is to say that both current waveforms deliver the same energy.

The high side switches are the ones having hard switching so they have more losses than the low-side devices. Freewheeling states are always taken with the low side switches ON to achieve better balance or power losses.

### 2.3. WAVEFORMS

Afterwards different features of this topology are shown. As the slope of the first stage is higher, it is needed a smaller leakage inductance for fitting the equations.

The current slope and the time of Powering state and Free-wheeling state modify depending on the turns ratio, in such a way that fulfils the converter's power. With a turn ratio close to 1:1 the slope and the primary current peak are higher, so it is needed less Powering Time for reaching 10 kW. In opposition, with turn's ratio higher than 7:1 the slope and the current peak in the primary are lower and it is needed much more Powering Time.
Short Free-wheeling states are not recommended because they increase switching losses, due to the reverse recovery, and they are difficult to control. Short Powering states are neither recommended for the same reasons and because they cause high current peaks in the primary that produce non-viable conduction losses.

In turn ratios 1:1 and 7:1, current in primary has to fulfill that both areas B1 and B2 are equal. Areas correspond to 10 kW of power. Therefore, for short Powering states, high current peaks are required.

In secondary, current has to fulfill that A1 is the same that A2. In this case, it does not matter how long are states. Current peak does not change as bases of both triangles are the same.
TECHNOLOGIES AND MATERIALS
3. TECHNOLOGIES AND MATERIALS

Different types of power semiconductor switches are designed for functioning in diverse conditions. Voltage, current and switching frequency of the application are the parameters that need to be considered for electing the right switch.

Increasing frequency allows the transformer to be smaller. As the converter’s layout depends on the size of the transformer and specifications establish that it is needed a high power density. Therefore, a high frequency is necessary.

MOSFET is the technology that best fits the exigencies. Some IGBTs are also good solutions.

The insulated Gate Bipolar Transistor (IGBT) is a minority-carrier device. It can be considered as a device with MOSFET input features and bipolar output characteristic, ergo is a voltage-controlled bipolar device. It incorporates the best characteristics of MOSFET and BJT in order to obtain optimal devices. [14]

Its main disadvantages are the reason for rejecting this technology:

- Switching speed is lower than in Power MOSFET. The turn-off speed is slow and in this full bridge topology, where switches are very often, this is an important drawback.
- The internal PNPN thyristor can produce latchup. [15]
3.1. MOSFET

A power MOSFET is a type of metal oxide semiconductor designed to cope with high levels of power. They have become the standard choice for a wide range of power conversion applications. Power MOSFETs are majority carriers devices, superior to Power Bipolar Junction Transistors (BJTs) and Insulated Gate Bipolar Transistors (IGBTs) in applications where switching losses are predominant. They can be paralleled for reducing conduction losses and for reducing its voltage drop, which increases with temperature. The main division of MOSFET is: [16]

- N-Channel Enhancement-Mode Power MOSFET
- P-Channel Enhancement-Mode Power MOSFET
- N-Channel Depletion-Mode Power MOSFET

N-Channel enhancement-mode is the most used in power switching circuits, as a result of having a lower on-state resistance in contrast with P-channel devices. An N-Channel depletion-mode Power MOSFET diverges from the enhancement-mode in that it is normally turned ON at 0V gate bias and demands a negative gate bias to block the current.

Figure 27 N-Channel Enhancement-Mode Power MOSFET Structure. [17]

A positive gate voltage ($V_{gs}$), higher than the gate threshold level ($V_{gsth}$), creates a n-type inversion channel under the gate oxide. This way, drain and source are connected and current is allowed to flow. The gate threshold voltage specifies the minimum voltage required for creating this n-type inversion channel. Power MOSFET has diverse intrinsic components as essential parts of its structure: [16]

- Parasitic capacitance: They tend to limit the frequency response of circuits. This capacitance can be divided two, Gate Capacitance caused by the channel charge and due to the structure of the transistor, and Diffusion Capacitance, formed by the source region.
- Body diode: An intrinsic diode is formed between the drain and source. It is appropriate for circuits where a path is required for reverse drain current, known as "free wheeling current".

The main features of Power MOSFETS are:

- The static behavior is determined by the circuit, on-resistance, and its own transconductance. There are three different regions of working: Ohmic, where the device acts as a resistance; Current-Saturated, where the drain current is defined by a function of the gate-source voltage and the transconductance, and Cut-off, where the device is an open-circuit.

- The on-resistance $R_{\text{DS(on)}}$ settles the conduction power dissipation and increases with raising temperature.

![](image1.png)

Figure 28 Increase on-resistance $R_{\text{DS(on)}}$ with with temperature $T_j$ for Power MOSFET. [24]

$R_{\text{DS(on)}}$ increases with temperature because of majority-only carrier movement. It guarantees thermal stability when paralleling the devices.

- The dynamic behavior is defined by the switching features of power MOSFET. The intrinsic capacitances, resistance, gate charge and the reverse recovery features of the free-wheeling diode are essential in the dynamic performance of the device.

- Parasitic capacitance, explained ahead, are the intrinsic capacitance of MOSFET. They are separated in three components, known as gate-to-source capacitance ($C_{\text{gs}}$), gate-to-drain capacitance ($C_{\text{gd}}$) and drain-to-source capacitance ($C_{\text{ds}}$). Nevertheless, data sheets usually group these capacitances into three other parameters:
  - Input Capacitance $C_{\text{iss}}$
  - Output Capacitance $C_{\text{oss}}$. Total energy charged at these capacitances on a single converter has to be lower than the magnetizing energy in order to switch transformer with ZVS.
  - Reverse transfer capacitance $C_{\text{rss}}$, related to reverse recovery losses.

$C_{\text{oss}}$ resonates with the parasitic inductance and causes noise. This could break the MOSFET as current could overcome the maximum current.

- Intrinsic Resistance, $R_g$, forms an RC circuit that defines constant times of voltage change at the MOSFET, and consequently its switching time.
- Heat generated within the chip is dissipated by means of a heat sink comprised of thermal resistances and thermal capacitances. This way, Power MOSFET has junction temperature limitation. This heat sink determines the final application and the power managed by the MOSFET.

Good switching properties are crucial for the full-bridge topology. Therefore, MOSFET is the technology chosen for the switches on the converter.

Materials of chips inside power electronic devices have been evolving very fast these past years. Nowadays, Silicon is still the main material used, but industries estimate that Silicon Carbide will soon be the most sold material. Gallium Nitride has an excellent future, but it is still not as developed as the other materials. [19]
3.2. SILICON

Power electronics and power system applications have long time behave with Silicon. High conduction losses of Silicon in MOSFET had been an important disadvantage. But manufacturers developed new Silicon-based materials and technologies, such CoolMos and OptiMos, that reduce the on-resistant, causing much less conduction losses. Anyway, Silicon devices have led power electronics industries. They are still not bad options.

However, new applications are demanding faster devices with high voltage and high switching frequency capability. Some advanced power conversion applications are requiring to operate at temperatures higher than 150°C junction temperature and high power densities. Silicon is not able to fulfill these inlexible restrictions without expensive cooling systems or large number of devices in series and parallel.

Wide-bandgap-based semiconductor materials such as Silicon-Carbide and Gallium Nitride propose multiple benefits for designing power electronic circuits. The superior physical properties of these semiconductors make possible less intrinsic carriers concentration, less reverse recovery losses and best conduction and switching losses, among other advantages.

3.3. SILICON CARBIDE

Silicon Carbide devices are great solutions for operating with high power and high voltage.

This material has been the main focus of research of new materials. Its wide bandgap is much larger than the bandgap of Silicon. Additionally, SiC has a higher electric field, allowing layer to be much thinner. This causes a smaller minorities concentration and less carriers charge storage, allowing devices to operate with high switching frequencies. Its high thermal conductivity along with the wide bandgap energy enables for power efficient high temperature applications.

Regardless of these advantages, Silicon Carbide has not started to be used in power devices until recently. Difficulty in manufacturing is the main lack that has delayed the development of SiC.

3.4. GALLIUM NITRIDE

Gallium Nitride (GaN) is a material that nowadays is not too developed. The main applications for GaN devices is operating with high frequencies, as its carriers’ density can change even faster than in SiC. As a result, reverse recovery losses are reduced tremendously. [21]

Industries are very optimistic with GaN. In contrast to the finest Silicon MOSFET, this material will allow high power density thanks to the ability to switch at high frequencies. Gallium Nitride could reach higher efficiencies in the full-bridge topology. Consequently, power density could improve by downsizing the size of passive components and by more simple cooling systems.

Breakdown voltage in GaN is larger than in SiC. As Silicon is the material more developed and more stretched at the moment, it usually operates in extreme conditions. But as SiC and GaN are not that developed, they probably do not perform
at the limit of their possibilities. For that reason, its possible that their voltage breakdown could be even bigger.

However, the on-resistance of MOSFETs built by Silicon, Silicon Carbide and Gallium Nitride are similar. The difference on their losses is allocated on switches.

![Figure 31 Theoretical on-resistance vs blocking voltage capability for Silicon, Silicon Carbide and Gallium Nitride. [22]](image-url)
INTERLEAVING OF MULTIPHASE CONVERTERS
4. INTERLEAVING OF MULTIPHASE CONVERTERS

Interleaving consists in producing a multiphase current thanks to various converters connected in parallel. There are as many phases as converters. The main advantage is that every converter handles less power so current peaks are lower.

\[ P_{\text{CONV}} = \frac{P_{\text{OUT}}}{n_{\text{CONV}}} \]  \hspace{1cm} (6)

where \( n_{\text{CONV}} \) is the number of converters in parallel and \( P_{\text{CONV}} \) power per converter. For this application, the output power is 10 kW. With lower power in a single converter, its current peaks are lower. This leads to lower switching losses. The rest of the equations for converters interleaved are the same as in a single phase converter.

In this application, interleaving helps to take advantage of the leakage inductance of the transformer. With a single converter, for most turn ratios it is mandatory to add another external inductance to the circuit. This is a big disadvantage as it would force to operate with specifications that would not produce the less losses possible, or to place an external inductance that would drop power density.

Definitely, this system allows to choose the turns ratio and the number of converters for the best efficiency, taking care of selecting a possible leakage inductance.

Current on output is the addition of the phased currents from every converter. As the turn ratio modifies slopes of the current waveform in a single transformer, current waveform on the output changes as well. Consequently, ripple on output is also determined by the turn ratio. Anyway, new ripple is always lower than in a single converter.

Interleaving also creates more robust converters. For example, in a six-phased converter, if some phase breaks, the converter is still able to provide five sixths of the total power. But, if a one-phased converter breaks, it is not able to supply any power.

There are thus some disadvantages to be considered. Using several numbers of converters also increases the volume of the total system. But, unlike the external
inductance, losses drop. This allows to save space from the cooling system, that does not need to be as powerful. Capacitance on the output filter also reduces as ripple is lower. As a result, the best relationship between volume, efficiency and inductance has to be found in order to build the converter that better fits specifications.

Figure 33 Top waveform: Output current (without taking into account the dead-time). Bottom waveform: Current in secondary of a single converter. Turn ratio = 7:1. 2 Parallel converters.

Figure 34 Top waveform: Output current (without taking into account the dead-time). Bottom waveform: Current in secondary of a single converter. Turn ratio = 2:1. 6 Parallel converters.
Another disadvantage is the control of the system. In interleaving is compulsory to use Peak Current Control, not been possible to reach some duty cycles. Nevertheless, with a single converter opened loop is feasible, Peak Current Control is not fundamental and a larger range of duty cycles is practicable.

As ripple on output modifies depending on the number of converters and the turn ratio on the transformer, different capacitor is needed for the output filter. At some turn ratios, a bigger number of parallel converters does not mean lower ripple, as it could be thought. Further information is given in paragraph (Simulations and Results).
DESIGN SPACE
5. DESIGN SPACE

In order to evaluate the efficiency of this converter, a proper calculation of losses in the devices as well as in the transformer is required. As it was explained before, the design and optimization of the transformer is out of the aim of this work so it will not be calculated. However, the optimized design is going to take into account some of the restrictions on the transformer design and the integration of the magnetics needed to achieve a good power density.

The parameters regarded for optimization are:
- Frequency
- Inductance
- Turns ratio of the transformer.
- Number of devices in parallel (Primary and secondary)
- Diodes or MOSFET in secondary
- Number of Parallel converters

5.1. LOSSES

The reverse recovery of transistors in the secondary side bridge that act can be neglected because the topology is forcing them to turn on and off with zero current. However, if the negative current slope is high this loss mechanism cannot be neglected and it is needed to calculate those losses if the asymmetry in the triangle is very high.

Once the power losses are calculated, thermal analysis is required to know what type of cooling system to choose. To maximize the power density, liquid cooling is required for the primary MOSFETs, the transformer, the secondary MOSFETs and the capacitance. This also minimizes the converters volume and weight because convectional heat sinks will be too long to fit the target weight and size.

MOSFETs have two kinds of losses. Conduction losses are determined by the topology and by the power specification. In the other hand, switching losses can be lowered, with a correct modulation of the triangle current.

\[ P_t = P_c + P_{sw} \]  

5.1.1. CONDUCTION LOSSES

Conduction losses in power MOSFET can be calculated supposing a constant resistance when conducting, the drain-source on-state resistance (\( R_{DSon} \)):

\[ P_{COND} = R_{DSon} \cdot i^2_{DRMS} \]  

Due to the plane temperatures while flying, \( R_{DSon} \) is taken at the temperature of 100ºC. With this \( R_{DSon} \), the worst scenario is analyzed for conduction losses.
Therefore, the instantaneous value of the MOSFET conduction losses is:

\[ p_{CM}(t) = u_{DS}(t) \cdot i_D(t) = R_{DSon} \cdot i_D^2(t) \]  

Some manufacturers give \( R_{DSon} \) referred to \( R_{DSonMAX} \) at 25ºC.

### 5.1.2. SWITCHING LOSSES

The general equations of switching losses are:

\[ P_{SWON} = E_{ON} \cdot f_{SW} \]  \hspace{1cm} (10)

\[ P_{SWOFF} = E_{OFF} \cdot f_{SW} \]  \hspace{1cm} (11)

Depending on the data-sheet of the MOSFET, there are two methods for obtaining the switching losses. Some manufactures do not give this information and needs to be calculated by means of a linear approximation of the MOSFET switching process, which represents the worst case calculation. But other manufactures deliver how \( E_{ON} \) and \( E_{OFF} \) fluctuate according to drain source current, providing an easier and better way for studying switching losses.
5.1.2.1. LINEAR APPROXIMATION

5.1.2.1.1. SWITCH-ON TRANSIENT

Switching losses are produced while voltage and drain-current are neither zero. In order to calculate these losses is necessary to estimate how long does MOSFET takes to switch.

Gate voltage is modified by the Driver. While this voltage does not reach the threshold voltage ($u_{GS(th)}$), no current flows through the MOSFET. The time taken depends on the gate resistor ($R_g$) and the input capacitance of MOSFET ($C_{iss}=C_{GD}+C_{GS}$). Higher $R_g$ and $C_{iss}$ implies higher time.

Starting from this point, drain-current starts to increase until, due to carriers on MOSFET, gate-source voltage is established in miller voltage. During this current rise-time, the drain-source voltage has the same value as when MOSFET was turn-OFF. In this application it would be 400V in primary and 28V secondary.

![Graph](image)

Figure 39 Top Part: Gate Voltage ($u_{GS}$) and current ($i_g$). Bottom part: Drain-source voltage ($u_{DS}$) without taking the reverse recovery of the free-wheeling diode into account.

Due to slow changes of carriers’ concentrations in other devices, reverse-recovery current has to be absorbed by the MOSFET, causing additional power losses. Further information is given on paragraph Reverse Recovery Losses.
After these devices have been switched off, the drain-source voltage is falling from $U_{DS}=U_{DD}$ to its on-state value $u_{DS}=R_{DSon}\cdot I_{ON}$. The Miller effect befalls and the gate-source voltage is settled at the $u_{GS}=U_{(plateau)}$.

**Figure 40** Top part: Power losses. Bottom part: Reverse-recovery effects on switching losses

The worst case value of the current rise-time $(tri)$ between zero and $I_{Don}$ can be read from the MOSFET data-sheet.

**Table: Electrical Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Values</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dynamic Characteristics</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Transconductance</td>
<td>$g_s$</td>
<td>$V_{GS}=2\cdot V_{DS(on) max}$, $I_D=100A$</td>
<td>73</td>
<td>146</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>$C_{iss}$</td>
<td>$V_{GS}=0V$, $V_{DS}=25V$, $f=1MHz$</td>
<td>-</td>
<td>5430</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>$C_{oss}$</td>
<td>$f=1MHz$</td>
<td>-</td>
<td>1915</td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>$C_{rss}$</td>
<td>-</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>$t_{(on)}$</td>
<td>$V_{DD}&gt;20V$, $V_{GS}=10V$</td>
<td>-</td>
<td>22</td>
</tr>
<tr>
<td>Rise time</td>
<td>$\tau$</td>
<td>$I_D=100A$</td>
<td>54</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>$t_{(off)}$</td>
<td>$R_D=2\cdot Z$</td>
<td>63</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>$\tau_{f}$</td>
<td>-</td>
<td>53</td>
<td></td>
</tr>
</tbody>
</table>

**Figure 41** Reading the current rise- (red) and fall-time (blue) from the data-sheet. [23]
The slope of the drain-source voltage is established by the gate current circulating through the gate-drain capacitance \( (C_{GS}=Crss) \). In order to calculate the voltage fall-time \((t_{fu})\) with an acceptable accuracy, the non-linearity of the gate-drain capacitance has to be taken into account. For engineering calculations, a two-point approximation is used. It is supposed that the value of the gate-drain capacitance is determined by the drain-source. The drain-source voltage during the fall time, the two-point approximation being taken into account, is shown in the figure of the Drain-Source voltage with the dotted line. Since this approximation is used only to establish the voltage fall time (as well as the rise time during switch off) and the drain-source voltage is adopted to have the linear form, it becomes clear that this analysis presents the worst-case for the switching losses calculation.

The gate current is determined by the Driver circuit. Consequently, gate resistance has to be modified in order to fulfill the following equation:

\[
I_{Gon} = \frac{U_{Dr} - U_{(plateau)}}{R_G} \tag{12}
\]

The voltage fall time can now be calculated as a median of the fall times defined through the gate current, the capacitances \( C_{GD1} \) and \( C_{GD2} \), and this voltage fall. The capacitance equation associates these parameters, and as a result, time is calculated.

**Figure 42** Reading the plateau voltage from the data-sheet. [23]

**Figure 43** Two-point representation of the gate-drain capacitance. [23]
5.1.2.1.2. SWITCH-OFF TRANSIENT

Switch-off process corresponds to the switching-on process of the MOSFET in the opposite order and thus will not be discussed exhaustively. Two important differences are:

- No reverse recovery takes place.
- The gate resistance has to fulfill other equation, as gate current is again determined by the Driver:

\[ I_{off} = \frac{U_{\text{plateau}}}{R_g} \]  \hspace{1cm} (13)

5.1.2.1.3. SWITCHING ENERGIES AND LOSSES

According to previous contemplations, for this application the only energy losses on turning ON are the reverse recovery losses. They are explained in paragraph (Reverse Recovery Losses).

The switch-off energy losses in MOSFET can be calculated estimating the area of Poff in Figure 40. The switch-off losses in the diode are normally \( (E_{offD} \approx 0) \). Therefore:

\[ E_{offM} = U_{DD} \cdot I_{Doff} \cdot \frac{t_{\text{tri}} + t_{\text{fu}}}{2} \]  \hspace{1cm} (14)

5.1.2.2. INTERPOLATION OF SWITCHING LOSS

If switching losses are given on the data-sheet, it is possible to pick different points from the graphs [24] and create them to a function. This allows to estimate the switching losses depending on the drain current.

![Figure 44 Clamped inductive energy vs drain current. [24]](image)
Matlab command ‘cftool’ interpolates these points, creating the function that fits the best the graphs. The equations obtained for $E_{onM}$ and $E_{offM}$ have the following general shape:

$$E_{onM} = a_{on} \cdot i_{Don}^4 + b_{on} \cdot i_{Don}^3 + c_{on} \cdot i_{Don}^2 + d_{on} \cdot i_{Don} + e_{on}$$ (15)

$$E_{offM} = a_{off} \cdot i_{Dooff}^4 + b_{off} \cdot i_{Dooff}^3 + c_{off} \cdot i_{Dooff}^2 + d_{off} \cdot i_{Dooff} + e_{off}$$ (16)

where coefficients vary in function of the MOSFET.

5.1.3. REVERSE RECOVERY LOSSES

These losses are part of the switching losses. The root of them is the mobility of the minority carriers on the diodes that are about to stop conducting. In order to block the current, the concentration of minorities on P and N side of diodes has to be lower than an equilibrium value. Otherwise, diode continues working. As density carriers is not able to drop at the same ratio as current, when it reaches zero, it continues to negative values. This phenomenon produces a waste of energy ($Q_{irr}$).

---

**Figure 45** Reduction of minority carrier concentration

**Figure 46** Time taken for the reduction of minority carrier concentration. [25]
The worst-case values of the reverse-recovery charge ($Q_{rr}$) and duration ($t_{rr}$), which will be used for calculating power losses, can be read from the MOSFET data-sheet.

![Reverse Diode Data Sheet](image)

Figure 47 Reading the reverse recovery time (red) and charge (blue) from the data-sheet. [23]

In this topology, MOSFETs where reverse recovery takes place are in the low MOSFETs of both bridges. Negative current values on this MOSFETs implicate the conduction of the “free-wheeling” diodes of the high MOSFETs, that it is actually where losses are produced.

Reverse recovery losses are calculated supposing that the time spent by the concentration of minority carriers to drop ($t_{rr}$) is constant and does not vary. Therefore, a higher negative slope of the current produces more losses as more current flows in the same amount of time.

![Reverse Recovery Losses](image)

Figure 48 Reverse recovery losses of MOSFETs in primary. Frequency = 100kHz.
Turn ratios close to 14:1 have a greater slope on the “Free-Wheeling” state that causes high reverse recovery losses. On the other side, turn ratios close to 1:1 and lower have high switching losses due to their high current peak. Therefore, converter should not have neither of these turn ratios.

5.2. CAPACITANCE

The capacitance has to be high enough in order to reduce ripple of the current on the output. As capacitance increases, ripple reduces.
Specifying the ripple on the output voltage, the capacitance can be calculated with the following equations:

\[
\Delta Q_1 = \frac{(I_{pk2} - I_{AVG2}) \cdot t_1}{2} \quad (17)
\]

\[
t_1 = \frac{(I_{pk2} - I_{AVG2}) \cdot L_t}{(n \cdot V_{IN} - V_{OUT})} \quad (18)
\]

\[
\Delta Q_2 = \frac{(I_{pk2} - I_{AVG2}) \cdot t_2}{2} \quad (19)
\]

\[
t_2 = \frac{(I_{pk2} - I_{AVG2}) \cdot L_t}{(V_{OUT})} \quad (20)
\]

As previous operations, an area, and therefore energy, is calculated. This time the area is the one confined between the output current waveform and the average current. The outcome is the energy that capacitance absorbs.

Both times, \( t_1 \) and \( t_2 \) are deduced by the capacitance’s equation:

\[
Voltage = L_t \frac{\Delta Current}{\Delta Time} \quad (21)
\]

\[
\Delta Q = \Delta Q_1 + \Delta Q_2 \quad (22)
\]

where \( \Delta Q \) is the energy denote previously.

Finally, the capacitance is:

\[
C = \frac{\Delta Q}{\Delta V_{OUT}} \quad (23)
\]

where \( \Delta V_{OUT} \) is the ripple at output voltage.
5.3. FREQUENCY

Frequency impacts on switching losses as in every cycle there is a specific amount of losses. So, if the period of cycles is decreased, there are more hard-switchings in primary per unit of time and therefore switching losses are increased.

Losses are energy per unit of time. This is another way to find the relationship between switching losses and frequency.

The current peak does not change with the frequency. And as conduction losses depend on this current peak, they do not change either. However, higher frequencies are desirable in order to achieve smaller magnetic component, which are usually bulky and they decrease the power density.

![Figure 53](image1.png) **Figure 53** Losses with a turn ratio of 1:1 for different number of MOSFETs in primary.

![Figure 54](image2.png) **Figure 54** Losses with a turn ratio of 1:1 for different number of MOSFETs in primary. Frequency = 100kHz
Capacitance on the output filter also modifies. With higher frequencies, the area that represents the energy absorbed by the capacitance drops (Principles of Operation) and consequently capacitance can be reduced as well.

Figure 55 Capacitance for different output voltage ripple.

Figure 56 Capacitance for different output voltage ripple. Frequency = 100kHz
Furthermore, if frequency increases, reverse recovery losses increase as well as there are more switches on turning-on on low transistor of both bridges.

![Reverse Recovery Losses vs Frequency](image)

**Figure 57 Relationship between reverse recovery losses and frequency.**

### 5.4. INDUCTANCE

Seeking a higher power density, Leakage Inductance of the transformer is used as the primary inductor in such a way that with a good design of the converter, it is not necessary to add external inductance. The geometry of the transformer, the accuracy in making the windings, the material and the Turn Ratio determines this leakage inductance, and normally is in the range of 5 to 20 µH on the primary side of the transformer.

In case of requiring more inductance, the external inductor could be placed in the primary or secondary side. In primary side the RMS current is lower. On the secondary side less inductance would be needed. The solution is not obvious as it is difficult to predict what option produces less losses. Anyway, the density power would increase considerably and for aircraft applications is not advisable.

There is also a relationship between frequency and inductance. As shows equation (5) (Principles of Operation), for a higher frequency, inductance is lower.
Accordingly to this result, in order to have sufficient with the leakage inductance of the transformer, the final design of the converter should work with a frequency of around 100kHz.

**5.5. TURN RATIO OF THE TRANSFORMER**

Turn changes the slopes on the Waveform Current. If the number of turns in primary, n1, is much bigger than the number of turns in secondary, n2, Powering Time increases in order to reach the average current expected in the output. On the other hand, if n2 is much bigger than n1, Powering Time drops while its own slope increases, so the output power remains the same. Either turn ratios produce high reverse recovery losses, because of the high slopes on Free-wheeling state and Powering state, respectively. For example, on the following figure of primary current blue and green waveform seem different, but both of them have high switching losses.

The first scenario has another difficulty. With the peak current mode control in discontinuous conduction mode, there is a stability problem at duty cycles higher than 0.66. Anyway, the stability range of peak current control can be extended to $0 \leq \text{Duty Cycle} \leq 1$ by adding to the controller of an artificial ramp with a slope of $m_1 > 0.086m_2$, or by addition of output voltage feedback. $m_2$ is the current slope of the Free-Wheeling state. [26]
Even so, unstable zone could be controlled with an opened loop control anyway. The problem is that just one single converter would be allowed.

On the second scenario, slopes in Powering state are too big, causing huge peak currents on the primary. This increases conduction losses and switching losses, as hard-switchings are made with higher currents. Therefore, turn ratio smaller than 1:1, with current peaks bigger than 1000 A are not possible configurations.

Accordingly to Figures 58 and 59, turn ratio also affects on the inductance demanded. Equation (5) (Principles of Operation) also explains this phenomenon, as d1 and d2 are the most influential parameters for calculating the inductance.

The current peak in secondary does not alter. Figure 21 (Topology) shows why. As the area confined by the current waveform is the same as the area confined by the average current, if dead time is established and does not modify, the base of the triangle does not fluctuate and consequently the height, the current peak in secondary, does not change. This same explanation justifies that capacitance for a single converter does not modify with the turn ratio.

5.6. NUMBER OF DEVICES IN PARALLEL IN PRIMARY AND SECONDARY

The number of devices in parallel in the primary is determined by how switching losses and conduction losses fluctuate with frequency. As every MOSFET has dissimilar $R_{DS}$ and $E_{OFF}$ equations, the number of MOSFETs in primary is dissimilar as well. The number of converters in parallel and the turn ratio also impact.
As shows the figure above, at different frequencies, diverse number of MOSFETs in the primary is needed. With more parallel MOSFETs there are more switching losses. Therefore, at high frequencies where these losses carry weight, less parallelize MOSFETs is demanded. Conduction losses do not change with frequency. That answers why conduction losses at 10 kHz, the hypothetical yellow line, is not discernible; it is hidden by the blue line, conduction losses at 100kHz.

Turn ratio reduces peak current in primary. The result is that switching and conduction losses drop. Therefore, for diverse turn ratio, different number of parallel devices are also needed.

On the secondary there are no hard-switchings. There are only conduction losses. As a result, losses can be dropped as desired with as many devices wanted. It is important to have always in mind that the final application forces to have a high density power.
5.7. DIODES OR MOSFETS IN SECONDARY

In order to select the technology that produces less losses, it has been studied the behavior of diodes against MOSFETs.

While conducting, if voltage-curves of diodes are linearized, diodes can be displaced by a voltage source and a resistance. Consequently, RMS current and average current are the parameters that increase losses:

\[ P_{\text{COND}} = V_d \cdot I_{\text{AVG}} + r_d \cdot I_{\text{RMS}} \]  

(24)

This equation results from the integral of conduction losses. MOSFET’s losses only have the resistance term. Therefore, apparently on MOSFETs there are less losses than in diodes. Simulations support this explanation.

Reverse recovery losses are about the same, since they are determined by the material of the chip inside the device.
5.8. NUMBER OF PARALLEL CONVERTERS

As it is explained in paragraph (Number of Devices in Parallel), the number of parallel converters impacts on the efficiency. Study on losses shows that, in general, with higher number of parallel converters, higher efficiencies can be reached.

![Figure 66 Efficiency based on converters on parallel and turn ratio. MOSFETs in primary = C2M0080120D. [28]](image)

As ahead, this standard depends on the MOSFETs characteristics and does not require to be fulfilled in every scenario. For example, with MOSFET C2M0040120D, at high turn ratios, as the number of converters grows, efficient goes slightly down.

Operating with various converters allows to take advantage of the leakage inductance of the transformer in an easier way. On paragraph (Inductance) it is introduced this fact. For the time of fabricating the converter, a good strategy is building firstly the transformer with the desired turn ratio, and then, depending on the leakage inductance measured, graphs declare the number of converters in parallel needed in order to achieve the efficiency wanted.

![Figure 67 Efficiency based on converters in parallel and turn ratio. MOSFETs in primary = C2M0040120D. [29]](image)
The number of parallel converters also influences on the capacitance at the output. If waveform current, ergo the Peak Current Control, on every converter are correctly phased, ripple on the output voltage falls and a lower capacitance is needed in the filter.

Figure 68 Capacitance determined by converters in parallel and turn ratio. Frequency = 100kHz.
SIMULATIONS AND RESULTS
6. SIMULATIONS AND RESULTS

6.1. CHOOSING PRIMARY AND SECONDARY DEVICES

Primary bridge MOSFETs operate with 400V, therefore the best materials are Silicon and Silicon Carbide. It is possible to discriminate two types of MOSFET side:

- High side has switching, conduction and reverse recovery losses. Consequently, the number of MOSFET in parallel per side and the MOSFET employed are determined by the configuration that reaches the lower losses.
- Low side only has conduction losses. For that reason, the MOSFET chosen is the one with less $R_{DS}$ at temperature of operation. Also a high number of MOSFET per side is desired.

Secondary bridge performs with 28V, for that reason GaN MOSFETs and diodes can be taken into account as alternatives to Silicon and Silicon Carbide MOSFETs. The four transistors mainly have conduction losses. Therefore, the same configuration selection as in low MOSFETs in the primary is applicable.

An important fact to take into account is that devices have to be able to endure the current that flows through them without breaking.

6.1.1. HIGH SIDE IN PRIMARY BRIDGE

Several devices have been studied. Research has been focused on Silicon Carbide MOSFETs, as they are better at high frequencies of switching. Anyway, some Silicon MOSFETs have been also investigated.

How switching and conduction losses matter is determined by the frequency. On low frequency, there are not too many switches per unit of time, so the best MOSFET for would be the one with lower $R_{DS}$. But as frequency increases, switching losses grow as well to a point where they are bigger than conduction losses. With high frequencies, the ideal MOSFET is the one with lower $E_{off}$.

![Figure 69 Comparison of Eoff of diverse MOSFETs at different drain-currents.](image)
The graph has the selection of the devices that have higher maximum current. MOSFET with the lower $R_{DS}$ is C2M0025120D from CREE. And as it is shown in the graph, MOSFET with lower $E_{off}$ at any drain-current is C3M0065090D.

![Design space zone for C2M0025120D](image1)

![Design space zone for C3M0065090D](image2)

The design zone of C3M0065090D is much more restrictive than the design space of C2M0025120D. On the final converter configuration these limitations are essentials.

On single phase, as it is shown in the figures above, it requires more number of parallel devices for not overcoming the maximum current.
6.1.2. LOW SIDE TRANSITOR IN PRIMARY BRIDGE

MOSFET with less Drain-Source Resistive is again C2M0025120D from CREE. So, four parallel MOSFETs of this kind are placed per low side.

6.1.3. TRANSISTORS IN SECONDARY BRIDGE

With 28V of voltage there is the possibility for GaN, in addition to Silicon and Silicon Carbide technologies. The best option is the one with better behavior conducting, as no hard-switchings take place, and for this application’s frequency reverse recovery losses are insignificant.

Higher number of parallel MOSFET in secondary implicates lower Conducting losses. Ideally it is desirable that this number to be the higher possible. But, there are some disadvantages, application forces to have high power density, and manufacturing would become harder. The number of MOSFET per side of the secondary bridge depends on the number of converters.

<table>
<thead>
<tr>
<th>Converters in Parallel</th>
<th>MOSFET in Parallel per Side in secondary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>4</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 6 MOSFET in parallel per side in secondary depending on parallel converters.

Same frequency (100kHz) is taken to compare different devices in secondary. This table has been designed trying to have a total of 32 secondary devices in every converter, in order to have a similar volume. Because of that, the multiplication of the number of converters times the number of MOSFET per side is the closest possible to eight. Maximum devices per side is four. Because of that, the number of parallel transistors per converter has to be close to eight.

The first device is a GaN MOSFET. On these devices, there are no reverse recovery losses.
Actually, as the secondary bridge has a different number of MOSFET depending on the number of converters, design space is even smaller for the table ahead. At least two GaN MOSFETs per side are needed in order to not exceed their maximum current.

The diode chosen is the one that endures the highest current. Even so, these devices do not break with 16 parallel diodes or more. This number would worsen a lot power density. Anyway, their losses are the worst compared with any other device.
The last option is a Silicon MOSFET. It is available for any number of converters in parallel and its losses are lower than with the GaN MOSFET. In this case, there are reverse recovery losses, as results of the high slope on current waveform. However, it is impossible to operate where these losses are high because control is unstable there.
The conclusion is that the best device for the secondary bridge is the Silicon MOSFET AUIRFS8409-7P, from INFINEON.

### 6.2. Switching vs Conduction Losses in Primary High Transistors

The next step is finding the frequencies when switching losses are lower than conduction losses and contrariwise. And it is determined by the MOSFETs used.
Following graphs contrast primary losses at different frequencies, 10kHz and 100kHz. They only gather information from C2M0025120D and C3M0065090D, the best MOSFETs on conduction and switching respectively.

With turn ratios close to 14:1, conduction and switching losses are lower in primary as current peak is also lower. Anyway, reverse recovery losses are bigger.

![Current on Primary](image)

**Figure 78** Contrast between current waveform in primary with a turn ratio of 1:1 and another one of 14:1.

Losses are calculated for the number of MOSFETs in high transistors that ensures the lower losses possible in every frequency.

At 10 kHz:

![Primary Losses (W) C3M0065090D](image)

**Figure 79** Primary losses of C3M0065090D. Frequency = 10kHz.
At frequencies close to 10kHz, with a low number of converters the best conduction MOSFET has lower losses. With a high number of converters, they are about the same.

At 100kHz:
At frequencies close to 100kHz, switching losses are predominant over conduction losses. Consequently, with no matter the number of converters, lower losses are reached with the best MOSFET on switching.

### 6.3. INDUCTANCE

Slopes on the current waveform determine the inductance required in order to obtain the state-times desired. Their relationship is indirect as it is shown in paragraph (Principles of Operation), a higher slope needs a lower inductance.

With low frequencies, the time demanded for reaching the current peak that delivers on the output the correct power is bigger than in high frequencies. Consequently, slope is smaller and inductance bigger in the first scenario than in the second one.
Using the leakage inductance of the transformer saves space from an external inductance. The problem is that it is not viable to create the transformer having in mind the final leakage inductance. Hence, with the final result is feasible to adjust the inductance modifying the frequency.

In a well-fabricated transform, leakage inductance is normally set around 10-20 µH. Therefore, frequency of operation is around 100kHz.

6.4. SINGLE PHASE VS MULTIPHASE CONVERTER

Discontinuous current forces this topology to have very restricted features in order to obtain a reasonable efficiency. With a single phase converter frequency has to be low in order to obtain an inductance close to the leakage inductance of the transformer.

![Inductance Single Phase](image)

Figure 85 Inductance required in single phase converter depending on turn ratio. Frequency = 30 kHz.

The final turn ratio has to be located between 5:1 and 9:1. Lower turn ratios have low efficiencies and high turn ratios have a lack of stability of their control.

![Design Space](image)

Figure 86 Design space of a single phase converter. Frequency = 30 kHz
Furthermore, reverse recovery losses grow at turn ratios close to 14:1.

![Reverse Recovery Losses](image)

*Figure 87 Reverse recovery losses depending on turn ratio. Frequency = 30 kHz*

And although efficiency is not bad, system is so bounded that any change on the transformer, on switches, on the output filter or on any part of the system, converter would not be well-integrated and waveforms would not be as expected. Considering the losses of the transformer, this efficiency would be worse.

![Efficiency](image)

*Figure 88 Efficiency depending on turn ratio. Frequency = 30 kHz (I)*
Multiphase converters allow to have another degree of freedom that makes converter more robust and helps to adjust the inductance in order to take benefit from the leakage inductance of the transformer.

Even better efficiencies are able to achieve.
6.5. CAPACITANCE

Capacitance is determined by the number of converters and turn ratio. With a single converter and a frequency of 100kHz, ripple of current waveform at the output does not change with the turn ratio. Therefore, setting the output voltage at 10 per cent, capacitance demanded is 160 μF.

But with more converters, different turn ratios produce different waveforms at the output, and consequently ripple changes as well (Interleaving of Multiphase Converters). Ripple drops and capacitance thus is not forced to be that big. Its size changes with turn ratio as well.

Figure 91 Capacitance depending on number of converters. Frequency = 100kHz. (I)

Figure 92 Capacitance depending on number of converters. Frequency = 100kHz. (II)
In some turn ratios capacitance placed on the filter could be zero. Duty cycles obtained by this turn ratios allow these results, as total current is correctly balanced by the addition of all the phased currents.

For example, in a two-phase converter, if we do not take account of d3 time, the Dead-Time, ripple is zero in the case that the duty cycle is half of the period. Adding another converter would increase ripple.

**TOTAL CURRENT**

![Current Waveform](image)

*Figure 93 Output current waveform when duty cycle = 0.5.*

As a result, contradicting what would be a more logical thought, at some turn ratios less converters have less ripple.

### 6.6. MAGNETIZING INDUCTANCE

Losses in transformer are reduced if switching is produced with ZVS. This is achieved if energy stored in MOSFETs’ $C_{oss}$ capacitor is lower than the magnetizing energy on the transformer. Magnetizing inductance has to be chosen in order to satisfy this requirement.

Due to this magnetizing current, current on dead-times is not zero. As a consequence, ZCS on MOSFETs is not achieved. Therefore, switching losses increase in configurations where high magnetizing current is needed.

This problem is not specific from this topology. Normally, in order to achieve ZCS, no ZVS is possible. And in order to achieve ZVS, no ZCS is possible.

![Magnetizing Current](image)

*Figure 94 Magnetizing current waveform referred to primary side of the transformer.*
Total magnetizing current is divided and flows through both sides of the transformer. Resistances in primary and secondary MOSFETs determine how much current circulates on the side. Anyway, magnetizing current on any side has to be higher than the energy stored on MOSFETs, as explained ahead. As a result, the side that requires the higher total magnetizing current sets the minimum possible.

Frequency affects on magnetizing current. With a higher frequency, a higher magnetizing current and a lower magnetizing inductance are demanded.

![Figure 95 Minimum total magnetizing current to achieve ZVS in primary.](image1)

![Figure 96 Minimum total magnetizing current to achieve ZVS in secondary.](image2)

Calculations are made in the primary side. Consequently, turn ratio modifies this current as well as it affects the value of secondary resistances in primary. MOSFET chosen for high transistors of primary bridge is C2M0025120D. At turn ratios higher than 4:1 (5:1, 6:1...) secondary side requires a higher magnetizing current. At the rest of turn ratio, it is the opposite; primary side requires a higher magnetizing current.
Figure 97 Maximum magnetizing inductance to achieve ZVS in primary.

Figure 98 Maximum magnetizing inductance to achieve ZVS in secondary.
BEST MULTIPHASE CONFIGURATIONS
7. BEST MULTIPHASE CONFIGURATIONS

After studying the different parameters for optimizing the converter, frequency should vary around 100kHz as leakage inductance on the transformer is situated between 10 and 20 µH. Interleaving also seems as a good idea as it makes converter more robust and efficient.

Best MOSFET for conducting is C2M0025120D, and for switching is C3M0065090D. But the second one is very bounded, it only runs for a few turn ratios and parallel converters. On high transistors of the primary bridge one of these kinds of MOSFET is going to be placed.

Figure 99 Design zone due to maximum drain-source current of devices and stable control. (I)

Figure 100 Design zone due to maximum drain-source current of devices and stable control. (II)
As one available area is a lot bigger than the other, MOSFET chosen for high transistors in primary bridge is C2M0025120D. This way, converter is even more robust. The number of parallel MOSFET that reaches the lowest losses is one.

![Primary MOSFETs Optimum C2M0025120D](image)

Figure 101 Optimum number of high MOSFETs on high side of primary bridge.

On low transistors of the primary bridge, devices placed are C2M0025120D, the best conducting MOSFET. Finally, in order to make a more robust converter, just one MOSFET is placed in these side. On every side of secondary bridge, devices placed are Silicon MOSFET, AUIRFS8409-7P.

Capacitor chosen for output filter is B32643B0394J1040 from EPCOS. It is a film capacitor of 0.39 µF. Connecting in parallel different capacitors it is possible to achieve the capacitance desired. Parallelizing also reduces ripple from the internal inductance and resistance of the capacitor. It is good to remember that sometimes more converters do not imply less ripple as it is explained in paragraph (Interleaving of Multiphase Converters). **Only integer turn ratios** are allowed to be chosen (2:1, 3:1, etc.). There are some good configurations for the converter:

![Efficiency HIGH C2M0025120D LOW C2M0025120D](image)

Figure 102 Different possible configurations.
• First Option: turn ratio between 4:1 and 6:1, and more than 4 converters. The best configuration regarding capacitance as well is turn ratio equal 5:1 and six converters. Then, at least one capacitor is needed. It is feasible to take advantage of the leakage inductance of the transformer.

![Figure 103 Different possible inductances.](image)

![Figure 104 Region situated the capacitance demanded on output at 100kHz.](image)
Figure 105 Number of capacitors depending on turn ratio and number of converters.

Maximum magnetizing inductance and minimum magnetizing current demanded on this option can be read on the following table. There is information from different frequencies, as with them converter could have a better efficiency counting the losses of the transformer.

<table>
<thead>
<tr>
<th>FREQUENCY (Hz)</th>
<th>MAGNETIZING CURRENT (A)</th>
<th>MAGNETIZING INDUCTANCE (uH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100k</td>
<td>1,328449328</td>
<td>237,12</td>
</tr>
<tr>
<td>110k</td>
<td>1,461294261</td>
<td>195,97</td>
</tr>
<tr>
<td>120k</td>
<td>1,594139194</td>
<td>164,67</td>
</tr>
<tr>
<td>130k</td>
<td>1,726984127</td>
<td>140,31</td>
</tr>
<tr>
<td>140k</td>
<td>1,85982906</td>
<td>120,98</td>
</tr>
<tr>
<td>150k</td>
<td>1,992673993</td>
<td>105,39</td>
</tr>
<tr>
<td>160k</td>
<td>2,125518926</td>
<td>92,62</td>
</tr>
<tr>
<td>170k</td>
<td>2,258363858</td>
<td>82,05</td>
</tr>
<tr>
<td>180k</td>
<td>2,391208791</td>
<td>73,18</td>
</tr>
<tr>
<td>190k</td>
<td>2,524053724</td>
<td>65,68</td>
</tr>
<tr>
<td>200k</td>
<td>2,656898657</td>
<td>59,28</td>
</tr>
</tbody>
</table>

Table 7 Maximum inductance and minimum magnetizing current demanded at different frequencies. Turn ratio = 5:1.

- Second Option: turn ratio between 6:1 and 9:1, and between 2 and 4 converters. Both best configurations regarding capacitance have 7:1 of turn ratio, but one has two and the other four converters. Without taking into account noise and difficulties in the building that could break MOSFETs, the best configuration would be the one with less converters. But, for security, the configuration preferred is the other with four converters, that also has less ripple. Again, there has to be at least only one capacitor on output filter, and leakage inductance of the transformer is enough. No external inductance is needed.
If float turn ratios were allowed, at some point the number of capacitors with a specific number of converters would be zero. For example, if turn ratio 7.14:1 was allowed, no capacitors would be needed with 2 parallel converters.
<table>
<thead>
<tr>
<th>FREQUENCY (Hz)</th>
<th>MAGNETIZING CURRENT (A)</th>
<th>MAGNETIZING INDUCTANCE (µH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100k</td>
<td>0.930392963</td>
<td>473.99</td>
</tr>
<tr>
<td>110k</td>
<td>1.023432259</td>
<td>391.73</td>
</tr>
<tr>
<td>120k</td>
<td>1.116471556</td>
<td>329.16</td>
</tr>
<tr>
<td>130k</td>
<td>1.209510852</td>
<td>280.47</td>
</tr>
<tr>
<td>140k</td>
<td>1.302550148</td>
<td>241.83</td>
</tr>
<tr>
<td>150k</td>
<td>1.395589445</td>
<td>210.66</td>
</tr>
<tr>
<td>160k</td>
<td>1.488628741</td>
<td>185.15</td>
</tr>
<tr>
<td>170k</td>
<td>1.581668037</td>
<td>164.01</td>
</tr>
<tr>
<td>180k</td>
<td>1.674707333</td>
<td>146.29</td>
</tr>
<tr>
<td>190k</td>
<td>1.76774663</td>
<td>131.30</td>
</tr>
<tr>
<td>200k</td>
<td>1.860785926</td>
<td>118.50</td>
</tr>
</tbody>
</table>

Table 8 Maximum inductance and minimum magnetizing current demanded at different frequencies. Turn ratio = 7:1.

- Third option: turn ratios between 6:1 and 9:1, and more than four converters. This is a viable option that would require an external inductance. It would drop power density. On the other hand, this option has better efficiency.

Anyway, increasing frequency allows to obtain around this configurations inductances close to the leakage inductance of the transformer. Efficiency slightly drops, but transformer can be smaller and have less losses.
At 200kHz, the best turn ratio possible is 8:1. Considering ripple on output, the worst number of converters is five, as it would require at least two capacitors. But in order to have the less weight possible, it is chosen is six converters. Anyway, it is possible to vary this number depending on the leakage inductance of transformers.
Figure 111 Region situated the capacitance demanded on output at 200kHz.

Figure 112 Number of capacitors depending on turn ratio and number of converters.

<table>
<thead>
<tr>
<th>FREQUENCY (Hz)</th>
<th>MAGNETIZING CURRENT (A)</th>
<th>MAGNETIZING INDUCTANCE (µH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>100k</td>
<td>0,833211233</td>
<td>604,89</td>
</tr>
<tr>
<td>110k</td>
<td>0,916532357</td>
<td>499,91</td>
</tr>
<tr>
<td>120k</td>
<td>0,99985348</td>
<td>420,06</td>
</tr>
<tr>
<td>130k</td>
<td>1,083174603</td>
<td>357,92</td>
</tr>
<tr>
<td>140k</td>
<td>1,166495726</td>
<td>308,62</td>
</tr>
<tr>
<td>150k</td>
<td>1,24981685</td>
<td>268,84</td>
</tr>
<tr>
<td>160k</td>
<td>1,333137973</td>
<td>236,28</td>
</tr>
<tr>
<td>170k</td>
<td>1,416459096</td>
<td>209,30</td>
</tr>
<tr>
<td>180k</td>
<td>1,49978022</td>
<td>186,69</td>
</tr>
<tr>
<td>190k</td>
<td>1,583101343</td>
<td>167,56</td>
</tr>
<tr>
<td>200k</td>
<td>1,666422466</td>
<td>151,22</td>
</tr>
</tbody>
</table>

Table 9 Maximum inductance and minimum magnetizing current demanded at different frequencies. Turn ratio $= 8:1$. 
As it is explained ahead, this study of the converter does not include the optimization of the transformer and does not calculate its losses at every frequency and turn ratio. Once both studies are joined together best configuration can be determined more accurately.
CONCLUSIONS
8. CONCLUSIONS

The goal of this project was the analysis and design of a DC/DC converter for aircraft applications. This converter is part of the output of an isolated rectifier unit for the distribution of electric power inside the airplane. For reducing fuel consumption of the plane, the DC/DC converter had to be as efficient and lightweight as possible. It had to be isolated as well. As a result, security was increased.

This work focuses on developing a methodology for finding the design space of the converter. Anyway, this methodology could be followed as well for finding the best configurations of any converter. Different parameters are studied for drawing this design space. However, it is not possible to determine which configuration is the best as the design of the transformer had not been approached. The complexity of the design of the transformer allows it to be developed in another final degree project.

Topologies that fit the specifications of the converter are half-bridge and full-bridge. Full-bridge is the chosen topology because transformer is simpler. Inside full-bridge there are different topologies. Each of them has advantages and disadvantages. Finally, the Triangular Current Waveform Full-Bridge has been chosen. In the secondary side, a full-bridge rectifier has been chosen.

The Triangular current waveform full-bridge is a topology that uses an inductance to achieve a triangular current waveform. It is desirable to take benefit of the leakage inductance of the transformer in order to reduce the volume. This topology has ZCS in the primary switches. It also minimizes the reverse recovery effect on the secondary bridge. The full-bridge topology needs a single magnetizing component and a single core. Therefore, transformer is simpler than in other topologies. Control is easier as well.

After every waveform cycle, a dead time has been added in order to have zero current while switching the devices, ZCS.

The parameters taken into account in drawing the design space of the converter are:

- Frequency
- Inductance
- Turn ratio
- Number of parallel devices in secondary and primary
- Diodes or MOSFET in secondary
- Number of parallel converters
- Stability
- Maximum current on devices

Frequency, inductance and turn ratio are related. The inductance needed on the topology is determined by the frequency and the turn ratio. Frequency has been chosen in order to take advantage of the leakage inductance of the transformer. A high frequency reduces losses and the size of the transformer.

Diodes have low maximum current and high losses. Therefore, in secondary, devices are MOSFET. At the frequency chosen, on the high side of the primary bridge switching losses predominate upon conduction losses. Consequently, one transistor has lower losses. On the down side of primary bridge, there are only conduction losses and four parallel transistors are placed. In the secondary there are mainly conduction losses and the number of parallel converters determines the number of devices in secondary.
Devices in primary side are 1200V SiC MOSFET with a low drain-source resistance (25mΩ at 25°C) and maximum current of 90A. There are four parallel MOSFETs in primary low side and only one transistor on the high side. In secondary, devices are 40V Silicon MOSFETs with a drain-source resistance is 0.75 mΩ at 25°C and maximum current of 240A. On this side the number of parallel devices depends on the number of parallel converters.

<table>
<thead>
<tr>
<th>Converters in Parallel</th>
<th>MOSFET in Parallel per Side in secondary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
</tr>
<tr>
<td>2</td>
<td>4</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
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<td>4</td>
<td>3</td>
</tr>
<tr>
<td>5</td>
<td>2</td>
</tr>
<tr>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>7</td>
<td>1</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 10 MOSFET in parallel per side in secondary depending on parallel converters.

Single phase forces converter to perform with low frequencies and high turn ratios. Anyway, as there is a stability problem with duty cycles higher than 0.67, turn ratio can not be 10:1 or higher. Maximum current on devices is another restriction to be fulfilled. As a result, in single phase converter it is needed two parallel devices in primary high side. Furthermore, capacitance on output is much higher. Best configuration for single phase converter is:

<table>
<thead>
<tr>
<th>FREQ (kHz)</th>
<th>TURN RATIO</th>
<th>PAR CONV</th>
<th>CAPACITANCE (μF)</th>
<th>MAG. CUR. *</th>
<th>EFFICIENCY</th>
<th>LOSSES (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30</td>
<td>9:1</td>
<td>1</td>
<td>531.46</td>
<td>0.23A</td>
<td>0.974</td>
<td>272</td>
</tr>
</tbody>
</table>

Table 11 Single phase converter configuration

Figure 113 Design space of a single phase converter.
In multiphase converter efficiency and volume increase. Anyway, cooling systems can be smaller and simpler. Output capacitance changes as well. At some turn ratios capacitance is reduced with more parallel converters, and in others, it is increased. Capacitor chosen is B32643B0394J1040 from EPCOS. It is a film capacitor of 0.39 µF.

In this case, there are the same restrictions as in single phase converter due to stability and maximum current on devices. Best configurations for multiphase converter are:
The magnetizing inductance of the transformer has to be correctly chosen in order to obtain enough magnetizing current on both sides of the transformer for achieving ZVS on it. This magnetizing current causes that in dead times current is not zero, and therefore there is no ZCS.

As it is explained ahead, it is not possible to determine which is the best solution. Future research lines on the transformer will allow to choose the configuration with lower volume, weight and losses.

**FUTURE RESEARCH LINES**

The first and immediate future research line of this work is designing the transformer on the converter. Once this is done, it is possible to compare this topology with others. Possible better topologies could be:
• A continuous current mode full-bridge converter. This topology has more hard-switchings. But switching losses on one device are lower than on one device on discontinuous current mode full-bridge converter.

• The Resonant Dual Active Bridge, where there are no hard-switchings.

Another future line is researching for a more stable controller, that could be control any duty cycle with any number of parallel converters.
TEMPORAL PLANNING AND BUDGET
9. TEMPORAL PLANNING AND BUDGET

The time taken on every task of this project is gathered on the following table:

<table>
<thead>
<tr>
<th>TASK</th>
<th>TIME (days)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INTRODUCTION TO TOPOLOGY</td>
<td>5</td>
</tr>
<tr>
<td>LIST OF PRIMARY BRIDGE DEVICES</td>
<td>10</td>
</tr>
<tr>
<td>LIST OF SECONDARY BRIDGE DEVICES</td>
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<td>10</td>
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<tr>
<td>MULTIPHASE CONVERTER; OPTIMIZATION OF INDUCTANCE</td>
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The average time taken in this project is three hours per day. Total time spent is 519 hours.
Taking into account that the average net salary of a junior engineer in Spain is 1917 Euros per month, and the standard workday has 160 hours per month, salary is estimated to 12 Euros per hour. [30]

As a result, the cost of the engineer developing this project is 6228 Euros.

It is also needed to take into account the work dedicated by the cotutor and the tutor of the project:

- 10% of the corresponding work of the cotutor (PhD student): 102.9 hours, 14 Euros per hour: 1440 Euros.
- 5% of the corresponding work of the tutor (university teacher): 51.45 Euros, 16.25 Euros per hour: 840 Euros.

Some programs used for developing this project and their licenses include more costs: PSIM and Simploerer.

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<tr>
<td><strong>Engineer (Student)</strong></td>
<td>6228 Euros</td>
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<tr>
<td><strong>Cotutor</strong></td>
<td>1440 Euros</td>
</tr>
<tr>
<td><strong>Tutor</strong></td>
<td>840 Euros</td>
</tr>
<tr>
<td><strong>PSIM</strong></td>
<td>50 Euros</td>
</tr>
<tr>
<td><strong>ANSYS SIMPLORER</strong></td>
<td>440 Euros</td>
</tr>
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<td><strong>TOTAL</strong></td>
<td>8998 Euros</td>
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Table 16 Total cost

The following GANT diagram represents the distribution of tasks through the time.
ANALYSIS AND DESIGN OF A DC/DC CONVERTER

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[21] INFINEON. *Introduction to Infineon's Combined Gallium Nitride-Based Technologies*.


[24] CREE. *C2M0025120D Data Sheet*.


[27] CREE. *C5D0065D*. Data Sheet.


[31] ETSII (Approved in 2014). *Proyecto Fin de Carrera, Trabajo Fin de Grado y Trabajo Fin de Master*. 

GLOSSARY
# 13. Glossary

<table>
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<tr>
<th>B</th>
<th>Bipolar Junction Transistor</th>
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</tr>
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<tr>
<td>D</td>
<td>derating</td>
<td>Operating at lower values than rated specifications to prolong its life.</td>
</tr>
<tr>
<td>I</td>
<td>Insulated Gate Bipolar Transistors</td>
<td>41</td>
</tr>
<tr>
<td>L</td>
<td>Latchup</td>
<td>Failure mechanism of CMOS integrated circuits characterized by excessive drain coupled with functional failure, parametric failure and/or device destruction.</td>
</tr>
<tr>
<td>M</td>
<td>MOSFET</td>
<td>Metal oxide semiconductor Field-effect transistor</td>
</tr>
<tr>
<td>R</td>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>Z</td>
<td>ZCS</td>
<td>Zero Current Switching</td>
</tr>
<tr>
<td></td>
<td>ZVS</td>
<td>Zero Voltage Switching</td>
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ANNEX
14. ANNEX

MATLAB SCRIPTS

SINGLE PHASE CURRENT WAVEFORM

```matlab
Pout=10000; 
vectVin=[400] ; 
Vout=28; 
vectN1 = [1,3,5,7,14]; 
vectfrec=[100000]; 
d3=0.05; 
d33 = d3*2; 

figure 
for ifs3=1:length(vectN1) 
    N1=vectN1(ifs3) 
    N2 = 1; 
    n=N2/N1; 
    for ifs2=1:length(vectfrec) 
        frec=vectfrec(ifs2) 
        fs=frec*2; 
        T=1/frec; 
        for ifs=1:length(vectVin) 
            Vin=vectVin(ifs); 
            d11=Vout*(1-d33)/(n*Vin); 
            d1=d11/2; 
            d2=d22/2; 
            R=(Vout*Vout)/Pout; 
            Iavg2= Pout/Vout; 
            Ld=((n*Vin-Vout)*d11*d11+Vout*d22*d22)/(2*Iavg2*fs); 
            Ipk2=(n*Vin-Vout)*d11/(Ld*fs); 
            Ipkl=n*Ipkl 
            Fsamp = 1e7*frec/10^4; 
            T2 = 1/Fsamp; 
            L = 1000; 
            t = (0:L-1)*T2; 
            cont=0; 
            y= zeros(1,length(t)); 
            for i=1:length(t) 
                if t(i) <= 1/frec*0.5 
                    if t(i) <= d1/frec 
                        y(i)=Ipkl/(d1/frec)*t(i); 
                    elseif and ((t(i)<=d1+d2)/frec),(t(i)>d1/frec)) 
                        y(i)=-Ipkl/(d2/frec)*t(i)+Ipkl*(d1+d2)/d2; 
                    else 
                        y(i)=0; 
                    end 
                end 
            end 

% Turn ratio 
% Frequency 
% Frequency of half cycle 
% Duty cycle of half cycle 
% Average current in secondary 
% Equation explained in Principle of Operation.
```
\( y(i) = 0; \)
else
\( t(i) \leq 1/frec \cdot (d1+0.5) \)
\( y(i) = Ipk1/(d1/frec) \cdot (t(i) - 1/frec \cdot 0.5); \)
elseif and \((t(i) \leq 1/frec \cdot (d1+d2+0.5)),(t(i) > 1/frec \cdot (d1+0.5))\)
y(i) = Ipk1/(d2*1/frec) \cdot (t(i) - 1/frec \cdot 0.5) - Ipk1*(d1+d2)/d2;
else
y(i) = 0;
end
end

% In an array different positions of current waveform are stored.
plot(t*10^6,y,'LineWidth',2)
hold on
title('Current Primary','FontName','Arial','FontSize',17)
ylabel('A','FontName','Arial','FontSize',14)
xlabel('usg','FontName','Arial','FontSize',14)
end
end
end

legend('1:1','3:1','5:1','7:1','14:1')

**SINGLE PHASE LOSSES CALCULATION**

\( P_{out\,Tot}=10000; \)
\( V_{in}=400; \)
\( V_{out}=28; \)
\( PAR = 1; \)
\( P_{out} = P_{out\,Tot}/PAR; \)
\( vectN1 = [1:1:14]; \)
\( N2 = 1; \)
\( frec=100000; \)
\( fs=frec*2; \)
\( T=1/frec; \)
\( vectMp1=[1:0.5:20]; \)
\( d3=0.05; \)
\( d33 = d3*2; \)
figure

for ifis=1:length(vectN1)
  N1=vectN1(ifi);
  n=N2/N1;

for ifis4=1:length(vectMp1)
  MP1=vectMp1(ifi)
  MP2=16;
  d11=Vout*(1-d33)/(n*Vin);
  d22=1-d11-d33;
  d1=d11/2;
  d2=d22/2;
  R=(Vout*Vout)/Pout;
ANÁLISIS Y DISEÑO DE UN CONVERTIDOR DC/DC

PABLO PÉREZ GARCÍA

\[ I_{avg} = \frac{P_{out}}{V_{out}}; \]
\[ \text{vectLd(ifs)} = \frac{((n \times V_{in} - V_{out}) \times d_{11} \times d_{11} + V_{out} \times d_{22} \times d_{22})}{2 \times I_{avg} \times f_{s}} \]
\[ L_{d} = \text{vectLd(ifs)} \]
\[ I_{pk2} = \frac{(n \times V_{in} - V_{out}) \times d_{11}}{L_{d} \times f_{s}}; \]
\[ I_{pk1} = n \times I_{pk2} \]

\% MOSFET modules
\[ R_{mosfet} = 0.0325; \]
\[ a_{off} = 0.0002334; \]
\[ b_{off} = 0.0021118; \]
\[ c_{off} = 0.0427; \]
\% Switching Losses
\[ E_{off} = (a_{off} \times (I_{pk1})^2 + b_{off} \times (I_{pk1}) + c_{off}) \times 10^{-3}; \]
\[ \text{vectPoffH1(ifs4)} = (E_{off}) \times f_{rec} \times MP1 \times \text{PAR}; \]
\% Conduction Losses
\[ \text{vectPcondH1(ifs4)} = R_{mosfet} \times I_{pk1} \times I_{pk1} \times d_{1} / (3 \times MP1) \times \text{PAR} \]
\[ \text{vectPcondL1(ifs4)} = R_{mosfet} \times I_{pk1} \times I_{pk1} \times (d_{1} + 2 \times d_{2}) / (3 \times MP1) \times \text{PAR} \]
\[ \text{vectPhigh1(ifs4)} = 2 \times (\text{vectPcondH1(ifs4)} + \text{vectPoffH1(ifs4)}); \]
\[ \text{vectPlow1(ifs4)} = 2 \times (\text{vectPcondL1(ifs4)}); \]
\[ \text{vectPmosfet1(ifs4)} = 2 \times (\text{vectPcondH1(ifs4)} + \text{vectPoffH1(ifs4)} + \text{vectPcondL1(ifs4)}); \]
\% MOSFET Secundario
\[ R_{mos2} = 0.000825; \]
\[ \text{vectPmosfet2(ifs4)} = 4 \times R_{mos2} \times I_{pk2} \times I_{pk2} \times (d_{1} + d_{2}) / (3 \times MP2) \times \text{PAR} \]
\% RENDIMIENTO
\[ \text{vectRendimiento(ifs4)} = \frac{P_{out}}{P_{out} + \text{vectPmosfet1(ifs4)} + \text{vectPmosfet2(ifs4)}} \]
\[ t_{2} = (0:length(\text{vectMp1}) - 1); \]
\end

MULTIPHASE CONVERTER

\% FIRST PART STORES IN A MATRIX THE NUMBER OF PARALLEL MOSFET IN PRIMARY HIGH SIDE FOR LOWER LOSSES
\[ PoutTot=10000; \]
\[ Vin=400; \]
\[ Vout=28; \]

PABLO PÉREZ GARCÍA
PAR = [1:1:8]; % Number of parallel converters
vectN1 = [1:1:14];
vectM1 = [1:1:20];

N2 = 1;
freq = 100000;
fs = freq*2;
T = 1/freq;
d3 = 0.05;
d33 = d3*2;

%% MOSFET PRIMARY
MOSFET = 'C2M0025120D'

Rmosfet = 0.0325;
RmosfetH = 0.0325;
RmosfetL = RmosfetH;

yoff = 0
zoff = 0
aoff = 0.2385;
boff = -2.483;
coff = 53.02;
uni_off = 10^(-6);

aon = 0.0003386;
bon = 0.003804;
con = 0.05711;

Qrr_data1 = 406;
V_data1 = 800;
Slope_data1 = 1000;

% Reverse recovery data
Qrr_data1 = Qrr_data1*10^(-9);
Slope_data1 = Slope_data1*10^6;

CossH = 400*10^-12;
CossL = 400*10^-12;

MP1_low = 1;
IlimH = 60;
IlimL = IlimH;

%% MOSFET SECUNDARY
MOSFETS = 'AUIRFS8409-7P';

Rmos2 = 0.000825;

MP2_1 = [4, 4, 3, 3, 2, 2, 1, 1];

Qrr_data2 = 34;
V_data2 = 28;
Slope_data2 = 100;
Qrr_data2 = Qrr_data2*10^(-9);
Slope_data2 = Slope_data2*10^6;
CossS = 4000*10^-12;
IlimS = 240;

for ifs1=1:length(PAR)
    Pout = PoutTot/PAR(ifs1);
    MP2=MP2_1(ifs1);
end

for ifs=1:length(vectN1)
    N1=vectN1(ifs);
    n=N2/N1;
end

for ifs4=1:length(vectMp1)
    MP1=vectMp1(ifs4);
end

d11=Vout*(1-d33)/(n*Vin);
d22=1-d11-d33;
d1=d11/2;
d2=d22/2;
R=(Vout*Vout)/Pout;
Iavg2= Pout/Vout;
vectLd(ifs)=((n*Vin-Vout)*d11*d11+Vout*d22*d22)/(2*Iavg2*fs);
Ld=vectLd(ifs);
Ipk2=(n*Vin-Vout)*d11/(Ld*fs);
Ipkl=n*Ipk2

%% MOSFET PRIMARY
Eoff= (yoff*(Ipkl)^4+zoff*(Ipkl)^3+aoff*(Ipkl)^2+boff*(Ipkl)+coff)*uni_off;
vectPoffH1(ifs4) = (Eoff)*frec*MP1*PAR(ifs1);
vectPcondH1(ifs4) = Rmosfet*Ipkl*Ipkl*d1/(3*MP1)*PAR(ifs1);
vectPcondL1(ifs4) = Rmosfet*Ipkl*Ipkl*(d1+2*d2)/(3*MP1)*PAR(ifs1);
vectQrr1(ifs4) = Qrr_data1*Vin*Ipkl*fs*PAR(ifs1)/(V_data1*Slope_data1*d22);
vectPrev1(ifs4) = vectQrr1(ifs4)*Vin*fs;
vectPhigh1(ifs4) = 2*(vectPcondH1(ifs4)+vectPoffH1(ifs4)) + vectPrev1(ifs4);
vectPlow1(ifs4) = 2*(vectPcondL1(ifs4));
vectPmosfet1(ifs4) = 2*(vectPcondH1(ifs4)+vectPoffH1(ifs4)+vectPcondL1(ifs4))+ vectPrev1(ifs4);

%% MOSFET SECONDARY
vectPmosfet2(ifs4) = 4*(Rmos2*Ipkl2*Ipkl2*(d1+d2)/(3*MP2))*PAR(ifs1);
%% EFFICIENT

vectRendimiento(if4) = Pout/(Pout + vectPmosfet1(if4) + vectPmosfet2(if4));
t2=(0:length(vectMp1)-1);
end

%% MINIMUM LOSSES; THIS IS THE MATRIX WHERE NUMBER OF PARALLEL MOSFETS DEPENDING ON TURN RATIO AND PARALLEL CONVERTERS IS STORE

Minimo(if1, if4)=find(vectPhigh1==min(vectPhigh1));
end
end

%% NEW PROGRAM; CALCULATES LOSSES WITH MINIMUM MOSFETS DEPENDING ON CONFIGURATION

for ifs=1:length(PAR)
    Pout=PoutTot/PAR(ifs);
    R=(Vout*Vout)/Pout;
    Iavg2= Pout/Vout;
    MP2=MP2_1(if4);
    for ifs3=1:length(vectN1)
        N1=vectN1(if4);
        N2 = 1;
        n=N2/N1;
        d11=Vout*(1-d33)/(n*Vin);
        d22=1-d11-d33;
        d1=d11/2;
        d2=d22/2;
        Ld(if4, ifs3)=((n*Vin*Vout)*d11*d11+Vout*d22*d22)/(2*Iavg2*fs);
        Ld_prim(if4, ifs3)=Ld(if4, ifs3)/(n^2);
        MP1 = Minimo(if4, ifs3);
        Ipk2(if4, ifs3)=(n*Vin-Vout)*d11/(Ld(if4, ifs3)*fs);
        Ipk1(if4, ifs3)=n*Ipk2(if4, ifs3);

        % The following was used for drawing the design space of every device
        if Ipk1(if4, ifs3)/MP1 <= IlimH
            IlimiteH(if4, ifs3) = 1;
        elseif
            IlimiteH(if4, ifs3) = 0;
        end;

        if Ipk1(if4, ifs3)/MP1_low <= IlimL
            IlimiteL(if4, ifs3) = 1;
        elseif
            IlimiteL(if4, ifs3) = 0;
        end;
    end
end
if $I_{pk2}(ifs, ifs3)/MP2 \leq I_{limS}$
   \[ I_{limiteS}(ifs, ifs3) = 1; \]
else
   \[ I_{limiteS}(ifs, ifs3) = 0; \]
end;

%% LOSSES PRIMARY

\[
E_{off} = \left( y_{off}(I_{pk1}(ifs, ifs3))^4 + z_{off}(I_{pk1}(ifs, ifs3))^3 + a_{off}(I_{pk1}(ifs, ifs3))^2 + b_{off}(I_{pk1}(ifs, ifs3)) + c_{off} \right) * u_{uni_off};
\]

\[
P_{offH1}(ifs, ifs3) = (E_{off}) * f_{rec} * MP1 * PAR(ifs);
\]

\[
P_{condH1}(ifs, ifs3) = R_{mosfet} * I_{pk1}(ifs, ifs3) * I_{pk1}(ifs, ifs3) * d1/(3*MP1) * PAR(ifs);
\]

\[
P_{condL1}(ifs, ifs3) = R_{mosfet} * I_{pk1}(ifs, ifs3) * I_{pk1}(ifs, ifs3) * (d1 + 2*d2)/(3*MP1\_low) * PAR(ifs);
\]

\[
Phigh1(ifs, ifs3) = 2*(P_{condH1}(ifs, ifs3) + P_{offH1}(ifs, ifs3));
\]

\[
Plow1(ifs, ifs3) = 2*(P_{condL1}(ifs, ifs3));
\]

%% Reverse recovery losses

\[
Q_{rr1}(ifs, ifs3) = Q_{rr\_data1}\_Vin*I_{pk1}(ifs, ifs3)*f*PAR(ifs)/(V_{data1}*Slope_{data1}*d22);
\]

\[
Prev1(ifs, ifs3) = Q_{rr1}(ifs, ifs3)*Vin*f;
\]

\[
P_{mosfet1}(ifs, ifs3) = 2*(P_{condH1}(ifs, ifs3) + P_{offH1}(ifs, ifs3) + P_{condL1}(ifs, ifs3)) + Prev1(ifs, ifs3);
\]

\[
P_{cond}(ifs, ifs3) = 2*(P_{condH1}(ifs, ifs3) + P_{condL1}(ifs, ifs3));
\]

%% CONCLUSION

\[
R\_rendimiento(ifs, ifs3) = P_{outTotal}/(P_{outTotal} + P_{mosfet1}(ifs, ifs3) + P_{mosfet2}(ifs, ifs3));
\]

\[
P\_perdidas(ifs, ifs3) = P_{mosfet2}(ifs, ifs3) + P_{mosfet1}(ifs, ifs3);
\]

end
%% MAGNETIZING CURRENT IS CALCULATED

vectFrec = [100000:10000:200000];

for ifsl=1:length(vectFrec)
    frec = vectFrec(ifsl);
    fs = 2*frec;

for ifs=1:length(vectN1)
    n=N2/8;
    d11=Vout*(1-d33)/(n*Vin);
    d1=d11/2;
    d22=1-d11-d33;

    Ld=((n*Vin-Vout)*d11*d11+Vout*d22*d22)/(2*Iavg2*fs);
    Ipk2=(n*Vin-Vout)*d11/(Ld*fs);

end

%% TOTAL MAGNETIZING CURRENT

Imag_Tot1(ifsl,ifs) = Imag1(ifsl,ifs)/((2*Rmos2/(n^2))/(RmosfetL + RmosfetH + 2*Rmos2/(n^2)));
Imag_Tot2(ifsl,ifs) = Imag2(ifsl,ifs)/((RmosfetL + RmosfetH)/(RmosfetL + RmosfetH + 2*Rmos2/(n^2)));

%% MAGNETIZING INDUCTANCE

Lmag_1(ifsl,ifs) = Vin*d1/(2*frec*Imag_Tot1(ifsl,ifs));
Lmag_2(ifsl,ifs) = Vin*d1/(2*frec*Imag_Tot2(ifsl,ifs));

Qrr2(ifsl,ifs) = Qrr_data2*Vin*Ipk2*fs/(V_data2*Slope_data2*d22);
Prev2(ifsl,ifs) = Qrr2(ifsl,ifs)*Vout*fs;

end

end

MULTIPHASE CAPACITANCE

PoutTot=10000;
Vin=400;
Vout=28;
Iavg22 = PoutTot/Vout
vectPAR = [1:1:8];
vectN1 = [1:1:14];
d3=0.05;
d33 = d3*2;
frec=100000;
fs=frec*2;
\[ T = \frac{1}{f_{rec}} \]

% Ripple on output voltage

\[ d_{Vout} = 0.10; \]
\[ \text{Ripple} = d_{Vout} \times Vout; \]

\[
\text{for} \, \text{ifs}=1:\text{length(vectPAR)} \\
\quad \text{Pout}=\text{PoutTot}/\text{vectPAR(ifs)}; \\
\quad \text{PR}=\text{vectPAR(ifs)}; \\
\quad \text{R}=(\text{Vout*Vout})/\text{Pout}; \\
\quad \text{Iavg2}= \text{Pout}/\text{Vout}; \\
\quad \text{num\_Vin} = 1; \\
\]

\[
\text{for} \, \text{ifs3}=1:\text{length(vectN1)} \\
\quad \text{N1}=\text{vectN1(ifs3)} \\
\quad \text{N2} = 1; \\
\quad \text{n}=\text{N2/N1}; \\
\quad \text{d11}=\text{Vout*(1-d33)/(n*Vin)}; \\
\quad \text{d22}=1-\text{d11-33}; \\
\quad \text{d1}=\text{d11}/2; \\
\quad \text{d2}=\text{d22}/2; \\
\quad \text{Ld}=(\text{n*Vin-Vout})*\text{d11*d11+Vout*d22*d22})/(2*\text{Iavg2*fs}); \\
\]

\[
\text{d11\_multi} = \text{Vout/(n*Vin)}; \\
\text{d22\_multi} = 1 - \text{d11\_multi}; \\
\]

\[
\text{Ld\_multi}=(\text{n*Vin-Vout})*\text{d11\_multi*d11\_multi+Vout*d22\_multi*d22\_multi})/(2*\text{Iavg2*fs}); \\
\]

\[
\text{Ipk2}=\text{(n*Vin-Vout)}*\text{d11}/(\text{Ld*fs}); \\
\text{Ipk1}=\text{n*Ipk2}; \\
\]

% The following calculates slopes on total current (adding the currents from every converter), and then its ripple and waveform.

\[
\text{while} \ (\text{num\_Vin*n*Vin - PR*Vout}) < 0 \\
\quad \text{num\_Vin} = \text{num\_Vin} + 1; \\
\text{end} \\
\]

\[
\text{Slope1} = \text{num\_Vin*n*Vin - PR*Vout}; \\
\text{Slope2} = (\text{num\_Vin-1})*\text{n*Vin - PR*Vout}; \\
\]

\[
\text{d11l}=-\text{Slope2}/(\text{Slope1-Slope2}); \\
\text{A} = \text{Slope1*d11l}/(\text{Ld\_multi*PR*fs}); \\
\text{Ipk22} = (2*\text{Iavg22 + A})/2; \\
\text{Ilow22} = (2*\text{Iavg22} - A)/2; \\
\]

\[
\text{t2} = (\text{Ipk22-Iavg22})*\text{Ld\_multi}/(-\text{Slope2}); \\
\text{delta\_Q2} = (\text{Ipk22-Iavg22})*\text{t2}/2; \\
\text{t1} = (\text{Ipk22-Iavg22})*\text{Ld\_multi/Slope1}; \\
\text{delta\_Q1} = (\text{Ipk22-Iavg22})*\text{t1}/2; \\
\]

% The following matrix stores the capacitance for every number of converters and turn ratio

\[
\text{C(ifs,ifs3)} = (\text{delta\_Q1+delta\_Q2})/\text{Ripple}; \\
\]
end
end