**DEPARTAMENTO DE AUTOMÁTICA, INGENIERÍA ELECTRÓNICA E
INFORMATICA INDUSTRIAL**

ESCUELA TÉCNICA SUPERIOR DE INGENIEROS INDUSTRIALES

CENTRO DE ELECTRÓNICA INDUSTRIAL

*Three Phase Buck type rectifier integrated
with Current Fed Full Bridge*

TESIS DOCTORAL

Autor: José María Molina García

Master en Electrónica Industrial por la Universidad Politécnica de Madrid

Directores: Pedro Alou Cervera

Doctor Ingeniero Industrial por la Universidad Politécnica de Madrid

Jesús Ángel Oliver Ramírez

Doctor Ingeniero Industrial por la Universidad Politécnica de Madrid

2016

Tribunal

Tribunal nombrado por el Mgfco. y Excmo. Sr. Rector de la Universidad Politécnica de Madrid, el día de de 2017.

Presidente:

Vocales:

Secretaria:

Suplentes:

Realizado el acto de lectura y defensa de la Tesis el día de de 2017 en la Escuela Técnica Superior de Ingenieros Industriales de la Universidad Politécnica de Madrid.

Calificación:

EL PRESIDENTE

LOS VOCALES

EL SECRETARIO

**Esta tesis está dedicada
a mis padres José María y Ana
y a mi hermano Sergio.**

Reflexiones

Al concluir esta tesis, concluyo a su vez una etapa importante en mi vida y de ahí que haya decidido expresarlo y compartir lo que ha significado para mí hacer esta tesis. Creo que nunca hubiera imaginado este destino cuando vivía en mi Fuenteálamo natal, “que no es un pueblo normal” donde viví mi infancia, rodeado de familia, amigos, viñas y olivares. Y, sin embargo, en este lluvioso sábado de noviembre, copa de vino a la izquierda y con la noticia del fallecimiento de Fidel Castro, aquí estoy, poniéndole el broche a mi tesis doctoral.

Para mí, la tesis ha sido como una gran aventura, con todos los ingredientes. Cuando llegué a Madrid, era lo más parecido a Alfredo Landa en “Vente para Alemania, Pepe”, aún recuerdo cómo en primera cena de navidad del CEI, invite al excelentísimo rector, Javier Uceda, hoy un gran consejero y amigo mío, a venir a Fuenteálamo a recoger olivas durante la navidad. En fin, dicen que si no te avergüenzas de tus primeros intentos, es que los hiciste demasiado tarde. Bromas aparte, la tesis ha sido un proceso de aprendizaje y lucha contra los elementos, en el que los problemas técnicos a veces han sido más fáciles de resolver que la lucha contra uno mismo. Aunque, como diría un buen amigo mío:

-¿Te cuento una cosa? Nunca dudé que la acabaría.

Y es que esa ha sido mi filosofía durante toda la tesis, poner fe y empeño, quizás a veces, más corazón que cabeza. Es muy complicado enfrentarse a cada reto que aparece en el camino sin mostrar debilidad, pero no es más que una señal de identidad del ser humano. Realizar la tesis te ayuda a ver realmente quien eres, porque la tesis sabrá sacar en algún momento tu lado más salvaje, más romántico, más tozudo, más inteligente, más tonto, más fuerte y más débil.

Pero lo que está claro, es que una vez recorrido el camino, siempre eres más fuerte, más hábil, más perseverante, incluso más creyente y sobretodo si lo has hecho, formando parte de un equipo (el CEI) que yo considero, el mejor del mundo. Si yo fuera Messi, querría jugar en el CEI.

Para concluir, me gustaría añadir, que si vendieran frascos de chistes y buen humor, deberían de dárteles con la matrícula del doctorado, porque son necesarios.

Muchas gracias

Agradecimientos

En primer lugar, me gustaría expresar mi agradecimiento a mis tutores, Pedro y Jesús. Hace ya más de 5 años, cuando empezamos a trabajar juntos en proyectos de investigación y ambos me habéis enseñado, y me seguís enseñando los rincones más escondidos de la electrónica. Ha sido un placer compartir este camino con vosotros, con nuestros congresos y nuestros viajes a reuniones. Muchas gracias a los dos.

I also want to express my gratitude to Professor Paolo Mattavelli, who was a very inspiring person who despite of having a very complex agenda, always found the time to teach me power electronics as well as playing tennis or running with me. Thank you very much for your help. Besides, I would like to express my gratitude to the Electric department of University of Padua, especially to professor Spiazzi, Buso, Corradini and my dear friend Tommaso.

Esta tesis no hubiera sido posible, sin una de las personas que más aprecio y admiro, ya que fue él quien me dió la oportunidad de subir al barco del CEI, allá por 2008. Señor Oscar García. *Katedratic* le estoy muy agradecido por haberme dado esta oportunidad y por enseñarme con paciencia en mis primeros pasos. Eres un ejemplo del que yo presumo de ser amigo.

Por supuesto, también me gustaría darle las gracias a Rafa Asensi, del que he aprendido tanto en los proyectos, como en sus clases magistrales, a las que siempre está dispuesto.

Gracias también a Miroslav, que desde el principio, a pesar de su carácter serbio, nunca ha dudado en ayudarme y enseñarme en cada uno de los retos que la electrónica nos ha puesto por delante, siendo un referente. Espero que podamos seguir trabajando juntos pronto.

Me gustaría agradecer la cercanía con la que Javier Uceda siempre me ha tratado. Sus consejos han sido y siguen siendo algo uno de mis tesoros.

Al equipo del CEI de los que he aprendido muchas cosas, Roberto, Yago, Apa, Jose Antonio, Nieves, Yolanda, Justo, Alfonso, Fernando y Noemí, grandes profesionales. Os deseo lo mejor.

A todos los estudiantes con los que he compartido esta aventura, Julio, Airán, Sisi, Marcelo, Peña, Benoit, Mora, Gabriel, David Aledo, Monica y David, Dejana

y mi compañero de congresos y cervezas, Vladimir, a todos muchas gracias por estos maravillosos años.

Como olvidar a mis amigos, con los que tantas experiencias hemos vivido, desde *Muchismo parties* a cervezas casuales, Dani, Juan, Ruben, Vincenzo, Victor, Carmen, Sanna, Alfonso, Yana, Alfonso (freak) y Varela, todo el tiempo que hemos disfrutado de Madrid juntos, de día y de noche, siempre pertenecerán a una de las épocas más felices de mi vida.

Como no, a mi amigo Eduardo de la Torre, con el que he vivido situaciones de los más divertidas, pero sobretodo, una persona con la que me he reído a carcajadas. Seguramente será porque tiene una risa profunda y tremendamente divertida, o simplemente, porque es Edu.

Ni en el mejor de los sueños, pensaría que alguien con tanta clase, conocimiento, y experiencia me acompañara en este complicado camino que es la tesis como lo ha hecho mi *tita Tere*. A ti, no puedo expresarte todo lo que has hecho por mi durante estos años, y que sigues haciendo siempre con una sonrisa, y a veces con un vino o una cerveza la Virgen. Gracias por cuidarme tanto.

Y por supuesto a Marcos, que sus consejos, siempre van a misa. Como dice Tere, *hazle caso al tito Marcos*.

Gracias a mi buen amigo David Meneses, con el que he tomado los aperitivos más divertidos de mi vida. Nos podían encontrar en la calle Ponzano, los sábados a medio día. Por otro lado, una persona con un vasto conocimiento sobre electrónica y que siempre tuvo un momento para ayudarme.

A mi querido Andresiño, con el que además de compartir piso y aprender gallego, he viajado y vivido experiencias por toda Europa. Gracias por tu apoyo continuo durante toda la tesis, y por esos viajes a Galicia. La verdad, no sé cómo habría sido la tesis sin ti, pero desde luego, que mucho más aburrida.

Por supuesto, gracias a la *crazy family*, Jorge y Sasa, con los que pasé la primera etapa de la tesis, y quien tuvieron bastante culpa de que hoy esté escribiendo estas líneas. No sé si habrá sido por la cabezonería de Jorge, con el que tantas partidas hemos ganado al fútbol o al amor de Sasa, seguramente a ambas cosas, pero lo cierto es que me ayudasteis a ser quien soy hoy.

Muchas gracias a Francisco, mi socio en esta nueva etapa, con el que no paro de aprender. Gracias por recordarme cada día, que hay que estar de buen humor, que hay que fluir, que todas las ideas y proyectos tienen muchas puertas de entrada, y que el fracaso, no existe mientras sigamos intentándolo.

Por supuesto, gracias a mi equipo actual de Sp, Juan Carlos, Andrea, Virginia y como no, a Diana que ha aguantado mis “momentos tesis” con paciencia.

A mis amigos de Fuenteálamo, Emilio, Juanjo, Ilaria, Taly, Gonzalo y Fardo, porque siempre habéis comprendido que la tesis era un duro camino y vuestro apoyo era necesario. Gracias de verdad.

No quiero olvidarme de Natalia, que en los últimos meses me ha regalado infinitas sonrisas y momentos de paz. Muchas gracias Nat.

Y para acabar, gracias a mis padres, a José María y Ana, porque nunca habéis dudado de mí, porque siempre habéis creído en mis proyectos e ilusiones. Por la educación que me habéis dado, por enseñarme que el esfuerzo es algo bonito y que con él, se puede llegar a la luna. Porque todo esto, no tiene sentido sin vosotros, sin vuestros abrazos, sin vuestras tortillas, vuestro cariño, porque solo espero haber estado a la altura y seguir estándolo, no como ingeniero o empresario, sino como persona, y como vuestro hijo, que tanto os quiere.

Gracias a mi hermano Sergio, por demostrarme que no llega antes el que más corre. Porque no imagino un hermano mejor, con tu paciencia y tu perseverancia, me haces estar orgulloso. Aunque me ganes con la bicicleta..De mayor, quiero ser como tú.

Muchas gracias a todos

Resumen en castellano

En los últimos años, la importancia de la energía eléctrica en aviónica ha ido en aumento, con la aparición de proyectos tan ambiciosos como “El avión más eléctrico”. Dado que, en aviónica, el peso es un factor muy importante, uno de los objetivos de los diseñadores de sistemas electrónicos de vuelo es incrementar la densidad de potencia de los mismos. La inclusión de convertidores conmutados permite ir aumentando la densidad de potencia a través de la inclusión de nuevos tipos de semiconductores que permiten aumentar la frecuencia de conmutación y, de este modo, reducir el tamaño de los magnéticos, los cuales representan una parte importante del volumen total del sistema. Concretamente, en los rectificadores trifásicos, que transforman la corriente alterna de los generadores a corriente continua para alimentar distintos tipos de cargas, los magnéticos no sólo los encontramos en el convertidor, sino también en los filtros EMI que se utilizan a la entrada de los mismos, con el objeto de mitigar los ruidos electromagnéticos producidos en las conmutaciones de los interruptores y poder cumplir con las normas de vuelo en cuanto a ruido electromagnético se refiere. De modo que el incremento de frecuencia de conmutación en los semiconductores se considera un método para lograr soluciones más compactas con niveles de potencia más altos.

En el repaso del estado del arte se han estudiado diferentes soluciones de rectificadores trifásicos conmutados. Se han analizado diferentes topologías teniendo en cuenta los requerimientos de ruido electromagnético de la norma militar MIL-STD-461E, MIL-STD-704F. Estos límites son muy estrictos, ya que son independientes de la potencia del convertidor. En este capítulo, se han simulado las diferentes topologías, tanto de tipo reductor como de tipo elevador, y se han calculado, para unas mismas condiciones, el tamaño de las bobinas del filtro necesarias para cumplir la norma. Algunas de estas topologías incluyen aislamiento galvánico un requerimiento muy común en aplicaciones de aviónica. Dado que el aislamiento galvánico es un requisito de algunas aplicaciones, en el capítulo se revisan algunas de las topologías con aislamiento galvánico más utilizadas para rangos de potencia de cientos a miles de vatios. Estas topologías están basadas principalmente en puentes, completos o medios, con funcionamiento clásico, o resonante, alimentadas en corriente o en tensión. Una vez repasadas estas topologías, se evalúan diferentes combinaciones entre el rectificador tipo reductor, el cual parece el más adecuado para los rangos de tensión y potencia en los que se enmarca esta tesis, y los diferentes convertidores CC/CC con aislamiento. Estas combinaciones se comparan con las soluciones de una sola etapa con aislamiento galvánico.

En esta tesis se ha analizado en detalle el rectificador trifásico tipo reductor y el puente completo alimentado en corriente. Este circuito permite reducir el número de magnéticos en el sistema, ya que la inductancia de salida del rectificador es compartida con la de entrada del puente completo alimentado en corriente. Esta solución abre las posibilidades de aplicar diferentes estrategias al sistema, dado que son dos etapas separadas. Por lo que, la motivación de esta tesis, es el análisis de este circuito, así como las posibles estrategias de control que puedan ayudar a mejorar la densidad de potencia del mismo.

En el tercer capítulo se presenta la principal contribución de la tesis, la sincronización entre la etapa del rectificador trifásico tipo reductor y el puente completo alimentado en corriente. El concepto de sincronización ya fue propuesto por otros autores, conectando el rectificador tipo reductor y un elevador como segunda etapa. A diferencia de esa solución, en el circuito propuesto en esta tesis se añade el transformador, lo que permite optimizar los voltios por segundo aplicados a la bobina intermedia y de esta forma reducir su tamaño.

Dado que este circuito dispone de dos variables de control (M y d), en este capítulo se evalúan las diferentes posibilidades de regulación disponibles. Estas posibilidades se clasifican en 3 estrategias. En la primera, se fija la variable de control del rectificador, M , y se modula el sistema con la variable de control del puente completo, D . En la segunda, se fija D y se regula el sistema con M , y en la tercera, se regula el sistema con las dos variables. En este capítulo, se analiza el impacto de las diferentes estrategias en el rendimiento.

En el capítulo cuarto se analizan las posibles implementaciones del control digital propuesto. En una primera parte se comparan soluciones de bajo coste basadas en FPGA y DSP. A continuación se introducen en la comparación los SoC, dispositivos en los que conviven FPGA, DSP y ADC. Se presenta el diagrama de bloques necesario para el control propuesto, donde se observan las necesidades de medidas del sistema tanto para la modulación como para la regulación del circuito. Las diferentes implementaciones posibles sobre el dispositivo SoC se comparan en cuanto al tiempo necesario para la ejecución y la complejidad.

En el capítulo quinto se validan los análisis teóricos presentados durante la tesis sobre un prototipo. En este capítulo se explica cómo se ha diseñado el prototipo del circuito así como del filtro EMI para cumplir con la normativa MIL-STD-461E, la cual es muy estricta. Aplicar esta norma afecta a la selección de los componentes y al diseño de los magnéticos por la aplicación de unos márgenes (*derating*) en cuanto a temperatura, tensiones y corrientes a soportar.

Adicionalmente, las normas limitan los armónicos debidos a las frecuencias de conmutación, los cuales deben ser atenuados por el filtro EMI. Los resultados que se obtienen de estos prototipos son analizados.

En el capítulo sexto, se analizan los resultados obtenidos, tanto teóricos como experimentales, presentando las aportaciones originales surgidas de este trabajo y se presentan las conclusiones obtenidas de esta tesis.

English summary

In the last years, the importance of the electrical energy in avionic applications has been increasing with numerous news and ambitious projects as “The More Electrical Aircraft” (MEA). Since in avionics, the weight is very importance, in order to reduce the consumption of fuel, one of the main goals for the designers of electronic systems has been increase the power density of the electronic systems. The introduction of commutated power supplies allows to increase the power density throughout using new type of semiconductors allowing increase the switching frequency. This fact helps to decrease the size of the magnetics, whose represents the most important part of the total volume of the system. In the three phase rectifiers, which transform the AC energy coming from the generators to DC to supply several loads, the magnetics can be found in the rectifiers but also in the EMI filters used to attenuate the noise induced by the switching frequency of the rectifiers. This EMI filters are needed to comply with the standards of avionic applications. Therefore, the increment of the switching frequency is a technique used to achieve higher power densities in the designs.

In the review of the state of the art has been study several solutions of commutated three phase rectifiers. Several topologies have been analyzed considering the standards MIL-STD-461E, MIL-STD-704F. The EMI noise requirement are very strict because are independent of the power of the converter. In this chapter, several topologies have been simulated both for buck type and boost type. For the same conditions, the size of the inductors of both kind of topologies have been calculated to comply with the standards. Some of these topologies include galvanic isolation, which is a very common requirement in avionic applications. Since galvanic isolation is a requirement of this applications, in this chapter some of the most used topologies with isolation for hundreds to thousands of watts are reviewed. These topologies are mainly based on Bridges (Full Bridge and Half Bridge) with classic or resonant configurations, current or voltage fed. Once these topologies have been reviewed, several power architectures based on combinations between buck type rectifiers, which it is the most suitable topology for the voltage and power range specified in this thesis, and the DC/DC with isolation commented previously. These solutions are compared with the solutions of only one stage with galvanic isolation.

In this thesis have been analyzed in detail the combination based on the buck type three phase rectifier and the Current Fed Full Bridge. This combination allows to reduce the total number of magnetics of the system because the output inductor of the rectifier is shared with the input inductor of the Current Fed Full Bridge. This combination gives the opportunity to analyze different control

strategies applied to both stages in order to improve the global response. Therefore, the analysis of the design of integrating both stages, analyzing the design and the control possibilities is the main motivation for this thesis.

In the third chapter is presented the main contribution of this thesis, the synchronization between the buck type stage and the Current Fed Full Bridge.

The concept of synchronization was proposed by other authors, connecting the buck type rectifier and a boost converter as a second stage. The different approach to this solution is the inclusion of a power transformer. The transformer allows to optimize the volts per second applied to an intermediate inductor and consequently, reduce its size.

Since this circuit has two variables of control (M and d), in this chapter the regulation possibilities are evaluated. There are three possible strategies. In the first strategy, the modulation index of the rectifier, M , is fixed and the system is modulated with d , the duty cycle of the Full-Bridge. In the second strategy, the duty cycle of the Full Bridge is fixed and the system is regulated with M . And the last strategy consists on regulate modifying both variables, M and d . The impact on the efficiency is analyzed in this chapter.

In the fourth chapter are analyzed some possible implementations of the digital control proposed. First at all, low cost solutions based on FPGA and DSP are compared. Then, SoC devices are introduced in the comparison. SoC are devices which includes microprocessor, FPGA and ADC, in the same chip. In the chapter is presented the block diagram of the control where can be appreciated the necessities of measurements of the control for the modulation and regulation of the circuit. Several possible implementations of the control in the SoC are compared in execution time and complexity.

In the fifth chapter, the theoretical analysis presented during the thesis under a prototype are validated. In this chapter is explained how the prototype have been designed and the considerations to comply with the standards MIL-STD-461E and MIL-STD-704F that has been applied. This standard affects to the selection of the components and the design of the magnetics, where a derating should be considered. Additionally, the standards specify the limits for the harmonics induced at the switching frequency by the rectifier, which affects to the design of the EMI filter. The experimental results obtained are analyzed.

In the sixth chapter, the results obtained, both theoretical and experimental are analyzed, highlighting the original contributions and presenting the conclusions of the work.

Figures Index

Figure 1. Evolution of the power generation capability in commercial aircrafts	27
Figure 2. Power distribution architecture in BOING 787	28
Figure 3. Autotransformer rectifier unit (ATRU) for the more electric aircraft based on the switching behavioral of a 12-pulse diode rectifier	29
Figure 4. Three-Phase Buck type rectifier	30
Figure 5. One stage Three-Phase Rectifier Architectures	31
Figure 6. Two stages power architecture	32
Figure 7. Three Phase rectifier system based on two stages, a Three-Phase Buck type Rectifier and Full-Bridge Phase Shift	32
Figure 8. CE102 limit belong to MIL-STD-461E [MIL-STD-461E]	37
Figure 9. Reference per year on Three-Phase PWM rectifiers in publication on conferences and Journals.	38
Figure 10. Three Phase Active Rectifier with input inductor.	39
Figure 11. V_a is the phase voltage measurements at the input, V_m is the modulation signal, PWM is the generated PWM.	39
Figure 12. Sinusoidal input current for the 3 phase PWM boost rectifier at 2 kW with 115 V_{rms} input voltage and 200 V of output voltage	40
Figure 13. Configuration of the input inductors and capacitor to comply with the standard MIL-STD-461E.....	40
Figure 14. FFT of the current of a 3 phase rectifier in a 2 kW load switching at 210 kHz and an input frequency of 400 Hz.....	41
Figure 15. Three Phase Buck type rectifier with Freewheeling diode	42
Figure 16. DC link current I , global average value I , voltage U across the buck- stage free-wheeling diode and related switching states j for different modulation methods proposed by [Baumann'07].....	43
Figure 17- Symmetric Modulation Method. Where I is the current through the inductance, and u is the voltage across the freewheeling diode [Nussbaumer'07].	44
Figure 18. Sinusoidal input current for the 3 phase PWM Buck type rectifier at 2 kW with 115 V_{rms} input voltage and 200 V of output voltage.	45
Figure 19. FFT of the current of a 3 phase Buck type rectifier in a 2 kW load, 200 V of output voltage, switching at 210 kHz and an input frequency of 400 Hz	45
Figure 20. Switching functions of the proposed advanced modulation scheme preventing sliding intersections of the filter capacitor voltages proposed by [Nussbaumer'07]; (a) ideal switching state sequence; (b) modified switching	

state sequence considering an overlapping time t when switching over from $j = (101)$ to $j = (011)$.	46
Figure 21. Sinusoidal input current for the 3 phase PWM Buck type rectifier with advanced modulation at 2 kW with 115 Vrms input voltage and 200 V of output voltage.	46
Figure 22. FFT of the current of a 3 phase Buck type rectifier with advanced modulation in a 2 kW load, 200 V of output voltage, switching at 210 kHz and an input frequency of 400 Hz	47
Figure 23. Unidirectional Three-phase buck type rectifier.	48
Figure 24. Single stage PWM rectifier with galvanic isolation [Vlatkovic'95]	49
Figure 25. Voltage and current at the input of the isolated rectifier [Vlatkovic'95] for a 2 kW prototype.	49
Figure 26. Swiss-Forward Rectifier.	50
Figure 27. Steady state behavior of the input voltage (light blue) and current (red) and output voltage (blue) and DC inductor current (green) [Silva'14]	50
Figure 28. Full-Bridge Phase Shift Topology	52
Figure 29. Waveform of the Full-Bridge Phase Shift [Sabate'90]	53
Figure 30. Current Fed Full-Bridge	54
Figure 31. Waveform of the Current Fed Full-Bridge [Watson'96]	55
Figure 32. Resonant Dual Active Bridge.	56
Figure 33. Proposed circuit	65
Figure 34 a) Scheme simplified of the circuit b) Voltages and current in the Link inductor	66
Figure 35. M and d relation	68
Figure 36. Current through the transformer depending on the duty cycle applied to the transformer for the same power transfer	69
Figure 37. Estimated efficiency in function of d for a fixed M .	69
Figure 38. M and d relation with value of n calculated for minimum input voltage	70
Figure 39. M and d relation with value of n calculated for nominal input voltage	71
Figure 40. M and d relation with value of n calculated for maximum input voltage	71
Figure 41. Regulation only with M in case A	73
Figure 42. Regulation with M and d	74

Figure 43. Regulation only with d	75
Figure 44. Energy stored in the Link inductor for different regulation modes	77
Figure 45. Envelope of v_d during a sixth of the input voltage period	78
Figure 46. a) $v_{FB} > v_d$ (α) b) v_d (α) $> v_{FB}$	79
Figure 47. Current Ripple in the Link inductor during a sixth of the input voltage period	79
Figure 48. a) Classic Architecture based on a Buck type rectifier with second stage based on a Full-Bridge b) Circuit Proposed, based on the Buck type rectifier and a Current Fed Full-Bridge	80
Figure 49. Equivalent circuit interval t_0 - t_1	83
Figure 50. Equivalent circuit interval t_1 - t_2	83
Figure 51. Equivalent circuit interval t_2 - t_3	84
Figure 52. Equivalent circuit interval t_3 - t_4	84
Figure 53. Equivalent circuit interval t_4 - t_5	85
Figure 54. Equivalent circuit interval t_5 - t_6	85
Figure 55. Equivalent circuit interval t_6 - t_7	86
Figure 56. Equivalent circuit interval t_7 - t_8	86
Figure 57. Waveforms of the proposed circuit	87
Figure 58. Duty cycle loss due to the leakage inductance	90
Figure 59. Required modulation index (M) of the rectifier as a function of the duty cycle (d) in the Full-Bridge	91
Figure 60. Required modulation index (M) of the rectifier as a function of the duty cycle (d) in the Full-Bridge for maximum, minimum and nominal input voltages	92
Figure 61. ZVS situation at high load states	93
Figure 62. NO ZVS situation at light load states	94
Figure 63. ZVS at high load states	95
Figure 64. ZCS operation in the low side switch	96
Figure 65. Efficiency and breakdown of losses	98
Figure 66. Internal architecture of a Zynq series	105
Figure 67. Block diagram of the control connected to the power stage	107
Figure 68. IIR filter architecture	108
Figure 69. PLL diagram	109
Figure 70. Block diagram of PI regulator	110

Figure 71. Scheme of the PI implemented in the programmable logic.....	111
Figure 72. Main phase voltages represented as V_{Ni} (for $i=R,S,T$), line to line voltages V_N , R_S , V_N , R_T , V_N , S_R , V_N , T_R , V_N , T_S and the 12 sectors defined sectors[Nussbaumer'07].....	112
Figure 73. Modulation methods studied by [Baumann'07]	113
Figure 74. Phase Shift Modulation for a Full Bridge considering the overlapping times	114
Figure 75. Architecture A.....	117
Figure 76. Time needed for each task of Architecture A in scale	117
Figure 77. Time needed for each task of Architecture B in scale.....	119
Figure 78. Architecture B	120
Figure 79. Time needed for each task of Architecture C in scale	121
Figure 80. Architecture C.....	122
Figure 81. Time needed for each task of Architecture D in scale	124
Figure 82. Architecture with external ADC	124
Figure 83. Time needed for each task of Architecture with DSP in scale.....	125
Figure 84. On the left side the DSP, TMS320C28346. In the right side, the ADC, ADS8556.....	125
Figure 85. Circuit developed in PSIM for simulation	131
Figure 86. Design consideration of a distributed power architecture	131
Figure 87. EMI filter based on three differential mode stages.....	132
Figure 88. Current at the input of the circuit for a load of 2 kW from a source of 115 Vrms and 48 V of output voltage.....	132
Figure 89. FFT of the current demanded for EMI filter	133
Figure 90. Input current and voltage phase to neutral of the same phase for 115 Vrms of input voltage and maximum power of 2 kW	134
Figure 91. V_d synchronized with VFW and the resulting current ILink	135
Figure 92. V_{diode} , VFB and ILink at 2 kW, 115 Vrms input voltage and 48 VDC of output voltage.....	135
Figure 93. I_T and V_T voltage though the transformer at 2 kW, V_{GS1} and V_{DS1} in Mosfet 1, V_{GS2} and V_{DS2} in MOSFET 2	136
Figure 94. Transformer current and voltage at light load state. ZVS is not obtained.....	137
Figure 95. ZVS of the switches M1 and M2 at light load states	138

Figure 96. Transformer voltage, current through the auxiliary path and the control signal of the auxiliary MOSFET	139
Figure 97. Energy stored in the link inductor, depending on the regulation strategy	140
Figure 98. Results of the inductor design in the tool PExprt	141
Figure 99. Transformer windings	142
Figure 100. Results of the PExprt tool for the transformer design	143
Figure 101. Prototype of the converter	143
Figure 102. EMI filter built	144
Figure 103. Input voltage and current of each phase of the rectifier at 1 kW	144
Figure 104. Measurements of the LISN of the current harmonics without filter and standard limit MIL-STD-461E	145
Figure 105. Measurements of the LISN of the current harmonics with filter and standard limit MIL-STD-461E	145
Figure 106. I_{LINK} Link inductance current, V_{FW} and $V_{TRAFOFB}$ for two different pulse width of the freewheeling diode voltage	146
Figure 107. a) I_{LINK} , V_{FB} and V_T b) I_{LINK} , V_{FW} and V_T during several input voltage source periods	146
Figure 108. Comparison of the current through the inductance. Left) Synchronized case. Right) Unsynchronized case	147
Figure 109. V_{DS} and V_{GS} for M1 and M2 at 10 % of load (200 W)	147
Figure 110. I_{M2} , V_{GS2} and I_T at 200 W (10% of the load)	148
Figure 111. Waveforms of I_{aux} , M_{aux} , M1 and M2	149
Figure 112. V_{GS} of M1(blue) and M4 (purple), I_{Dout} (green) and I_{aux} (yellow)	149
Figure 113. Measurements of the converter efficiency in % of load	150
Figure 114. Load step from maximum power (2 kW) to 500 W.	151
Figure 115. Sector representation of the input voltages	160
Figure 116. Modulation in sector 1. Conduction states for the symmetrical modulation	161
Figure 117. Modulation in sector 2. Conduction states for the symmetrical modulation	162
Figure 118. Modulation in sector 3. Conduction states for the symmetrical modulation	163
Figure 119 Modulation in sector 4. Conduction states for the symmetrical modulation	164

Figure 120. Modulation in sector 5. Conduction states for the symmetrical modulation	165
Figure 121. Modulation in sector 6. Conduction states for the symmetrical modulation	166
Figure 129. Procedure to design inductors proposed by Magnetics.....	171
Figure 130. Internal Architecture in Zynq	183
Figure 131. Reports of the utilization of the FPGA	186

Table Index

Table 1. Comparison between rectifiers topologies for Three Phase Rectifier Systems.....	57
Table 2. Comparison between Rectifiers Architectures with galvanic isolation.....	59
Table 3. Parameters considered for the comparison	81
Table 4. Inductances obtained.....	82
Table 5. Specifications for the proposed design	88
Table 6. Comparison between a DSP Piccolo from TI, TMS320F28075 and an FPGA, Spartan 3 XC3S50 from Xilinx	104
Table 7. Comparative between a DSP from TI and a SoC from Xilinx	106
Table 8. Blocks definitions	115
Table 9. Time needed for each task in Architecture A	118
Table 10. Time needed for each task in Architecture B.....	120
Table 11. Time needed for each task in Architecture C	122
Table 12. Time needed for each task in Architecture D	123
Table 13. Time needed for each task in Architecture with DSP+ADC	126
Table 14. Comparison between architectures	126
Table 15. Specifications of the system	130
Table 16. Rectifier measurements for different switching frequencies.....	151

Acronym Index

ADC	Analog to Digital Converter
ALE	Address Latch Enable
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
CAN	Controller Area Network
CPLD	Complex Programmable Logic Device
DAC	Digital to Analog Converter
DSP	Digital Signal Processor
EB	Evaluation Board
HW	Hardware
IEEE	Institute of Electrical and Electronic Engineers
I/O	Input/Output
I ² C	Inter Integrated Circuit
JTAG	Joint Test Action Group
FPGA	Field Programmable Gate Array
LDR	Light Dependent Resistor
LUT	Look Up Table
MAC	Multiplier Accumulator
MEA	More Electric Aircraft
MEM	Micro Electromechanical System
MSPS	Mega Sample per Second
NCAP	Network Capable Application Processor
OTP	One Time Programmable

PC	Personal Computer
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read Only Memory
SoPC	System on Programmable Chip
SPI	Serial Peripheral Interface
STIM	Smart Transducer Interface Module
SW	Software
TEDS	Transducer Electronic Data Sheet
TII	Transducer Independent Interface
USB	Universal Serial Bus
UWB	Ultra Wide Band
VHDL	Very High Speed Integrated Circuit Hardware Description Language
WSN	Wireless Sensor Network
μ C	Microcontroller
μ P	Microprocessor
ZVS	Zero Voltage Switching
ZCS	Zero Current Switching

Index

Chapter 1 Introduction.....	25
1 Introduction.....	27
1.1 Overview.....	27
1.2 Thesis organization.....	32
Chapter 2 : State of the Art on Isolated Three-Phase Controlled Rectifiers	35
2 Technical Background.....	36
2.1 Harmonic Regulations	36
2.2 Active Rectifiers	37
2.3 DC/DC converters with galvanic isolation as a second stage	51
2.4 Summary of the comparison	57
2.5 References	60
Chapter 3 Three Phase Buck type Rectifier integrated with a Current Fed Full-Bridge	63
3 Introduction.....	64
3.1 Proposed circuit	65
3.2 Control strategies.....	72
3.3 Impact on the inductor energy depending on the control strategy	75
3.4 Volt per second reduction in the Link inductance	77
3.5 Comparison of the energy stored in the inductance between the proposed solution and a classic Buck type rectifier for a specific case.....	80
3.6 Circuit Operation.....	82
3.7 Design issues	88
3.8 Semiconductor Losses	96
3.9 Conclusions.....	99

3.10	References	100
Chapter 4	Digital Control: Control Strategies, Modulations and Implementations.....	102
4	Introduction.....	103
4.1	Digital Control implementation alternatives	103
4.2	Control Architecture of the Converter.....	107
4.3	Alternative Implementations of the control in a Zynq	115
4.4	Conclusions.....	127
4.5	REFERENCES.....	128
Chapter 5	Experimental Results.....	129
5	Introduction.....	130
5.1	Simulations	131
5.2	Prototype design	139
5.3	Prototype results	144
5.4	Impact on the Buck type rectifier switching frequency variations.....	151
5.5	Summary and Conclusions.....	152
Chapter 6	Summary and Conclusion	154
6	Summary and conclusions	155
6.1	Diffusion of the results.....	158
Annex I	Equivalent Circuits	159
7	Equivalent Circuits for each interval of the modulation.....	160
Annex II	EMI Filter Design.....	168
8	EMI filter design	169
Annex III	MathCad	174
9	MathCad Calculations.....	175
Annex IV	Design in Zynq	182

10	Design of the Digital Control in Zynq	183
10.1	Main Architecture	183
10.2	Report of the VHDL Design	184

Chapter 1

Introduction

1 Introduction

1.1 Overview

The explosive growth in the global commercial aircraft orders has also triggered a surge in business for the existing participants in the aircraft electrical power system industry. The tendency today is going to the “More Electric Aircraft” (MEA). A conventional aircraft is based on a combination of mechanical, pneumatic, hydraulic and electrical system. However, the new designs, are becoming more and more electric. As it is shown in Figure 1, the actual aircrafts have increased more than 5 times the electrical power compared with the conventional aircraft. These new aircrafts have replaced pneumatic, hydraulic and mechanical networks by power electronics systems, rising more than 1MW of power generation capability in the main engine architecture.

Figure 1. Evolution of the power generation capability in commercial aircrafts

The main motivation of replacing the classical systems by power electronics solutions is the reduction on weight and volume, reducing the consumption fuel. The desired electrical solutions should provide high efficiency values as well as controllability for the demanded power and a more intelligent maintenance.

Figure 2 shows an example of a Power Architecture in the BOING 787 [Izquierdo'10], where an electrical bleedless system has been proposed for the air

conditioning as well as for the Wind Ice Protection System (WIPS), replacing conventional pneumatic and hydraulic systems. As it is appreciated in Figure 2, there are different sources and different bus of energy where the loads can be connected: two DC buses of 270 VDC and 28 VDC, and two Three-Phase AC buses providing 230 VAC and 115 VAC . This thesis is centered in supplying DC loads, from the Three-Phase AC sources, therefore, from now on, the analysis will be focused in AC/DC systems, usually called, Rectifiers.

Figure 2. Power distribution architecture in BOING 787

From the power electronics point of view, is important to analyze the electrical features of the sources or generators and the design constrains, established for the manufactures and the safety commissions. The systems studied in this work are supplied from the Three-Phase AC sources with a frequency variable between 398-403 Hz and 115 VAC (detailed specifications of these sources can be found in [MIL-STD-741F]). Regarding the electrical restrictions for the rectifiers connected to the AC buses these are principally related to Electromagnetic Interferences (EMI), total harmonic distortion (THD), power factor (PF), galvanic isolation, wide range of temperature operation, transient responses and derating in components. Some applications desire unidirectional circuit, to protect the generator of reverse current. Additionally, each load can have additional restrictions. The restrictions considered

for the present work are: THD lower than 10% for the whole power range, PF higher than 0.95 at maximum power, 115 °C of maximum temperature (70 °C of ambient temperature), up to 70 % in component derating, galvanic isolation and limits CE102 in MIL-STD-461E for EMI noise.

To comply with these restrictions, different rectifier systems have been proposed in the literature. Three-Phase rectifiers have progressed a lot in the last years with more than 3000 publications in the last 15 years. Since, the main goal of the researchers has been developing rectifiers with low harmonic content, rectifiers based on switching solutions should be considered. In the following classification, a brief description of the two most used rectifier solutions in avionics is presented. First, rectifiers based on autotransformer and passive components and second, active rectifiers, where most of the researches are contributing.

1) Rectifiers based on autotransformer and passive components:

Figure 3. Autotransformer rectifier unit (ATRU) for the more electric aircraft based on the switching behavioral of a 12-pulse diode rectifier

Actually, rectifiers based on autotransformer are the most common in aircraft power system. Figure 3 shows an example of an autotransformer rectifier. This type of rectifier is very robust. The autotransformer together with combinations of diodes bridges achieves to rectify the energy coming from the Three Phase generator with a low level of harmonic distortion, decreasing up to 10 % of THD in the best cases [Skibinski'03]. The lack of switching devices helps to get low EMI noise. It is important to note, that the autotransformer does not provide galvanic isolation to the system, consequently, a second stage would be needed. The disadvantage of these rectifiers is that they are very heavy and the future MEA is trying to decrease the weight on board to save energy.

2) Active Rectifiers

The Active Rectifiers, are characterized using active components as transistors, usually IGBT or MOSFET technologies, to rectify the AC voltage of the generators trying to generate the minimum harmonic content in the voltage and current.

Figure 4 shows an example of one active rectifier topology, based on a buck type configuration.

Figure 4. Three-Phase Buck type rectifier

The family of the active rectifiers is studied deeply in [Kolar'13]. These rectifiers need to be modulated to achieve a sinusoidal input current and this modulation is done using measurements of the system variables, which is one of the main differences with the passive rectifiers. These measurements increase the information provided to the central system, which is very appreciated in complex systems, giving the opportunity to inform of failures and do diagnosis of the circuit.

The possibility of controlling the rectifier helps to manage the power provided to the loads or the voltages and currents levels. The reduced number of magnetics, compared with an autotransformer, decreases the weight and the volume considerably. Nevertheless, these rectifiers are also called PWM rectifier, which demand a pulsating current to the source. Therefore, to get a sinusoidal waveform at the input, an EMI filter is needed to filter this pulsating current. This is the main drawback of the PWM rectifiers. The EMI filter in avionic applications, where the standards of noise are very restrictive, increase the weight and volume of the system up to 30% according with [Heldwein'09].

Once rectifiers are studied, there are two requirements that needs to be analyzed: galvanic isolation and output regulation. Galvanic isolation is not included in most of the rectifiers topologies, passive or actives, therefore a second stage would be necessary.

Regarding the regulation, there are several possibilities depending on the topologies chosen. The single stage topologies usually have only one parameter to regulate the system. Nevertheless, most of the architectures analyzed in this thesis have two variables to be controlled, one for each stage, therefore, the regulation options should be analyzed for each case.

In order to study the state of the art, a brief classification of architectures of rectifiers meeting the requirements discussed previously is presented.

1) Single Stage Architectures:

The architectures based on one stage, represented in Figure 5, includes an isolated transformer. These architectures are based on active rectifiers. The power density can be incremented with these topologies, but also there are some drawbacks as the complex control.

Figure 5. One stage Three-Phase Rectifier Architectures

An example of these topologies is presented in [Vlatkovic'95]. The prototype presented by the author achieves efficiency around 93%.

2) Two Stage Architectures:

Figure 6 shows an architecture based on two stages. These architectures are needed when the rectifier does not include galvanic isolation. The regulation is another reason to use this configuration when the first stage is based on passive rectifiers. Two stages architectures can be regulated with a single loop or with two control loops. Regarding the efficiency, these topologies process the power twice, consequently the global efficiency is affected.

Figure 6. Two stages power architecture

An example of two stages architectures has been developed in CEI-UPM, based on a first stage of a Three-Phase Buck type Rectifier and a Full-Bridge as a second stage [Silva'13]. Figure 7 represents the prototype built.

Figure 7. Three Phase rectifier system based on two stages, a Three-Phase Buck type Rectifier and Full-Bridge Phase Shift

During this thesis, the state of the art of Three Phase rectifier architectures with galvanic isolation are reviewed. In avionic or military application, the impact of the constrains in the design is considerable and the difficulties to improve the power density of the system increase. In this thesis a Three Phase Rectifier Architecture is proposed and the impact of different control strategies is analyzed. Since the actual tendency is to use Digital Control in Three Phase Rectifiers, several implementations in a SoC device are compared and discussed.

1.2 Thesis organization

Following the introduction chapter, which briefly describes the motivation for the work, five more chapters provide details of the background and analysis as follows:

- **Chapter 2** – This chapter provides an analysis of the state of the art of Three-Phase rectifier architectures and present the desired requirements to be

complied. Most suitable topologies for given specifications for the AC/DC stage, DC/DC stage and the resultant architectures are compared.

- **Chapter 3** - This chapter presents in detail the architecture proposed in this thesis and its main contribution. Providing guidelines for its design. In this chapter are the most important contribution of the thesis.
- **Chapter 4** - The implementation of the proposed control, which is a contribution of the thesis is discussed in this chapter, after analyzing the existing alternatives.
- **Chapter 5** - This chapter introduces the simulations and experimental results obtained with the prototype built to demonstrate the theoretical analysis for the proposed topology.
- **Chapter 6** - This chapter highlights the contributions of the presented work and discusses future work.

Chapter **2** :

State of the Art on Isolated Three-Phase Controlled Rectifiers

2 Technical Background

This chapter gives an overview of rectifier circuits, focused on three phase systems and looking over common regulations and standards about the harmonic content.

In order to understand the evolution of the three phase rectifiers [Kolar'11], a brief classification with some examples is given in this chapter. Advantages and drawbacks for different rectifier applications are also discussed.

Rectifiers are usually the front-end converter in high power systems, however, most of the systems need a second stage for several reasons such as regulation of the output voltage or including galvanic isolation. Therefore, DC/DC converters are commonly connected as a second stage. In this chapter some typical DC/DC topologies for this purpose are reviewed. Once both stages are reviewed separately, a vision of the global system with two stages is studied. Several power architectures combining different topologies are proposed and compared.

2.1 Harmonic Regulations

The proliferation of electronic equipment, in households and industrial places, has incremented the harmonic content injected to the grids, requiring to create standards to limit the harmonic content of the current demanded by the equipment to the sources. Manufactures of electronic equipment connected to the grid should limit the reactive power demanded to the grid. In special environments such as aircrafts or military equipment, the standards to comply are very restrictive for security reasons. The standard considered in the present thesis is the MIL-STD-461E. The limit for the harmonics in this standard is independent of the power for the applicable frequency range, from 10 kHz to 500 kHz. The specific limit considered in this thesis is CE102 which belongs to MIL-STD-461E [MIL-STD-461E] and is represented in Figure 8.

Since the size of the EMI filter to comply with the present standard can represent a 30% of the total volume of the system, the reduction of the harmonics produced by the power stage is an important challenge for the engineers. During this chapter, the harmonic content produced by different rectifiers topologies is shown and compared. Additionally, different modulation strategies applied to the rectifiers in order to reduce the noise and therefore, the EMI filter are shown. Galvanic isolation is one of the requirements considered in this thesis, therefore, the DC/DC

topologies reviewed include galvanic isolation and are suitable for the range of kilowatts.

Figure 8. CE102 limit belong to MIL-STD-461E [MIL-STD-461E]

2.2 Active Rectifiers

There is a tendency in the industry to move from passive rectifiers to active rectifiers. The main motivation of this fact is the reduction of the size and weight of the actual solutions. From the point of view of the source, an ideal rectifier should behave as a resistor, so ideally, the current demanded will be in phase and perfectly sinusoidal, achieving power factor equal to 1. This challenge is addressed by the design of the input filters but also by the control in active rectifiers.

The design of these filters is a big challenge because the limits for the harmonics of the standard MIL-STD-461E are independent of the power, for example, the limit of the harmonic for an active rectifier of 100 W, supplied from 115 Vrms with a switching frequency of 210 kHz is 74 dBuV, which is the same for a rectifier of 10 kW. Considering this value as the result of a measurement in a LISN equipment, where the resistance at this frequency is 40 Ohms, the equivalent current harmonic limit is 125 uA (-78 dBA) at 210 kHz. If the switching frequency is higher than 500 kHz, the limit decreases up to 40 uA. This values shows how strict is this standard.

Figure 9. Reference per year on Three-Phase PWM rectifiers in publication on conferences and Journals.

In the last decade, the interest on three phase rectifiers and the tendency to control these systems has presented an impact on the number of publications on Three-Phase PWM rectifiers, finding more than double number of publications on 2014 than in 2002. Figure 9 presents this fact.

One of the main goals of using active rectifiers is to being able to control the power flow (output voltage, output current or protections are some features available for a controlled system), needed in most of the typical applications. As has been explained during this chapter, other feature required in avionic applications is the galvanic isolation. Since this thesis is focused in active rectifiers, in the following analysis, rectifier topologies are divided in active rectifiers with and without galvanic isolation.

2.2.1 *Active Rectifiers without galvanic isolation*

Three Phase Active Rectifiers are the evolution of the passive rectifiers, substituting diodes for switches or simply adding switches to diode bridges. As an example, substituting diodes for switches, a fully controlled rectifier is obtained as it is shown in Figure 10. This is a four quadrant rectifier with capability of control the input power factor. Controlling the switches according to a PWM modulation as a function of the input parameters (Voltage, current or both) a sinusoidal input current with low THD can be obtained.

Figure 10. Three Phase Active Rectifier with input inductor.

This rectifier can be controlled with a PWM classical modulation as is presented in [Ziogas'85]. This modulation consists on comparing the reference with a triangular waveform to generate the gate signals. This modulation is appreciated in

Figure 11. A sinusoidal signal is compared with a triangular waveform, and the PWM signals are generated. A complementary signal to the PWM is also generated for the other switch of the branch. It is common to add a dead time between these two signals, in order to avoid short circuits, although some power modules that includes the switches and driver, provides this dead time.

Figure 11. V_a is the phase voltage measurements at the input, V_m is the modulation signal, PWM is the generated PWM.

The PWM signals should be applied to the branch corresponding with the voltage phase used to generate them.

The rectifier of Figure 10 is simulated under the specifications of 2 kW of output power, 200 V_{dc} of output voltage, 210 kHz of switching frequency, supplied from a 115 V_{rms} phase to neutral and 400 Hz source. Figure 12 shows the input current demanded by the rectifier to the source.

Figure 12. Sinusoidal input current for the 3 phase PWM boost rectifier at 2 kW with 115 V_{rms} input voltage and 200 V of output voltage

In order to comply with the standard in this simulation and being able to provide 2 kW to the load, an EMI Filter is added. The EMI filter circuit is shown in Figure 13. The configuration used includes two inductors of 500 uH and a capacitor of 0,66 uF.

Figure 13. Configuration of the input inductors and capacitor to comply with the standard MIL-STD-461E

The current obtained using this EMI filter and this PWM modulation presents a very low THD, minor than 1%. In order to analyze the EMI noise for this modulation, the input current spectrum is studied in Figure 14, where both,

switching frequency and the frequency of the input source present peaks on the FFT. Analyzing the harmonic content, multiples of the grid frequency as the third harmonic (1,2 kHz) and harmonics multiples of the switching frequency (at 420 kHz, 630 kHz and 840 kHz) are also appreciated in Figure 14. Regarding the standard to be complied (MIL-STD-461E), the main harmonic of the switching frequency presents an amplitude of -88 dB being smaller than the limit of -78 dB at this frequency.

Figure 14. FFT of the current of a 3 phase rectifier in a 2 kW load switching at 210 kHz and an input frequency of 400 Hz

After the implementation of [Malesani'87] moving the inductor from the input to the output, creating a Buck type rectifier, the author [Williams'95] introduces the Freewheeling diode (FW) in the Three-Phase Active rectifier, between the bridge of switches and the output filter. The inclusion of this diode provides an additional level to the modulation (3 levels). This fact helps to create a new modulation method and improve the quality of the sinusoidal input current, reducing the EMI filter size. From this topology the Buck type rectifier, which is shown in Figure 15 [Nussbaumer'07] is derived.

Figure 15. Three Phase Buck type rectifier with Freewheeling diode

This is an unidirectional topology proposed to be used in aircraft applications in [Silva'11]. The main advantages of this topology are: it does not need a pre-charge circuit, it can still operate with power factor correction when one main phase fail and it is easy to control.

In order to maximize the output voltage, the two largest voltages of the input are used during each 60° interval of the modulation selecting the branch that should conduct. The modulation schemes of this rectifier have been studied by [Baumann'00], and extended in [Baumann'01], [Baumann'08]. In this analysis, the author proposes four modulation schemes. In Figure 16 these modulation methods are shown.

The main idea of this modulation is to achieve in each switching period, a specific value of the input current, using the information of the input voltages. The input current is controlled to be in phase with the voltage. The demanded current to the input source is the resulting average value of combining three different states during the switching period. These states are: the higher line voltage of the input, the lower line voltage and the freewheeling state, which applies zero volts to the output filter.

Several modulations are proposed in [Baumann'00] and shows in Figure 16. The main difference between those modulation is the resultant current ripple shape and amplitude.

Figure 16. DC link current I , global average value I , voltage U across the buck-stage free-wheeling diode and related switching states j for different modulation methods proposed by [Baumann'07].

Figure 17 shows the modulation method selected in this thesis. This modulation is selected because the symmetrical order helps to synchronize the rectifier stage with the DC/DC stage. In this modulation method, the freewheeling state is placed in the middle of the period. With this symmetrical combination, the current ripple obtained is shown in Figure 17.

Figure 17- Symmetric Modulation Method. Where I is the current through the inductance, and u is the voltage across the freewheeling diode [Nussbaumer`07].

The Buck type rectifier of Figure 15 is simulated applying this modulation strategy. This modulation allows to obtain a sinusoidal input current with a relatively low EMI filter at the input respect to the previous circuits. Figure 18 shows the input current of the rectifier, using this modulation method. The EMI filter needed to comply with the MIL-STD-461E (without consider the common mode noise) is based on two stages of differential mode L-C filters. The value of the inductor is 80 μH and 0,66 μF for the capacitance in each stage, this represents a cut off frequency of 22 kHz. The current measured at the input of the filter is shown in Figure 18.

Figure 18. Sinusoidal input current for the 3 phase PWM Buck type rectifier at 2 kW with 115 Vrms input voltage and 200 V of output voltage.

With this filter, the current harmonics are reduced to comply with the standard. Figure 19 shows the current spectrum of this current. As it is observed, the harmonics due to the switching frequency at 210 kHz is under the limit of -78 dB.

Figure 19. FFT of the current of a 3 phase Buck type rectifier in a 2 kW load, 200 V of output voltage, switching at 210 kHz and an input frequency of 400 Hz

The actual modulation presents a problem when the measurements of two line to line voltage are equal. The problem is, the intersection between the measurements of the input voltages create a confusion in the system for a few high frequency cycles. This problem introduces a low frequency distortion, increasing the THD. However,

[Nussbaumer'06] presents an improvement on the modulation solving this problem, thus reducing the THD. The improvement in the modulation consist on overlaps the drive signals in the switches for a short time in order to avoid this problem as it is shown in Figure 20.

Figure 20. Switching functions of the proposed advanced modulation scheme preventing sliding intersections of the filter capacitor voltages proposed by [Nussbaumer'07]; (a) ideal switching state sequence; (b) modified switching state sequence considering an overlapping time t when switching over from $j = (101)$ to $j = (011)$.

The resultant filter needed using this modulation method is reduced from 80 μH to 60 μH , keeping the same capacitor of 0,66 μF , these values provides a cut off frequency of 25 kHz. The current obtained at the input of the rectifier is shown in Figure 21.

Figure 21. Sinusoidal input current for the 3 phase PWM Buck type rectifier with advanced modulation at 2 kW with 115 Vrms input voltage and 200 V of output voltage.

Figure 22. FFT of the current of a 3 phase Buck type rectifier with advanced modulation in a 2 kW load, 200 V of output voltage, switching at 210 kHz and an input frequency of 400 Hz

Figure 22 shows the current spectrum of the Buck type rectifier using the advanced modulation strategy. As can be observed, the harmonic of the switching frequency is attenuated complying with the MIL-STD-461E and reducing the inductor of the EMI filter, consequently, reducing the size of the filter. The author [Nussbaumer'07] presents a guide to develop a differential mode EMI filter for this rectifier. Also [Silva'11] and [Molina'14] contributed to the EMI filter design for Three Phase buck type rectifiers.

Figure 23 represents the same concept of rectifier of Figure 15 with a different implementation of the switches. The circuit reduces the number of switches and increments the number of diodes, presenting an increment in conduction losses [Kolar'11], but reducing the control complexity.

Figure 23. Unidirectional Three-phase buck type rectifier

2.2.2 Active Rectifiers with Galvanic Isolation

Galvanic isolation is a feature required in rectifiers architectures for some specific applications. Typical industrial applications with galvanic isolation are military, aerospace or the future smart grids. Galvanic isolation increases the weight and the volume of the converter, therefore, in order to keep high power density, architectures based on one stage, called, “single stage rectifiers” are proposed in the literature. A single stage example is the rectifier proposed by [Vlatkovic’95]. The circuit, shown in Figure 24, is a PWM three phase rectifier, with four quadrant switches, connected to a high frequency transformer through an inductor, and having a diode bridge in the secondary of the transformer and an L-C filter in the output.

Since the transformer and the diode bridge are not switching elements, the differential EMI noise measured at the input is similar to a PWM three phase full bridge rectifier.

Figure 24. Single stage PWM rectifier with galvanic isolation [Vlatkovic'95]

The rectifier built by the author as demonstrator, presents low harmonics and unity power factor. In Figure 25 the experimental results provided by the author are shown.

Figure 25. Voltage and current at the input of the isolated rectifier [Vlatkovic'95] for a 2 kW prototype.

The control published in [Vlatkovic'95] is based on a digital control implemented in a microcontroller, measuring the three input voltage to modulate the converter.

Other example of a single stage rectifier, is the modified Swiss rectifier, denominated, Swiss-Forward rectifier, designed and developed at CEI and published by [Silva'14]. Figure 26 shows the circuit.

Figure 26. Swiss-Forward Rectifier.

The principle of operation of the Swiss-Forward Rectifier is similar to the Swiss Rectifier [Soeiro'12], where the buck-type DC/DC converters are replaced by isolated forward-type DC/DC converters, adding two transformers and the diodes D_+ and D_- . The author built a demonstrator to show how a low THD and a high power factor can be obtained with this rectifier. Figure 27 shows the experimental results obtained by the author [Silva'14].

Figure 27. Steady state behavior of the input voltage (light blue) and current (red) and output voltage (blue) and DC inductor current (green) [Silva'14].

2.2.3 *Discussion for the analyzed AC/DC topologies*

Three phase active rectifiers have improved their features in terms of power density and controllability because of the demand of electronic systems in fields as avionics, telecommunication or military applications, where the rectifiers have an important role.

The result is a large number of new topologies. The selection of the suitable topology for each case requires an extensive analysis of each circuit for the given specifications. Active topologies are able to operate as resistance, achieving low distortion in the input current and voltage, one of the main requirements in rectifiers to decrease the EMI filter volume and weight.

The solutions based on one stage obtain higher power density when there are small variations in the input and output voltages.

The controllability of the active rectifiers allows correcting the phase shift added by the input EMI filter capacitors, achieving unity power factors. The big difference between the isolated rectifiers and the non-isolated is the compact solution obtained.

It is important to highlight the impact of the modulation method used to control the Buck type rectifier. Using an advanced modulation method, the EMI filter can be reduced. This modulation helps to decrease the EMI noise and the current ripple in the output inductance of the rectifier.

2.3 *DC/DC converters with galvanic isolation as a second stage*

Galvanic isolation is a requirement in rectifiers that increments considerably the complexity of the system. The galvanic isolation can be placed in the rectifier stage, but usually is included in a second stage. The DC/DC stage with isolation is more complicated than the basic topologies due to the difficulties of adding a transformer. This is because the design should consider the parasitic effects of the transformer (Leakage inductance, magnetizing inductance...) and its impact on the operation of the circuit. Additionally, there is an increment of the volume and weight of the system.

Since this thesis is focused in Three-phase systems for medium power, typical DC-DC topologies with galvanic isolation for power range from hundreds of watts to units of kilowatts are analyzed in this section. Three different topologies of DC-DC converters are shown below.

2.3.1 Phase Shift Full-Bridge

The classic Phase Shift Full-Bridge (PSFB) is a very common topology in medium and high power applications. This topology can achieve ZVS, therefore is also used in high voltage applications, where the switching losses are significant due to the energy stored in the parasitic capacitors [Sabate'90]. The Figure 28 shows this circuit.

Figure 28. Full-Bridge Phase Shift Topology

The design of the transformer is critical to achieve ZVS in the switches, specially, in the branch which works delayed, where the commutation occurs under minimum current through the transformer. The goal during the design of the transformer is to integrate the parasitic (leakage and magnetizing inductance) in the operation of the circuit.

ZVS is achieved in these circuits using the energy stored in the leakage inductance and this energy is dependent on the current through the transformer. Other parameter considered during the design, should be the magnetizing inductance, which can help to obtain ZVS during the light load states, where the current through the transformer is almost zero. In [Sabate'90]-[Molina'12], the authors present design guidelines to select the leakage inductance needed, additionally in [Molina'15] a design using the magnetizing inductance to achieve ZVS at light loads without adding an additional inductance is presented.

Transformer voltage and leakage inductance current are shown in Figure 29 for the PSFB. The Phase Shift control is based on applying complementary signals to the switches of each leg, leaving a dead time between both, and delaying the signals from one leg (M1 and M2) respect to the other (M3 and M4) to change the effective duty cycle of the converter, and consequently the power delivered to the output.

Figure 29. Waveform of the Full-Bridge Phase Shift [Sabate'90]

With this control method, the switches present different switching conditions depending on the leg. One of the legs switch with the current due to the output inductance. In Figure 29 is represented during the interval t_4 - t_5 . During this interval, it is achieved the maximum current. This fact helps to discharge the parasitic capacitances of the switches, achieving zero voltage switching (ZVS) easily.

The other leg switch with the current due to the leakage inductance, in Figure 29 is represented in the interval t_2 - t_4 . As can be observed, the current is smaller in this case. In light load situations this current is near to zero, making difficult reach ZVS.

When there is not enough energy in the leakage inductance to achieve ZVS, there are two options. Add an external inductance, or increment the magnetizing current to maintain a minimum current in the transformer, even for no load conditions, ZVS can be achieved using this current. Interesting design guidelines and implementations of this circuit are studied in depth by [Redl'90] and [Redl'93].

2.3.2 Current Fed Full-Bridge

A variation of the classic topology Full Bridge is the Current Fed version. Figure 30 shows the Current Fed proposed by [Watson'96] with an auxiliary circuit to avoid resonances.

Figure 30. Current Fed Full-Bridge

The author proposes a phase shift control for this current fed Full-Bridge. Unlike the classic Full-Bridge studied previously, the phase shift occurs between the upper side MOSFETs (M_1 and M_3) and the low side MOSFETs (M_2 and M_4), a difference of the classic Full Bridge where the phase shift occurs between MOSFETs of one branch (M_1 and M_2) and MOSFETs of the other branch (M_3 and M_4). Other difference is how is implemented the dead time. In this case the dead time is implemented as an overlapping time between M_1 and M_3 , and between M_2 and M_4 .

Figure 31. Waveform of the Current Fed Full-Bridge [Watson'96].

This topology is used in fuel cell and battery applications, connected as a second stage of a rectifier [Watson'96]. As occur for the Full-Bridge topology, soft switching is achievable, using the energy stored in the leakage inductance. During the overlapping period, zero current switching (ZCS) in the low side MOSFETs is achieved. ZVS is achieved for every switch, presenting higher problems at light load for the switches of the low side, because the commutation occurs under low current through the transformer. A method to obtain soft switching at light load has been proposed by [Prasanna'13].

The function of the auxiliary path is to allow conducting the current supplied by the inductor when the Full-Bridge does not demand any current. If there is not any possible path to continue circulating the current of the inductor, a spike would appear across the input of the Full-Bridge.

2.3.3 Series resonant Dual Active Bridge (SRDAB)

The SRDAB is a suitable topology for bidirectional systems. This circuit is based on two Full-Bridge connected through a transformer, with a series resonant tank. This

topology is compared with the non-resonant Dual Active Bridge in [Krismer'05]. In this paper, the author provides a comparison between both converters and suggest to add a second stage in order to keep high efficiency and being able to regulate the output voltage.

The author [Pavlović'12] proposes a pulse modulation technique for this topology, achieving high efficiency for a fixed operation point. The selection of the resonant frequency and its relation with the switching frequency will affect to the behavior of the converter, presenting huge differences in the efficiency.

In the solution proposed by [Pavlovic'12] the switching frequency is equal to the resonant frequency. This system is able to achieve high power densities, nevertheless it works without any regulation.

Figure 32. Resonant Dual Active Bridge

Another possibility, instead of operating at resonant frequency, is to select a different switching frequency, close to the resonant frequency. In comparison with the previous solution, the efficiency is penalized, however regulation of the output voltage is possible, therefore a second stage would not be necessary.

2.3.4 Discussion for the analyzed DC/DC topologies

Bridge topologies (Full-Bridge, Half-Bridge or Resonant Full-Bridge) are convenient solutions as second stage in rectifier architectures of several kilowatts where galvanic isolation is needed.

In this subsection, three of them have been presented. All these solutions present high efficiency, achieving ZVS for all the semiconductors, and also ZCS in the case of the SRDAB and in the CFFB in the low side switches.

Nevertheless, at light load, Bridges use to lose ZVS and a typical solution is including an extra inductor, increasing the weight and volume of the converter. Other solutions to keep ZVS at light load are discussed in this thesis.

Regarding the control, the Phase shift Full-Bridge is simple. There are several chips to control in close loop this topology.

The Current Fed Full-Bridge is very similar to the previous one, with the difference, that it is not very common to find a standard chip for this topology.

However, the control of the SRDAB, with phase shift modulation, it is more complex, because of the number of switches and the complexity of the regulation. The control used for a SRDAB should have high PWM resolution, because the regulation range is very tiny. Therefore, to regulate this converter, the discrete increments for the phase shift modulation should be very small.

2.4 Summary of the comparison

During this chapter, rectifier topologies and DC/DC converters with isolation have been studied for a specific range of power and considering the requirements of avionic applications. Comparison between the presented circuits and combinations of them are outlined below.

Table 1 shows a comparison between the rectifiers studied in this chapter in terms of energy stored in the inductors, the number of switches and galvanic isolation.

The energy stored in the inductors is calculated considering the EMI inductors needed to comply with the standard MIL-STD-461E and also the high frequency inductors included in buck type topologies. In electrical terms, the calculations have been done for a source of 115 Vrms and an output voltage of 2 kW. The switching frequency is 210 kHz. The designs used in the comparison of the topologies Single Stage isolated 3P PWM rectifier and the Swiss-Forward rectifier are lightly different to these specifications, because have not been designed to the same purpose, therefore, the parameters have been scaled to have a fair comparison.

Table 1. Comparison between rectifiers topologies for Three Phase Rectifier Systems

	Energy in the inductors	Switches BV	Complexity	Galvanic Isolation
3P Boost type PWM rectifier	19,8 mJ	$\sqrt{3} \hat{V}_{l-n}$	Low	NO
3P Buck type Rectifier	10,7 mJ	$\frac{3}{2} \hat{V}_{l-n}$	Low	NO
3P Buck type Rectifier With Advance Modulation	9,9 mJ	$\frac{3}{2} \hat{V}_{l-n}$	Medium	NO
Single Stage 3P Isolated PWM rectifier	17,2 mJ	$\sqrt{3} \hat{V}_{l-n}$	High	YES
Swiss-Forward	25,3 mJ	$\frac{3}{2\sqrt{2}} \hat{V}_{l-n}$	Medium	YES

The result of these comparisons is that the energy in the Buck type rectifier presents the lower value, especially when the advance modulation is used, which allows to reduce from 80 uH the input inductor to 60 uH. The single stage solutions present an interesting value, considering that includes galvanic isolation. However, to have a vision of the power density, the Break Down Voltage (BV) of the semiconductors combined with the information of the energy stored in the inductors is studied and the result is that the Swiss Rectifier presents the lowest values and the Single stage and the Boost rectifier the highest. The Buck type rectifiers are in the middle. Nevertheless, with the new SiC technology the designs can be made to for high Break Down voltages without penalizing the power density.

The last feature to be compared, is the galvanic isolation. Only the Single Stage solution provides galvanic isolation, therefore, the rest of them should include a second stage to have galvanic isolation and comply the requirements established in this thesis.

This thesis analyzes AC/DC rectifiers architectures with galvanic isolation, with the goal to achieve high power density and low harmonics. To comply with these specifications, in Table 2 some combinations of rectifier stages with galvanic isolation are compared. Based on the previous analysis, a Buck type rectifier is combined with several DC/DC stages to be compared with a single stage solution. The DC/DC topologies used in the comparison are: Phase Shift Full Bridge, Series Resonant Dual Active Bridge and the Current Fed Full-Bridge.

Table 2 shows that considering the Energy Stored in the inductors, including the inductors of the EMI filter and the High frequency inductors, the best combination

is the 3P Buck type together with the Current Fed Full Bridge. The success of this solution lies in the integration of both stages, sharing the output inductor of the rectifier. Nevertheless, the combinations of the Buck type with PSFB and SRDAB need an additional inductor for the output filter, which increase the energy needed. The single stage solution presents better results than the combination of PSFB and SRDAB but not as good as the CFFB.

Other parameter compared is the number of semiconductors. Clearly the single stage solution is the topology with minor number of semiconductors followed by the combination of 3P Buck type with PSFB.

Depending on the application, the circuit needs regulation or works at fixed point of load. For this reason, the possibilities of regulation are presented in Table 2. The combinations of the 3P Buck type with PSFB and CFFB and the single stage solution can be regulated. Nevertheless, the SRDAB is a topology that provides good results for fixed input and output voltage, working as a DC/DC transformer, if there is change the efficiency drops drastically.

Table 2. Comparison between Rectifiers Architectures with galvanic isolation

	Rectifier Energy	Switches/Diod es	Regulation
Single Stage 3P Isolated PWM Rectifier	17,2 mJ	12/4	Yes
Buck type+PSFB	19,5 mJ	10/9	Yes
Buck type+SRDAB	19,5 mJ	14/7	No
Buck type+CFFB	9,9 mJ	11/9	Yes

To conclude this analysis, there are several combination of rectifier architectures studied in the literature. However, for the specifications stablished in this thesis (400 Hz and 115 Vrms at the input, 2 kW and 48 V at the output, MIL-STD-461E, galvanic isolation) the Buck type architectures are more suitable, in their single stage representation or in combination of stages. With the calculations of energy stored in the inductors the best architecture for this specification is the Buck type with the CFFB, although, regarding the number of semiconductors, the single stage solution use less number of semiconductors.

2.5 References

- [Izquierdo'10] D. Izquierdo, R. Azcona, F. del Cerro, C. Fernandez, and B. Delicado, "Electrical power distribution system (hv270dc), for application in moreelectric aircraft," in Proc. Twenty-Fifth Annual IEEE Applied Power Electronics Conf. and Exposition (APEC), 2010, pp. 1300-130
- [Vlatkovic'95] Vlatkovic, V.; Borojevic, D.; Lee, F.C., "A zero-voltage switched, three-phase isolated PWM buck rectifier," *Power Electronics, IEEE Transactions on* , vol.10, no.2, pp.148,157, Mar 1995 doi: 10.1109/63.372599
- [Kolar'11] Kolar, J.W.; Friedli, T., "The essence of three-phase PFC rectifier systems," in *Telecommunications Energy Conference (INTELEC)*, 2011 IEEE 33rd International , vol., no., pp.1-27, 9-13 Oct. 2011
- [MIL-STD-461E] <http://snebulos.mit.edu/projects/reference/MIL-STD/MIL-STD-461E.pdf>
- [Ziogas'85] Ziogas, Phoivas D.; Kang, Y.-G.; Stefanovic, Victor R., "PWM Control Techniques for Rectifier Filter Minimization," *Industry Applications, IEEE Transactions on* , vol.IA-21, no.5, pp.1206,1214, Sept. 1985.
- [Malesani'87] X. Li, G. C. M. Meijer, R. de Boer, M. Van der Lee, "A High-Performance Universal Interface", in *Proceedings of the 1st ISA/IEEE Conference on Sensors for Industry*, pp. 19 – 22, Rosemont, Illinois, USA, November 2001.
- [Williams'95] Williams, B.W.; Mirkazemi-Moud, M.; Tooth, D.; Finney, S.J., "A three-phase AC to DC converter with controllable displacement factor," in *Power Electronics Specialists Conference, 1995. PESC '95 Record., 26th Annual IEEE* , vol.2, no., pp.996-1000 vol.2, 18-22 Jun 1995.
- [Nussbaumer'07] Nussbaumer, T.; Baumann, M.; Kolar, J.W., "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," *Power Electronics, IEEE Transactions on* , vol.22, no.2, pp.551,562, March 2007.
- [Baumann'00] Baumann, M.; Drofenik, U.; Kolar, J.W., "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage," in *Telecommunications Energy Conference, 2000. INTELEC. Twenty-second International* , vol., no., pp.461-470, 2000
- [Baumann'01] Baumann, M.; Kolar, J.W., "Comparative evaluation of modulation methods for a three-phase/switch buck power factor corrector concerning the input capacitor voltage ripple," in *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual* , vol.3, no., pp.1327-1332 vol. 3, de2001
- [Baumann'08] Baumann, M.; Nussbaumer, T.; Kolar, J.W., "Comparative evaluation of modulation methods of a three-phase buck + boost PWM rectifier. Part I: Theoretical analysis," *Power Electronics, IET* , vol.1, no.2, pp.255,267, June 2008.
- [Nussbaumer'06] Nussbaumer, T.; Heldwein, M.L.; Kolar, J.W., "Differential Mode Input Filter Design for a Three-Phase Buck-Type PWM Rectifier Based on Modeling of the EMC Test Receiver," in *Industrial Electronics, IEEE Transactions on* , vol.53, no.5, pp.1649-1661, Oct. 2006.

-
- [Silva`11] Silva, M.; Hensgens, N.; Oliver, J.; Alou, P.; Garcia, O.; Cobos, J.A., "New considerations in the input filter design of a three-phase buck-type PWM rectifier for aircraft applications," Energy Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.4087-4092, 17-22 Sept. 2011.
- [Molina`14] Molina, J.M.; Zhao, S.; Silva, M.; Oliver, J.A.; Alou, P.; Torres, J.; Arevalo, F.; Garcia, O.; Cobos, J.A., "Power distribution in a 13 kW three-phase rectifier system: Impact on weight, volume and efficiency," in Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp.906-911, 16-20 March 2014.
- [[Silva`14] Silva, M.; Hensgens, N.; Oliver, J.; Alou, P.; Garcia, O.; Cobos, J.A., "Isolated Swiss-Forward three-phase rectifier for aircraft applications," Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp.951-958, 16-20 March 2014.
- [Soeiro`12] Silva, M.; Hensgens, N.; Oliver, J.; Alou, P.; Garcia, O.; Cobos, J.A., "New considerations in the input filter design of a three-phase buck-type PWM rectifier for aircraft applications," Energy Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.4087-4092, 17-22 Sept. 2011.
- [Sabate`90] Sabate, J.A.; Vlatkovic, V.; Ridley, R.B.; Lee, F.; Cho, B.H., "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual , vol., no., pp.275-284, 11-16 March 1990.
- [Molina`12] Molina, J.M.; Garcia, O.; Asensi, R.; Alou, P.; Oliver, J.A.; Cobos, J.A., "Adaptive control for ZVS three phase full active bridge converter with ARCN," in Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.1324-1330, 5-9 Feb. 2012.
- [Redl`90] Redl, R.; Sokal, N.O.; Balogh, L., "A novel soft-switching full-bridge DC/DC converter: Analysis, design considerations, and experimental results at 1.5 kW, 100 kHz," in Power Electronics Specialists Conference, 1990. PESC '90 Record., 21st Annual IEEE , vol., no., pp.162-172, 0-0 1990.
- [Redl`93] Redl, R.; Balogh, L.; Edwards, D.W., "Switch transitions in the soft-switching full-bridge PWM phase-shift DC/DC converter: analysis and improvements," in Telecommunications Energy Conference, INTELEC '93. 15th International , vol.1, no., pp.350-357 vol.1, 27-30 Sep 1993
- [Watson`96] Watson, R.; Lee, F.C., "A soft-switched, full-bridge boost converter employing an active-clamp circuit," in Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE , vol.2, no., pp.1948-1954 vol.2, 23-27 Jun 1996
- [Prasanna`13] Prasanna, U.R.; Rathore, A.K., "Extended Range ZVS Active-Clamped Current-Fed Full-Bridge Isolated DC/DC Converter for Fuel Cell Applications: Analysis, Design, and Experimental Results," Industrial Electronics, IEEE Transactions on , vol.60, no.7, pp.2661-2672, July 2013
- [Krismer`05] Krismer, F.; Biela, J.; Kolar, J.W., "A comparative evaluation of isolated bi-directional DC/DC converters with wide input and output voltage range," Industry Applications Conference, 2005. Fourtieth IAS Annual Meeting. Conference Record of the 2005 , vol.1, no., pp.599-606 Vol. 1, 2-6 Oct. 2005.
-

[Pavlovic`12] Pavlovic, Zoran; Oliver, Jesus A; Alou, Pedro; Garcia, Oscar; Cobos, Jose A, "Bidirectional multiple port dc/dc transformer based on a series resonant converter," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1075,1082, 17-21 March 2013

Chapter 3

Three Phase Buck type Rectifier integrated with a Current Fed Full-Bridge

3 Introduction

In the previous chapter, the power architectures suitable for the specifications applied in this thesis have been reviewed. Several solutions of rectifier systems with galvanic isolation for medium power range are studied and compared.

There are mainly two types, rectifiers with galvanic isolation, usually known as “single stage rectifier” and rectifiers without isolation. The topologies with galvanic isolation are complex to modulate, presenting limited control possibilities. Additionally, the hardware implementation can also present a big challenge due to the number of switches and magnetics in a single topology.

However, the rectifiers without galvanic isolation, are simpler and present more control possibilities in order to be integrated in a bigger architecture.

Once the results are compared, the best solution in a tradeoff between power density, number of semiconductors and regulation possibilities is the Buck type Rectifier together with the CFFB. Additionally, this topology has not been studied in the literature, therefore, it is the main contribution of this thesis.

The circuit explored in this thesis is based on two stages. In [Uan-Zo-li’03], [Seixas’04] and [Cortes’14], solutions with autotransformer as a rectifier are proposed, presenting a good result but a very heavy solution. In most of these solutions, the authors use a Full Bridge as a second stage to provide isolation to the architecture.

In the last years, researches are focused in finding solution with active rectifier to decrease the weight of the system, keeping good results in terms of THD. In [Silva’13] a power architecture using an active rectifier in the first stage and a Full Bridge in the second stage is proposed.

As a result of the analysis of the second chapter, the solution based on a Buck type rectifier [Malesani’87]-[Nussbaumer’07] integrated with a Current Fed Full Bridge [Watson’96] is selected to being studied in this thesis.

This thesis proposes a control architecture for the converter presented in Figure 33 considering that both topologies are sharing an inductor. The schematic of the proposed architecture studied is shown in Figure 33.

Figure 33. Proposed circuit

3.1 Proposed circuit

The circuit proposed in this thesis is represented in Figure 33. In previous works, other authors have presented ideas of integrating a Buck type rectifier with other current fed circuits. In [Baumann'01]-[Baumann'08] the author proposes the integration of a Three Phase Buck type rectifier [Malesani'87] with a Boost converter. The resultant topology shares the output inductance of the rectifier with the input inductance of the boost converter. This circuit allows increasing the output voltage range of the system without increasing considerably the complexity of the circuit. Nevertheless, this system does not include galvanic isolation. The circuit proposed in this thesis integrates the buck type rectifier with a Current Fed Full Bridge [Watson'96]-[Chen'08], adding galvanic isolation to the system.

The control of the proposed topology is implemented in a single device. The selected controller is a system on chip (SoC), which integrates in a single chip a field programmable gate array (FPGA) together with a microprocessor (Dual core ARM A9) and an ADC.

This control implementation is explained in detail in chapter 4. The rectifier part is modulated using "Modulation Method 1", explained in [Baumann'01], while the CFFB is controlled through a phase shift modulation. To avoid undesired resonances, an active clamp circuit (C_{aux} , M_{aux}) is added to the CFFB.

In order to analyze and explain the main contributions of this work, a simplified circuit is shown in Figure 34. Consist on two pulsating voltage sources, connected through a Link inductor. The voltage $v_d(t)$ represents the voltage across the freewheeling diode of the rectifier. In this simplification, it is considered square and with constant amplitude, the variation of the pulse width and the amplitude of $v_d(t)$

are determined by the modulation index, M and the input voltage $v_{in}(t)$, (where $\widehat{V_{in}}$ represents the peak amplitude of the line to neutral voltage). $v_{FB}(t)$ is the rectified voltage of the transformer of the CFFB which is also square. The pulse width is determined by d , which is the duty cycle of the square voltage applied to the transformer. The amplitude of $v_{FB}(t)$ depends on the turn ratio of the transformer and the output voltage of the converter.

Figure 34 a) Scheme simplified of the circuit b) Voltages and current in the Link inductor

The variables of the system are M and d . As it is appreciated in Figure 34 b), M , controls the average value of $V_d(t)$, fixing the maximum pulse width for each specific input voltage and d represents the pulse width of the voltage applied to the transformer in an ideal situation where there are no losses of duty cycle.

Analyzing this simplified circuit and controlling M and d , the voltage applied to the inductor can be controlled and consequently, the current ripple. To reduce the current ripple, both voltages should be synchronized. The synchronization is necessary for achieving the results explained in this thesis. With these premises, reducing the volts per second applied to this inductor, its size can be reduced. Controlling the amplitude of $V_{FB}(t)$ and $V_d(t)$ becoming both values as similar as possible and synchronizing them, in an ideal case, the inductor could be removed. Nevertheless, this situation does not occur when losses and non ideal waveforms are considered.

To analyze the current ripple that appear through the inductor, the first parameter that should be fixed is the turn ratio of the transformer, because the amplitude of $V_d(t)$ depends on this value being represented as $V_d = n V_o$.

Figure 34 b) represents $V_{FB}(t)$ and $V_d(t)$ synchronized and the resultant current ripple. The current ripple without consider parasitic effects is represented by equation (1), where L_{Link} is the inductance shared between the rectifier and the CFFB, n is the turn ratio, V_o the output voltage and f_s the switching frequency. For

this simplified analysis the pulse width used are M and d . There is two scenarios, first, when the pulse width of V_d is higher than V_{FB} and vice versa.

$$\Delta i(M, d_{eff}) = \begin{cases} \frac{(V_o n - \frac{3}{2} \hat{V}_{IN}) d}{L_{Link} f s} & \text{for } M > d \\ \frac{(\frac{3}{2} \hat{V}_{IN} - V_o n) M}{L_{Link} f s} & \text{for } d > M \end{cases} \quad (1)$$

Simplifying, the current ripple is ideally zero when equation (2) is fulfilled, where $\hat{V}_{IN}$ is the peak of $v_{in}(t)$ and V_o is the DC output voltage.

$$V_o n = \frac{3}{2} \hat{V}_{IN} \quad (2)$$

Therefore for a given input and output voltage, selecting n according to equation (3) the current ripple is ideally zero at $\hat{V}_{IN}$. During this chapter, the effect of the parasitic as well as the input voltage range on the current ripple is further analyzed.

$$n = \frac{3 \hat{V}_{IN}}{2 V_o} \quad (3)$$

Since the analysis is centered on the inductor, the volts per second are analyzed in order to find the relation between voltages, and control variables M and d . The volt per second balance in the inductor is given by equation (4).

$$V_o n d = \frac{3}{2} \hat{V}_{IN} M \quad (4)$$

$$M = \frac{2 V_o n d}{3 \hat{V}_{IN}} \quad (5)$$

Regarding equation (5), M and d are equal (Equation (6)) when the input voltage is equal to the value used to calculate the turn ratio n in (3)

$$d = M \quad (6)$$

This relation is shown in Figure 35.

Figure 35. *M and d relation*

This curve represents the relation of M and d when $v_{in}(t)$ is equal to the value used for the calculation of n , therefore (6) is complied. Selecting any point of this curve for a specific input voltage, the system provides the same output voltage and an ideally zero current ripple.

Ideally, for each input voltage there are infinite combinations of M and d that provides the same output voltage keeping a minimum current ripple in the inductor. Within all M and d values, the control should select a combination of them.

The criterion to select this combination is based on the efficiency of the converter provided for each point. Low values of M and d increase the rms value of the currents, increasing the conduction losses, therefore, it is recommended set the operating zone at high values of M and d , where the efficiency is higher. The efficiency drops specially for the Full Bridge stage. This fact is represented in Figure 36, where can be appreciated that for the same power transfer the shape of the current presents a higher rms value when d is lower, concentrating the power transfer in a considerably reduced period of time.

Figure 36. Current through the transformer depending on the duty cycle applied to the transformer for the same power transfer

In Figure 37 is represented an estimation of the efficiency in function of d , for a fixed M . The green square on the top represents a desired work space, with high values of M and d .

Figure 37. Estimated efficiency in function of d for a fixed M

This area represents the values of d and M where the resultant rms value of current is smaller, and the resultant conduction losses decreases.

In rectifier systems it is common to have an input voltage range, where the generator can vary its output voltage. Considering a wide input voltage range, the curve that relates M and d changes depending on the input voltage considered to achieve ideally zero current ripple. Three design cases for the turns ratio have been considered. As it will be observed in the equations of losses, conduction losses are predominant

3.1.1 Turns ratio design cases

- Case A

In this case the turn ratio of the transformer is calculated as $n = \frac{3 \hat{V}_{inMIN}}{2 V_o}$, ensuring ideally zero current ripple for minimum input voltage ($\hat{V}_{inMIN}$) of the input voltage range. Figure 38 shows the relations between M and d for a minimum, maximum and nominal input voltage.

Figure 38. M and d relation with value of n calculated for minimum input voltage

- Case B

In this case n is selected as $n = \frac{3 \hat{V}_{INnom}}{2 V_o}$, ensuring ideally zero current ripple for nominal input voltage ($\hat{V}_{INnom}$) of the input voltage range. Figure 39 shows the relations between M and d for a minimum, maximum and nominal input voltage. In this case, the curve of V_{INnom} is very close to the ideal one, nevertheless the minimum input voltage curve cannot use values of d higher than 0.7, losing regulation capability with d. The curve of V_{INmax} it is also limited in terms of M up to 0.78.

Figure 39. M and d relation with value of n calculated for nominal input voltage

Figure 40. M and d relation with value of n calculated for maximum input voltage

-
- Case C

Designing for $n = \frac{3\hat{V}_{iMAX}}{2V_o}$, ensuring ideally zero current ripple for maximum input voltage ($\hat{V}_{INmax}$) of the input voltage range, the resultant regulation map is shown in Figure 40. For the curve of $\hat{V}_{INmin}$ the range of d is limited up to 0.5, 50% of the whole range. Since this curve is so far from the curve of ideal zero current ripple, the current ripple will increase. These design criteria keep the ideal zero ripple for the maximum input voltage, but with just a brief variation of the input voltage, achieve low current ripple it is not possible.

3.2 Control strategies

In this section, possibilities of controlling the system are studied. There are two variables of control, M and d , to regulate the converter under input voltage changes and load steps. Each control strategy will be suitable for a turn ratio criterion. In the previous subsection three different calculation of n are presented. Each case studied corresponds with a control strategy proposed. Therefore, the selection of n affects to the regulation possibilities.

3.2.1 Strategy I: Fixing d , regulating with M

The first strategy proposed keeps constant d , the duty cycle of the CFFB, and regulates the system with M , the modulation index of the rectifier. This strategy is evaluated for the case A of the previous analysis, where the turn ratio is calculated for the minimum input voltage. This case is selected because since d will be fix, in the curve of M and d shown in Figure 41, d can be fixed with the higher point possible, and for every input voltage change or load changes, the rectifier will be able to regulate the system only with M . In Figure 41 it is appreciated the arrow of points that the control uses to regulate the converter. Considering that the efficiency is higher with high values of d and M , the point selected is situated in the upper and right side of the square as in Figure 37.

Figure 41. Regulation only with M in case A

3.2.2 Strategy II: Regulating with M and d

The second strategy proposes using both control variables. This strategy is evaluated when the turn ratio is calculated for having ideally zero current ripple at the nominal voltage, case B.

Figure 42. Regulation with M and d

3.2.3 Strategy III: Fixing M , regulating with d

The last strategy is similar to the first one, where the system is controlled only with one variable, and the other is fixed. In this case, the strategy fixes M , the modulation index of the rectifier, and regulates with d . This strategy is evaluated for the Case C, where n is calculated for having ideally zero current ripple with the maximum input voltage. As it is appreciated in Figure 43, with case C, every change in the input voltage can be solved only varying d .

Figure 43. Regulation only with d

3.3 Impact on the inductor energy depending on the control strategy

The control strategy affects the energy stored in the inductor, since these parameters affect to the voltage across this inductor. The value of the inductance is given by equation (7), where $\sqrt{3}\widehat{V_{in}}$ is the peak voltage in the freewheeling diode (equivalent to the line to line peak voltage), d is the duty cycle of the Full-Bridge, n is the turn ratio, V_o is the output voltage, f_{sw} is the switching frequency and Δi is the current ripple.

$$L = \frac{(\sqrt{3}\widehat{V_{in}} - \frac{V_o n}{d})(\sqrt{3}M)}{2f_s \Delta i} \quad (7)$$

As it is appreciated, the selection of M and d is relevant for the energy stored in the inductance. The regulation strategies can change this variables, modifying the current ripple. Additionally, the average current through the Link inductor depends

on the voltage v_d , which depends on the Modulation index M as it is represented in equation (8).

$$I_{avg} = \frac{P_o}{V_d} = \frac{2 P_o}{3 M \hat{V}_{in}} \quad (8)$$

$$E_{LINK} = \frac{1}{2} L_{LINK} i^2 \quad (9)$$

As can be appreciated in equation (8), the average current through the inductance depends on M and consequently on the regulation strategy. For the same amount of power under input voltage variations, the current through the inductance and consequently the energy stored in the inductance (calculated with equation (9)) are affected. For regulation strategy III, where M is constant, and II, where at least in a specific range of input voltage M is also constant, input voltage changes are appreciated in the amount of current. Increments on the current are analyzed in this section as increments of the total energy stored in the inductance.

Figure 44 shows the energy stored in the inductance for each regulation strategy in function of the input voltage for a specific value of inductance and power. As it is expected, low values of voltage, increment the current through the inductance in order to keep the same amount of power. The peak of energy which it is found it for low values of input voltage affects to the implementation of the inductance. A high value of energy is translated as an increment of volume of the core, in order to avoid a magnetic saturation.

Figure 44. Energy stored in the Link inductor for different regulation modes

Figure 44 shows how the different strategies of control affects to the energy stored in the inductance. One of the main aspects that define the peak of energy is the input voltage range. Considering the specific input voltage range of 80-150 V in Figure 44, regulation strategy III, reach the highest value.

However, in case a narrower input voltage range is considered, for example if the voltage range considered were very tiny, for example. 110-120 V, strategy I would present the peak of energy.

The behavior of each strategy is as follow.

Strategy I is constant the whole input voltage range because M is fixed, and the current through the inductance it is constant because changes in the input voltage, are compensated with M .

Strategy II presents two states. When is governed by M , the energy is constant, because M keeps the current constant through the inductance. Nevertheless for low values of input voltage, d is regulating the system and the current through the inductance increases.

Strategy III is changing in the whole range, because the system is regulated with M , therefore every change of M , modify the current through the inductance.

The selection of a specific strategy depends on the control necessities, however, analyzing the energy needed in the inductance before building the magnetic it is necessary to avoid future problems of saturation or overheating.

3.4 Volt per second reduction in the Link inductance

The reduction of the volts per second applied to the inductor is the main goal of the control strategies. In this point, the voltage applied and the resulted current ripple are studied. The reduction of the volts per second applied to the Link inductance helps to decreases size and volume of this element increasing the power density of the converter as well as decreasing the losses.

From the point of view of the inductor, the voltage v_d , follows an envelope with a period equal to a sixth of the input voltage, this voltage is represented in Figure 45. This voltage is square, and its frequency is in the order of hundreds of kHz, but its amplitude is modulated with this envelope. V_{FB} is also square, but its amplitude is constant. The basic idea to have the minimum volts per second applied to the

inductance, is synchronizing both voltages. This synchronization is feasible with a considerable reduction of the volts per second compared with a case where both voltages are random one respect to the other. In Figure 46 this situation of synchronization is represented at a time scale of switching frequency.

The advantage of the proposed solution, is the inclusion of the transformer, who besides of adding galvanic isolation, have the possibility of selecting the turn ratio of the transformer, and adjusting the voltage level. This parameter helps to increase the regulated input voltage range.

To keep the average value of v_d constant, during a sixth of the input voltage period, the pulse width of this signal is modulated, having the maximums when the amplitude of v_d is minimum and vice versa.

As can be expected, v_d is changing its amplitude and pulse width. Considering this and the fact that v_{FB} is keeping constant the amplitude, equation (10) calculate the current ripple through this inductance.

Figure 45. Envelope of v_d during a sixth of the input voltage period

$$v_d(\alpha) = \hat{V}_{in}\sqrt{3} \sin(\alpha) \text{ for } \frac{\pi}{3} < \alpha < \frac{2\pi}{3} \quad (10)$$

Therefore, considering the envelope of v_d , and assuming that $v_d(t)$ and $v_{FB}(t)$ are square and should be synchronized, with this assumption, two scenarios are possible: the duty cycle of $v_d(t)$ is higher than $v_{FB}(t)$ or smaller. The value of the ripple is different for each scenario and this is quantified in equation (11), where T is the period of the switching frequency.

$$\Delta i(\alpha) = \begin{cases} [v_{FB} - v_d(\alpha)] d \frac{T}{L_{Link}} & \text{for } v_{FB} > v_d(\alpha) \\ [v_d(\alpha) - v_{FB}] \frac{\hat{V}_{in} 3 M}{v_d(\alpha) 2} \frac{T}{L_{Link}} & \text{for } v_d(\alpha) > v_{FB} \end{cases} \quad (11)$$

Both scenarios are represented in Figure 46. The current ripple is smaller in Figure 46.a) where both voltages are very similar in amplitude and higher than voltage of Figure 46.b) where the differences of voltages provokes a higher current ripple.

Figure 46. a) $v_{FB} > v_d$ (a) b) $v_d > v_{FB}$

The evolution of the current ripple within a sixth of the input voltage period is shown in Figure 47. The current ripple is zero when both voltages are equal in pulse width and amplitude. The peak occurs for the peak input voltage where the pulse width of v_d is minimum.

Figure 47. Current Ripple in the Link inductor during a sixth of the input voltage period

3.5 Comparison of the energy stored in the inductance between the proposed solution and a classic Buck type rectifier for a specific case

One of the main goals of the proposed circuit is to improve the power density, therefore, in order to quantify this improvement, the results obtained are compared with a classic Buck type rectifier circuit. This comparison is carried out calculating the energy stored in the inductors of both circuits for the same specifications.

The reduction of the volts per second applied to the inductance in the proposed circuit compared with a classic Buck type rectifier is observed in the value of the energy. These two architectures are shown in Figure 48. The first Architecture a), is based on a Buck type rectifier and as a second stage, a Full-Bridge. Architecture b) is the proposed circuit.

As it is appreciated, in the proposed architecture (b), there is not output inductor. This fact helps to increase the power density, nevertheless, should be considered that in the proposed topology, the output capacitor need to store much more energy than the output capacitor of the classic solution.

Figure 48. a) Classic Architecture based on a Buck type rectifier with second stage based on a Full-Bridge b) Circuit Proposed, based on the Buck type rectifier and a Current Fed Full-Bridge

To quantify the improvement, the intermediate inductance needed is calculated for the proposed circuit, for a given input and output voltage, same modulation index

(M) for the rectifier, same switching frequency and current ripple through the inductance. Table 3 shows these specifications.

Table 3. Parameters considered for the comparison

V_o	48 V
$\hat{V}_{in}$	163 V
V_{DC}	200 V
f_s	200 kHz
M	0,82
d	0,82
n	4
Δi	2 A

During this chapter the impact of M and d in the efficiency are evaluated and the analysis shows that to obtain high efficiency, high values of d and M should be selected, concretely for this case, M=0,82 and d=0,82.

The inductance is calculated for the worst situation. This is, in a Buck type rectifier with fixed output voltage, when the voltage across the freewheeling diode is maximum. With equation (12) this inductance is calculated. In this equation, V_{DC} is the output of the rectifier (equation (13)), $\sqrt{3}\hat{V}_{in}$ is the peak of the line to line voltage, and the current ripple fixed is 20 % of the current through the inductance for the converter working at 2 kW, this is, 2 A. It is considered that the converter works with high values of M, however, the inductance should be calculated for the minimum M. The minimum M, which is obtained from the division of V_{DC} and $\sqrt{3}\hat{V}_{in}$ should allows the converter to reach the output voltage desired.

$$L = \frac{(V_{DC} - \frac{V_{DC}^2}{\sqrt{3}\hat{V}_{in}})}{f_s \Delta i} \quad (12)$$

$$V_{DC} = \frac{3 M \hat{V}_{in}}{2} \quad (13)$$

In the circuit proposed the worst case of current ripple occurs in the same interval than the previous circuit, for maximum voltage across the freewheeling diode (Peak of line to line voltage). However, in this case the voltage applied to the inductance is fixed by the output voltage and the turns ratio. Equation (14) calculates the inductance for the proposed circuit.

$$L = \frac{(\sqrt{3} \widehat{V_{in}} - \frac{V_o n}{d})(\sqrt{3} M)}{2 f_s \Delta i} \quad (14)$$

The values of inductances obtained are shown in Table 4, reducing the energy stored in the intermediate inductance in the proposed circuit for the same conditions up to 42 % respect to the basic circuit.

Table 4. Inductances obtained

L_{BUCK}	145 uH
L_{PROPOSEDCIRCUIT}	84 uH
Stored Energy reduction	42 %

It is important to notice, that selecting a higher value of n, the current ripple could be reduced, because the difference of voltages will be small, but, this fact would have a negative impact on the efficiency of the circuit.

3.6 Circuit Operation

The behavior of the circuit proposed have been explained with simplified models, however, in this section a detailed analysis is presented.

The operation of the circuit during a switching frequency period is presented, showing the most relevant waveforms. The waveform analyzed below to an interval of the input voltage where $V_R > V_S > V_T$. The waveforms are shown in Figure 57. The equivalent circuits for every interval are presented in annex I.

Interval t_0 - t_1 (Figure 49). The rectifier is in a freewheeling state, therefore there is not power transfer from the input to the output. M2 is switched OFF and M3 and M4 conduct the inductor current. During this interval, the voltage applied to the transformer is zero and the magnetizing current I_{Lmag} flows in primary. The parasitic capacitance of MOSFET M1 is discharged with the energy stored in the leakage inductance of the transformer allowing ZVS at medium and high power states. For

low power states, where the current through the transformer it is not enough to achieve ZVS during this commutation, the magnetizing current is used to achieve ZVS. Both output diodes are OFF and the capacitor provides the energy to the load.

Figure 49. Equivalent circuit interval t_0-t_1

Interval t_1-t_2 (Figure 50). M1 is switched ON and M3 is switched OFF and the current starts to circulate through the transformer and consequently through the secondary side diode. In the primary side of the transformer appear v_{FB} , which amplitude is (15), where n is the number of turn. The auxiliary path starts conducting the difference between inductor current and transformer current. In the initial state the inductor current is only the magnetizing current, therefore, initially, the auxiliary path conducts the whole inductance current through the body diode of the MOSFET.

$$v_{FB} = V_o * n \quad (15)$$

Figure 50. Equivalent circuit interval t_1-t_2

Interval t_2-t_3 (Figure 51). M_{R+} and M_{T-} are switched ON and the Freewheeling state ends. The voltage v_{RT} , appears in the freewheeling diode, therefore the slope of the Link inductor current decreases because the voltage applied is smaller. M_{aux} is

switched ON and the difference between inductor current and transformer current conducts by the MOSFET. Equation (16) relates these three currents.

$$i_L = i_T + i_{aux} \quad (16)$$

Figure 51. Equivalent circuit interval t_2 - t_3

Interval t_3 - t_4 (Figure 52). Once, M_R and M_T are ON, M_S is turned ON and the voltage applied to the freewheeling diode increases to v_{RS} , the difference between phase R and S. The current in the Link inductor has a ripple due to the difference between v_{RS} and v_{FB} . The volts per second applied to the inductor in this stage should be minimized as studied in this chapter, having v_{RS} and v_{FB} as similar as possible.

According with equation (16), the current through the auxiliary path is decreasing until crossing zero and the current in the transformer is increasing with a slope due to the leakage inductance.

Figure 52. Equivalent circuit interval t_3 - t_4

Interval t_4 - t_5 (Figure 53). The current in the transformer continue increasing, and the current of the auxiliary path becomes negative.

Figure 53. Equivalent circuit interval t_4-t_5

Interval t_5-t_6 (Figure 54). M_5 is switched OFF and the voltage applied to the freewheeling diode decreases to v_{RT} .

Figure 54. Equivalent circuit interval t_5-t_6

Interval t_6-t_7 (Figure 55). M_R is switched OFF, the voltage in the freewheeling diode drops to zero and another freewheeling state starts. The slope of the inductor current decreases. The current through the auxiliary path and the current in the transformer reach the maximum value, i_L , and $2 * i_L$, respectively.

Figure 55. Equivalent circuit interval t_6 - t_7

Interval t_7 - t_8 (Figure 56). The interval of power transfer to the secondary ends by switching OFF the MOSFET M_{aux} and switching ON M_2 , creating a short circuit in one branch, that conducts the whole Link inductor current.

Figure 56. Equivalent circuit interval t_7 - t_8

Figure 57. Waveforms of the proposed circuit

3.7 Design issues

Design guidelines for the proposed converter are addressed in this section. A specific design with the requirements presented in Table 5 it is included to quantify and validate the design guidelines.

Table 5. Specifications for the proposed design

$\widehat{V}_{IN}$	$115\sqrt{2} V_{ac} (108\sqrt{2} - 118\sqrt{2} V_{ac})$	P_o	2 kW
V_o	48 V _{DC}	PF	> 0,95
Input Frequency	400 Hz (398-403 Hz)	THD	< 10%
f_{sw}	210 kHz		

3.7.1 Power stage

The main contribution of this work, is to analyze how to design and control a Three-Phase Buck type Rectifier integrated with a Current Fed Full-Bridge achieving the smaller inductive value possible.

The basic idea of reducing the inductor size is based on synchronizing the voltages across the inductor in order to reduce the volts per second applied to the inductor. Being both voltage waveforms very similar, the next step is to make the corresponding amplitudes as similar as possible. The transformer provides to the circuit galvanic isolation and also, another degree of freedom for the converter, the turn ratio. The turn ratio allows the designer to change the voltages to the inductor. The voltage that impose the Full-Bridge to the inductor, is the output voltage, referred to the primary side. Since this parameter cannot be modified during the operation of the circuit, should be calculated at the beginning, considering the impact that this parameter has on the operation.

Assuming a regulated output voltage, the main parameter that should be analyzed to calculate n and to achieve a low value of current ripple, is the input voltage range. In a circuit where the input voltage range is very limited, the calculation of n has no discussion, n should allow that the average voltage imposed by the rectifier after the Freewheeling diode is as similar as possible to the maximum voltage in the primary of the transformer (Equation (17)).

$$V_o n = \frac{3}{2} \hat{V}_{IN} \quad (17)$$

Nevertheless, for wide input voltage ranges, the value of V_{in} used for the calculation of n will depend on the control strategy selected.

During the explanation of the control strategies and the inductor current, the relation between the parameters M and d has been considered ideal.

In this section, the real relation is presented including the parasitic. In equation (18) the ideal gain of the circuit in function of the control parameters is presented. Since, there are losses in the duty cycle that represents d and the real duty cycle applied to the transformer, equation (20) consider this effect. When a voltage is applied to a primary side of a transformer, the real voltage that appears in the secondary has lost a percent of the initial duty cycle applied. This fact is due to the leakage inductance. When the voltage applied to the primary side, the current should increase with a slope depending on the value of the leakage inductance (L_{lk}), therefore, if L_{lk} is high, the slope is lower and the time needed to reach the desired current is higher.

This effect is observed in Figure 58, where the voltage v_{T2} has a pulse width shorter than v_{T1} , which is the voltage applied by the Full Bridge to the transformer.

Figure 58. Duty cycle loss due to the leakage inductance

Regarding this effect, the ideal relation between input and output voltage, depends only of M and d (equation (18)). In this equation is considered that the duty cycle applied to the Full-Bridge is represented in the output, with the same value. Nevertheless, in the transformer, there are losses of duty cycle [Sabate'90]. The bridge, applies a duty cycle to the primary of the transformer, but regarding the secondary of the transformer, can be observed that the pulse width obtained has decreased respect to the primary pulse width. In Figure 58 is appreciated this effect. This duty cycle lost is due to the overlapping time K_{tov} in the pairs of switches M1-M3 and M2-M4 and due to the finite slope of the current through the transformer. The current slope is limited by the parasitic of the transformer, therefore, as large is the leakage as large is the duty cycle lost.

Therefore, (18) is transformed in (19)(22), where this effect is considered. In this new equation, R represent the dependency on the load of the value of the current through the transformer. As it has been explained, the duty cycle loss is produced during the time K_{tov} , and is proportional to the leakage inductance.

$$2 V_o n d = 3 M \hat{V}_{IN} \quad (18)$$

$$2 V_o n d = 3 M \hat{V}_{IN} - L_{lk} \frac{2 V_o}{R n (d + K_{tov}) T} \quad (19)$$

The representation of equation (19) in function of M is represented in (20).

$$M = \frac{(d^2 n^2 + d n^2 K_{tov} + 2 \frac{L_{lk}}{R T}) V_o}{[d n + n K_{tov}] 3 \hat{V}_{in}} \quad (20)$$

Figure 59 shows a particular case to compare the differences between the real and the ideal relation of M and d. This particular case is calculated with the parameters of Table 5.

As it is appreciated in Figure 59, the differences of the real and the ideal are higher for low values of M and d. This is due to the increment of the current through the transformer, increasing the loss of effective duty cycle. Therefore, in order to maintain the desired output voltage, this effect is compensated with an increment of M.

Figure 59. Required modulation index (M) of the rectifier as a function of the duty cycle (d) in the Full-Bridge

Since the input voltage range for this particular case is narrow (108-118V) as it is appreciated in the limit curves for maximum and minimum input voltage of Figure 60, the regulation strategy selected is I, which regulates the system with M keeping

d fixed. In order to obtain a high efficiency, the typical working point is placed in the right upper corner ($d=0.85$ and $M=0.85$).

Figure 60. Required modulation index (M) of the rectifier as a function of the duty cycle (d) in the Full-Bridge for maximum, minimum and nominal input voltages

3.7.2 Soft Switching operation

The analysis of the ZVS is addressed in this section. In order to reduce the number of magnetics of the system, the transformer leakage inductance should be included in the operation of the system to obtain soft switching transitions without adding any external inductance. Figure 61 shows how the energy stored in the leakage inductance is used to discharge the parasitic capacitance of M1 and M2. The current through the primary is represented as i_T and the voltage applied as v_{FB} . The voltages V_{DS1} and V_{DS2} are discharged when the auxiliary circuit is opened with the energy stored in the leakage inductance. These waveforms are obtained for high power situations, where the current through the primary is high during the commutation.

Figure 61. ZVS situation at high load states

Nevertheless, during light load states, the current through the transformer during the commutation instant is very small, and not enough to achieve ZVS. Figure 62 shows a very light load state where the current through the transformer is very low when the commutation occurs, therefore the switches of the upper side, M1 and M3 do not have enough current and consequently energy in the leakage inductance to discharge the parasitic capacitance of M1 as it is shown in the Figure 62. The switches of the low side have more time to discharge the capacitance, therefore can keep ZVS for a wider power range.

Figure 62. NO ZVS situation at light load states

To solve this problem, the current through the magnetizing current is introduced in the operation. The value of the current needed is obtained decreasing the magnetizing inductance. In Figure 63 the commutations of the switch M1 is done under almost no current conditions, therefore, the magnetizing current helps to discharge these capacitors. In this figure, in the current through the primary shows that is the result of the primary current plus the magnetizing current, i_{Lmag} .

Figure 63. ZVS at high load states

The value of the leakage and magnetizing inductance needed should be calculated according with [Sabate`90].

To achieve the desired leakage inductance, techniques of interleaving should be used in the design of the transformer.

The ZCS operation only is achievable in switches M_2 and M_4 due to the natural operation of the circuit. When the auxiliary switch is open and both low side switches are conducting, zero volts are applied to the transformer, and the current drops with a slope dependent of the output voltage referred to primary and the leakage inductance. During the overlapping time between both switches, the current drops to zero, allowing ZCS operation. Figure 64 shows this phenomenon.

Switches M_1 and M_3 are carrying the input current during the commutation and do not present ZCS.

Figure 64. ZCS operation in the low side switch

3.8 Semiconductor Losses

The power losses consist of the losses in the semiconductors, losses in the magnetic components and losses in the EMI filter. The losses in the magnetic components are calculated using the tool PExprt from ANSOFT. The losses in the semiconductor of the rectifier part are calculated as shown below, based on the analysis of [Nussbaumer'07]:

$$I_{DS,avg} = I_{s,avg} = \frac{\hat{I}_N}{\pi} \quad (21)$$

$$I_{DS,rms} = I_{s,rms} = \frac{\hat{I}_N}{\sqrt{M} \pi} \quad (22)$$

$$I_{DF,rms} = \left(\frac{1}{M} - \frac{3}{\pi} \right) \hat{I}_N \quad (23)$$

The equations (21), (22) and (23) represent the current through the switches (S), series diode (DS) and freewheeling diode (FW).

Conduction losses are calculated with (24), (25) and (26).

$$P_{c,S} = 6 I_{s,rms}^2 R_{ds} \quad (24)$$

$$P_{c,DS} = 6(I_{DF,rms}^2 R_{ds} + I_{DS,avg} V_D) \quad (25)$$

$$P_{c,DF} = (I_{DF,rms}^2 R_{ds} + I_{DS,avg} V_D) \quad (26)$$

Equations (27) and (28) stand for the total switching losses of the rectifier.

$$P_{OFF,total} = \frac{6}{\pi} V_N^2 \left(\frac{1}{2} C_{O,S} + \frac{3}{2} C_{O,D} \right) \left(\frac{14\pi - 9\sqrt{3}}{32} \right) \quad (27)$$

$$P_{ON,total} = \frac{6}{\pi} V_N \frac{\sqrt{3}}{4} I_L t_{tr} f_{sw} \quad (28)$$

$$I_{LINK} = \frac{P_o \sqrt{2}}{M V_{in,rms} 3 \eta} \quad (29)$$

$$I_{M,rms} = \sqrt{\left(\frac{1}{T} \right) \left(\frac{4 I_{LINK}^2 t_a}{3} + I_{LINK}^2 t_b \right)} \quad (30)$$

$$I_{Maux,rms} = \sqrt{\left(\frac{1}{T} \right) \left(\frac{2 I_{LINK}^2 t_a}{3} \right)} \quad (31)$$

$$I_{D,avg} = \frac{P_o}{2 V_o} \quad (32)$$

$$t_a = d \frac{T}{2} - t_d \quad (33)$$

$$t_b = PW - d \frac{T}{2} - OV \quad (34)$$

PW is the width of the pulse, OV is the overlapping time between the MOSFETs and T is the switching period.

The currents through the principal MOSFETs, the auxiliary MOSFET and the diodes in the secondary side are represented in (29), (30), (31) and (32). Conduction losses are calculated in (35) as explained in [Stupar'12], in respect to the switching losses; all the switches have ZVS but only low side MOSFETs present ZCS, therefore

Equation (36) accounts for the switching losses due to the turn off of these two MOSFETs.

$$P_{c,M} = 4 I_{M,rms}^2 R_{M,ds} + I_{Maux,rms}^2 R_{Maux,ds} \quad (35)$$

$$P_{off,M} = \left(V_{FB,MAX}^2 I_{off} \frac{t_{ru} + t_{ri}}{2} \right) \frac{f_{sw}}{2} \quad (36)$$

An example for a particular case, based in the specifications of Table 5 shows that the losses of the system are principally conduction losses, as it is appreciated in Figure 65. Since, the goal of this work it is not optimizing the circuit from the efficiency point of view, it has not been analyzed possible improvements in the efficiency curve, adding semiconductors in parallel or other techniques to reduce conduction losses.

Figure 65. Efficiency and breakdown of losses

3.9 Conclusions

In this chapter the main contribution of this thesis is presented, an integrated Three-Phase buck type rectifier with an isolated DC/DC converter based on a current fed Full-Bridge working synchronized. The topology has only two magnetic components because both stages share the intermediate inductor.

There are two variables of control (M and d), one for each stage, the relation between them is analyzed for a fixed input and output voltage. The result of this analysis is that high values of M and d helps to improve the efficiency because low values of d , increases the rms value of the current through the transformer, increasing the losses.

The selection of the turn ratio of the transformer has an important impact on the control, because affects to the relation between the control variables M and d . The conclusion is that the optimum value of n should be using the nominal values of the input referred to the intermediate stage and the output voltage. For a variable input voltage, the best option is to select the intermediate value.

Considering both control variables, three different strategies have been analyzed. The conclusion is, for very restrictive specifications of bandwidth in the control, the strategy of vary M and d is the most appropriate. However, for a non very demanding requirements, fix d at a studied value, allowing high efficiency of the full bridge and regulate the system with M , is a very simple and useful solution. The strategy of regulating only with d can affects considerably to the efficiency, therefore, it is not recommended.

The strategy selected will affects to the inductor design, because each strategy changes the current through the inductance, and consequently the energy stored.

Some design issues have been discussed. Since the switching losses in a Full-Bridge can be very important, soft switching is studied, with the goal of does not add an external inductance. For high power states, the circuit achieves ZVS using the energy of the leakage inductance. Nevertheless, for light load states, ZVS becomes more complex, because when switches that commutates with almost zero current through the transformer ($M1$ and $M3$) there is not enough energy stored in the leakage inductance to discharge the parasitic capacitances, therefore, the magnetizing current has to be incremented and used to achieve ZVS at light load states. Of course, incrementing this current, the circulating currents and the conducting losses are also incremented.

ZCS it is achieved in a natural way for the two low side switches, nevertheless, increase the magnetizing inductance can slow down the total ZCS, having a commutation with the magnetizing current through the switch.

As it has been appreciated, one of the key points of the design is the transformer, where the magnetizing inductance and the leakage inductance need to be calculated with detail. Another effect to be considered from the leakage inductance, is the duty cycle loss produced due to the finite slope during the transitions which is considered during the analysis of the gain of the circuit.

3.10 References

- [Uan-Zo-li'03] Uan-Zo-li, A.; Burgos, R.; Wang, F.; Boroyevich, D.; Lacaux, F.; Tardy, A., "Comparison of prospective topologies for aircraft autotransformer-rectifier units," Industrial Electronics Society, 2003. IECON '03. The 29th Annual Conference of the IEEE , vol.2, no., pp.1122,1127 Vol.2, 2-6 Nov. 2003
- [Seixas'04] Seixas, F.J.M.; Barbi, I., "A 12 kW three-phase low THD rectifier with high-frequency isolation and regulated DC output," Power Electronics, IEEE Transactions on , vol.19, no.2, pp.371,377, March 2004
- [Cortes'14] Cortes, P.; Bortis, D.; Pittini, R.; Kolar, J.W., "Comparative evaluation of three-phase isolated matrix-type PFC rectifier concepts for high efficiency 380VDC supplies of future telco and data centers," Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on , vol., no., pp.1,10, 26-28 Aug. 2014.
- [Silva'13] Silva, M.; Hensgens, N.; Molina, J.M.; Vasic, M.; Oliver, J.; Alou, P.; Garcia, O.; Cobos, J.A., "Interleaved multi-cell isolated three-phase PWM rectifier system for aircraft applications," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1035,1041, 17-21 March 2013
- [Malesani'87] X. Li, G. C. M. Meijer, R. de Boer, M. Van der Lee, "A High-Performance Universal Interface", in *Proceedings of the 1st ISA/IEEE Conference on Sensors for Industry*, pp. 19 – 22, Rosemont, Illinois, USA, November 2001.
- [Nussbaumer'07] Nussbaumer, T.; Baumann, M.; Kolar, J.W., "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," Power Electronics, IEEE Transactions on , vol.22, no.2, pp.551,562, March 2007.
- [Watson'96] Watson, R.; Lee, F.C., "A soft-switched, full-bridge boost converter employing an active-clamp circuit," Power Electronics Specialists Conference, 1996. PESC '96 Record., 27th Annual IEEE , vol.2, no., pp.1948,1954 vol.2, 23-27 Jun 1996
- [Baumann'00] Baumann, M.; Drofenik, U.; Kolar, J.W., "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a

DC/DC boost converter output stage," in Telecommunications Energy Conference, 2000. INTELEC. Twenty-second International , vol., no., pp.461-470, 2000

[Baumann'08] Baumann, M.; Nussbaumer, T.; Kolar, J.W., "Comparative evaluation of modulation methods of a three-phase buck + boost PWM rectifier. Part I: Theoretical analysis," Power Electronics, IET , vol.1, no.2, pp.255,267, June 2008.

[Chen'08] Ren-Yi Chen; Tsorng-Juu Liang; Jiann-Fuh Chen; Ray-Lee Lin; Kuo-Ching Tseng, "Study and Implementation of a Current-Fed Full-Bridge Boost DC-DC Converter With Zero-Current Switching for High-Voltage Applications," Industry Applications, IEEE Transactions on , vol.44, no.4, pp.1218,1226, July-aug. 2008

[Baumann'01] Baumann, M.; Kolar, J.W., "Comparative evaluation of modulation methods for a three-phase/switch buck power factor corrector concerning the input capacitor voltage ripple," in Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual , vol.3, no., pp.1327-1332 vol. 3, de2001

[Sabate'90] Sabate, J.A.; Vlatkovic, V.; Ridley, R.B.; Lee, F.; Cho, B.H., "Design considerations for high-voltage high-power full-bridge zero-voltage-switched PWM converter," in Applied Power Electronics Conference and Exposition, 1990. APEC '90, Conference Proceedings 1990., Fifth Annual , vol., no., pp.275-284, 11-16 March 1990.

[Nussbaumer'07] Nussbaumer, T.; Baumann, M.; Kolar, J.W., "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," Power Electronics, IEEE Transactions on , vol.22, no.2, pp.551,562, March 2007.

[Doval-Gandoy'00] J. Doval-Gandoy, and C. M. Penalver. "Dynamic and steady state analysis of a three phase buck rectifier." Power Electronics, IEEE Transactions on, vol. 15, no. 6, pp. 953-959, Nov. 2000.

[Stupar'12] A. Stupar, T. Friedli, J. Miniböck, M. Schweizer, and J.W. Kolar, "Towards a 99% efficient three-phase buck-type PFC rectifier for 400 V DC distribution systems," Power Electronics, IEEE Transactions on, vol. 27, no. 4, pp. 1732-1744, Apr. 2012.

[Molina'15] Molina, J.M.; Alou, P.; Oliver, J.A.; Silva, M.; Cobos, J.A., "Three-Phase Buck type Rectifier topology integrated with Current Fed Full-Bridge," Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE , vol., no., pp.84,91, 15-19 March 2015.

Chapter 4

Digital Control: Control Strategies, Modulations and Implementations

4 Introduction

In the previous chapter the control strategies proposed are theoretically analyzed, however, in this chapter the implementation is discussed.

In this chapter, the influence of the platform where the control is implemented is analyzed. Several implementation alternatives are compared in detail. The results of this comparison will determine the most appropriate platform depending on the requirements of the system.

4.1 *Digital Control implementation alternatives*

Within the digital control, researchers and industry are implementing three main options in the actual designs: Microcontrollers, DSPs and FPGA. Microcontrollers are the slowest, when complex operation are needed, therefore they are not considered in this analysis. DSPs are devices similar to microprocessors, executing the process sequentially. However, FPGA lacks of predefined architecture, are blank circuits, where the user creates the hardware for each specific function. From a functionality point of view, DSPs execute the operations in a sequential order, while FPGA can execute the operations in parallel.

This behavior is a design constrain when the number of operations is high, because the time of execution of the control can be long. In Table 6, a commercial DSP (Piccolo TMS320F28075) and a FPGA (Spartan 3 LX45) from Xilinx are compared. In this table, both low cost devices are compared in the terms of the internal architecture as the number of MMACS (Millions Multiply-accumulate per second), the number of processors and the functionality. The number of PWM outputs is also compared: while in the DSP are determined by the model, in the FPGA depends on the maximum of I/O pins available.

The importance of the parallel operation affects in the time needed for the loop execution, where parallel operation can help to reduce the execution time.

Table 6. Comparison between a DSP Piccolo from TI, TMS320F28075 and an FPGA, Spartan 3 XC3S50 from Xilinx

	DSP Piccolo TMS320F28075	FPGA Spartan 3 XC3S50A-4VQG100C
Performance	240 MMACS (floating point unit)	14500 MMACS (fix point)
Peripheral	Fixed	Flexible
Processor Cores	Dual	Multiples
PWM OUTPUTS	24	68
Modulation Scheme	Flexible PWM	Flexible PWM
ADC	3 channels (3,1 MSPS)	NO
Design Environment	C (Higher Level of Abstraction)	VHDL/Verilog
Cost per chip	10 €	7,36 €

Low cost DSP are simple and usually include ADC in the same chip. The execution time in a low cost FPGA can be higher but in low cost FPGA the ADC it is not usually included in the system. Therefore, an additional chip has to be implemented, increasing the BOM of the system.

There are new devices in the market that combines microprocessors and FPGA including an ADC, theses devices are known as System on Chip (SoC). The series Zynq from Xilinx are SoC that include two ARM cores in silicon, an ADC and Programmable Logic. Figure 66 shows the internal architecture of a Zynq. As it is observed, there are a lot of internal IP already developed to be used in the designs, just using this single chip.

Figure 66. Internal architecture of a Zynq series

These devices provide the advantages of the FPGA and the DSP, but also increment the difficulty of being configured and used. Additionally, one of the main disadvantages of these devices is the consumption. Nowadays, SoC devices present higher consumptions than DSP or classic FPGAs.

In Table 7 a comparison between features of a DSP commonly used for control power converters and the Zynq SoC is presented. In this table, it is appreciated that both systems are very powerful. In both devices there are two cores, DSP cores are

optimized for calculations, managing PWMs and ADC, allowing communications with low power consumption. The ARM A9 cores included in the Zynq device, are very powerful compared with the microprocessors included in the common DSPs, but does not include PWM modules (or other modules included that helps during the design of a control) which should be designed by the user, while in the DSP are already included. The complexity is the main constrain of the SoC. The advantage is: the number of PWM modules needed by the user it is only limited by the number of outputs of the chip. Both include in the same chip an ADC, which reduce the number of chips in the system. In Table 7, it is also shown, that the Zynq chip, since is a new device, it is considerably more expensive than the DSP.

Table 7. Comparative between a DSP from TI and a SoC from Xilinx

	DSP TMS320F28377D	Zynq XC7020
PWM Modules	24	Limited by the output pins
Cores	2 X 32 bits 200 MHz	2 x ARM A9 32 bits 667 MHz
ADC	4 inputs (16 bits/1.1MSPS or 12 bits/ 3.5 MSPS)	17 inputs Dual channel 12 bits 1 MSPS
MIPS/CLOCK FREQUENCY	800 MIPS	250 MHz
DAC	3	NO
Operating System	NO	LINUX BASED
Cost EB/CHIP	159 € / 29 €	495 € / 99 €
Power Consumption	1,2 W	2 W
Connectivity	SPI/UART/CAN/I2C/USB	USB/SPI/UART/I2C/VGA/ HDMI/AUDIO
Control Design Complexity	Low	High
Supply Design Complexity	Low	High

To conclude this part, two very powerful devices are compared, a Delfino DSP from TI and a Zynq SoC from Xilinx. In this case both includes not only the ADC in the chip, also several blocks of communications and peripherals. As presented in the previous comparison, DSP are optimized for controlling converters, and SoC are not. Therefore, the complexity of using SoC is higher. However, the inclusion of two

ARM A9 makes this device very powerful for many applications. In order to analyze the possibilities of a SoC for controlling power converters, in this thesis, a SoC device is used to control the power stage.

4.2 Control Architecture of the Converter

The control architecture proposed in this thesis is represented together with the power stage in Figure 67. As can be appreciated in this figure, the strategy I, which in Chapter 3 is selected for the specific case of this thesis only needs to measure the input voltages and the output voltage. The input voltages are measured to create the modulation and the output voltage to regulate the converter.

Figure 67. Block diagram of the control connected to the power stage

4.2.1 Filtering of measurements

To filter the measurements, a digital IIR (Infinite Impulse Response) filter is applied. If the sampling frequency of this filter is the switching frequency, aliasing problems are avoided and the noise due to this frequency is also rejected. This IIR filter is designed to filter without adding significant phase to delay the measurements. The diagram of this filter is shown in Figure 68. In this filter, the output is dependent on the current input as well as previous inputs and outputs.

Figure 68. IIR filter architecture

For this system, a second order low pass filter has been selected, where its transfer function is shown in (37).

$$\frac{y(n)}{x(n)} = \frac{a_2 z^2 + a_1 z + a_0}{b_2 z^2 + b_1 z + b_0} \quad (37)$$

The filter is implemented in the ARM core. Designing the filter in the ARM allows to develop a second order filter, without increasing the complexity of the implementation and reaching the desired execution time of the filter.

Nevertheless, for high bandwidth requirements it is recommended to implement the filter in the Programmable Logic to accelerate the execution time.

4.2.2 PLL (Phase Lock Loop)

In order to be synchronized with the input voltage to achieve unity power factor, a PLL is introduced in the system. This PLL estimates the angle of the measured voltages, adding an offset, to compensate the delay introduced by the capacitance of the filter. With this estimated angle, the sector is detected to apply the corresponding modulations

The block diagram of the PLL implemented in the ARM is shown in Figure 69, where θ_{ref} is the angle reference, which will correct the error between the real voltage and the measured after analog and digital filters. The angle $\theta_{estimated}$ is

obtained after doing the transformation of the voltages V_R , V_S and V_T to the d,q domain, through the operations shown in equations (38), (39) and (40).

In principle, V_{qref} and the angle θ_{offset} should be zero. However, if the measurements present a delay, θ_{ref} can be modified, in order to correct the error. For example, the delay introduced by the filters, can be corrected introducing a value of θ_{ref} different from zero.

Figure 69. PLL diagram

$$\begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (38)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta) \end{bmatrix} \begin{bmatrix} \alpha \\ \beta \end{bmatrix} \quad (39)$$

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \gamma) & \cos(\theta + \gamma) \\ -\sin(\theta) & -\sin(\theta - \gamma) & -\sin(\theta + \gamma) \end{bmatrix} \begin{bmatrix} V_R \\ V_S \\ V_T \end{bmatrix} \quad (40)$$

The output of the controller PI is ω , the angular frequency, and integrating it, the result is the estimated angle.

This PLL is implemented in the ARM core. Once the voltages are measured, filtered and reconstructed with the estimated angle by the PLL, these voltages are used to detect the sector and to modulate the rectifier.

In a system with more restrictive specifications of Bandwidth, the PLL could be implemented in the FPGA to reduce the execution time.

4.2.3 Output Voltage Controller

The controller for the output voltage is implemented with a PI regulator. In this case, the regulator is implemented in the ARM.

The transfer function of the controller used is represented in equation (41).

$$\frac{y(n)}{x(n)} = \frac{a_0 + a_1 z^{-1}}{1 - z^{-1}} \quad (41)$$

The block diagram of the PI regulator, with transfer function expressed in (41), is shown in Figure 70. Where e_k is the current error and e_{k-1} the error from the past registered at sampling frequency. The coefficients a_0 and a_1 are calculated in Matlab for the sampling frequency equal to the switching frequency of the Full-Bridge.

Figure 70. Block diagram of PI regulator

This regulator has been developed also in the FPGA to test the functionality. The Zynq device includes MAC blocks for multiplications where operation between signals of 18 x 25 bits can be introduced. This fact is used for giving as much precision as possible in the operations with the coefficients.

The regulator developed in the FPGA is shown in Figure 71. The difference respect to the previous design, is that, in order to obtain the best timing result, the intermediate signals are registered at the higher frequency possible. This frequency is the clock frequency of the FPGA block and it is limited by the critical paths.

In Figure 71 it is appreciated where has been placed this high frequency registers.

Figure 71. Scheme of the PI implemented in the programmable logic

4.2.4 Three Phase Buck type rectifier modulation

This block creates the PWM duty cycles based on some assumptions in order to simplify the calculations as it is detailed in [Nussbaumer'07]. These assumptions for the applied modulation are:

The filter capacitor voltages $V_{Cin,i}$ at the input of the rectifier are purely sinusoidal and are in phase with the mains phase voltages $V_{in,i}$, then $V_{Cin,i} \approx V_{in,i}$ ($i=R,S,T$) with:

$$V_{in,R} = \hat{V} \cos(\theta_{estimated}) \quad (42)$$

$$V_{in,S} = \hat{V} \cos(\theta_{estimated} - \frac{2\pi}{3}) \quad (43)$$

$$V_{in,T} = \hat{V} \cos(\theta_{estimated} + \frac{2\pi}{3}) \quad (44)$$

- Where $\theta_{\text{estimated}}$ is the angle estimated by the PLL. Therefore, the voltage drop across the input inductors is neglected.
- The mains currents are assumed to be equal to the fundamental component of the rectifier input currents therefore the reactive currents due to the filter capacitors are also neglected.
- The current through the Link inductors is assumed to be constant, the ripple due to the switching frequency is neglected.

This modulation divides the full period of the input voltage in 12 intervals (each 30°), in Figure 72, the author [Nusbaumer'07] describes the different intervals, determined by the different relations of the instantaneous voltages.

In the ANEX I, the modulation sector is presented in detail.

Figure 72. Main phase voltages represented as V_{Ni} (for $i=R,S,T$), line to line voltages $V_{N, RS}$, $V_{N, RT}$, $V_{N, SR}$, $V_{N, TR}$, $V_{N, TS}$ and the 12 sectors defined sectors[Nussbaumer'07]

In [Baumann'07] four modulation methods are proposed for this converter. In this thesis, modulation method 1 is used because it reduces the losses respect to the others.

Figure 73. Modulation methods studied by [Baumann'07]

Using this modulation method, the duty cycle is calculated for each switch and send it to the PWM generators. These blocks, designed in the FPGA, compare the duty cycle generated by the modulation with a triangular waveform, generating the PWM.

4.2.5 Modulation of the Current Fed Full-Bridge Phase Shift

The control of the full bridge is based on a phase shift modulation. There are several strategies proposed in Chapter 3. Depending on the strategy selected, the phase shift is fix or variable. For the strategy used in this thesis, the phase shift is fixed. The FPGA block that generates the PWM signals for the Full-Bridge, considers the overlapping time, and includes an auxiliary switch, for the auxiliary circuit [Watson'96]. The representation of this modulation is shown in Figure 74.

Figure 74. Phase Shift Modulation for a Full Bridge considering the overlapping times

4.2.6 Sampling of Measurements

Measurements are sampled with the ADC included in Zynq. The internal ADC of the Zynq, is a peripheral that is connected through the internal BU. The internal Bus included in the Zynq is called AXI BUS, and connects the FPGA part, the ARM cores and the peripherals as the ADC.

The ADC is dual, and has 17 multiplexed inputs, and a maximum sample frequency of 1 MSPS. The ADC is able to sample at this frequency 2 channels at the same time, nevertheless, for each pair of channels added, the sampling frequency is divided by 2.

The ARM cores that are connected to the AXI Bus include a software driver to manage the ADC. This software allows the user to select the mode of operation, the channels to be enabled and it also includes functions to perform averages.

This way to use the ADC is very simple, but has some timing constraints. Since, the ADC is connected to the AXI BUS, the driver has to ask for measurements in series and then, the ADC sends the measurements to the ARM through the AXI Bus. The resultant delay of this process is relatively high, around 1 μ s for each measurement. If we consider that the ADC needs 1 μ s to make a conversion, the total time spent to have the measurement in the ARM is 2 μ s.

Another way to manage the ADC is using a hardware driver in VHDL, from the IPs provided by the manufacturer. This driver asks for samples to the ADC in specific instants, and having the samples with minimum delay. After that, this driver can send the measurement to the ARM or to other hardware block. In this last case, there is not delay, and the block can obtain the samples with the only delay of the sampling frequency of the ADC, 1 us.

Details about the impact on the ADC mode will be given in the next section.

4.3 *Alternative Implementations of the control in a Zynq*

In this subsection, different implementations of the control in a Zynq device are discussed and compared in order to find the optimal design in terms of execution time.

Table 8. Blocks definitions

ADC	Measurement from the ADC
VL	Voltage Loop including a PI regulator
IIR	Second Order Digital Filter Infinite Impulse Response
PLL	Phase-Locked Loop
dq	$\alpha\beta$ to dq Transformation
PT	Park Transformation
WR	Time needed to write the duty cycle in the hardware block
HW delay	Delay to write from the microprocessor to the Programmable Logic
WRM	Time to write the ADC measurement from ADC Driver to the microprocessor

First at all, some considerations of the architecture are going to be explained. The connection between the microprocessors (in this architecture only one is used), peripherals and FPGA is made through an internal bus. When the information travels through the bus, the bus adds a delay. Therefore, to achieve the faster response possible, the connection through the bus, should be minimized, connecting

signals between peripherals without using the BUS. For example, one of these signals can be the duty cycle from a regulator block to a PWM generator block, connecting this signal by hardware between blocks without use the bus minimize the critical path for the time constraints.

In the designs shown below, the blocks of the control are implemented in software and hardware, and the resultant timing is compared.

Table 8 describes the blocks with the acronyms that will be used in the following section. Additionally, these designs have been done for the circuit studied in this thesis, with the following switching conditions: The Buck rectifier working at 210 kHz (9,52 us) and the Full Bridge working at 105 kHz (4,76 us).

In the information provided below the operations made in the software use the floating point unit and the operations in the FPGA use fix arithmetic point with resolution of 25 bits for the coefficients of the controllers.

4.3.1 Architecture A: ADC managed by software, blocks with complex operations, regulators in the ARM and PWM generators in FPGA

This architecture is represented in Figure 75. This implementation manages the ADC from the microprocessor, which is also in charge of the blocks that include operations with sines or cosines and the regulators. Also the communication with the user is made through the ARM processor. The user can modify the voltage reference or the regulator parameters through this communication. Every block that needs a signal from the ADC is in the microprocessor, therefore, the ADC samples only crosses the AXI BUS once.

The Park transformation block generates the signals that the modulator, implemented in hardware, uses to build the PWM signals. Also, the block that creates the PWM signals for the Full-Bridge is implemented in hardware.

Figure 76 shows the scheduling in time of this implementation. In the figure are represented the tasks that are implemented in the microprocessor (the PWM generators implemented in the FPGA are not included because the time consumption is negligible compared with the task developed by the ARM core).

Figure 75. Architecture A

Figure 76. Time needed for each task of Architecture A in scale

In Table 9, the time required by each task is shown. In order to avoid aliasing problems, the sample frequency is selected to be equal to the switching frequency of the Full-Bridge stage. This is achieved configuring an interruption subroutine as it is shown in Figure 76.

Table 9. Time needed for each task in Architecture A

ADC	6 μ s (3 x 2 μ s)
VL	120 ns
IIR	120 ns
PLL	500 ns
dq	100 ns
PT	1,3 μ s
WR	700 ns (7 registers x 100ns)
Total time	8,84 μs
T_{samp}	9,52 μ s (105 kHz)

4.3.2 *Architecture B: ADC managed by the FPGA and the blocks with complex operations and regulators implemented in the ARM*

This architecture, shown in Figure 78, differs from the previous one in the management of the ADC by the FPGA. With this driver, the measurements are faster, and can be sent to the microprocessor.

Figure 77 shows the time used for each task in this Architecture. In this case, the measurements are obtained in half of the time of Architecture A, but it is necessary to send them, to the microprocessor, therefore an additional delay appears (WRM).

Figure 77. Time needed for each task of Architecture B in scale

Table 10 shows the time used in Architecture B for each task. In this case, the total time is lower than the used in Architecture A, but not enough to increase the sampling frequency to 210 kHz (4,76 us).

Figure 78. Architecture B

Table 10. Time needed for each task in Architecture B

ADC	3 us (3 x 1us)
WRM	300 ns (3 x 100ns)
VL	120 ns
IIR	120 ns
PLL	500 ns
dq	100 ns

PT	1,3 us
WR	700 ns (7 registers x 100 ns)
Total time	6,24 us
T_{samp}	9,52 us (105 kHz)

4.3.3 Architecture C: ADC managed by the FPGA and blocks with complex operations and regulators in the FPGA

Architecture C (Figure 80) is much faster than the previous architectures because every task is done in the FPGA. The critical path on the design limits the time needed to execute the whole control. This critical path can be minimized using pipelines techniques. The most critical operations are the sines and cosines, which are done using IPs from the manufacturer of FPGA. This block needs less than 10 clock cycles to perform an operation, and several of this blocks can be placed in parallel, therefore in less than 10 cycles the required sines and cosines operation can be done.

Figure 79. Time needed for each task of Architecture C in scale

Since the total time is less than 4,76 us, the sampling frequency can be incremented up to the switching frequency of the first stage, the Buck type rectifier. As can be observed in Table 11, the bottle neck to increment the sampling frequency is the ADC.

Figure 80. Architecture C

Table 11. Time needed for each task in Architecture C

ADC	3 us (3 x 1us)
HW delay	100 ns
Total time	3,1 us
$T_{\text{samp}}/2$	4,76 us (210 kHz)

4.3.4 Architecture D: External ADC managed by the FPGA and blocks with complex operations and regulators in FPGA

In Figure 81 is shown Architecture D. In previous Architectures it has been observed that the sampling frequency it is limited by the ADC. Nevertheless, increase the sampling frequency beyond the switching frequency it is not very common. However, in order to demonstrate how to decrease the ADC time, the ADS8556 external ADC is proposed. This ADC is able to sample up to 6 channels in parallel at 760 kSPS. These samples can be sent directly to the corresponding FPGA block without crossing the BUS. With this ADC, the task of sample takes 1,6 μ s.

Assuming that the sampling frequency is, at least, 2 times the switching frequency, the duty cycle can be updated every switching cycle at a maximum frequency of 290 kHz.

In Table 12 this values are shown and the representation of tasks is shown in Figure 81.

Table 12. Time needed for each task in Architecture D

ADC	1,6 μ s
HW delay	100 ns
Total time	$\approx 1,7 \mu$ s
$T_{\text{samp}}/2$	4,76 μ s (210 kHz)

As it is observed in Figure 81 the total time is very short compared with the sampling period. That will allow increasing the switching frequency.

Figure 81. Time needed for each task of Architecture D in scale

Figure 82. Architecture with external ADC

4.3.5 Architecture based on a DSP with external ADC

In this section, Architectures based on the SoC Zynq have been shown, therefore, in order to have a comparison with a solution implemented in a DSP, this Architecture

has been implemented in a DSP from TI, using the experimental kit TMS320C28346 and an external ADC, ADS8556 which is able to provides 6 samples in parallel at 720 kSPS. Figure 84 shows these elements.

Figure 83. Time needed for each task of Architecture with DSP in scale

Figure 84. On the left side the DSP, TMS320C28346. In the right side, the ADC, ADS8556

Figure 83 shows the time schedule in the DSP. The DSP asks for the samples, applies a IIR filter and the voltage regulator calculates the modulation index to control the output voltage. Using the Park transformation together with a PWM generator, the PWM with the appropriate duty cycle for each interval are applied to the switches. The PWM modules are implemented in the FPGA, working independently. Since these modules are working independently only need to update the duty cycle

Table 13 shows the time required by each task.

Table 13. Time needed for each task in Architecture with DSP+ADC

ADC	1,6 us
IIR	0,5
VL	0,5 us
PT	1,5 us
Total tasks	4,1 us
T_{samp}/2	4,76 us (210 kHz)

4.3.6 Comparison of the results

The Architectures analyzed present differences in how the blocks are connected, in the complexity and mainly in the minimum time to perform all the operation. Table 14 shows a comparison between these architectures. The faster architectures are Architecture D and the one based on DSP, but both, use an external ADC, which make the system more complex and more expensive. The problems of having an external ADC are mainly 3, the size, increment of the BOM and the complexity of the layout.

On the other side, we have the architectures that use the internal ADC of the Zynq. The ones that use the ADC from the ARM are slower, but if the switching frequency selected is not higher than 110 kHz a complex system with floating point operations, filters, regulators, up to 4 measurements and modulation can be implemented updating the duty cycle every switching period. This solution is the one selected in this thesis.

For switching frequencies up to 150 kHz just adding a driver in hardware to manage the ADC would be enough to achieve the desired result. Nevertheless, when the necessities of bandwidth increase, as it is expected, the task needs to be implemented in the FPGA.

Table 14. Comparison between architectures

Architecture	A	B	C	D	Based in DSP
Total time	8,84 us	6,24us	3,1 us	1,7 us	4 us

Number of measurements	3	3	3	3	3
Sampling Period	9,52 us	9,52 us	4,76 us	4,76 us	4,76 us
Number of chips	1	1	1	2	2
Complexity	Language C	VHDL	VHDL	VHDL and Layout	VHDL and Layout

4.4 Conclusions

In the first part of the chapter, low cost DSP and FPGA are compared and the result is that DSP are more appropriate because low cost FPGAs do not have ADC integrated.

However, high performance DSPs are compared with SoC devices and the result depends on the requirement of the system. For high bandwidth requirements SoC are better, but in terms of cost DSP are cheaper.

Different implementation in a SoC of the control of the circuit proposed in this thesis, are compared. The difference between the implementations is where the control blocks (controllers, modulators...) are implemented, in the ARM processor or in the FPGA. The result is, the more blocks are implemented in the FPGA higher bandwidth can be achieved. Specially, the blocks with high impact in the timing is the related with the ADC. Nevertheless, to be able to update the duty cycle every switching frequency at higher frequency than 300 kHz, an external ADC will be needed, increasing the complexity of the system.

However, if the requirements of bandwidth allow updating the duty cycle at frequencies lowers than 200 kHz, a simple control, using the ARM for complex operations like the Park Transformed, and the FPGA for the PWM modules can be implemented achieving very successful results.

4.5 REFERENCES

[DeCastro'04] "Control digital basado en FPGA para convertidores conmutados" UPM thesis at 2004.

[Lin_MacCleery'12]ftp.ni.com/evaluation/powerdev/niweek2012/ETS_Day1/Lin_MacCleery_Final_ETIS_2012.pdf

[Nussbaumer'07] Nussbaumer, T.; Baumann, M.; Kolar, J.W., "Comprehensive Design of a Three-Phase Three-Switch Buck-Type PWM Rectifier," Power Electronics, IEEE Transactions on , vol.22, no.2, pp.551,562, March 2007.

[DeCastro'03] de Castro, A.; Zumel, P.; Garcia, O.; Riesgo, T.; Uceda, J., "Concurrent and simple digital controller of an AC/DC converter with power factor correction based on an FPGA," in Power Electronics, IEEE Transactions on , vol.18, no.1, pp.334-343, Jan 2003

Chapter 5

Experimental Results

5 Introduction

In this chapter, simulations and experimental results of the prototypes built to demonstrate the theoretical analysis are presented.

During this thesis a Three Phase Buck type rectifier integrated with a current fed Full-Bridge is studied with the purpose of reducing the size of the Link inductance. The EMI filter should attenuate the noise of the switching frequency. Since, the EMI filter can represent a significant part of the volume of the system, the EMI filter designed is also presented and simulated to analyze its impact on the power factor and the THD obtained.

The output voltage of this converter can be controlled with the duty cycle of the Full-Bridge (d) and with the Modulation Index (M) of the rectifier. These two variables give the opportunity to create different modulation strategies. In this thesis, the modulation strategy used is based on fix the variable d , and regulates the system with M , like it was presented in chapter 3.

The simulations and experimental results presented in this chapter are obtained with this control strategy

After showing simulations of the circuit, the experimental results will demonstrate the behavioral in a real prototype.

Table 15. Specifications of the system

$\hat{V}_{IN}$	$115\sqrt{2} V_{ac} (108\sqrt{2} - 118\sqrt{2} V_{ac})$	P_o	2 kW
V_o	48 V _{DC}	PF	> 0,95
Input Source Freq	400 Hz (398-403 Hz)	THD	< 10 %
f_{sw}	210 kHz		

5.1 Simulations

The circuit simulated in PSIM is represented in Figure 85. The specifications fixed to these simulations are presented in Table 15.

Figure 85. Circuit developed in PSIM for simulation

In order to comply with the military standards of EMI MIL-STD-461E and keep high power factor, the EMI filter is based on 3 differential mode stages with capacitive and inductive damping [Silva'12] [Molina'14]. In this design, the inductor value is 160 μH in each stage and 0,47 μF of the capacitor. The damping values are 160 μH for the inductance and 0,22 μF for the capacitance. In both cases, resistors of 20 Ohms are used. It is important to highlight that the size of the damping inductance is negligible compare with the main inductors.

The design of the filter is calculated to comply with the MIL-STD-461E considering the possibility of including several converters in parallel. When several converters are working in parallel and there is not possibility to ensure interleaving in the commutations, the noise produced at the switching frequency can be increased if every converter are switching simultaneously. In the worst case, the EMI filter should attenuate additionally to the standard, $20 \times \text{Log}(n)$ dB more than for a single converter, where n is the number of converters in parallel [Molina'14]. In Figure 86 this consideration is graphically explained.

Figure 86. Design consideration of a distributed power architecture

The inclusion of parallel channels with power converter switching without interleaving makes even more restrictive the standard. The interleaving is not possible due to the specifications of this system. The standard MIL-STD-461E limits the harmonic of 210 kHz at -77 dBA, with the consideration of 7 channels in parallel, including the dB as was explained previously, the limit down to -94 dBA.

In Figure 87, the common mode filter it is not represented, but in the real prototype is included. In the ANNEX II, the details of the common mode stage are included. The details of the design of this filter are presented in ANNEX II.

Figure 87. EMI filter based on three differential mode stages

Figure 88 shows the current demanded by the EMI filter and the rectifier. The current presents a very low THD (<2%) as was expected using this EMI filter.

Figure 88. Current at the input of the circuit for a load of 2 kW from a source of 115 V_{rms} and 48 V of output voltage

To analyze the harmonics of the current of Figure 88, in Figure 89 is represented the FFT of the current where the harmonics of the switching frequency can be observed at 210 kHz. As it has been explained before, the limit to comply with the MIL-STD-461E is -94 dBA and the simulations shown in Figure 89 is -105 dBA. With this information, the simulation verifies the theoretical analysis.

Figure 89. FFT of the current demanded for EMI filter

One of the goals of increasing the switching frequency of the rectifier to increase the value of the cut-off frequency of the EMI filter, reducing the size of the inductors. Nevertheless, the standard MIL-STD-461E is becoming more restrictive for higher frequencies up to 500 kHz.

The Power Factor obtained is 0,99 (Figure 90) at maximum power. The Power Factor is dependent on the load, decreasing its value when the load decreases. For applications where there are restrictions of PF at light loads there are several possible solutions.

Figure 90. Input current and voltage phase to neutral of the same phase for 115 Vrms of input voltage and maximum power of 2 kW

The first solution to improve the PF is to decrease the capacitance in the filter. Since, there is inductive damping, the capacitive damping can be rejected.

Other solution is to include a PLL in the control. With a PLL, introducing the delay measured, the PF can be corrected.

These two solutions can be combined. During the experimental tests under the prototypes, both solutions have been tested, and the one that provides better results is to apply a PLL and keep both damping.

One of the contributions to the control is to synchronize the voltage imposed by the rectifier in the freewheeling diode and the input voltage of the Full-Bridge. Figure 91 shows both voltages, synchronized at the middle of the period and the current induced through the Link inductor. The voltage across the freewheeling diode is the result of the symmetrical modulation method, where, for a constant output voltage would obtain a symmetrical ripple in the current. However, in this case, the voltage fixed by the Full-Bridge is not constant but pulsated, representing the rectified voltage of the transformer.

Figure 91. V_d synchronized with VFW and the resulting current I_{Link}

Since the voltage V_d is changing its shape as it observed in Figure 92, the current ripple is changing was explained in chapter 3. It can be appreciated that the maximum ripple occurs when the voltage V_d is maximum, thus being the maximum the difference between V_d and V_t . In the case of study, this maximum ripple corresponds to 1,9A.

Figure 92. V_{diode} , V_{FB} and I_{Link} at 2 kW, 115 Vrms input voltage and 48 VDC of output voltage

Obtaining soft switching is very important for the correct behavioral of this circuit as explained in chapter 3. Therefore, the ZVS capability is simulated with the parameters of parasitic capacitances and parasitic inductances in the transformer, obtained from measurements in an impedance analyzer.

Figure 93 shows V_{gs} and V_{ds} of switches M1 and M2, achieving ZVS for full load operation. Additionally, it is appreciated the voltage and the current through the transformer. Looking in detail, it can be observed that the transition occurs when current through the transformer is maximum.

Figure 93. I_T and V_T voltage through the transformer at 2 kW, V_{GS1} and V_{DS1} in Mosfet 1, V_{GS2} and V_{DS2} in MOSFET 2

On the contrary, at light load conditions hard switching of the switch M1 is observed in Figure 95. As explained in chapter 3, this circuit achieves ZVS discharging the parasitic capacitance of the MOSFET with the energy stored in the leakage inductance of the transformer. therefore, for light load conditions, the high side MOSFETs commutates when there is not enough energy in the transformer to discharge the capacitance as it is observed in Figure 95.

Figure 94. Transformer current and voltage at light load state. ZVS is not obtained

To solve this problem, the magnetizing inductance is decreased to increase the magnetizing current. Consequently, when the current through the transformer is close to zero, this current is still conducting, helping to achieve ZVS. This fact presents two drawbacks: increase the circulating current through the circuit and full ZCS it is not achieved.

Figure 94 shows the impact on the commutations of having enough magnetizing current through the transformer.

Figure 95. ZVS of the switches M1 and M2 at light load states

The auxiliary switch allows the current to continue circulating when the Full-Bridge short circuit the transformer and it is not demanding input current, avoiding spikes due to big changes in the inductor current.

In Figure 96 is observed the voltage in the transformer, the current through the auxiliary path and $V_{GS_{aux}}$ of the auxiliary switch. At the beginning, the current is flowing through the parasitic diode, because $V_{GS_{aux}}$ is still off. Once, the switch is ON, the current flow through the switch. The current changes from positive to negative when the current through the Link inductance is equal to the current demanded by the Full Bridge.

Figure 96. Transformer voltage, current through the auxiliary path and the control signal of the auxiliary MOSFET

5.2 Prototype design

5.2.1 Semiconductors

The system is designed for an application in which 65% derating in the semiconductor is required, and considering an ambient temperature of 70 °C, the maximum temperature in the semiconductors is 115 °C. The semiconductors used for the rectifier (M_{R+} , M_{R-} , M_{S+} , M_{S-} , M_{T+} , M_{T-}) are SIHG47N60S from VISHAY with a BV of 600 V, the series diode is a MUR3020WT from ON SEMICONDUCTOR with a BV of 600 V and the freewheeling diode is a C3D10065A from CREE with a BV of 650 V. The upper side MOSFET and the auxiliary MOSFET of the FB part (M_1 , M_3 and M_{AUX}) are STW20NK50Z from ST with a BV of 500 V and the low side (M_2 , M_4) are SIHG47N60S from VISHAY with a BV of 600 V. The output diodes (D_{OUT-1} , D_{OUT-2}) are VS-80CPQ150PbF from VISHAY with a BV of 150 V. The output capacitance is 100 μ F and the auxiliary capacitance is 1 μ F.

5.2.2 Inductors design

In this section the design of the inductors, depending on the control strategy is addressed. The major contribution of this work is using this inductance as output inductance of the rectifier and input inductance of the Full-Bridge.

This fact, together with the proposed synchronization of both stages, allows decreasing the total size of the inductors in the circuit.

The design of the inductor is done fixing a maximum ripple of 20% of the average current. As has been discussed during the thesis, V_d and V_{FB} are kept synchronized, thus affecting the volts per second balance in the inductor.

The variations in the energy stored in the link inductor are due to the variations in the voltage at the freewheeling diode. This voltage is controlled by M , therefore, if M is fixed when there is an input voltage variation, the voltage will be constant and the current increases to maintain the same amount of power, increasing the energy stored in the inductance. However, if M keep this voltage constant independently of the input voltage, the energy will be constant.

Figure 97 represents the energy stored in the inductance for the proposed control strategies in function of the input voltage. As expected, when regulation strategy I is selected, the energy is constant, because M is keeping V_d constant. Regulation strategy II is varying the whole input voltage range, because M is fixed. However, regulation strategy III has two intervals: when M is fixed, for lower values, and when M is regulating where the energy is constant.

For cases where the input voltage does not present huge changes, the impact it is not significant in the inductance size, but the effect of the selecting control strategy should be considered when a system is designed for a huge input voltage range, because the impact on the selection of the strategies. For this specific case, strategy I and II are the best, but for simplicity strategy I is selected.

Figure 97. Energy stored in the link inductor, depending on the regulation strategy

The value of inductance calculated with equation (7) is 150 μH . The inductor is divided in two cores, one in the power rail and other in the return rail of the current. Both are designed with a ETD34 N27 from EPCOS, wire AWG 22 (25 turns). The design has been done using PExprt from ANSYS. The results obtained with this tool are shown in Figure 98.

The losses in the selected inductor are obtaining considering the finite elements analysis run in the tool PeMag, another tool from Ansys. It is appreciated that the losses are mainly losses in the windings (2,647 W), about a 97 % of the losses. Due to the diameter of wire selected (0,5 mm), the current density though the wire is 4,28 A/mm^2 . In the core, the losses are about 72 mW.

Figure 98. Results of the inductor design in the tool PExprt

5.2.3 Transformer design

As described during the thesis, the transformer is one the key elements of the design for 2 main raisons. First, it provides galvanic isolation and second, its functionality is integrated in the operation of the Full-Bridge to achieve ZVS. To achieve ZVS, a minimum value of Leakage inductance is needed. To achieve this value of leakage inductance, there are two options: one is to include an external inductance, and

other solution is to design a transformer, theoretically worse, which would increase the leakage inductance (and consequently, the field H and the copper losses). In this thesis, the idea of increasing the power density, the solution adopted is to use the leakage inductance of the transformer in the operation.

Therefore, the design of the transformer should meet the specific values of leakage inductance and magnetizing inductance. In this case, 2 μH of Leakage and 500 μH of magnetizing inductance. To achieve 2 μH of leakage inductance the windings are made following interleaving techniques. These techniques, consist of wind together wires from primary and secondary. Since there are 15 turns in primary and 3 in secondary, the number of parallel windings in the secondary side is 5, in order to keep every turn of primary together with a secondary. This configuration can be observed in Figure 99.

Figure 99. Transformer windings

The design of the transformer has been done with the tool from ANSYS, PExprt. The transformer designed for the specifications of Table 5 is an ETD59 3C90 core from Ferroxcube with Litz wire (400x0.07mm). The primary has 15 turns and both secondary have 3 turns (with 5 parallel windings). The result of this design is shown in Figure 100. It is appreciated, that winding losses are predominant for this transformer, representing 67 % of the total. The magnetizing inductance calculated in the tool is 1,89 mH, nevertheless to achieve the desired value of 500 μH , a gap of 0,5 mm is included in each leg. The value of leakage inductance obtained is 2,3 μH , close enough to the necessary value to achieve ZVS. It is not common, that applying interleaving techniques as it is shown in Figure 99, the obtained leakage inductance matches the desired value, because usually, these techniques try to decrease as much as possible the leakage inductance and the strategy in this case is to have a big enough value that allows to achieve ZVS without adding an external inductance.

Figure 100. Results of the PExprt tool for the transformer design

5.2.4 Prototypes

Once the components are described and the magnetics designed, the prototype is built. In Figure 101 and Figure 102 are shown the prototype of the converter and the EMI filter.

Figure 101. Prototype of the converter

Figure 102. EMI filter built

5.3 Prototype results

The prototypes are tested in the Laboratory of CEI-UPM, in Madrid.

Figure 103 shows the input current and voltages and the measurements of THD in current (3%) and the power factor of 0,95 at maximum power.

Figure 103. Input voltage and current of each phase of the rectifier at 1 kW

In order to analyze if the system is complying with the required standards, two measurements with a LISN equipment to the input current of the rectifier stage are made. Figure 104 shows the measurement without filter.

Figure 104. Measurements of the LISN of the current harmonics without filter and standard limit MIL-STD-461E

However, Figure 105 shows the measurements of the current with the filter, meeting the requirements of EMI.

Figure 105. Measurements of the LISN of the current harmonics with filter and standard limit MIL-STD-461E

The synchronization of V_d and V_{FB} is shown in Figure 106 for two different pulse width of V_d . It is observed that in the first case, the ripple is similar to the simulated in Figure 91, however in the second case, both signals have the same pulse width and the current ripple is almost zero.

Figure 106. I_{LINK} Link inductance current, V_{FW} and $V_{TRAFOFB}$ for two different pulse width of the freewheeling diode voltage

In order to compare the simulation with the experimental results Figure 107, shows the system at full power (2 kW) and the simulated current ripple obtained follows the same pattern than the one presented in Figure 92, with a maximum current ripple of 1,9 A.

To demonstrate that the synchronization is important to decrease the current ripple, Figure 108 shows the case for the system synchronized (Left) and the system without any control of synchronization. It is appreciated that for the synchronized case, the current ripple is substantially smaller than the other case.

Figure 107. a) I_{LINK} , V_{FB} and V_T b) I_{LINK} , V_{FW} and V_T during several input voltage source periods

Figure 108. Comparison of the current through the inductance. Left) Synchronized case. Right) Unsynchronized case

The ZVS is achieved as it is shown in Figure 109, even at light load (200W, 10% of load). In this picture the gate signals of M1 and M2 are represented and their corresponding drain source voltages.

Figure 109. V_{DS} and V_{GS} for M1 and M2 at 10 % of load (200 W)

Figure 110 shows the current through the transformer and through the MOSFET M2, and V_{GS} of the same MOSFET at 10% of the load. It is appreciated that at light load, when the signal V_{GS} of M2 drops to zero, the MOSFET is still conducting the magnetizing current. This fact does not allow to achieve ZCS in the low side MOSFETs.

Figure 110. I_{M2} , V_{GS2} and I_T at 200 W (10% of the load)

The auxiliary circuit control signal and the current through the auxiliary path, together with V_{GS} of M1 and M2 are shown in Figure 111. It is observed that the driver signal of the auxiliary MOSFET is switched ON, 1 μs after the current is already conducting through the switch.

Figure 111. Waveforms of I_{aux} , M_{aux} , $M1$ and $M2$

Figure 112 shows the current through the output diode. It is observed in this current a resonance during the slop, due to the resonance between the Link inductance and the output capacitor.

Figure 112. V_{GS} of $M1$ (blue) and $M4$ (purple), I_{Dout} (green) and I_{aux} (yellow)

The efficiency measurements for the whole system, including the EMI filter, which has an efficiency of 98%, are presented in Figure 113. It is observed that the peak of efficiency is achieved at medium power (1,1 kW) and then, start to decrease.

The drop in the efficiency is caused by the increased in magnetizing current in the transformer primary side. As previously introduced, this current helps to reduce the switching losses. However, it also increases the conduction losses due to the increase in the circulating current in the bridge. Furthermore, the off losses are affected since the off transition no longer occurs with zero current but with the magnetizing current.

The drop of efficiency is due to the increment of circulating currents in primary because of the magnetizing current, which helps to decrease the switching losses at low power state but produce conducting losses and get worse the ZCS, because the current in primary never goes to zero, the minimum value is the magnetizing current.

Figure 113. Measurements of the converter efficiency in % of load

Since the goal of this thesis is centered on the power stage, a simple regulator has been implemented without a detailed analysis in order to demonstrate the functionality of the control strategy proposed. The regulator used, with a sampling frequency of 105 kHz is shown in equation (45). This regulator has a bandwidth of 60 Hz.

$$\frac{y(n)}{x(n)} = \frac{1.066 \cdot 10^{-5}}{1 - z^{-1}} \quad (45)$$

The results of the system under load steps is shown in Figure 114. This Figure shows the input current, the current through the Link inductor and the output voltage. The variation of the output voltage ripple amplitude is analyzed, and the result is that can be due to the high equivalent resistance of the output capacitors.

Figure 114. Load step from maximum power (2 kW) to 500 W.

5.4 Impact on the Buck type rectifier switching frequency variations

In this section, the impact of the switching frequency on the rectifier stage is studied (In this section the DC/DC it is not considered). The behavior of the system under different switching frequencies is measured, the results of the system at maximum power are presented in Table 16.

Table 16. Rectifier measurements for different switching frequencies

160 kHz			210 kHz			260 kHz		
η	THD	PF	η	THD	PF	η	THD	PF
94,5%	5,5%	0,99	95,3%	5,5 %	0,99	93,5%	9%	0,99

The results show that there is a drop of 2% in the efficiency and an increment of the THD of 3,5 % at 260 kHz. The impact of decreasing the switching frequency is reduced.

5.5 Summary and Conclusions

In this chapter the theoretical analysis presented in this thesis is verified with simulations and with a prototype. The prototype built shows that the design of the magnetics are key points of the design. Simulations and experimental results demonstrates the theoretical analysis of the reduction of the current ripple using the control strategy I. ZVS is achieved in the prototype as was calculated, nevertheless, ZCS is not obtained totally due to the magnetizing current.

The efficiency obtained from the prototype, note a non very typical curve because during the theoretical analysis, the losses associated to the magnetizing current are neglected and the ZCS is lost.

The theoretical analysis has been verified in the simulations, concretely, the functionality of the EMI filters, obtaining sinusoidal input currents with very low harmonics, the ZVS conditions of the switches of the Full Bridge for several load levels and the synchronization of both power stages to achieve the minimum ripple in the inductance.

These experiments have been tested in the real prototype obtaining waveforms very similar to the obtained in the simulations. The overall peak efficiency obtained by the whole system including the EMI filter is 94 %, at medium load, and 90 % at maximum power.

.

Chapter 6

Summary and Conclusion

6 Summary and conclusions

In this thesis the integration of the Three Phase Buck type rectifier and the Current Fed Full-Bridge is proposed as a solution for avionic applications. One of the reasons is because this circuit allows to comply with the EMI restrictions of the standard MIL-STD-461E. The main contribution of this thesis is the integration of these two topologies, analyzing the modulation, the control and the transformer ratio to minimize the size of the shared inductance.

The **first contribution** of this thesis is the theoretical analysis of the operation of the proposed circuit. This contribution is based on the synchronization of both stages, selecting the turn ratio which helps to reduce the volts per second applied to the inductor, reducing the current ripple. Additionally, with the control variables M and d , two parameters are optimized in a tradeoff, the current ripple and the efficiency.

The resultant topology has only two magnetic components, the intermediate inductor and the transformer. Both stages can be controlled separately, the Buck type rectifier controlling the modulation index M , and the Full Bridge, controlling the duty cycle d .

The relation between these two control variables (M and d) in a system with narrow input and output voltage ranges is analyzed. The result of this analysis is that high values of M and d helps to improve the efficiency. Low values of d increase the rms value of the current through the transformer, increasing the losses.

The fact that higher values of M and d provide higher efficiency affects to the selection of the turn ratio of the transformer, which has an important impact on the control, affecting to the relation between the control variables M and d . The conclusion is that, through a tradeoff between efficiency and current ripple the optimum value of turn ratio corresponds to the division of the average value of the freewheeling diode voltage and the output voltage.

In order to quantify the reduction of the volts per second applied to the inductor, for given conditions, the design of the inductor for the proposed circuit is compared with an inductor designed for a Buck type Rectifier with fixed output voltage, achieving a **reduction of a 42 % of the energy stored in the inductance** for the same current ripple desired.

The **second contribution** of this thesis is the analysis of the modulation strategies of the circuit.

Three different strategies of regulation have been analyzed. These strategies are: Fix M and regulate with d, Fix d and regulate with M and regulate with both.

The conclusion is, for narrow input and output voltage variations, the strategy of fix d and regulated with M provides the best results. One of the reasons is because the efficiency of the Full-Bridge is very dependent on the duty cycle, because of the utilization of the transformer, therefore, in order to keep a high efficiency in the Full-Bridge stage, fix D and modulate with M is considered the best solution.

The topology selected for the DC/DC is able to achieve ZVS from a specific value of load using the leakage inductance of the transformer. To increase the ZVS range, there are two options: add an external inductance, what implies the inclusion of additional circuits to avoid unexpected resonances and losses in the effective duty cycle applied to the transformer. Other option is reducing the magnetizing inductance, increasing the magnetizing current. This option increases the losses due to the circulating currents.

In this thesis, the first option is avoided to reduce the number of magnetic components, therefore, the leakage inductance calculated to obtain ZVS for loads bigger than 20 % without reducing considerably the effective duty cycle in the transformer is **2 uH**.

Since, the hard switching at light loads can produce fails in the circuit, the magnetizing inductance is reduced from 500 uH to 200 uH to increase the current through the transformer during the commutations.

For higher loads than 20%, the circuit achieves ZVS using the energy stored in the leakage inductance. However, for light load states, ZVS is obtained with the magnetizing current, thus losing ZCS and increasing the off-switching losses.

ZCS is achieved in a natural way for the two low side switches. However, increasing the magnetizing inductance provokes that this commutation occurs with the magnetizing current.

The conclusions of this analysis show that the key points in the design are the design of the transformer, where the magnetizing inductance and the leakage inductance need to be carefully designed, and the selection of the operating point M and D, which affects to the current ripple and the efficiency. For the specifications established in this thesis, the transformer with a **Leakage inductance of 2 uH and a Magnetizing inductance of 200 uH** allows to obtain ZVS in the whole range of load.

The **third contribution** of this thesis is the analysis of possible implementations of the control. To control the system, a SoC device is used, a Zynq from Xilinx. These devices include an ADC, a FPGA and a microprocessor in the same chip. Therefore,

the different blocks included in the control (PWM generators, Regulators, ...) can be implemented in both sides, in the FPGA or in the microprocessor. Different implementations are analyzed and the result of this analysis, shows that the higher number of blocks are implemented in the FPGA the higher switching frequency can be used. Specially, the blocks related with the ADC present higher impact in the timing. For rectifier applications, it is not common to have switching frequencies higher than the 500 kHz, therefore, with the internal ADC in the SoC, with a sample frequency of 1 MHz can be used.

The theoretical analysis done during this thesis is validated with simulations and with a prototype. The key elements of the prototype are the design of the magnetics. Simulation and experimental results validates the theoretical analysis of the reduction of the current ripple using the control strategy I (Fix d and regulates with M). ZVS is achieved in the prototype, nevertheless, the switch OFF commutations are done with the magnetizing current. Regarding the EMI measurements, the prototype complies with the standard MIL-STD-461E and the measurements of THD and PF are below to the limits.

The prototype obtains a peak efficiency of 94% at medium power and 90 % at maximum power. The THD is below 5 % in the whole power range, with values of 3% at maximum power. In terms of PF, the system keeps the PF higher than 0,66 in the whole power range, obtaining 0,99 at maximum power.

6.1 Diffusion of the results

[Molina`11] Molina, J.M.; García, O.; Asensi, R.; Oliver, J.A.; Alou, P.; Cobos, J. A., "Red adaptativa de conmutación suave para convertidor trifásico en puente activo completo para aplicaciones de vehículos eléctricos". "SAAEI 2011, Actas del XVIII Seminario Anual de Automática, Electrónica Industrial e Instrumentación", 05/07/2011 - 08/07/2011, Badajoz, España. ISBN 978-84-933682-3-4. pp. 1-8

[Molina`12] Molina, J.M.; Garcia, O.; Asensi, R.; Alou, P.; Oliver, J.A.; Cobos, J.A., "Adaptive control for ZVS three phase full active bridge converter with ARCN," in Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.1324-1330, 5-9 Feb. 2012.

[Silva`13] Silva, M.; Hensgens, N.; Molina, J.M.; Vasic, M.; Oliver, J.; Alou, P.; Garcia, O.; Cobos, J.A., "Interleaved multi-cell isolated three-phase PWM rectifier system for aircraft applications," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1035,1041, 17-21 March 2013

[Molina`13] Molina, J.M.; Zhao, S.; Silva, M.; Oliver, J.A.; Alou, P.; Torres, J.; Arevalo, F.; Garcia, O.; Cobos, J.A. "3-Phase Rectifier System with very demanding dynamic load: Architecture analysis and control strategy". "Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI)", 10/07/2013 - 12/07/2013, Madrid (Spain). ISBN 978-84-15302-60-5. pp.

[Zhao`14] Zhao, S.; Molina, J.M.; Silva, M.; Oliver, J.A.; Alou, P.; Torres, J.; Arevalo, F.; Garcia, O.; Cobos, J.A. Design of energy control method for three-phase buck-type rectifier with very demanding load steps," 2014 IEEE Applied Power Electronics Conference and Exposition - APEC 2014, Fort Worth, TX, 2014, pp. 2713-2718.

[Molina`14] Molina, J.M.; Zhao, S.; Silva, M.; Oliver, J.A.; Alou, P.; Torres, J.; Arevalo, F.; Garcia, O.; Cobos, J.A., "Power distribution in a 13 kW three-phase rectifier system: Impact on weight, volume and efficiency," in Applied Power Electronics Conference and Exposition (APEC), 2014 Twenty-Ninth Annual IEEE , vol., no., pp.906-911, 16-20 March 2014.

[Molina`15] Molina, J.M.; Alou, P.; Oliver, J.A.; Silva, M.; Cobos, J.A., "Three-Phase Buck type Rectifier topology integrated with Current Fed Full-Bridge," Applied Power Electronics Conference and Exposition (APEC), 2015 IEEE , vol., no., pp.84,91, 15-19 March 2015.

[Zhao`16] Zhao, S.; Molina, J.M.; Silva, M.; Oliver, J.A.; Alou, P.; Torres, J.; Arevalo, F.; Garcia, O.; Cobos, J.A. "Design of Energy Control Method for Three-Phase Buck-Type Rectifier With Very Demanding Load Steps to Achieve Smooth Input Currents," in IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 3217-3226, April 2016.

Annex I

Equivalent Circuits

7 Equivalent Circuits for each interval of the modulation

During a half of a period of the input voltage, there are different sectors as it is shown in **¡Error! No se encuentra el origen de la referencia..** The combination of the active switches to achieve the desired current in each sector is presented in this Annex.

Figure 115. Sector representation of the input voltages

Figure 116. Modulation in sector 1. Conduction states for the symmetrical modulation

Figure 117. Modulation in sector 2. Conduction states for the symmetrical modulation

Figure 118. Modulation in sector 3. Conduction states for the symmetrical modulation

Figure 119 Modulation in sector 4. Conduction states for the symmetrical modulation

Figure 120. Modulation in sector 5. Conduction states for the symmetrical modulation

Figure 121. Modulation in sector 6. Conduction states for the symmetrical modulation

Annex II

EMI Filter Design

8 EMI filter design

The values of the inductance and the capacitance of the EMI filter for a Buck type rectifier are calculated with the explained Matlab scrip. The inputs of the scrip are:

- Simulated noise to attenuate without filter (A)
- Limit of the standard to be complied (B)
- Margin (C)
- Maximum power (Pmax)
- Input and output voltage of the rectifier (Rms value of Vin, Vo)
- Number of stages of the filter (n)
- Switching frequency (fs)
- Frequency of the grid (fgrid)

$$att = A - B + C \quad (46)$$

$$R = \frac{V_o^2}{P_{max}} \quad (47)$$

$$w_c = \frac{2 \pi f_{sw}}{\sqrt{10^{\frac{att}{20 \cdot n}}}} \quad (48)$$

$$w_{grid} = 2 \pi f_{grid} \quad (49)$$

$$C = \frac{1}{R \sqrt{w_c^2 - w_{grid}^2}} \quad (50)$$

$$L = \frac{1}{\omega_c^2 C} \quad (51)$$

These equations are combined in the following Matlab Scrip:

```
function [C,L,fc] = EMIGENERATOR(INITIALATT,MINATT,Pn,fs,Margen, n, Vo, Vin)
c=Margen;
a=INITIALATT;
b=MINATT;
required=a-b+c;
Ull=Vin*sqrt(3);
P=Pn;
etapas=n;
f=fs;
R=(Vo^2)/P;
wc=(2*pi*fs)/sqrt(10^(required/(20*etapas)));
w=2*pi*fgrid;
C=1/(R*sqrt(wc^2-w^2));
L=1/(wc^2*C);
fc=wc/(2*pi);
end
```

Once L and C are known, following the procedure detailed by Magnetics in its catalogue (**Error! No se encuentra el origen de la referencia.**) knowing the electric values as the rms input current and the desired inductance, calculated in the previous study, the design of the inductor can be realized. During the study and design of the EMI filter several references have been used and presented in this Annex.

Inductor Core Selection Procedure

Only two parameters of the design application must be known to select a core for a current-limited inductor; inductance required with DC bias and the DC current. Use the following procedure to determine the core size and number of turns.

1. Compute the product of LI^2 where:
 L = inductance required with DC bias (mH)
 I = DC current (A)
2. Locate the LI^2 value on the Core Selector Chart (page 20, 21 & 22). Follow this coordinate to the intersection with the first core size that lies above the diagonal permeability line. This is the smallest core size that can be used.
3. The permeability line is sectioned into standard available core permeabilities. Selecting the permeability indicated will tend to be the best trade-off between A_L and DC bias.
4. Inductance, core size, and permeability are now known. Calculate the number of turns by using the following procedure:
 - (a) The inductance factor (A_L in nH/T²) for the core is obtained from the core data sheet. Determine the minimum A_L by using the worst case negative tolerance (generally -8%). With this information, calculate the number of turns needed to obtain the required inductance from:

$$N = \sqrt{\frac{L \cdot 10^3}{A_L}}$$

Where L is required inductance (μ H)
 - (b) Calculate the bias in A-T/cm from:

$$H = \frac{NI}{l_e}$$
 - (c) From the Permeability vs. DC Bias curves (pages 26 through 28), determine the rolloff percentage of initial permeability for the previously calculated bias level. Curve fit equations shown in the catalog can simplify this step. They are also available to use on Magnetics website: <http://www.mag-inc.com/design/design-guides/curve-fit-equation-tool>
 - (d) Multiply the required inductance by the percentage rolloff to find the inductance with bias current applied.

- (e) Increase the number of turns by dividing the initial number of turns (from step 4(a)) by the percentage rolloff. This will yield an inductance close to the required value after steps 4 (b), (c) and (d) are repeated.

- (f) Iterate steps 4 (b), (c) and (d) if needed to adjust turns up or down until the biased inductance is satisfactorily close to the target.

5. Choose a suitable wire size using the [Wire Table](#) (page 23). Duty cycles below 100% allow smaller wire sizes and lower winding factors, but do not allow smaller core sizes.

6. Design Checks

- (a) **Winding Factor.** See p.13 for notes on checking the coil design.
- (b) **Copper Losses.** See p.13 for notes on calculating conductor resistance and losses.
- (c) **Core Losses.** See p.14 for notes on calculating AC core losses. If AC losses result in too much heating or low efficiency, then the inductor may be loss-limited rather than current-limited. Design alternatives for this case include using a larger core or a lower permeability core to reduce the AC flux density; or using a lower loss material such as MPP in place of Kool Mu, or High Flux in place of XFLUX.
- (d) **Temperature Rise.** Dissipation of the heat generated by conductor and core losses is influenced by many factors. This means there is no simple way to predict temperature rise (ΔT) precisely. But the following equation is known to give a useful approximation for a component in still air. Surface areas for cores wound to 40% fill are given with the core data in this catalog.

$$\Delta T (^{\circ}\text{C}) = \left(\frac{\text{Total Losses (mW)}}{\text{Component Surface Area (cm}^2\text{)}} \right)^{0.833}$$

Figure 122. Procedure to design inductors proposed by Magnetics

References

- [Wang'13] Wang; Ruxi Blanchette, H.F.; Mingkai Mu; Boroyevich, D.; Mattavelli, P., "Influence of High-Frequency Near-Field Coupling Between Magnetic Components on EMI Filter Design," *Power Electronics, IEEE Transactions on*, vol.28, no.10, pp.4568,4579, Oct. 2013
- [Hensgens'12-1] Hensgens, N.; Silva, M.; Oliver, J.A.; Cobos, J.A.; Skibin, S.; Ecklebe, A., "Optimal design of AC EMI filters with damping networks and effect on the system power factor," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE*, vol., no., pp.637,644, 15-20 Sept. 2012
- [Hensgens'12-2] Hensgens, N.; Silva, M.; Oliver, J.A.; Alou, P.; Garcia, O.; Cobos, J.A., "Analysis and optimized design of a distributed multi-stage EMC filter for an interleaved three-phase PWM-rectifier system for aircraft applications," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, vol., no., pp.465,470, 5-9 Feb. 2012
- [Boroyevich'14] Boroyevich, Dushan; Zhang, Xuning; Bishnoi, Hemant; Burgos, Rolando; Mattavelli, Paolo; Wang, Fred, "Conducted EMI and Systems Integration," *Integrated Power Systems (CIPS), 2014 8th International Conference on*, vol., no., pp.1,14, 25-27 Feb. 2014
- [Dong'12] Dong Dong; Xuning Zhang; Fang Luo; Boroyevich, D.; Mattavelli, P., "Common-mode EMI noise reduction for grid-interface converter in low-voltage DC distribution system," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE*, vol., no., pp.451,457, 5-9 Feb. 2012
- [Zhang'13] Xuning Zhang; Burgos, R.; Boroyevich, D.; Mattavelli, P.; Fei Wang, "Improved common-mode voltage elimination modulation with dead-time compensation for three-level neutral-point-clamped three-phase inverters," *Energy Conversion Congress and Exposition (ECCE), 2013 IEEE*, vol., no., pp.4240,4246, 15-19 Sept. 2013

Annex III

MathCad

9 MathCad Calculations

Gain of the circuit, M and d Relation and Current Ripple

$$L_{lk} := 2 \quad t_2 := 0.05 \quad T_1 := 4.8 \quad U_{rms} := 115 \quad L_{in} := 60 \quad V_o := 48$$

$$G_1(d, R_1, M, n) := \frac{[(d) \cdot n + n \cdot t_2] \cdot (M \cdot 3)}{\sqrt{2} \cdot (d)^2 \cdot n^2 + \sqrt{2} \cdot (d) \cdot n^2 \cdot t_2 + \sqrt{2} \cdot 2 \cdot \frac{L_{lk}}{R_1 \cdot T_1}}$$

$$d_1 := 0.005, 0.01 \dots 1$$

$$M(d, R1, n, U_{ms}) := \frac{\left[\sqrt{2} \cdot (d)^2 \cdot n^2 + \sqrt{2} \cdot (d) \cdot n^2 \cdot t2 + \sqrt{2} \cdot 2 \cdot \frac{Llk}{R1 \cdot T1} \right] \cdot V_o}{[(d) \cdot n + n \cdot t2] \cdot U_{ms} \cdot 3}$$

M and d relation / Turn ratio variation

M and d relation / Input Voltage variation (n=5)

Current Ripple

$$U_{ins}(\alpha, U_{rms}) := U_{rms} \cdot \sqrt{2} \cdot \sqrt{3} \cdot \sin(\alpha) \quad \psi := \frac{\pi}{3}, 1.06..2 \cdot \frac{\pi}{3}$$

$$V_a(\alpha, d, U_{rms}) := U_{ins}(\alpha, U_{rms}) - \frac{U_{rms} \cdot 3 \cdot M(d, 1.2, 5, 115)}{(d) \cdot \sqrt{2}}$$

$$riz(\alpha, d, R1, n, U_{rms}) := \begin{cases} \left[\frac{U_{rms} \cdot 3 \cdot M(d, R1, n, U_{rms})}{(d) \cdot \sqrt{2}} - U_{ins}(\alpha, U_{rms}) \right] \cdot (d) \cdot \frac{T1}{Lin} & \text{if } V_a(\alpha, d, U_{rms}) < 0 \\ \left[U_{ins}(\alpha, U_{rms}) - \frac{U_{rms} \cdot 3 \cdot M(d, R1, n, U_{rms})}{(d) \cdot \sqrt{2}} \right] \cdot \frac{\sqrt{2}}{U_{ins}(\alpha, U_{rms})} \cdot \frac{T1}{Lin} & \text{if } V_a(\alpha, d, U_{rms}) > 0 \end{cases}$$

Current ripple for d=0,9 (red), d=0,7 (blue), d=0,5 (green)

LOSS ESTIMATION IN THE AB-RECTIFIER

INPUTS

$$n := 5 \quad V_{rms} := 115 \quad V_o := 48 \quad P_o := 2000 \quad L_{lk} := 2 \quad T_o := 9.6 \quad OV := 0.6 \quad PW := 5.4 \quad t_{dead} := 0.1 \quad \tau_{aux} := 1 \quad f_1 := 210000 \quad f_2 := 105000 \quad PF := 0.95 \\ t_{tr} := 5 \times 10^{-9}$$

INTERMEDIATE VARIABLES

$$V_{dc}(M) := \frac{(V_{rms} \cdot M \cdot 3)}{\sqrt{2}} \quad PH(d) := \left[(d) \cdot \frac{T_o}{2} \right] + 0.4 \quad ta(d) := PH(d) - OV - t_{dead} \quad t3(d) := PW - PH(d) \quad Idc(M, Po) := \frac{P_o}{V_{dc}(M) \cdot 0.97} \\ tb(M, n) := \frac{(2 \cdot Idc(M, Po) \cdot L_{lk})}{n \cdot V_o}$$

SEMICONDUCTORS DATA

Rectifier

$$R_{dsr} := 0.07 \quad C_{ossr} := 2 \cdot 10^{-10} \quad R_{diodeserie} := 0.055 \quad V_{fdiodoserie} := 0.85 \quad C_{ossds} := 1 \cdot 10^{-10} \quad R_{dfw} := 0.075 \quad V_{ffw} := 1.5 \quad M_{Parallel} := 1 \quad DS_{Parallel} := 1 \quad FW_{Parallel} := 2$$

CF-Full-Bridge

$$R_{dsf} := 0.03 \quad C_{ossf} := 1 \cdot 10^{-10} \quad R_{dsaux} := 0.03 \quad C_{ossaux} := 1 \cdot 10^{-10} \quad R_{direct} := 7 \cdot 10^{-3} \quad V_{fdirect} := 0.71 \quad MF_{Parallel} := 1 \quad DR_{Parallel} := 1$$

BUCK TYPE RECTIFIER

$$I_{imp}(Po) := \frac{\sqrt{2} \cdot P_o}{3 \cdot V_{rms} \cdot PF}$$

MOSFET

SERIES DIODE

FW DIODE

$$I_{rmsM}(M, Po) := \frac{I_{imp}(Po)}{\sqrt{M} \cdot \pi} \quad I_{avgM}(Po) := \frac{I_{imp}(Po)}{\pi} \quad I_{rmsSD}(M, Po) := \frac{I_{imp}(Po)}{\sqrt{M} \cdot \pi} \quad I_{avgSD}(Po) := \frac{I_{imp}(Po)}{\pi} \quad I_{avgFW}(M, Po) := \left(\frac{1}{M} - \frac{3}{\pi} \right) \cdot I_{imp}(Po) \quad I_{rmsFW}(M, Po) := I_{imp}(Po) \cdot \sqrt{\left(\frac{1}{M^2} - \frac{3}{\pi \cdot M} \right)}$$

LOSSES IN THE RECTIFIER

CONDUCTION LOSSES

$$P_M(M, Po) := 6 \cdot (I_{rmsM}(M, Po))^2 \cdot \frac{R_{dsr}}{M_{Parallel}} \quad PSD(M, Po) := 6 \cdot \left(I_{avgSD}(Po) \cdot V_{fdiodoserie} + I_{rmsSD}(M, Po)^2 \cdot \frac{R_{diodeserie}}{DS_{Parallel}} \right) \quad PFWD(M, Po) := \left(I_{avgFW}(M, Po) \cdot V_{ffw} + I_{rmsFW}(M, Po)^2 \cdot \frac{R_{dfw}}{FW_{Parallel}} \right)$$

$$P_{cond}(M, Po) := P_M(M, Po) + PSD(M, Po) + PFWD(M, Po)$$

SWITCHING LOSSES

$$P_{off} := \left(\frac{6}{\pi} \right) \cdot (V_{rms} \cdot \sqrt{3})^2 \cdot (0.5 \cdot M_{Parallel} \cdot C_{ossr} + 1.5 \cdot DS_{Parallel} \cdot C_{ossds}) \cdot \left(\frac{14 \cdot \pi - 9 \cdot \sqrt{3}}{32} \right) \cdot f_1$$

$$P_{on}(M, Po) := \left(\frac{6}{\pi} \right) \cdot V_{rms} \cdot \sqrt{2} \cdot \sqrt{3} \cdot Idc(M, Po) \cdot t_{tr} \cdot \frac{f_1}{4} \quad P_{sw}(M, Po) := P_{off} + P_{on}(M, Po)$$

MAGNETICS

$$P_{inductor} := 5$$

$$P_{rect}(M, Po) := P_{cond}(M, Po) + P_{sw}(M, Po) + 0.05 \cdot Idc(M, Po)^2$$

CF FULL-BRIDGE

$$I_{rmsMosfet}(M, d, Po) := \sqrt{\left(\frac{1}{T_o} \right) \cdot \left(\frac{4 \cdot Idc(M, Po)^2 \cdot ta(d)}{3} + Idc(M, Po)^2 \cdot t3(d) \right)} \quad I_{rmsMaux}(M, d, Po) := \sqrt{\left(\frac{1}{T_o} \right) \cdot \left(\frac{2 \cdot Idc(M, Po)^2 \cdot ta(d)}{3} \right)} \quad I_{rmsd}(M, d, Po, n) := \sqrt{\frac{Idc(M, Po)^2 \cdot n^2}{3 \cdot T_o} \cdot (8 \cdot tb(M, n) + 4 \cdot ta(d))} \\ I_{avgd}(Po) := \frac{P_o}{2 \cdot V_o}$$

LOSSES IN THE CF FULL-BRIDGE

CONDUCTION

$$P_{condM}(M, d, Po) := 4 \cdot I_{rmsMosfet}(M, d, Po)^2 \cdot \frac{R_{dsf}}{MF_{Parallel}} \quad P_{condMaux}(M, d, Po) := I_{rmsMaux}(M, d, Po)^2 \cdot \frac{R_{dsaux}}{MF_{Parallel}} \quad P_{condiodo}(M, d, Po, n) := 2 \cdot \left(I_{rmsd}(M, d, Po, n)^2 \cdot \frac{R_{direct}}{DR_{Parallel}} + I_{avgd}(Po) \cdot V_{direct} \right)$$

The Switching OFF losses are only considered in the Low side Mosfets

$$U_{dd} := 270 \quad C_{gd} := 7 \cdot 10^{-12} \quad R_g := 1 \quad U_p := 4 \quad I_{don} := 12 \quad I_{doff} := 10 \quad t_{fi} := 0.4 \cdot 10^{-9}$$

$$t_{ru} := (U_{dd} - I_{don}) \cdot R_g \cdot \frac{C_{gd}}{U_p}$$

$$P_{soff} := \left[U_{dd} \cdot I_{doff} \cdot \frac{(t_{ru} + t_{fi})}{2} \right] f_2 \quad P_{soff} = 0.121$$

MAGNETICS

$$R_{w1} := 17 \times 10^{-3} \quad R_{w2} := 2.8 \cdot 10^{-3}$$

$$I_{rmsTRAFO}(M, d, Po) := \sqrt{\frac{(I_{dc}(M, Po))^2 \cdot 2}{3 \cdot T_o} \cdot (8 \cdot t_b(M, n) + 4 \cdot t_a(d))} \quad P_{trafo} := 12$$

$$I_{rmsTRAFO}(0.8, 0.15) = f(any1) \rightarrow any1$$

$$P_{tcondFBantiguo}(M, d, Po, n) := P_{condM}(M, d, Po) + P_{condMaux}(M, d, Po) + P_{condiodo}(M, d, Po, n) + 0.1 \cdot I_{rmsTRAFO}(M, d, Po)^2 + P_{soff}$$

$$P_{tcondFB}(M, d, Po, n) := P_{condM}(M, d, Po) + P_{condMaux}(M, d, Po) + P_{condiodo}(M, d, Po, n) + 0.1 \cdot I_{rmsTRAFO}(M, d, Po)^2$$

Losses in the secondary Diode Calculated through the approximation to a straight line of the curve of the datasheet

$$\underline{Vdf} := 1 \quad \underline{Vdi} := 0.4 \quad \underline{Ifin} := 77 \quad \underline{Istart} := 1 \quad \underline{q} := 4$$

$$\underline{k} := \frac{(Vdf - Vdi)}{(Ifin - Istart)} \quad \underline{Udo}(t) := Vdi + k \cdot \left(\frac{Ifin}{q} \right) t$$

$$\underline{Pll}(t) := Udo(t) \cdot \left[\left(\frac{Ifin}{q} \right) t \right]$$

$$\underline{Losses} := \left[\frac{1}{9.8} \int_0^{3.1} Udo(t) \cdot \left[\left(\frac{Ifin}{q} \right) t \right] dt \right] = 6.74$$

EFFICIENCY

$$PT(M, d, Po, n) := PtcondFB(M, d, Po, n) + Prect(M, Po) + Psoff$$

Efficiency, Current Ripple and corresponding Modulation Index in function of duty cycle of the FB for 2 kW, fixed input and output voltage (115Vrms, 48 Vdc)

$$d1 := 0.005, 0.01..1$$

Efficiency of the circuit for fixed M (red) and fixed d (blue) for 2 kW and fixed input and output voltage

Global efficiency, conduction losses and switching losses

Annex IV

Design in Zynq

10 Design of the Digital Control in Zynq

10.1 Main Architecture

The design presents the architecture shown in [Error! No se encuentra el origen de la referencia.](#).

Figure 123. Internal Architecture in Zynq

10.2 Report of the VHDL Design

Device Utilization Summary (actual values)				[-]
Slice Logic Utilization	Used	Available	Utilization	Note(s)
Number of Slice Registers	3,067	106,400	2%	
Number used as Flip Flops	3,066			
Number used as Latches	1			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	4,089	53,200	7%	
Number used as logic	3,891	53,200	7%	
Number using O6 output only	3,107			
Number using O5 output only	102			

Number using O5 and O6	682			
Number used as ROM	0			
Number used as Memory	165	17,400	1%	
Number used as Dual Port RAM	0			
Number used as Single Port RAM	0			
Number used as Shift Register	165			
Number using O6 output only	133			
Number using O5 output only	0			
Number using O5 and O6	32			
Number used exclusively as route-thrus	33			
Number with same-slice register load	23			
Number with same-slice carry load	10			
Number with other load	0			
Number of occupied Slices	1,969	13,300	14%	
Number of LUT Flip Flop pairs used	5,450			
Number with an unused Flip Flop	2,533	5,450	46%	
Number with an unused LUT	1,361	5,450	24%	
Number of fully used LUT-FF pairs	1,556	5,450	28%	
Number of unique control sets	222			
Number of slice register sites lost to control set restrictions	928	106,400	1%	
Number of bonded IOBs	78	200	39%	
Number of LOCed IOBs	25	78	32%	
Number of bonded IOPAD	130	130	100%	
IOB Flip Flops	12			
Number of bonded IPADs	32			
Number of LOCed IPADs	5	32	15%	
Number of RAMB36E1/FIFO36E1s	8	140	5%	
Number using RAMB36E1 only	8			
Number using FIFO36E1 only	0			
Number of RAMB18E1/FIFO18E1s	0	280	0%	
Number of BUFG/BUFGCTRLs	2	32	6%	
Number used as BUFGs	2			
Number used as BUFGCTRLs	0			
Number of IDELAYE2/IDELAYE2_FINEDELAYS	0	200	0%	
Number of ILOGICE2/ILOGICE3/ISERDESE2s	1	200	1%	
Number used as ILOGICE2s	1			
Number used as ILOGICE3s	0			
Number used as ISERDESE2s	0			
Number of ODELAYE2/ODELAYE2_FINEDELAYS	0			
Number of OLOGICE2/OLOGICE3/OSERDESE2s	11	200	5%	
Number used as OLOGICE2s	11			
Number used as OLOGICE3s	0			
Number used as OSERDESE2s	0			
Number of PHASER_IN/PHASER_IN_PHYs	0	16	0%	
Number of PHASER_OUT/PHASER_OUT_PHYs	0	16	0%	
Number of BSCANs	1	4	25%	
Number of BUFHCEs	0	72	0%	
Number of BUFMRs	0	16	0%	
Number of CAPTUREs	0	1	0%	
Number of DNA_PORTS	0	1	0%	

Number of DSP48E1s	1	220	1%	
Number of EFUSE_USRs	0	1	0%	
Number of FRAME_ECCs	0	1	0%	
Number of ICAPs	0	2	0%	
Number of IDELAYCTRLs	0	4	0%	
Number of IN_FIFOs	0	16	0%	
Number of MMCME2_ADVs	0	4	0%	
Number of OUT_FIFOs	0	16	0%	
Number of PHASER_REFS	0	4	0%	
Number of PHY_CONTROLS	0	4	0%	
Number of PLLE2_ADVs	0	4	0%	
Number of PS7s	1	1	100%	
Number of STARTUPs	0	1	0%	
Number of XADCs	1	1	100%	
Number of RPM macros	9			
Average Fanout of Non-Clock Nets	3.96			

Figure 124. Reports of the utilization of the FPGA

¡Error! No se encuentra el origen de la referencia. shows the resources used by the design in the FPGA for the blocks of Rectifier Modulation and the control of the Full Bridge.