Thin Absorbers for Defect-Tolerant Solar Cell Design

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Abstract — Thin silicon wafers provide a pathway to lower cost and lower capital intensity PV module manufacturing. They can also produce higher-efficiency devices with less expensive feedstock and crystallization processes because they require shorter diffusion lengths and operate at higher carrier injection. Through simulation, we show that thin Si wafers can be incorporated into high-efficiency cells with greater defect tolerance than thick wafers. Experimentally, we demonstrate the importance of excellent surface passivation to realizing the efficiency potential of thin silicon solar cells and show that such passivation can be achieved in silicon/amorphous silicon heterojunction devices.

Index Terms — silicon, photovoltaic cells, heterojunction.

I. INTRODUCTION

Defects, including point defects like metal impurities and structural defects like dislocations and grain boundaries, limit the performance of many low-cost silicon (Si) materials developed for photovoltaics (PV) [1]–[3]. Avoiding these defects requires highly-refined Si feedstock and expensive crystal growth techniques, contributing significant costs to Si PV module production [4]. Furthermore, feedstock production and crystallization are the most capital-intensive processes in Si PV module production, and the cost of capital equipment (capex) can limit the growth of PV manufacturing capacity [5]. As cost must be decreased and growth sustained to meet climate targets [6], identifying ways to enable low-cost/low-capex Si absorbers is crucial.

Thinner absorbers are more tolerant to point defects and structural defects for three reasons [7]–[9]: 1) they require shorter diffusion lengths for high performance due to the smaller device thickness; 2) with similar total absorption, they operate at higher minority carrier injection levels (*i.e.*, higher operating voltage); 3) they have a smaller total number of defects.

Point 2 above increases the operating voltage of the solar cell and is known to reduce Shockley-Read-Hall (SRH) recombination at some point defects [10] as well as the recombination activity of dislocations and grain boundaries by reducing the charging of these defects [11]. Having a smaller volume of material in the base reduces its dark recombination current ($J_{0,\text{bulk}}$), increasing open-circuit voltage (V_{OC}) and efficiency. By maintaining efficiency with higher defect concentrations, thinner absorbers can enable lower-cost and lower-capex wafer technologies.

Efficient thin absorbers also directly reduce Si PV module cost and capex. First, thinner wafers reduce the amount of feedstock needed to produce a module with a given power output. Second, they contribute to higher throughput crystal growth, ingot cropping, wire sawing, diffusion from gas sources, and wet chemical processing.

Improved manufacturing techniques for passivating dielectrics like silica, alumina, and hydrogenated amorphous silicon (a-Si:H) have enabled device architectures that can achieve high efficiency with thin absorbers [12]. Previously, devices with thin absorbers were limited by surface or contact recombination regardless of how defect-tolerant the bulk might be. The passivated emitter and rear cell (PERC) [13] and silicon heterojunction (SHJ) (*e.g.*, [14]) are examples of device architectures that can accommodate thin Si absorbers and have been successfully commercialized. Wider band gap heterojunction emitters, like gallium phosphide (GaP), are also being investigated [15] because they have the potential to reduce parasitic absorption and increase carrier selectivity. Light-trapping schemes that enable high current densities on absorbers as thin as 10 μm have been demonstrated [16], overcoming the difficulties of absorption in thin Si wafers.

Here, we explore the potential for high-efficiency advanced cells with thin absorbers containing relatively high concentrations of metal impurities. We fabricate thick and thin silicon heterojunction cells with and without intentional contamination with iron (Fe). Our results highlight experimentally the importance of excellent surface passivation and light trapping. Simulations fit to these results suggest that thin cells with high defect concentrations have higher efficiency potential than thick cells, indicating a path to defect-tolerant device design.

II. EXPERIMENTAL METHODS

A. Wafer Thinning and Intentional Contamination

We start with high-lifetime (greater than 7 ms) 4"-diameter *n*-type float zone (FZ) Si wafers, ground to a thickness of 145 μm . Half of these wafers are thinned to 60 μm in KOH solution. Half of the thin wafers and half of the thick wafers receive a standard chemical cleaning and are intentionally contaminated with Fe by submersion for 10 minutes in a solution of H_2O : NH_4OH : H_2O_2 at 70 °C containing 30 ppb Fe,

followed by a 1-hour anneal at 975 °C in nitrogen ambient. Subsequently, the Fe-contaminated silicon oxide and around 5 μm of the underlying wafer are removed by etching in a HF: H₂O₂: H₂O solution, followed by an HF: HNO₃: CH₃COOH solution. Finally, a standard chemical cleaning is performed. The final total Fe concentration in the wafer bulk is determined through secondary ion mass spectrometry (SIMS) measurement, obtaining a mean value of $3 \times 10^{13} \text{ cm}^{-3}$.

B. Silicon Heterojunction Cell Fabrication

The heterojunction is formed using plasma enhanced chemical vapor deposition (PECVD) to grow intrinsic ((i)-Si:H) and doped ((n+)-a-Si:H and (p+)-a-Si:H) hydrogenated amorphous layers, forming a *i-p/i-n* stack. Indium tin oxide (ITO) is sputtered on both sides. The ITO layer on the rear is thicker and absorbs less infrared light. Silver (Ag) is sputtered on the rear to act as a rear reflector. The device is shown schematically in Fig. 1.

Fig. 1. Structure of the silicon heterojunction solar cell. The cell surface is not textured. The amorphous layers are 10 nm-thick. The front ITO and the ITO-IR are 80 and 280 μm -thick, respectively, and the silver is 280 μm -thick.

C. Cell Characterization

Effective minority carrier lifetimes are measured after the *i-p/i-n* stack formation, using a Sinton WCT-120 lifetime tester and photoluminescence imaging. After completing the sputtering, the external quantum efficiency (EQE) and reflectance are measured. J_{sc} values are obtained by integrating the product of the EQE curves and the solar spectrum. The open-circuit voltage (V_{oc}) and pseudo-fill factor ($\text{p}FF$) are acquired using the Sinton Suns- V_{oc} tester at 25 °C. Front metallization of the cell is not required since the V_{oc} and $\text{p}FF$ can be measured by probing the ITO directly.

III. EXPERIMENTAL RESULTS

Lifetime measurements indicate that the lifetimes of 60 μm wafers and the contaminated 145 μm wafer are limited by surface passivation. This limitation is indicated in the case of the uncontaminated wafers by the difference between the lifetime of the thick and thin wafers (5.5 and 1.6 ms,

respectively), and in the case of the contaminated wafers by lifetimes (12.9 μs for the 145 μm wafer and 7.8 μs for the 60 μm wafer) significantly lower than the SRH lifetime associated with the measured Fe concentration (around 50 μs at the doping concentrations of these wafers). Photoluminescence (PL) imaging (Fig. 2) also suggests poor surface passivation of the contaminated wafers, particularly in the 145 μm wafer. Extraction of the emitter recombination current (J_{oe}), here attributed to recombination at the Si/a-Si interface, confirms that the surface passivation quality is significantly worse in the intentionally contaminated wafers. For the uncontaminated wafers J_{oe} is on the order of single fA/cm², while for the contaminated wafer, J_{oe} is two orders of magnitude higher.

Fig. 2. Photoluminescence images of wafers 60 μm and 145 μm thick, both uncontaminated (top row) and intentionally contaminated with $[\text{Fe}] = 3 \times 10^{13} \text{ cm}^{-3}$ (bottom row). All wafers have intrinsic and doped a-Si:H stacks and ITO on the front and rear. Average effective lifetimes measured on a Sinton WCT-120 at $\Delta n = 10^{15} \text{ cm}^{-3}$ are (a) 1.6 ms, (b) 5.5 ms, (c) 7.8 μs , and (d) 12.9 μs .

The surface morphology of the contaminated wafers is not as smooth as that of the uncontaminated wafers. We attribute this difference to the etching step performed after the contamination. Surface morphology plays a critical role in surface passivation quality, particularly when a-Si:H is used as a passivating layer. Therefore, an improved etching process or avoiding the necessity for the etching step by contaminating at the ingot rather than wafer level could address the issues with passivating the surfaces of the contaminated wafers.

For the uncontaminated wafers, pseudo-efficiencies (η) of 19.2% and 18.6% are obtained for the thick and thin cells, respectively (Fig. 3). As expected, the V_{oc} of the thin wafer is higher (738 vs. 725 mV), though this is not enough to

compensate for the lower current (30.7 vs. 32.7 mA/cm² as measured by EQE). However, due to the poor passivation of the contaminated wafers, the V_{OC} is actually slightly lower for the thinner cell (595 vs. 600 mV), and the pseudo- η (14.3% and 14.9%) are well below the potential dictated by the bulk lifetime.

Fig. 3. Suns- V_{OC} measurements on wafers of 60 μm and 145 μm thick, both uncontaminated and intentionally contaminated with $[\text{Fe}]=3\times 10^{13} \text{ cm}^{-3}$. All wafers have intrinsic and doped a-Si:H stacks and ITO on the front and rear.

Fig. 4. External quantum efficiency and reflectivity of 60 μm and 145 μm -thick wafers, both uncontaminated and intentionally contaminated with $[\text{Fe}]=3\times 10^{13} \text{ cm}^{-3}$. All wafers have intrinsic and doped a-Si:H stacks and ITO on the front and rear. High reflectivity at long wavelengths is due to the lack of surface texturing. Integrating the EQE curves gives J_{SC} values of 32.7 mA/cm² for the uncontaminated 145 μm cell, 30.7 mA/cm² for the uncontaminated 60 μm cell, 31.4 mA/cm² for the contaminated 145 μm cell, and 29.9 mA/cm² for the contaminated 60 μm cell.

Fig. 4 shows the external quantum efficiency and reflectivity of the four wafers. Note that with the Ag rear reflector, all light that is not absorbed should be reflected. Because the cells are not textured, the reflectivity is quite high, leading to the low current densities extracted. The lack of texturing also amplifies the difference in absorption between the two cells. The effect of the poor surface passivation can be seen in the EQE data as well. The diffusion length dictated by the bulk lifetime lies between 60 and 145 μm , so the extracted current density should not be significantly reduced for the thin cells. However, the integrated EQE for the 60 μm contaminated wafer gives a current density of only 29.9 mA/cm², contributing to the low pseudo- η of the thin contaminated cell.

IV. FITTING AND EFFICIENCY POTENTIAL

The uncontaminated wafers are simulated in Sentaurus Device [17] using the model from [18] with parameters from [19], including the treatment of ITO as a metal. The doping of the p-a-Si:H layer was increased to $6\times 10^{13} \text{ cm}^{-3}$ to account for the high pFF in the Suns- V_{OC} measurements. The density of interface traps (D_{it}) was varied to fit the measured Suns- V_{OC} curves, with the best fit for the uncontaminated samples found for a value of $5\times 10^{11} \text{ cm}^{-2}$. The fits are shown in Fig. 5. Fitting D_{it} for the V_{OC} of the contaminated samples further confirms the hypothesis that they are surface-limited, with an increase of over an order of magnitude needed.

Fig. 5. Measured Suns- V_{OC} (symbols) and simulated $J-V$ curves fitted to these data (black solid lines) on planar uncontaminated wafers of 60 μm and 145 μm thick. Simulated $J-V$ curves for textured 60 μm (red lines) and 145 μm -thick (blue lines) cells with $[\text{Fe}]=10^{14}$, 10^{13} , and 10^{12} cm^{-3} . Simulations show higher efficiency potential for thinner heavily contaminated wafers, with efficiencies up to 19.5%.

In order to determine the efficiency potential of thin Si heterojunctions with high concentrations of point defects, we use fit to the uncontaminated wafers. We simulate a textured surface using an optical generation profile simulated in OPAL2 [20] using the experimental front-side a-Si:H and ITO stack. To account for the greater surface area, we increase D_{it}

to $8 \times 10^{11} \text{ cm}^{-2}$. We simulate $[\text{Fe}] = 10^{12}$, 10^{13} , and 10^{14} cm^{-3} . The results are shown in Fig. 5. In each case, the efficiency of the thin cell exceeds that of the thick cell. At lower $[\text{Fe}]$, this difference is driven by higher V_{OC} . As $[\text{Fe}]$ increases, the higher J_{SC} due to greater absorption in the thicker cell is reduced due to the larger diffusion length requirement. For $[\text{Fe}] = 10^{14} \text{ cm}^{-3}$, even though the J_{SC} of the thin cell has started to decrease, both V_{OC} and J_{SC} are higher than for the thicker cell. We also note that the efficiency potential for thin wafers with high defect concentrations is relatively high, with a simulated efficiency of 19.5% for $[\text{Fe}] = 10^{12} \text{ cm}^{-3}$ even though these simulations include no light-trapping structures on the rear of the cell.

VI. CONCLUSION

Our simulations suggest that the efficiency potential of Si solar cells with thin absorbers is high. However, as the experiments here show, the surface passivation must be excellent in order to realize this potential. Based on these results, we expect that with surface passivation of the quality achieved on uncontaminated 60 μm -thick Si wafers using a-Si:H stacks and established front and rear light-trapping structures, efficiencies around 20% could be achieved with defect concentrations above 10^{12} cm^{-3} . We note as well that the SRH lifetime associated with interstitial Fe in *n*-type Si has very little injection-dependence. With a more injection-dependent defect, the higher injection-level associated with thin cells would also improve the bulk minority carrier lifetime.

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