**ESCUELA TECNICA SUPERIOR DE INGENIEROS
INDUSTRIALES**

**Physics-based Analytical Modelling
and Optimization of the GaN HEMT
with the Field-Plate Structure for
Application in High-Frequency
Switching Converters**

PhD Thesis

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Nani i dedi,

Zbog beskrajne ljubavi i vere u naučna dostignuća.

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Abstract

The purpose of this thesis is to present a novel, physics-based, capacitive model for Gallium Nitride High Electron Mobility Transistors that contain gate field-plate structure. The proposed methodology is fully analytical, providing a set of equations between the design parameters and input, output and reverse capacitance of the device. Together with previously proposed physics-based analytical models for output characteristics of a HEMT, proposed capacitive model gives the complete model of a GaN switching device. Therefore, it can be implemented into power loss models for the topology of interest and used for device design optimization by power losses minimization.

The target application of the device modelled in this work is a high-frequency (HF) DC/DC converter used as a dynamic power supply in Envelope Tracking and Envelope Elimination and Restoration techniques. The main challenge in these HF topologies is to increase the efficiency of the signal transmission together with the bandwidth. Since AlGaN/GaN HEMTs present a technological solution that does not contain p-n junctions, their capacitances are significantly lower comparing to Si MOSFETs. Therefore, they present excellent candidates for switching devices in high-frequency converters. Furthermore, using proposed physics-based capacitive model, their design can be optimized for a particular application. That was the main motivation for the work presented in this thesis.

The main contributions of this thesis are the proposed capacitance model together with the optimization process of the HEMT design. The model was verified by experimental characterization of the device. Additionally, in order to verify its applicability for the design optimization process, model was implemented into a power loss model of a high-frequency buck converter. Simulated efficiency curves showed very good agreement with the measurements, verifying the precision of the proposed methodology.

Furthermore, the obtained model showed that field-plate design dominantly influences Miller's charge in the device and determines the breakdown voltage rating. Therefore, the field-plate was optimized separately from other design parameters, by minimizing gate-to-drain charge for a target breakdown voltage. Furthermore, implementation of the obtained physics-based model into a power loss model of a buck converter and variation of different design parameters, provided directions in which parameters should be changed (increased/decreased) in order to minimize the power losses. This resulted in the optimized design of the device that reduced total losses in

the converter for 80%, at 20MHz of switching frequency and output power of 20W. Total loss breakdown showed that switching losses that presented 81% of the total losses were decreased for 76% due to highly improved capacitance characteristics of the device.

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Acronyms and Symbols

Acronyms

HEMT – High Electron Mobility Transistor

MISHEMT – Metal Insulator Semiconductor High Electron Mobility Transistor

GIT – Gate Insulated Transistor

2DEG – Two Dimensional Electron Gas

HF – High Frequency

EA – Envelope Amplifier

ET – Envelope Tracking

EER – Envelope Elimination and Restoration

RFPA – Radio Frequency Power Amplifier

FOM – Figure Of Merit

SOA – State Of the Art

WBG – Wide Band-gap

GaN – Gallium Nitride

SiC – Silicon Carbide

Si – Silicon

MOSFET – Metal Oxide Semiconductor Field Effect Transistor

FET – Field Effect Transistor

LGA – Line Grid Array

WCDMA – Wide Code Division Multiple Access

64QAM - 64 Quadrature Amplitude Modulation

CAVET - Current-Aperture Vertical Electron Transistor

FEA - Finite Element Analysis

2D - Two Dimensional

MODFET- Modulation Doped Field Effect Transistor

GCA - Gradual Channel Approximation

SP - Surface Potential

DHFET - Double Heterojunction Field Effect Transistor

Si₃N₄ - Silicon Nitride

SiO₂ - Silicon Oxide

Symbols

R_{sheet} - Sheet resistance of the channel

q - Electron charge

μ - Field dependent mobility of electrons in the channel

n_{2DEG} - 2DEG sheet density in the channel

R_{on} - On-resistance of a switching device

Q_{gate}- Total gate charge

V_{gs} - Gate-source voltage

V_{ds} - Drain-source voltage

V_{dg} - Drain-gate voltage

C_{iss} - Input capacitance of the device
 C_{oss} - Output capacitance of the device
 C_{rss} - Reverse capacitance of the device
 C_{gs} - Gate-source capacitance
 C_{ds} - Drain-source capacitance
 C_{gd} - Gate-drain (Miller's) capacitance
 E_f - Fermi-level energy [eV]
 v_{drift} - drift velocity of the electrons in the channel
 I_d - drain-source current
 g_m - Transconductance
 σ_{PZ} - polarization-charge sheet density [C/m²]
 n_{PZ} - polarization sheet density [σ_{PZ}/q]
 E_0 - the first energy subband in the quantum well [eV]
 E_1 - the second energy subband in the quantum well [eV]
 L_{fp} -field-plate length
 W_g -gate width
 L_g -gate length
 L_{gs} -gate-source distance
 L_{gd} -gate-drain distance
 t_{ox} -insulator thickness below the field-plate extension
 T_{gate} - gate-electrode height
 m - Aluminum mole fraction in AlGaIn layer

d_{AlGaN} – thickness of AlGaN layer

v_{SAT} – saturation velocity of electrons in the channel

E_c – Critical value of lateral electric field in the channel for which device enters saturation

E_x –lateral component of the electric field in the channel

v_a – the potential inside AlGaN layer

v_g – the potential inside GaN layer

E_a – vertical component of the electric field in AlGaN layer (perpendicular to the channel)

E_g – vertical component of the electric field in GaN layer (perpendicular to the channel)

V_{th} – effective threshold of the device

D - vector of electric displacement

ϕ_m – Schottky barrier height at gate/ AlGaN heterojunction

ϕ_{mi} – Metal – insulator height at field-plate electrode/insulator junction

ΔE_c – the height of the quantum well [V]

ϵ_a – permittivity of AlGaN layer

ϵ_g – permittivity of GaN layer

ϵ_{ox} – permittivity of insulator below the field-plate

μ_{LF} – Low field mobility of electrons in the channel

$R_{\text{S_CM}}$ – Source resistance due to metallization and contacts

$R_{\text{D_CM}}$ – Drain resistance due to metallization and contacts

$R_{\text{S_DRIFT}}$ – Source drift resistance

R_{D_DRIFT} - Drain drift resistance

n_{S0} – 2DEG sheet density in the source and drain drift areas

w_a – the thickness of field-plate insulator together with the thickness of AlGaIn layer

w_g – the width of the depletion region in GaN layer, perpendicular to the channel (when device is in the OFF state)

$n_{2DEG,FP}$ – the density of the 2DEG in the channel below the field-plate extension

V_{ds}^I – drain-source voltage for which vertical depletion ends

$C_{gd,y}^I$ – the part of C_{gd} capacitance caused by vertical depletion of the 2DEG below the field-plate

b^I – lateral extension of the depletion area around the drain-side gate edge

b^{II} – lateral extension of the depletion area around the field-plate edge

$C_{gd_top_top_pad}$ – fringing capacitance between the pads that connect all gate and drain fingers

$C_{ds_top_top}$ – drain-source capacitance due to fringing between electrodes

$C_{gs_bottom_top}$ – gate-source fringing capacitance between the bottom of the gate electrode and the top of the undepleted 2DEG in the source drift region

$C_{gs_sw_top}$ – gate- source fringing capacitance between the sidewall of the gate electrode and the top of the undepleted 2DEG in the source drift region

$C_{gs_top_sw}$ – gate-source fringing capacitance between the bottom of the gate electrode and the sidewall of the source

$C_{gs_multifinger}$ – gate-source fringing capacitance between the areas that connect all gate and source fingers in the multifinger layout of the device

E_{cgd} – energy in the gate-drain capacitor

V_{in} – input voltage of a buck converter

V_{max} – maximum voltage of the generated envelope, equal to the input voltage of the converter

η_{64QAM} – the average efficiency of the generated 64QAM signal

$E_{critical}$ – the critical value of GaN material, chosen from the literature. Corresponds to the electric field value when impact ionization starts

E_{crit} – the chosen value for maximum electric field in the channel in the optimized design (with predefined safety margin)

E_{peak1} – the peak value of the field in the channel (around the drain-side gate edge) when vertical depletion ends

E_{peak2} – the peak value of the field in the channel (around the field-plate edge) for drain-source voltage equal to the breakdown rating of the device

b_1 - lateral extension of depletion area in the channel (around the drain-side gate edge), for electric field equal to E_{peak1}

b_2 - lateral extension of depletion area in the channel (around the field-plate edge), for electric field equal to E_{peak2}

$V_{ds,max}$ - breakdown voltage rating of the device

P_{cond} – conduction losses in the converter

P_{switch} - switching losses in the converter

P_{total} - total losses in the converter

Chapter1. Introduction and Motivation

1. Introduction and Motivation

1.1. Why Wide-Band Gap (WBG) devices in power electronics applications?

POWER electronics can be defined as the application of solid-state electronics to convert and control the electric power. In the modern world of today, the increased concern for energy delivery and environmental protection gives power electronics one of the key roles in human society.

Power semiconductor devices are the key solid-state components in the overall power conversion system and most often, they are the ones that consume the largest portion of power losses in that system. Therefore, the development of power semiconductor devices has been the driving force in the power electronics systems. Recently, silicon (Si)-based devices have dominated the power device market due to mature and well-established fabrication technology. However, there are applications where Si devices have reached their limit, in terms of thermal capabilities, voltage breakdown or frequency of operation. This has created a growing need for power device technologies that can deliver high-temperature, high-power density and high-frequency operation. The semiconductor materials that can provide the aforementioned enhancement in the performance are wide-bandgap materials, which are characterized, among other things, by larger energy bandgaps between the conduction and the valence band comparing to Silicon. Only this feature can provide higher operating temperatures, due to higher energy “obstacle” that must be overcome by intrinsic carriers. Having very low intrinsic carrier concentration that gives negligible junction leakage, the wide bandgap devices can avoid thermal runaway breakdown up to 500°C. Wide bandgap devices are also characterized by additional material properties that are highly desirable for high-voltage, high-temperature and high-frequency operation.

1.1.1. Basic physical features of Wide Band Gap (WBG) materials

A substantial amount of research and development activity has occurred in the past 20 years in the silicon carbide (SiC) and gallium nitride (GaN) domains. These efforts have delivered several classes of power semiconductor devices, with voltage ratings from 30V to 10kV and growing, for a wide variety of applications. Circuit and device researchers collaborated in parallel to demonstrate the efficiency of these technologies in applications from Envelope

tracking (30V), laptop chargers (200V) to plug-in hybrid vehicle battery chargers (1200V) and fault current limiters for the electric power grid (10kV). The applications with voltage rating from 30-200V will be referred to as “low voltage” applications, while ratings between 200-600V and higher will be named “medium” and “high” voltage applications [Reusch 2015]. Additionally, the switching frequency up to 500kHz will be referred to as “low frequency applications” while frequencies higher than 1MHz will be called “high frequency applications” [Ji 2013].

Table 1-1 Properties of wide bandgap materials in comparison to Si [Zhang 2002, Nanjo 2013].

Material Property	Si	4H-SiC	GaN	Diamond
Bandgap (eV)	1.1	3.26	3.40	5.45
Critical Electric Field (MV/cm)	0.3	3	3.3	5.6
Electron mobility (cm ² /Vs)	1500	1000	2000	2200
Electron Saturation Velocity (10 ⁷ cm/sec)	1	2.0	2.5	2.7
Thermal Conductivity (W/cm K)	1.5	4.5	1.3	20

Today, SiC and GaN are the most promising among all wide bandgap semiconductor materials [Hudgins 2003, Zhang 2002]. Table 1.1 compares the material properties of Si, SiC, GaN and Diamond. Although having the best properties by far, the price for Diamond makes it unsuitable for wide range of applications.

The SiC and GaN have almost three times larger bandgap ($\sim 3\text{eV}$) compared with Si ($\sim 1\text{eV}$). As it was already explained, the energy bandgap between the conduction and the valence zone influences the operating temperature of the semiconductor material, giving higher or lower concentration of intrinsic carriers. Since intrinsic concentration causes a thermal runaway, SiC and GaN devices can operate at higher temperatures comparing to Si, while providing higher reliability at temperatures at which Si devices can also operate. Furthermore, the critical electric field of SiC and GaN is one order of magnitude higher than in the case of Si. This property directly enables thinner drift layers for a target breakdown voltage, and therefore, smaller on-resistance of the device. High electron mobility of GaN together with higher saturation drift velocity directly provide the possibility of operation at higher switching speed. Finally, the increased thermal conductivity in the case of SiC devices, provides an easier extraction of the dissipated power. However, in the case of GaN devices, this value is slightly lower comparing to Silicon, which is why SiC is used as a substrate material in GaN HEMTs when thermal management of the device needs to be improved.

Observing the values for each of the aforementioned properties, it can be seen that SiC switches are more suitable for high-power, lower switching frequency applications, while GaN devices are targeting high switching speed and low power applications.

1.1.2. SiC power devices

Due to significant improvements in SiC material growth technology, SiC-based power devices are available for high-power, high-temperature and, comparing to Si devices, higher switching frequency applications. Once considered for the major defects in the bulk and epitaxial layers of SiC, micropipes, have been nearly eliminated, while other defects have densities below 1000 cm^{-2} . Comparatively, GaN can have bulk defect densities that exceed 10^6 cm^{-2} and therefore, cannot be used as a substrate in GaN power devices.

Speaking of SiC power devices, SiC Schottky diodes, p-i-n diodes and merged p-n-Schottky (MPS) diodes show significant performance improvement in comparison to their Si counterparts. For example, commercially available Si

Schottky diodes are usually rated at maximum breakdown voltages $<100\text{V}$. Beyond this limit, Si Schottky diodes cannot compete with Si p-i-n diodes, due to their unacceptably large on-resistance. In comparison to their Si counterparts, novel SiC Schottky diodes can block thousands of volts because SiC has much larger breakdown electric field [Mantooth 2015].

A SiC vertical power MOSFET is a next-generation switching device expected to replace conventional power devices based on Si in many applications, because it can operate with lower power losses at a higher switching speed and at higher operating temperatures. In the past ten years, a lot of effort has been devoted to developing SiC power MOSFETs and a great progress has been achieved. The first SiC power MOSFET was demonstrated in 1994, in the form of a vertical trench gate structure (UMOSFET), with a breakdown voltage of 150V [Palmour 1994]. Later on, UMOSFETs were replaced by planar gate MOSFETs fabricated using double implantation. The devices were called DMOSFETs and one of these SiC power MOSFETs has the highest reported breakdown voltage of 10kV [Ryu 2004]. However, 10kV SiC MOSFETs are not mature enough to be commercially available at the moment.

Regarding commercially available SiC power MOSFETs, the company Wolfspeed (ex Cree) offers the devices with the highest breakdown voltage of 1700V , while several manufacturers such as Microsemi, Rohm, Infineon and STMicroelectronics, manufacture devices with 1200V of the breakdown rating.

The application of SiC power switches varies from converters for industrial drives and traction systems which develop several megawatts of the output power [Filsecker 2014], to aircraft, electric vehicles, photovoltaic and induction heating applications which demand several kilowatts [Sarnago 2014, Escobar-Mejia 2014, Wang 2013, Friedli 2009, Burger 2009] or several tens of kilowatts [Chen 2014, Calderon-Lopez 2014, Rothmund 2015]. Due to aforementioned advantages of SiC over Si, significantly higher efficiencies and operating temperatures have been achieved.

1.1.3. GaN power devices

At present, two types of GaN power devices have been reported: GaN high electron mobility transistors (HEMTs) and GaN Schottky diodes. In the past decade, these devices have made a great progress on their characteristics, due to improvement of device structure on one hand and GaN material quality on the other.

The cross-section of a typical AlGaIn/GaN HEMT is shown in Fig. 1.1. The HEMT has three contacts: source, gate and drain. A thick layer of undoped GaN is grown on the substrate, which can be Si, SiC or sapphire. On the top of the undoped GaN layer, a thin layer of Aluminum GaN (AlGaIn) with higher energy bandgap comparing to GaN is built. Due to the difference in the energy bandgaps, the quantum well is formed at GaN/AlGaIn heterojunction. The existence of a quantum well, together with strong built-in polarization field inside AlGaIn layer, P, generates the most distinctive feature of a HEMT: 2-D electron gas (2DEG).

Figure 1-1 The cross-section of an AlGaIn/GaN High Electron Mobility Transistor (HEMT)

The 2DEG is being formed in the quantum well in undoped GaN layer, having therefore very high electron carrier mobility, μ (in the range 1200-2000cm²/Vs). Using n_{2DEG} for the sheet density of the 2DEG and q for the electron charge, sheet resistance of the channel can be calculated as: $R_{sheet}=(qn_{2DEG})^{-1}$. It can be concluded that high mobility of the 2DEG significantly decreases sheet resistance of the channel. Furthermore, the polarization field is sufficiently strong to provide 2DEG densities of 10¹⁷m⁻², causing no necessity for additional doping of AlGaIn layer. However, due to strong piezoelectric effect, GaN devices are inherently normally-on devices.

The first field-effect transistor (FET) based on AlGaAs/GaAs heterostructure was proposed in [Mimura 1980]. Afterwards, FET based on

AlGaIn/GaN heterostructure was presented in [Khan 1994]. Since then, GaN transistors have been reported and applied in RF and microwave areas [Mishra 1997, Sheppard, 2000; Shen 2001, Lee 2008, Dobush 2013]. In [Nomura 2006], an AlGaIn/GaN FET with a breakdown voltage of 750V and very low specific on-resistance of $6.3\text{m}\Omega\text{cm}^2$ was proposed. In [Wu 2008], a 97.8% efficiency GaN HEMT boost converter with 300W of the output power and 1MHz of switching frequency was demonstrated. This 175-350V hard-switching boost converter was based on a high-voltage GaN HEMT with more than 900V of breakdown voltage. Another 120W boost converter based on 940V/4.4A GaN HEMT was reported in [Saito 2008], and a power efficiency of 94.2% was achieved at 1MHz of switching frequency. Furthermore, a 600V half-bridge module using two GaN transistors and two SiC Schottky diodes was constructed in [Nomura 2008]. This module demonstrated a good reliability after 400h of high temperature (250°C) testing. Observing the cross-section of the AlGaIn/GaN HEMT, it can be seen that no single p-n junction exists in this structure, which creates one of the major advantages of these devices in comparison to their Si counterparts: significantly decreased capacitances. This feature makes them excellent candidates for high-switching frequency applications, where high parasitic capacitances cause the highest portion of the power losses.

Speaking of high-switching frequency applications, [Rodriguez 2014] proves the advantage of GaN HEMTs application in high-frequency PWM buck converters. The results are presented for discrete-device and integrated implementations of a synchronous buck converter. Discrete devices as well as integration of two switches in a half-bridge configuration were done by TriQuint Semiconductor. The discrete solution provided more than 10W of the output power supplied from 40V with efficiencies higher than 95%, when operating at 10MHz of switching frequency. The integrated solution provided more than 3W of the output power supplied from 30V, with efficiencies higher than 90% operating at 40MHz of switching frequency. As a practical application of this technology, dynamic power supply for Radio Frequency Power Amplifier in Envelope Tracking technique was addressed. It was demonstrated that a synchronous buck converter with discrete GaN HEMTs operating at 20MHz of switching frequency is capable of accurately tracking a 3-MHz envelope bandwidth of a WCDMA signal with peak power of 10W, achieving the efficiency of 90%.

1.2. State Of the Art in commercially available GaN power switches

Due to normally-on nature of AlGaIn/GaN heterojunction, depletion mode (normally-on) devices were the first fabricated devices. However, since normally-off power switches are preferable in power electronics applications, a significant research effort has been put into development of normally-off structure. These efforts resulted in commercially available GaN devices with positive threshold voltage, while application of multiple field-plate structure increased the breakdown voltage up to 650V [GaN Systems]. At the moment, vertical AlGaIn/GaN devices are not commercially available, due to high defect density in GaN bulks. Still, a significant research breakthrough has been made in this direction [Chowdhury 2013] opening the possibility for the commercial availability of this structure in the future.

In order to quickly compare different switching devices with the same voltage rating, in terms of power loss performance, the Figure Of Merit defined as a product of on-resistance and gate charge can be used:

$$FOM = R_{on}Q_{gate} \quad (1.1)$$

This FOM is the simplest one among several [Baliga 1987] and can be used for quick comparison between the devices with the same breakdown voltage and similar current ratings. However, for further and more detailed comparison among devices (in order to choose the best device for a particular topology), it is necessary to implement a power loss model. In this section, Si and GaN devices will be compared using this simple FOM, since the goal is to roughly estimate the power loss performance of these two technologies.

Regarding the devices rated for higher voltage applications (around 600V), the leading manufacturers on the market are companies GaN Systems and Panasonic. GaN Systems provide the breakdown voltage rating of 650V which is the highest breakdown voltage reported for commercially available GaN HEMTs. Their GS66504B GaN HEMT with the rating (650V, 15A) has a Figure Of Merit:

$$FOM_{GaN\ Systems} = R_{on}Q_{gate} = 100m\Omega \cdot 3nC = 300 \cdot 10^{-12}C\Omega \quad (1.2)$$

Speaking of Panasonic GaN HEMTs, their maximum voltage rating is 600V. Their PGA26C09DV device with (600V, 15A) rating has a Figure Of Merit equal to:

$$FOM_{Panasonic} = R_{on}Q_{gate} = 70m\Omega \cdot 8nC = 560 \cdot 10^{-12}C\Omega \quad (1.3)$$

In order to compare GS66504B from GaN Systems to the best Si MOSFET that can be found on the market, the FOM of IPT65R195G7 CoolMOS C7 Gold series power transistors from Infineon will be calculated.

The rating of the device is (700V, 18A) and its FOM is equal to:

$$FOM_{IPB60R199CP} = R_{on}Q_{gate} = 195m\Omega \cdot 20nC = 3900 \cdot 10^{-12}C\Omega \quad (1.4)$$

Comparing the value from (1.4) to a FOM value from (1.2), it can be seen that GaN HEMT from GaN Systems has thirteen times better value for FOM, which makes a significant difference in terms of power loss performance. This difference is caused by almost seven times higher gate charge and two times higher on-resistance of the Si power transistor.

Speaking of GaN HEMTs optimized for high switching-frequency and lower voltage applications, the company Efficient Power Conversion Corporation (EPC) provides the best devices available on the market. They design and manufacture devices with high range of breakdown voltage ratings: from 30V up to 450V [EPC online]. Regarding the application in Envelope Tracking switching power supplies (which is the target application in our work as will be explained in the following section), EPC provides two devices with optimized characteristics in terms of parasitic capacitances: EPC 8004 and EPC 8008. The rating of both devices is (40V, 2.7A) while the corresponding FOM values are:

$$FOM_{EPC8004} = R_{on}Q_{gate} = 110m\Omega \cdot 0.37nC = 40.7 \cdot 10^{-12}C\Omega \quad (1.5)$$

$$FOM_{EPC8008} = R_{on}Q_{gate} = 325m\Omega \cdot 0.177nC = 57.5 \cdot 10^{-12}C\Omega \quad (1.6)$$

Although having slightly higher value for FOM, the EPC8008 contains extraordinary low value for total gate charge and very low values for input and output capacitance in the complete range of drain-source voltages (Fig. 1.2.). Since one of the goals of this work was to optimize the capacitive part of a GaN HEMT for high-switching frequency application, we find the characteristics of this device impressively good. Therefore, from the power loss point of view, we can say that this device is the best device for our target application.

Additionally, EPC provides Line Grid Array (LGA) package for their GaN power transistors. This package can be treated as an optimum one for HF switching frequency application, due to very low values of parasitic inductances in gate, drain and most importantly- source.

Figure 1-2 The input, output and reverse capacitance dependence on drain-source voltage, when device is in the OFF state for EPC8008 [EPC online].

In order to make comparison between GaN and Si technology for 40V rated devices, the FOM for IRLML0040TRPbF (40V, 3.6A) Si MOSFET will be calculated and compared to the FOM values for EPC8004 and 8008:

$$FOM_{IRLML0040TRPbF} = R_{on}Q_{gate} = 56m\Omega \cdot 2.6nC = 145.6 \cdot 10^{-12}C\Omega \quad (1.7)$$

Observing the obtained value and comparing it to the values from (1.5) and (1.6), it can be seen that FOM of this Si MOSFET is 2.5 worse than the FOM of corresponding GaN devices, in particularly due to approximately 10 times higher value for total gate charge.

1.3. Different types of normally-off lateral GaN power switches

From the previously presented principle of operation, it can be clearly seen that AlGaIn/GaN HEMTs are normally-on devices with a negative threshold voltage, since the channel is created as soon as AlGaIn/GaN heterojunction is made. However, power electronic applications demand normally-off devices. Therefore, a lot of research effort has been put into development of normally-off GaN HEMTs. Several methods of achieving normally-off operation will be presented in this section.

1.3.1. Recessed-gate structure

The AlGaN/GaN HEMT with a recessed-gate structure was the first proposed technique for achieving normally-off operation of the device [Saito 2006]. The recessed gate structure was combined with the source field-plate structure in order to increase the breakdown voltage of the device. The cross-section of the device is shown in Fig. 1.3.

Figure 1-3 The cross-section of the device with recessed gate structure [Saito 2006].

The basic idea that lies behind the recessed gate is the reduction in the AlGaN layer thickness, which directly decreases the $n_{2\text{DEG}}$ sheet density in the channel for the same gate-source voltage. This effect will be shown in the model for $n_{2\text{DEG}}(V_{gs})$ in Chapter 3. Basically, the gate-source voltage control of the 2DEG in the channel can be changed through two parameters of AlGaN layer: Aluminum mole fraction, m and thickness, d_{AlGaN} . This was expected since 2DEG is formed due to difference in polarization-induced fixed charges in AlGaN and GaN layers. Since d_{AlGaN} together with m determines polarization charge in AlGaN layer, it will directly influence the amount of 2DEG in the channel when V_{gs} is equal to 0V. In order to avoid significant increase in on-resistance by reducing the AlGaN thickness and therefore the 2DEG sheet density along the complete drain-source distance, the recession is done only

below the gate. In this way, the normally-off operation is being achieved and only a small increase of the on-resistance is expected, due to reduction of 2DEG density below the gate.

In [Saito 2006], the threshold voltage of -0.14V was achieved. Although still slightly negative, the threshold was shifted for couple of Volts towards the positive values and the proposed concept was verified. Additional analysis showed that Metal-Insulator-Semiconductor (MIS) structure with a recessed gate can provide a threshold voltage higher than 1V and this will be analyzed in the following section

1.3.2. Recessed gate with multicap layer

The improvement of previously presented recessed structure in terms of positive threshold voltage together with high current density, using multichannel transistor with two AlGaIn/GaN interfaces and a recessed gate MIS structure was proposed in [Kanamura 2010].

The device proposed in [Kanamura 2010] is shown in Fig. 1.4. The structure consists of AlGaIn/GaN MISHEMT grown on SiC substrate with n-GaN/AlN/n-GaN triple cap layer. The thickness of each cap layer is 2nm while the thickness of AlGaIn is 25nm.

The first n-GaN cap layer is used to reduce the surface oxidation and trapping effect that cause low-frequency dispersion (relevant when devices are operated in Power Amplifiers) and current-collapse or dynamic on-resistance (relevant when devices are operated in switching converters). Since traps are contained at the surface of AlGaIn layer, a thin cap of GaN can significantly reduce this effect, since electrons during the OFF-state will be “held” in GaN cap layer by the barrier formed at n-GaN/AlGaIn heterojunction (Fig. 1.5).

The second 2nm AlN layer inserted between two GaN caps causes conduction band banding to the downside, because of a strong polarization field at the interface between AlN and GaN (Fig. 1.5). This band banding causes the increase in a 2DEG sheet density in the main channel. As a result, the sheet resistance of the device with triple cap layer is 27% lower comparing to the structure with only one GaN cap layer while the breakdown voltage remains the same.

However, observing the conduction band profile from Fig. 1.5 on the right, it can be seen that a second 2DEG might be generated in the n-GaN cap layer on the bottom side, for higher values of V_{gs} . If Fermi level starts to touch the conduction band at the gate contact, this 2DEG can cause significant gate

leakage. Therefore, the application of the oxide in the recessed structure is necessary in order to suppress the gate-drain leakage.

Finally, the surface GaN cap mostly has the role of keeping the smooth surface morphology on the strained AlN layer, since the microscopic measurements showed that in the case of double AlN/GaN cap, a lot of cracks were observed.

The presented structure showed excellent performance and was commercially developed by Toshiba, Fujitsu, NTT and Transphorm [Chowdury 2013].

Figure 1-4 The cross-section of the device with recessed gate structure with multilayer cap [Kanamura 2010].

Figure 1-5 The effect of the second AlN cap layer [Kanamura 2010].

1.3.3. Gate-Injection Transistor (GIT)

Gate Injection transistor (GIT) was proposed for the first time in [Uemoto 2007], as a variation in AlGa_N/Ga_N HEMT structure which will provide enhancement mode (normally-off) operation together with increased conductivity in the channel. This new device principle uses p-type of AlGa_N layer only below the gate electrode (Fig. 1.6).

As it was mentioned in the previous section, in order to achieve the enhancement (normally-off) mode of operation, it is necessary to reduce the 2DEG density in the channel. Since the 2DEG is caused by the difference between the polarization-induced fixed charges in AlGa_N and Ga_N layers, reduction of the Aluminum mole fraction, m , or the thickness of AlGa_N layer, d_{AlGa_N} , effectively reduces 2DEG sheet density and shifts the threshold voltage towards positive values. This influence of m and d_{AlGa_N} on the 2DEG sheet density in the channel will be directly shown through the model for $n_{2\text{DEG}}(V_{\text{gs}})$ in the Chapter 3. This approach would easily provide normally-off operation. However, the resulting drain current would be low, since the positive gate-source voltage that can be applied is limited by low Schottky barrier height on the AlGa_N layer. In order to elaborate this in more detail, it is necessary to emphasize that Schottky barrier height directly depends on m . On the other hand, gate-source voltage increase is limited by the value of Schottky barrier height since for high V_{gs} , Fermi level becomes equal to and higher than the conduction band level in AlGa_N layer. Therefore, electrons start to “leak” into AlGa_N and eventually, into the gate when Fermi level touches the conduction band at gate/AlGa_N heterojunction. That’s when the gate breakdown happens, due to increased gate leakage and thermal runaway in the device. Having the limitation of V_{gs} in mind, low values of $n_{2\text{DEG}}$ in the channel will cause significant increase in the sheet-resistance and the overall on-resistance of the device. This is the reason why a simple decrease in Aluminum mole fraction or the thickness of AlGa_N layer is not an efficient way for obtaining normally-off devices.

In the GIT approach, the p-type of AlGa_N provides both: normally-off operation together with increased current capability for high gate-source voltages. The normally-off characteristic is obtained by the p-type of AlGa_N layer which lifts up the potential at the channel, as shown in Fig. 1.7.

Figure 1-6 The cross-section of the Gate Injection Transistor (GIT), [Uemoto 2007].

Figure 1-7 The band-diagram of the GIT under a gate bias of 0V [Uemoto 2007].

Figure 1.8 illustrates the basic operation of the GIT. At gate voltage of 0V, the channel under the gate is fully depleted and the drain current doesn't flow. For gate voltages up to the forward built-in voltage of the p-n junction, V_F , the GIT operates as a Field Effect Transistor (FET). Further increase of gate-source voltage (exceeding the V_F) results in hole injection from the p-AlGaN to

the channel. It is worth noticing that injection of the electrons from the channel into the gate is well suppressed by the heterobarrier at AlGa_{0.2}N/GaN.

Figure 1-8 The schematics of the various GIT operation conditions with various gate voltages. (a) Normally-off operation with fully depleted channel under the $V_{gs}=0V$. (b) FET operation without hole injection at $V_{th} < V_{gs} < V_F$. (c) GIT operation with hole injection at $V_{gs} > V_F$ [Uemoto 2007]

The holes injected to the channel, accumulate equal number of electrons coming from the source in order to keep the charge neutrality. The accumulated electrons are moved by the drain bias with high mobility, while the injected holes stay in the channel area below the gate, due to significantly lower mobility. This so called “conductivity modulation” results in a significant increase of the drain current, while keeping the gate leakage current low.

[Uemoto 2007] provides the simulations of drain and gate current as a function of gate-voltage, for both: Schottky-gate HFET (a typical HEMT from Fig. 1.1.) and a GIT transistor. Observing these simulations, it can be seen that drain current of a conventional HEMT saturates for V_{gs} around 2V, when gate current rapidly increases. On the contrary, the drain current of the GIT is dramatically increased by the aforementioned conductivity modulation. Significant gate leakage current is prevented by the barrier of p-type doped AlGaIn layer, for V_{gs} up to 6V (Fig. 1.9.). The major penalization of the device performance is related to the existence of a p-n junction which increases the total input capacitance of the device. This structure has been commercially implemented by Panasonic.

Figure 1-9 Simulated drain and gate current as a function of the gate voltage for both GIT and a conventional HEMT [Uemoto 2007].

1.4. Vertical GaN power devices-CAVET structure

Power devices in GaN can be either lateral devices grown on sapphire, Si or SiC substrate or vertical devices grown on GaN bulk substrates. Lateral devices are significantly more mature while development of vertical power switches is more difficult due to high defect densities in GaN bulk.

As it was previously shown, the lateral AlGaIn/GaN HEMTs have the source, gate and drain electrodes fabricated on the same plane on top (Fig. 1.1.). In the case when no field-plate is applied, the distance between gate and drain sustains the blocking voltage in the OFF state of the device and therefore, determines the breakdown voltage rating and on-resistance of the switch. The extension of gate electrode called field-plate structure is applied in order to increase the breakdown voltage rating by splitting the peak of the electric field at the drain-side gate edge on two. In this case, as it will be shown in Chapter 6, the peaks of the electric field and therefore the breakdown voltage rating are determined by the field-plate length and the thickness of the oxide below the extension. Still, the field-plate length influences the gate-to-drain distance and therefore the switching on-resistance. Therefore, for high power (>50kW) application where high breakdown voltages (>1.2kV) are required, the lateral topology becomes highly unattractive in performance, cost and manufacturability, due to high on-resistance values and very large chip areas.

Vertical device structure is defined by source and gate fabricated on the top plane and drain electrode fabricated on the bottom plane. The source current flows underneath the gate area and then vertically towards drain. In a vertical device, many sources can be placed in parallel, therefore decreasing the overall on-resistance of the device.

In Si MOSFET technology, vertical devices are fully mature, commercially available and highly applied in high-power converters. In GaN technology, vertical devices are not commercially available and still are in a research state. Although the structure called Current-Aperture Vertical Electron Transistor (CAVET) has been successfully demonstrated, a great deal of effort is needed in material growth, device design and processing, in order to match the performances demonstrated by state-of-the-art AlGaIn/GaN lateral HEMTs. The so called current blocking layer (CBL) shown in Fig. 1.10, which is used to create a barrier to vertical current flow through any other path in the device other than the channel below the gate, is one of the most important and most critical designs in this type of the devices [Chowdhury 2013].

The CAVET GaN device operating principle is based on the idea to use the AlGaIn/GaN junction in order to provide high horizontal mobility of the

electrons in the channel and vertical device structure in order to decrease the on-resistance for high breakdown voltages. Since vertical devices sustain the blocking voltage in the vertical direction in the bulk material of the device, the chip area for a specific current rating is smaller comparing to lateral design. Additionally, the high field region is buried in the bulk which decreases current collapse occurrence and associated dynamic on-resistance. Therefore, extensive device passivation and field-plating are significantly reduced or completely eliminated. This device structure was proposed in 2000 by Yaacov at [Ben-Yaacov 2004] and was originally designed for RF application for dispersion free performance, due to high field region located inside the GaN bulk instead of the AlGaN surface. Later in 2009, the device was redesigned and reported as a high-voltage switch for power electronics application, demonstrating a very promising depletion and enhancement operation modes [Chowdhury 2008].

Figure 1-10 The cross-section of CAVET GaN device [Chowdhury 2013]

1.5. Field-plate application in GaN power switches

Since vertical AlGaIn/GaN structures that would provide significant increase in the breakdown voltage rating could not be manufactured, the field-plate technology in lateral devices was used for this purpose. Additionally, field-plates provided suppression of the current-collapse phenomenon, due to reduction of the electric field at the drain-side gate edge and therefore, reduction of gate leakage in the off-state.

In [Zhang 2000], the first AlGa_N/Ga_N HEMT of 570V of voltage breakdown rating was reported, using the extension of the gate electrode as the field-plate structure. The field-plate principle is very simple – the idea is to spread the peak of the electric field at the drain-side gate edge into two smaller peaks: at the drain-side gate edge and the field-plate edge (Fig. 1.11.). Since the reduction of the electric field peak at the gate edge reduces the gate leakage current in the OFF state of the device, the surface trapping effect will be reduced, and therefore the associated current collapse phenomenon. The penalization in the device characteristics is the inevitable increase in Millers capacitance.

Through the years, single and multiple field-plates structures designed as the extension of gate and/or source electrode have been proposed [Chu 2011]. Therefore, the voltage rating of lateral HEMTs was significantly increased, avoiding extreme increase in gate-to-drain distance which would lead to extremely higher on-resistance, but penalizing the capacitive part. For example, the multiple-structure from Fig. 1.12 was used for design of 1200V device [Chu 2011]. Figure 1.13 shows measured Miller's capacitance dependence on applied drain-source voltage (taken from [Chu 2011]) and authors directly show the influence of each field-plate structure on each part of this capacitance.

Figure 1-11 *The cross-section of an AlGa_N/Ga_N HEMT with the gate field-plate structure and the electric field distribution in the OFF state.*

Figure 1-12 The cross-section of an AlGaIn/GaN HEMT with one gate and double source field-plates, [Chu 2011].

Figure 1-13 The measurement of Miller's capacitance dependence on drain-source voltage in the OFF state of the device, [Chu 2011].

1.6. The main objectives of the thesis

There are two main objectives of this thesis-the first one is a development of a physics-based fully analytical model for input, output and reverse capacitance of a GaN HEMT with the gate field-plate structure (shown in Fig. 1.14), and the second is the optimization of the device design for high-frequency switching application, using previously obtained model.

The motivation for the development of an analytical, physics-based model for capacitive part of this structure was found in the necessity for this type of device models when design optimization is performed, having in mind that this type of models for AlGaIn/GaN HEMT with the field-plate structure has not been proposed so far. This structure was usually analyzed using Finite Element Analysis (FEA) simulations. Although FEA simulations are quite useful for the field-plate design optimization for a given breakdown voltage, their drawback is a necessary fitting of the design equations to the simulated data curves, which makes the optimization valid only for the simulated structure. Therefore, FEA cannot be used for the complete design optimization of the device. On the other hand, the physical models implemented into FEA design simulation software are quite complex and time consuming. Therefore, these physics-based models are not suitable for incorporation into iterative optimization tool which is used for obtaining the optimum device design for a particular application.

As it will be shown in the next Chapter, the analysis of State-Of-the Art in physics-based analytical models demonstrated that AlGaIn/GaN HEMTs **without the field-plate structure** have been highly investigated and completely modeled in terms of output I-V characteristics and C-V characteristics. Since the field plate influence on the I-V output characteristics and switching on-resistance is negligible, the I-V models from previous works can be applied in case of HEMTs that contain the field plate, without expectation of a significant error. **However, the input, output and reverse capacitance of the device are strongly affected by the type and the geometry of the field plate and previously proposed charge models cannot be used.**

The optimization of the device design for high-frequency switching application is the second objective of this thesis. The motivation for this is found in the significant performance improvement of the converter that would employ the switching device with the optimized design.

Figure 1-14 The cross-section of the analyzed GaN HEMT with the gate field-plate structure when the device is in the OFF state.

1.6.1. Physics-based model for input, output and reverse capacitance of an AlGaIn/GaN HEMT with a field-plate structure

In order to improve the design of existing GaN devices for a particular application, it is required to obtain a reliable physics-based model that provides the connection between the device design parameters (geometry and spacing between the electrodes, type and geometry of the field plate, etc.) and electrical characteristics in terms of switching on-resistance and parasitic capacitances. In general, the physics-based model can be used to calculate the power losses in a certain topology where the device is applied, or to optimize the device design from the application point of view. This process is described by the block diagram in Fig. 1.15 where starting from the device itself and following the blocks in the counter clockwise direction, the overall efficiency of the chosen topology is being estimated. Alternatively, starting from a certain application and following the same blocks in the clockwise direction, the device design is being optimized by power losses minimization. In both cases, the device description through analytical equations is needed. Therefore, a physics-based model is a necessary link between the device itself and its application.

Figure 1-15 The block scheme of a device design optimization.

As it was already mentioned, the models for output I-V characteristics of the devices without the field-plate structure can be applied in modeling of AlGaInGa(1-x)N/GaN HEMTs that contain the field-plate extension, since the only influence exists in the drift resistance below the field-plate. As it will be shown in Chapter 3, this modification in the drift part of the overall on-resistance of the device, can be neglected, without causing a significant error. However, the field-plate design in terms of thickness, length and material below the electrode extension, determines the Miller's capacitance dependence on the applied drain-source voltage. Since Miller's charge defines the duration of the "plateau" in gate-source signal and directly influences the switching losses, a precise capacitance model is necessary for device design optimization by power loss minimization, especially in high-frequency switching applications. Therefore, **new capacitance model needs to be obtained** and combined with the existing I-V model, in order to complete the analytical physics-based model for this structure.

1.6.2. The optimization of a device design for application in high-frequency buck converter using previously developed capacitance model

Device design optimization for a target application is shown in Fig. 1.15. The target application for GaN device that will be analysed and modelled in this work is a high frequency (HF) DC-DC converter called Envelope Amplifier (EA), used as a dynamic power supply in Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) transmission techniques. The topology that will be used for EA is a simple buck converter. The main challenge in EA design is to increase the bandwidth of the signal transmission together with the overall efficiency of the converter [Hoversten 2010, Wang 2005, Yu 2012, Raab 1996, Wang 2006, Norris 2012, Vasic 2010, Cucak 2013]. Since increase in bandwidth implies increase in switching frequency, GaN HEMTs present excellent candidates for power switches due to much better FOM values in comparison to Si MOSFETs. It is expected that GaN HEMTs will be able to switch at significantly higher frequency, providing much better efficiency. Furthermore, if a physics-based analytical model of the device is developed, the design of the device can be optimized for this particular application, providing optimum performance and minimum power losses in the converter.

1.7. The organization of the thesis

Following the Introduction and Motivation chapter, the work covered in this thesis is presented through six chapters. The organization of the thesis and the summary of analysis and work presented in each chapter, are the following:

- **Introduction and Motivation** addresses the advantages of wide-bandgap over Silicon devices, provides an insight into different Gallium Nitride HEMT structures and operating principles, State Of the Art in commercially available GaN devices and finally, the main objectives of this thesis.
- **Chapter 2** gives the detailed review of **State Of the Art, in the domain of physics-based models for AlGaIn/GaN HEMTs**. Analyzing many different works, it has been established that physics-based, fully analytical model for capacitive part of AlGaIn/GaN HEMT with the field-plate extension of the gate electrode has not been reported so far.
- **Chapter 3** presents **the existing physics-based analytical model for I-V output characteristics of a GaN HEMT without the field-plate structure**. Since COMSOL simulations showed that gate field-plate has a negligible influence on the I-V characteristics, this model was used in

our work for the description of the I-V part. **The contribution** was made through additional **modeling of source and drain drift resistances and inclusion of these resistances into extrinsic model of a device.**

- **Chapter 4** presents the **first main contribution of the thesis- the proposed physics-based fully analytical model for input, output and reverse capacitance dependence on the applied drain-to-source voltage, when the device is in the OFF state.** The complete methodology for calculation of Miller's (C_{gd}), output ($C_{oss}=C_{gd}+C_{ds}$) and input capacitance ($C_{iss}=C_{gd}+C_{gs}$) is presented. The experimental characterization is performed in order to quantify the precision of the model.

- **Chapter 5** presents simulation results of the power loss model for a high-frequency buck converter, when previously modeled and experimentally obtained curves for I-V and C-V characteristics are implemented. Additionally, simulated efficiency curves are compared to the measured ones, using the prototype of a high-frequency buck converter that used modeled GaN HEMT as the main switch. Furthermore, additional simulations with different device package and synchronous buck configuration were performed, in order to see how they influence the overall efficiency of the converter.

- **Chapter 6** presents the **second main contribution of the thesis which is the final optimization of the device design,** using previously proposed physics-based model. In order to perform the optimization of the device design for a target breakdown voltage, **the analytical relations between the peaks of the channel electric field and the design of the field-plate were derived.** Final simulations are performed in order to compare the efficiency of the converter when nominal and optimized design are used.

- **Summary and future work** provides the summary of work presented in this thesis, highlights the main contributions and discusses the future work.

Chapter2. State Of The Art in physics-based models of AlGa_N/Ga_N HEMTs

2. State Of The Art in physics-based models of AlGaN/GaN HEMTs

2.1. Analysis and modeling of AlGaN/GaN HEMTs with and without the field-plate structure - device characteristics of interest

Observing the physics-based models for AlGaN/GaN HEMT structure with and without the field-plate, we can distinguish models that are focused on different aspects of the device performance i.e. models of different features of a HEMT. For example, [Sacconi 2001] models the output characteristics of the device but taking into account a specific influence of a crystal structure polarity on the piezoelectric and spontaneous polarization effects. In [Islam 2002], the temperature-dependent nonlinearities in transconductance, output power gain and power added efficiency are modeled, considering the RF application of AlGaN/GaN HEMTs. In [Park 2004], thermal conductivity dependence on the type of the substrate (SiC, sapphire) has been modeled. In [Kaushik 2013], the model for a particular way of current collapse which is seen as “kink” effect has been proposed, relying on the virtual gate creation.

Speaking of AlGaN/GaN devices, breakdown and trapping effects are highly investigated topic. Since the breakdown voltage rating is one of the key features of the device, the analysis and modeling of breakdown mechanisms is crucial for further examination and design. On the other hand trapping effects and associated current-collapse or, in the case of switching application – “dynamic on-resistance” phenomenon, are very important for the quality of device performance. Therefore, many of previously presented works in the SOA were focused on these two topics.

2.1.1. HEMT breakdown mechanism

The breakdown mechanisms in AlGaN/GaN HEMTs with and without the field-plate structure were and still are highly investigated topic.

Up to know, the most detailed analysis of AlGaN/GaN HEMTs breakdown mechanisms is presented in [Zhao 2016], proposing a modified breakdown characterization method and addressing six main leakage currents in GaN-based HEMTs. As a summary, it has been established that these devices

can suffer from two types of breakdown: the breakdown initiated by impact ionizations which occurs if electric field at the drain-side gate edge or field-plate edge reaches the breakdown strength of the GaN material, or the breakdown due to thermal runaway. According to [Zhao 2016], the thermal runaway is caused by the increased values of gate-leakage and buffer leakage current, when drain-source voltage is being increased. Since leakage currents produce thermal energy, the temperature is increased which further increases the gate leakage current. Therefore, a kind of uncontrolled positive feedback is being formed, leading to thermal runaway. In order to illustrate the relation between breakdown curves and breakdown mechanisms, the relation between leakage currents and thermal runaway together with impact ionization has been analyzed. It was found that leakage current values affect both breakdown mechanisms. Therefore, reduction in leakage can alleviate both the thermal runaway and impact ionization process, therefore improving breakdown voltage of the device.

Speaking of HEMTs that do not contain the field-plate, the following works are highly important in analysis and modeling of the device breakdown. In [Turuvekere 2013], modeling of different gate-leakage mechanisms in AlGaIn/GaN HEMTs has been proposed and experimentally verified, while [Turuvekere 2014] furthermore analyzed the dominant mechanisms of the gate leakage current depending on the Aluminum mole fraction in AlGaIn layer. In [Ghosh 2015], the reverse and forward gate-leakage current are analytically modeled in a surface-potential-based compact model.

Speaking of impact ionization in terms of breakdown initiation, [Schimizzi 2012] provided a temperature dependent impact-ionization-initiated RF breakdown model, giving the relations between the impact ionization in the channel on one hand and gain saturation, power added efficiency and the output power on the other (observing the devices that are operated in RF power amplifier circuits). In [Hanawa 2014], a 2-D analysis of the breakdown characteristics in AlGaIn/GaN HEMTs is performed for various permittivities and thicknesses of passivation layer, showing that OFF-state breakdown voltage increases with increase of relative permittivity of the passivation layer. Furthermore, different technological methods for breakdown voltage increase of HEMTs without the field-plate, have been proposed. One of them is presented in [Lu, Palacios 2010] which can be applied to the HEMTs grown on Si substrate. In that work, new technological approach is used for the removal of the original Si substrate and subsequent transfer of the AlGaIn/GaN HEMT structure to the insulating carrier wafer (such as glass or polycrystalline AlN). In this way, the existence of a substrate-GaN buffer leakage current which plays an important role in the breakdown of these devices is canceled. As a proof of the proposed

methodology, an AlGaIn/GaN HEMT of 1500V of the breakdown voltage was obtained, without an application of the field-plate. Furthermore, in [Choi 2006], Fe doping of a GaN buffer, showed significant improvement in the stabilization and robustness of the OFF-state breakdown characteristics.

In order to improve the design of AlGaIn/GaN HEMTs in terms of breakdown voltage rating and robustness, it was necessary to provide physics-based models and detailed analysis of the breakdown voltage mechanisms. Since this is a very complex topic, not that many analytical models for different types of breakdown were presented in the literature. As it was explained in the Introduction of this thesis, the major design modification that increases the breakdown voltage rating of GaN HEMTs is the field-plate technology [Karmalkar 2001]. Since the field-plate extension reduces the peak of the electric field at the drain-side gate edge, the structures with more than one field-plate extension were investigated and presented in the literature [Xing 2004, Chu 2011]. In addition to that, different field-plate technology called “integrated slant field-plate” was proposed in [Dora 2006] in order to increase the breakdown voltage even more.

2.1.2. Trapping and current collapse

Besides the breakdown analysis, the trapping mechanisms in GaN HEMTs with and without the field-plate are highly investigated topic.

Speaking of HEMTs without the field-plate, the following works are very important in analysis and modeling of trapping effects. [DasGupta 2012] provided a thorough analysis of Aluminum mole fraction and passivation influence on trapping and slow detrapping effects in AlGaIn/GaN HEMTs. [Joh 2011] proposed a new methodology for investigation of the trapping characteristics in GaN HEMTs, based on the current-transient measurements while [Chini 2013, Bisi 2014] investigated the advantages and limitations of the current-transient methods used for study and modeling of deep level traps in GaN HEMTs.

Since one of the reasons for the field-plate application is the reduction of current-collapse phenomenon and related dynamic on-resistance occurrence, many papers investigated the field-plate influence on the suppression of trapping effects. One of the most complete works related to this topic is presented in [Huang 2014]. In that work, the quantification of the field-plate effect on current collapse has been provided, by physics-based modeling of current collapse. Furthermore, the laboratory setup for current collapse measurements has been presented and used for the measurements on

AlGaN/GaN HEMTs with different field-plate designs as well as on HEMTs without the field-plate structure. The proposed model has been verified through the experimental results. It has been shown that field-plate design reduces the gate-edge peak electric field which leads to reduced gate leakage current and electron trapping, which in turn improves the current collapse performance. On the other hand, it was demonstrated that the second peak of the lateral electric field at the surface of AlGaN, increases the electron detrapping rate and accelerates the electrons hopping in the traps along the AlGaN surface, which additionally reduces the density of trapped electrons and results in notable suppression of current collapse.

Nevertheless, the physics-based models of interest in our work are models of I-V and C-V characteristics, since these models describe the most important characteristics in terms of switching operation of the device. In order to avoid significant increase in the complexity of the model, the impact ionization was considered for the breakdown mechanism, while the trapping effects were not modeled due to presence of field-plate in the analyzed design. Furthermore, in the capacitance modeling of the device, trapping and detrapping of surface charge will not be “visible” in the MHz frequency range due to the fact that dynamic on-resistance recovery time is in the milliseconds-range [Bisi 2014].

2.2. AlGaN/GaN HEMTs without the field-plate structure

From the modeling point of view, AlGaN/GaN HEMTs without the field-plate structure present the devices that were designed and manufactured first and therefore, the complete analytical physics-based models for I-V and C-V characteristics of these devices already exist. Additionally, the analytical models of their predecessors, AlGaAs/GaAs HEMTs, can be used applying some modifications, due to the presence of a strong built-in polarization in the AlGaN layer.

The reason why AlGaN/GaN devices without the field-plate extension were completely modeled, lies not only in the fact that they were the first fabricated devices but also in the fact that additional single or multiple field-plate extension of gate and/or source electrode, increases the complexity of the device structure and therefore, complicates the corresponding modeling analysis. From this reason, all of the proposed physics-based models of the devices that contain single or multiple field-plate (depending on the target voltage breakdown), are completely or partially based on numerical analysis.

2.2.1. Models for 2DEG sheet density dependence on gate-source voltage

The starting point for development of an I-V model, certainly is a model for 2DEG density dependence on the applied gate-source voltage, $n_{2DEG}(V_{gs})$. In order to model this, it is necessary to provide a model for Fermi level dependence on gate-source voltage, $E_f(V_{gs})$, or in other words, Fermi level dependence on the 2DEG sheet density, $E_f(n_{2DEG})$.

The first models for $E_f(n_{2DEG})$ were proposed more than 30 years ago for AlGaAs/GaAs HEMTs, and the same methodology can be applied for AlGaN/GaN HEMTs. In the first approximation [Delagebeadeuf 1982] assumed $E_f=0$ in the equation for $n_{2DEG}(V_{gs})$, while [Lee 1983] assumed a linear approximation of $E_f(n_{2DEG})$. In [Kola 1988], commonly used second order approximation is proposed while in [Shey 1989] non-linear dependence $E_f(n_{2DEG})$ was proposed. Although these approximations lead to simple expressions for $n_{2DEG}(V_{gs})$, the results were accurate only for one range of device operation. Therefore, [DasGupta 1993] proposed $E_f(n_{2DEG})$ as a simple polynomial dependence which provided both –more precise and analytical expression for $n_{2DEG}(V_{gs})$.

Regarding the model for polarization charge which is one of the key points in obtaining precise $n_{2DEG}(V_{gs})$ model, work from [Ambacher 1999] modeled 2DEG density induced by spontaneous and piezoelectric polarization charge in N- and Ga-face AlGaN/GaN wurtzite structure. This model is very important since it will be used for calculation of the polarization charge in many $n_{2DEG}(V_{gs})$ models.

[Rashmi 2002] proposed a new model for $n_{2DEG}(V_{gs})$ which consisted of three different approximations of $E_f(n_{2DEG})$ relation, depending if a device is operating in “weak”, “moderate” or “strong” inversion (making the analogy with MOSFET operation modes) and using the polarization charge model from [Ambacher 1999]. Due to excellent trade-off between the complexity and precision, this model was chosen for implementation in our work.

Furthermore, [Yu 2003] proposed a model for $n_{2DEG}(V_{gs})$ that takes into account nonlinear dependence of spontaneous and piezoelectric polarization on Al mole fraction. In [Li 2008] previously proposed $n_{2DEG}(V_{gs})$ models are improved by employing the Robin boundary condition when solving 1-D Schrodinger equation. In [Cheng 2009], improved model that included parasitic channel conduction in AlGaN layer for high gate-source voltages is presented, giving the estimation of the onset voltage for this parasitic channel. However,

the model from [Cheng 2009], was based on numerical methods which are not suitable for implementation in circuit simulators and that was the main drawback of this model. Furthermore, [Khandelwall 2011] provided an unified analytical model for $n_{2DEG}(V_{gs})$ using different approximations for $E_f(n_{2DEG})$ in two different regimes of operation: Region I of subthreshold defined for $E_f - E_0 < 0$ and Region II above the threshold defined for $E_f - E_0 > 0$, where E_0 is the first energy subband in the quantum well. However, the model from [Khandelwall 2011] did not take into account the parasitic channel conduction for higher gate-source voltages. The drawback of the model from [Cheng 2009] was resolved in [Karumuri 2014] who proposed fully analytical model for $n_{2DEG}(V_{gs})$, avoiding numerical methods, that took into account electron charge in AlGaIn layer and the parasitic channel conduction. Therefore, the model correctly predicted the saturation of a 2DEG density at higher gate-source voltages.

The main limitation in the precision of previously presented “threshold-based” models, lies in the definition of the threshold, which is based on the Fermi level at the source-end of the device for which we assume to be unchanged along the channel (taking the bottom of the conduction band as a reference). Since the Fermi level can vary significantly under different gate-to-channel voltages as shown in [Cheng 2011], negligence of this variation when defining the threshold voltage will bring some inherent errors into the model. Therefore, different kind of physics-based model for $n_{2DEG}(V_{gs})$ and I-V and C-V characteristics of the device, based on surface-potential (SP) analysis was proposed in [Cheng 2011] and [Khandelwal 2012]. In [Cheng 2011] a SP-based drain current model was presented, taking into consideration only the first energy level in the quantum well (E_0). As shown in [Khandelwal 2012] this does not provide sufficient accuracy, especially when gate-source voltage is close to the threshold value. Therefore, [Khandelwal 2012] proposed a SP-based analytical model for all intrinsic charges (gate, drain and source) in AlGaIn/GaN HEMT, considering two important energy levels in the quantum well (E_0 and E_1). The proposed model provided much better accuracy in the whole range of gate-source voltages.

2.2.2. Models for I-V characteristics

Speaking of analytical models for I-V characteristics, the main difference between them lies in the models used for charge-control dependence, $n_{2DEG}(V_{gs})$ and the drift velocity dependence on the lateral component of the electric field in the channel, $v_{drift}(E)$. Charge-control models were presented in the previous section, while different drift-velocity models will be addressed through the State Of the Art review in this section. Additionally, when speaking about different

models for output I-V characteristics, the saturation region in $I_d(V_{ds}, V_{gs})$ curves can be modeled taking into consideration the channel length modulation (or not), depending on how important the saturation region of operation is. Finally, it is important to highlight that the same I-V models can be used for the devices with and without the field-plate structure, without expectation of a significant error. This will be elaborated in detail in the following chapter.

As in the case of charge-control models, the models for I-V characteristics exist since the early 1980's. The first models were focused on AlGaAs/GaAs HEMTs but almost the same methodology (with the exception of polarization model) can be applied for AlGaN/GaN HEMTs as well.

The first model for AlGaAs/GaAs I-V characteristics was proposed in [Delagebeadeuf 1982]. This model was based on a charge-control model that neglected the value of the Fermi level voltage in the calculation of $n_{2DEG}(V_{gs})$. Additionally, the mobility of 2DEG carriers, μ , was treated as a parameter which is independent on the lateral component of the electric field in the channel, E . This gave two-piece linear model for the drift-velocity dependence on the electric field, $v_{drift}(E)$ and penalized the precision of the I-V characteristics. These issues were improved in [Lee 1983], where the charge-control model that took into account Fermi level dependence on the gate-source voltage was applied. In the work of [Lee 1983], linear approximation of $E_f(n_{2DEG})$ was used. Necessary parameters were obtained by curve-fitting according to the simulation results of a Fermi-Dirac's statistics for n_{2DEG} . Additionally, the field-dependent mobility was used, giving the three-piece linear approximation for the velocity-field characteristic.

Observing the models proposed in [Delagebeadeuf 1982], [Lee 1983] and [Çil, 1985], it can be seen that conduction through the AlGaAs layer which is typical for higher values of gate-source voltages was neglected. Since the occurrence of this conduction causes the saturation of the 2DEG in the quantum well, these models were unable to predict experimentally observed decrease in transconductance for higher gate-source voltages. Therefore, further works were focused on modeling of this "parallel-MESFET" conduction so that obtained models are valid for the entire range of applied V_{ds} and V_{gs} . Speaking of AlGaAs/GaAs HEMTs, this was done for the first time in [Wang 1986], modeling the current through the AlGaAs layer as a function of the current carried by 2DEG, which made the model significantly more complex. In [Hughes 1987], on the other hand, Poisson and drift diffusion equations were solved numerically in order to derive two dimensional electron gas concentration and the AlGaAs current component as a function of gate-source voltage. Besides taking into consideration AlGaAs conduction, the model from

[Ahn 1994] included the effect of mobility degradation with increase of electric field in the channel, channel length modulation in the saturation region of operation and drain and source series resistances.

When comparing AlGaIn/GaN HEMTs to previously modeled AlGaAs/GaAs HEMTs, we observe that the main difference between them lies in the strong built-in spontaneous and piezoelectric polarization which exists in AlGaIn/GaN HEMTs and gives the possibility to design and manufacture these devices without any additional doping. Therefore, the main difference between the I-V models lies exactly in the charge-control model that takes into account this polarization-induced 2DEG and neglects the “doping-induced” charge (if the AlGaIn layer is unintentionally doped). The work from [Ambacher 1999] modeled 2DEG induced by spontaneous and piezoelectric polarization charge in N- and Ga-face AlGaIn/GaN heterostructures, providing the basis for the first analytical model for I-V characteristics of these devices, presented in [Rashmi 2001]. The I-V model from [Rashmi 2001] used field-dependent mobility from [Lee 1983] and neglected the values of Fermi level voltage in the $n_{2DEG}(V_{gs})$ charge-control model that was used. The saturation region of operation was precisely modeled, taking into account channel length modulation. This was done by dividing the channel into two regions: low-field region where Gradual-Channel-Approximation (GCA) stands and a high-field region where velocity saturation exists. The goal of precise modeling of saturation in I-V curves was to provide a precise model for output conductance in the saturation region, which presents an important microwave signal parameter. Furthermore, [Rashmi 2002] provided an improved analytical model for $n_{2DEG}(V_{gs})$ that was incorporated into the model for I-V characteristics. The proposed charge-control model used three different approximations for the Fermi level dependence on 2DEG sheet density, $E_f(n_{2DEG})$ depending if a device operates in weak, moderate or strong “inversion”. This model provided an excellent trade-off between the complexity and precision and therefore, was used for $n_{2DEG}(V_{gs})$ and $I_d(V_{ds}, V_{gs})$ models in this thesis.

In [Li 2008], a threshold-voltage-based analytical model for the current-voltage characteristics of AlGaIn/GaN HEMTs is proposed. As it was already mentioned in the previous section, [Li 2008] proposed numerically more complex but improved charge-control model of $n_{2DEG}(V_{gs})$ (by employing Robin boundary condition when solving 1-D Schrödinger equation). Comparing to the $E_f(V_{gs})$ obtained when 1-D Schrödinger equation was solved using Dirichlet’s condition in [DasGupta 1993], much more precise $E_f(V_{gs})$ was obtained. In addition to that, [Li 2008] proposed a modified Polyakov-Schwierz mobility model for implementation into I-V characteristics of the device. The proposed field-dependent mobility model was able to precisely describe negative

differential mobility in $v_{drift}(E)$ dependence (comparing to conventional and widely used Canali model from [Turin 2005]). Additionally, it provided a better fit of drift velocity in the high-field region, comparing to Canali model. Overall, these improvements provided very good agreement between the measurements and the predicted curves for $I_d(V_{ds}, V_{gs})$, $I_d(V_{gs})$ and $g_m(V_{gs})$, where $g_m(V_{gs})$ is the transconductance dependence on the applied gate-source voltage. On the other hand, complexity of the model was significantly increased, especially due to precise modeling of negative differential mobility and drift velocity in high-field region, which are important for precision in the transition and saturation zones in I-V characteristics. Since these zones are not of interest for switching application, this model was not the chosen one in our work.

Comparing to threshold-based model from [Li 2008], surface-potential based model from [Cheng 2009] provided an unified charge-control model that takes into consideration parasitic channel conduction in AlGaIn layer for high gate-source voltages. Using this improved $n_{2DEG}(V_{gs})$ and simplified $v_{drift}(E)$ model, the I-V characteristics were obtained, showing very good agreement with the measurements in the full range of V_{ds} and V_{gs} . It should be mentioned that, benefiting from the unified $n_{2DEG}(V_{gs})$ expression, the I-V expression has a second-order continuity which means that transconductance and output conductance (obtained by differentiating I_{ds} with respect to V_{gs} and V_{ds}) are continuous. This is very important for the simulation speed and convergence performance of the model. Still, the complexity of the surface-potential models is too high and calculatively demanding, from the point of view of implementation into circuit simulators. Additionally, higher range of gate-source voltages is not of interest in switching mode of operation of the device. Therefore, this model was not the chosen one in our work.

2.2.3. Models for C-V characteristics

Speaking of C-V models of AlGaIn/GaN HEMTs without the field-plate structure, it can be said that they are highly investigated topic. Nevertheless, the majority of proposed models is focused on modeling of the dependence of input capacitance, C_{iss} , (often referred to as total gate capacitance) on the applied gate-source voltage, for drain-source voltage equal to zero volts. These models are obtained using different, previously presented charge-control models for $n_{2DEG}(V_{gs})$. Additionally, gate-source and drain-source capacitance dependencies on the applied drain-source voltage were obtained as the derivative of the total gate charge with respect to gate-source and drain-source voltages. Since the total gate charge was obtained using the charge-control model for $n_{2DEG}(V_{gs})$, we can say that obtained capacitance-dependencies are

valid only above the threshold voltage, i.e. when the transistor is turned-on. Therefore, these models are focused on microwave performance of the device. On the other hand, when speaking of switching application, the crucial behavior is a capacitance dependence on drain-source voltage in the subthreshold region of operation, i. e. when the device is turned-off.

Speaking of total gate capacitance dependence on the applied V_{gs} , [Chattopadhyay 2006] presented a compact analytical charge-control model to describe the gate capacitance of AlGaIn/GaN Modulation-Doped HEMTs (MODFETs), which are similar to HEMTs with the exception of AlGaIn layer being intentionally doped. This model took into account the capacitance components due to 2DEG, neutralization of donors in AlGaIn layer and contribution of free electrons in AlGaIn layer, when parasitic conduction through AlGaIn occurs. The model is temperature dependent, since it is based on proposed temperature-dependent charge-control model, in which, effective threshold voltage and Fermi-level dependence on gate-source voltage change with temperature. Still, this model gives a compact model for total gate capacitance (input capacitance of the device), without separation of gate-source and gate-drain parts. In addition to that, it is valid in the range of gate-source voltages where charge-control model is defined, meaning above the threshold. In [Gangwani 2007], the total gate capacitance dependence on the applied gate-source voltage was separated into gate-source and gate-drain capacitances dependence on V_{gs} , using the charge-control model from [Rashmi 2002].

In [Cheng 2009], an unified charge-control model that takes into account the current conduction through AlGaIn layer for high gate-source voltages was proposed. This charge model was used for obtaining $C_{gs}(V_{gs})$ for two different values of V_{ds} , as well as for $C_{gd}(V_{ds})$ for two different values of V_{gs} . From the curves obtained for $C_{gs}(V_{gs})$ for two drain-bias voltages, it can be concluded that the dependence of C_{gs} on V_{ds} is relatively weak, as the 2DEG sheet density in HEMT is primarily modulated by the gate-source voltage. It has been concluded that for V_{gs} lower than the threshold, C_{gs} consists only of gate-source fringing capacitance which does not depend on the applied V_{ds} . This conclusion was important for further analysis of capacitance behavior in terms of device modeling for switching application. On the other hand, two $C_{gd}(V_{ds})$ dependencies for two values of V_{gs} (higher than the threshold) showed that the highest dependence of C_{gd} on V_{ds} when transistor conducts, exists for low values of V_{ds} , i.e. when device conducts in the linear part of I-V characteristics. As we move towards higher and higher values of V_{ds} i.e. more and more deeply into the saturation region, this dependence decreases. To summarize, we can say that C-V model from [Cheng 2009] provided some useful conclusions about non-linear C-V behavior in AlGaIn/GaN HEMTs, but is primarily focused on

capacitance-behavior when the device is in the on-state, and therefore, cannot be used for modeling of capacitances in the deep subthreshold region.

Similar approach to [Cheng 2009] has been used in [Yigletu 2013], where $C_{gs}(V_{gs})$ and $C_{gd}(V_{ds})$ (for V_{gs} higher than the threshold) were obtained using different, but also unified charge-control model, proposed in [Khandelwal 2011]. This charge-control model and therefore C-V model is simplified comparing to the one in [Cheng 2009] since only the contribution of the first energy subband in the quantum well, E_0 , is taken into account.

Furthermore, surface-potential (SP) models for C-V characteristics were developed and proposed. Comparing to previously presented “threshold-based” models, SP models are emphasized for the next-generation compact modeling, due to their inherent symmetry and their use of a single expression to describe all the regions of device operation. In [Khandelwal 2012], using a SP calculation, expressions for gate, drain and source charge are proposed. Gate charge was calculated using a SP-model for 2DEG sheet density dependence on gate-source voltage and the potential inside the channel. Furthermore, drain and source charges are determined as a predefined partition of the channel charge. Again, $C_{gs}(V_{gs})$ and $C_{gd}(V_{ds})$ for three different values of V_{gs} higher than the threshold, are calculated and compared to the experimental measurements. One step further was made in [Khandelwal 2013] where also using a SP model for charge-control of the 2DEG, $C_{gs}(V_{ds})$ was obtained in addition to $C_{gd}(V_{ds})$. In [Hou 2013], a compact physics-based model, using division-by-charge method has been proposed. Both $C_{gd}(V_{ds})$ and $C_{gs}(V_{ds})$ for different values of V_{gs} higher than the threshold value were proposed, showing an excellent agreement with Silvaco simulations. However, all of the previously presented models are based on the charge-control models for n_{2DEG} sheet density, meaning that they are valid for on-state of a device, while the parasitic capacitance components which are dominant in the subthreshold region of operation were not modeled.

One of the works that provided excellent qualitative explanations for C_{gd} , C_{ds} and C_{gd} dependencies on V_{gs} and V_{ds} for AlGaIn/GaN HEMTs in microwave applications, is the work from [Liu 2011]. That work was focused on the influence of SiN passivation on I-V and C-V characteristics of AlGaIn/GaN HEMTs. As it was explained in many papers, the passivation of AlGaIn surface is applied in order to decrease the density of surface traps and therefore, suppress the current collapse phenomena. In [Liu 2011]2004, the measurements of the aforementioned dependencies were carried out before and after the passivation of the device, and each change was qualitatively explained, addressing the physical origin of each of these capacitances. It was concluded that passivation increases $C_{gs}(V_{gs})$ values in the area of V_{gs} below the threshold,

since the capacitance values in this range are dominantly determined by the fringing capacitance, which is increased when SiN layer (as a material with higher dielectric constant comparing to air) is induced. On the other hand, for values higher than the threshold, C_{gs} is dominantly determined by the change of the 2DEG density in the channel. Therefore, in this range of V_{gs} , the difference in C_{gs} values before and after passivation becomes negligible. Regarding the $C_{gd}(V_{ds})$, it was discovered that in the complete range of V_{gs} , this capacitance has higher values after the passivation (which is expected due to higher fringing part of the capacitance), but also has a higher decrease-rate with increase of V_{ds} after the passivation, comparing to $C_{gd}(V_{ds})$ dependence before passivation. This is explained by the fact that after passivation, the change in depletion region in the channel at the drain-side gate-edge is more sensitive to the variation in the applied V_{ds} , since the surface-charge trapping is reduced.

Finally, [Zhang 2014] presented a SP-based model for $C_{gd}(V_{ds})$ and $C_{gs}(V_{ds})$ which takes into consideration parasitic (fringing) components of these capacitances, in addition to the 2DEG control model. Therefore, the proposed model is valid from the deep subthreshold to the maximum values of gate-source voltage and gives the non-linear dependencies for $C_{gd}(V_{ds})$ and $C_{gs}(V_{ds})$ for AlGaIn/GaN HEMTs without the field-plate, which can be used in physics-based modeling of switching devices.

Observing previously presented State-Of-the Art in physics-based models of AlGaIn/GaN HEMTs without the field-plate structure, we can summarize that many different analytical models for charge-control of the 2DEG and I-V characteristics of the device, has been proposed. Furthermore, many analytical models describes the input capacitance dependence on the applied gate-source voltage, as well as gate-source and gate-drain capacitance dependence on the applied drain-source bias, when the transistor conducts. This type of capacitance models is valid only above the threshold, meaning that these models are focused on a microwave performance of the device. Finally, [Zhang 2014] proposed the capacitance model that takes into consideration parasitic (fringing) components of $C_{gd}(V_{ds})$ and $C_{gs}(V_{ds})$ which present the dominant part of capacitances in the subthreshold region of operation. Therefore, the C-V model of the devices without the field-plate has been developed in terms of not only a microwave but a switching application as well. To conclude, we can say that AlGaIn/GaN HEMT structure without the field-plate was modeled completely, in terms of I-V and C-V characteristics.

2.3. AlGaIn/GaN HEMTs with one or multiple field-plate structure

The application of field-plate structure with a goal of device breakdown-voltage increase, was proposed in the early 2000's, by the group from University of California, Santa Barbara led by U. K. Mishra. This group conducted many research activities on the topic of analysis, design and optimization of GaN HEMTs with the field-plate structure. Through the years, many other research centers became involved with this topic, investigating different aspects of the gate field-plate application, different field-plate architectures (single and multiple) and the most important effects of the field-plate on the AlGaIn/GaN HEMT performance: breakdown voltage increase and suppression of current collapse phenomena.

2.3.1. Analysis and modeling using numerical simulations

In [Zhang 2000], the first AlGaIn/GaN HEMT of 570V of voltage breakdown rating was reported, using the extension of the gate electrode as the field-plate structure. Furthermore, in [Xing 2004], double gate-field-plate structure was proposed and used for fabrication of 900V AlGaIn/GaN HEMT. In [Saito 2005] the analysis of a double field-plate device, made through the extensions of drain and source electrodes was presented. The analysis of this structure was based on a TCAD tool simulations that used Finite Element Analysis. Additionally, that work provided an optimization of an on-resistance-breakdown voltage dependence by minimization of contact lengths and contact resistivity, i. e. contact resistances of the device. In [Karmalkar 2001], a detailed study of a device with single gate field-plate structure in terms of breakdown voltage dependence on the field-plate thickness, length and type of the oxide has been carried-out using 2D simulations. Some of the crucial **conclusions** about the relations between the breakdown voltage and thickness and length of the field-plate were obtained and will be presented here:

1. **maximum breakdown voltage** will be obtained for **an optimum thickness**. This is because, for large values of thickness, the effect of field-plate vanishes and the field distribution consists of a single triangular lobe near the gate edge. On the other hand, for thickness equal to zero, the presence of field-plate simply extends the gate electrode for the value equal to the field-plate length, so the field distribution is the same as for large values of thickness, only shifted to a "new" gate edge.

In both cases, for extremely high and low values of the oxide thickness, the breakdown voltage is low. **The breakdown voltage reaches its maximum for some value of thickness in between.**

2. **The breakdown voltage will not increase for increase of the field-plate length beyond a certain point.** This is, because, the field distribution along the 2DEG consists of two triangular lobes with peaks near the gate-edge and the field-plate edge. The breakdown voltage presents the total area under these lobes for a given peak of the electric field. The increase in this area will saturate as the overlap of the lobes decreases with increase in field-plate length.

Furthermore, the work presented in [Karmalkar, 2005] provided very important guidelines on optimization of a field-plate design (thickness, length and oxide material) for a given breakdown voltage. The optimization was done with a goal of obtaining the optimum electric-field distribution at the surface and in the channel together with the minimization of the gate capacitance increase. The aforementioned guidelines are given in a form of a simple model that relies on the curve fitting according to the results of 2D numerical simulations. Although very useful for optimization of a field-plate design for a given breakdown, model lacks the analytical background and is valid only for the simulated structure. Therefore, the model from [Karmalkar, 2005] is not suitable for implementation into iterative design optimization algorithms and cannot be used for general device design optimization. The extension of this model is given in [Karmalkar 2006] where the relations between the peaks of the electric field in the channel and the applied drain-source voltage were obtained. This model proposes that the complete distribution of the electric field can be approximated as a superposition of triangular distributions, which are analogous to the ones of a depletion layer in a p-n junction. Consequently, it demonstrated that the peak of the electric field in the channel increases as a square root of the drain-source voltage, which is an important conclusion and a very useful approximation. The model also allows the estimation of the electric field reduction and breakdown voltage improvement when comparing these devices to the devices that do not contain the field-plate. Still, the model is based on the previous work from [Karmalkar, 2005] where the peaks of the electric field are related to the thickness and length of a field-plate by curve fitting according to the numerical simulations. Therefore, this extended model is valid only for the simulated structure and lacks the analytical background as well.

Finally, important work in this area, also based on 2D simulations, was presented in [Visalli, 2010] where the effect of a gate field-plate structure in the case modified GaN HEMT that contains double AlGa_N/Ga_N/AlGa_N

heterostructure was investigated. Previous work of this group [Visalli, 2009] showed that double heterojunction FETs (DHFETs) are better comparing to single AlGaIn/GaN HFETs in terms of higher breakdown voltage and lower on-resistance, due to improved channel carrier confinement and the higher critical electric field of the AlGaIn buffer layer. However, as demonstrated in [Visalli, 2009], these devices with large gate-to-drain distance (approximately L_{gd} higher than $8\mu m$), have a breakdown voltage which does not linearly increase with L_{gd} , due to a double leakage path between the Silicon substrate and the metal contacts, which makes the device break at the silicon interface. In [Visalli, 2010] it has been shown that the effect of the field-plate on these devices is not significant, since the breakdown is still dominantly caused by the silicon substrate leakage. The increase in breakdown voltage due to application of field-plate in DHFETs, exists only for devices small L_{gd} (lower than $8\mu m$ approximately) and this increase is more than double of the breakdown voltage rating of a DHFET without the field-plate. This was an important conclusion for analysis of a slightly modified structure of GaN HEMTs.

2.3.2. Analytical models

Speaking of analytical models for AlGaIn/GaN HEMTs with one or multiple field-plate structure, the models presented in the literature so far, were mostly focused on the calculation of surface-potential distribution and the channel electric field, with the aim of a field-plate design optimization for a given breakdown voltage. However, the optimum electric field management is the only considered criterion in the optimization process, while the associated Miller's capacitance that is crucial for high-frequency power performance is not taken into account.

The first surface-potential model for a single-gate field-plate structure was given in [Kaddeche 2009]. In [Kaddeche 2009], simplified analytical model for calculation of the electric-field profile in the channel for this device structure was presented. The model was used for an approximate prediction of the channel electric field peak under different drain-source voltages. Additionally, different values for oxide thickness and length were used in order to estimate the electric field distribution for different designs.

More mature analytical approach based on conformal mapping technique was given in [Coffie 2014]. In [Coffie 2014], the proposed analytical model was capable of determining the number of field-plates needed for a target breakdown voltage. Additionally, it provided the universal design rules in terms of determination of a necessary field-plate length, L_{fp} , and a field-plate

distance from the channel, a , based on aspect ratio L_{fp}/a . Therefore, the optimization of the field-plate design has been proposed in order to provide optimum electric field management (equal peaks of the electric field at the gate edge and the field-plate edges). However, the increase of the associated Miller's capacitance, which is crucial for high-frequency applications, is not taken into account.

Finally, [Ahsan 2016] provided analytical surface-potential based model for AlGaIn/GaN MISHEMT that contains double field-plate structure through the gate and source electrode extensions. The model was developed for a Metal-Insulator-Semiconductor (MISHEMT) structure, but since the proposed methodology is based on surface-potential determination, the same approach can be used for AlGaIn/GaN HEMTs. The model is based on the presentation of the complete device through the series combination of three independent devices: the intrinsic transistor (without any field-plate structure), the transistor with only gate field-plate structure and the device with only source field-plate structure. The surface-potential was obtained for each of these transistors separately and from these expressions, the intrinsic charges for each transistor, required to find the capacitances are obtained. The obtained model for input, output and reverse capacitance dependence on the applied drain-source voltage are valid in the subthreshold region of operation, and therefore can be used for physics-based modeling of these devices when they are applied as switching devices. However, there is a drawback of the proposed model which makes it inappropriate for implementation into iterative design optimization algorithms. The drawback contains in the numerical solving of the relation between the Fermi level and the applied gate-source voltage. The presented surface-potential methodology proposes an iterative reevaluation of Fermi level using so called Householder's numerical method. Therefore, the complexity level of the proposed methodology is too high from the point of iterative algorithms for device design optimization.

2.3.3. Analysis and modeling of Miller's capacitance

The non-linear dependence of Miller's capacitance on the applied drain-source voltage is of a crucial importance for device performance in high-frequency switching applications. However, up to date, most of the works presented in the literature, are focused on the analysis of this dependence in the case of GaN HEMTs designed for microwave application. Additionally, with the exception of the model from [Ahsan 2016] presented in the previous section, all of these models lack the analytical approach. As it will be shown in this section, some of the works measured $C_{gd}(V_{ds})$ curves using devices with different field-plate

design and therefore, gave some general directions about the influence of the field-plate design on the $C_{gd}(V_{ds})$ dependence. Others, however, provided very good qualitative analysis about the physical origin of Miller's capacitance (in different ranges of applied drain-source voltage) but without any analytical model which would provide the relations between the Millers capacitance and the design parameters of the device.

The work presented in [Wu 2004] was the first reported work, which provided some qualitative explanations of Miller's capacitance origin and presented a simple guideline on the field-plate design in the case of AlGaN/GaN devices for microwave application. In [Okamoto 2004], additionally, a simple model for C_{gd} that includes/excludes the capacitance under the field-plate electrode at lower/higher drain biases was given, using the maximum stable gain (MSG) estimations based on s-parameters measurements. The maximum stable gain measurements showed that although significant reduction in MSG was observed with the increase of the field-plate length at lower drain biases, its dependence becomes negligibly small with increase of the drain bias over the certain value. Based on this conclusion, simplified model that takes into account the field-plate effect on the $C_{gd}(V_{ds})$ at low drain-bias was proposed. In [Saito 2007], gate-drain charge measurements were done together with the measurements of dynamic on-resistance for the devices with single-source and double gate and source field-plate structures. The double field-plate structure showed significant reduction of dynamic on-resistance, comparing to the single field-plate structure, while increasing the amount of total gate-to-drain charge. The preferable structure was analysed in terms of target application of the device (low power- high frequency or vice versa). In [Chiu 2013], the characteristics of HEMTs with various source field-plate and gate-drain dimensions were carried out again only experimentally. Based on these measurements, the influence of design variation on the suppression of dynamic on-resistance, off-state breakdown voltage, RF performance and low-frequency noise were measured and studied. It was found that the field-plate extension significantly improves the off-state breakdown and supresses the current-collapse phenomena, but weakens the frequency response and power added efficiency because of the increase in the "feedback" C_{gd} capacitance.

In [Chu 2011], Miller's capacitance of a GaN HEMT with single- gate and double-source field-plate structure was measured and different parts of this non-linear dependence on the applied drain-source voltage were qualitatively analysed. The depletions of the 2DEG leftovers under each of the field-plate extensions were qualitatively explained and identified as the origins of the nonlinearities in the $C_{gd}(V_{ds})$ dependence. This analysis provided an excellent physics-based insight on the origin of Miller's capacitance under different drain-

source voltages and gave the important directions in physical modelling of this capacitance.

The summary of existing physics-based models in State Of the Art for I-V and C-V characteristics of AlGa_N/Ga_N HEMTs with and without the field-plate is shown in Fig. 2.1.

2.4. Conclusions

Previously presented State Of the Art of different models of AlGa_N/Ga_N devices, showed that these devices, containing (or not) single or multiple field-plate structure, were and still are a highly investigated topic. Many different features of these devices that are not in the focus of our modelling activity (such as dynamic on-resistance, trapping effects and breakdown voltage), have been widely investigated and modelled. Since the goal of our physics-based model is to optimize the device design for high-frequency switching application, the characteristics of interest are I-V and C-V characteristics. **While AlGa_N/Ga_N devices that do not contain the field-plate extension have been completely analytically modelled in terms of I-V and C-V characteristics, the structures with one or multiple field-plate structure were mostly analyzed using numerical simulations (Fig. 2.1).** Since the presence of the field-plate does not alter I-V characteristics significantly, **the I-V models of AlGa_N/Ga_N HEMTs without the field-plate can be used for devices that contain the field-plate extension, without expectation of significant error.** However, **the field-plate design significantly influences the C-V characteristics of the device, and therefore previously obtained models for HEMTs without the field-plate cannot be used.**

Currently, most of the existing analytical models for Ga_N HEMTs that contain the field-plate are focused on the calculation of the surface-potential distribution and the channel electric field, with the aim of field-plate design optimization for a given breakdown voltage [Kaddeche, 2009, Coffie, 2014]. **However, the optimum electric field management is the only considered criterion in this optimization process, while the associated Miller's capacitance that is crucial for high frequency power performance is not taken into account.**

Finally, the model from [Ahsan, 2016] presented an analytical surface-potential based model for input, output and reverse capacitance in a subthreshold regime, in the case of HEMT structure with double gate and source field-plates. The work from [Ahsan,2016] provided the C-V models that are actually the objectives of our work, but with a major drawback contained in the

complex, unified expression for Fermi-level dependence on the gate voltage (taken from [Khandelwal 2012]) which needs to be solved numerically. Since precise Fermi-level calculation is the basis of surface-potential calculation and the whole capacitance model, the numerical re-evaluation of Fermi level gate voltage dependence presents a major drawback of the model, making it significantly more complex and unsuitable for implementation into design optimization algorithms.

Finally, observing the works that were focused on **Miller's capacitance analysis of HEMTs with one or multiple field-plate structure**, we can find many papers that provide good qualitative explanation of the physical origin of this capacitance. **However, the complete analytical model was found to be missing.** Since Miller's capacitance crucially determines the switching losses by determining the duration of the "plateau" time in gate-source signal, **analytical physics-based model of this capacitance is crucial for device optimization for high-frequency switching application.** That was the main motivation for the work presented in this thesis.

Figure 2-1 The summary of SOA physics-based models for AlGaIn/GaN HEMTs with and without the field-plate structure

Chapter3. The existing physics-based model for I-V characteristics of a GaN HEMT with the field-plate structure

3. The existing physics-based model for I-V characteristics of a GaN HEMT with the field-plate structure

3.1. Model for 2DEG density dependence on the gate voltage

The key point in obtaining a reliable physics-based model of a GaN High Electron Mobility Transistor (HEMT) certainly is the dependence of the Two-Dimensional Electron Gas (2DEG) sheet density on the applied gate-to-source voltage. The 2DEG is formed in the triangular quantum well at GaN/AlGaN heterojunction and presents a heart of the device operation. The principle of HEMT operation is based on overlapping of two depletion areas: the one formed at gate/AlGaN Schottky contact and the other formed at AlGaN/GaN heterojunction. This overlapping is necessary in order to prevent any current conduction through AlGaN layer and is obtained by using specific values for the thicknesses of AlGaN and GaN layers. In the following derivation of the 2DEG sheet density dependence on the gate-source voltage, 2DEG (V_{gs}), the trapping charge in AlGaN and GaN layers will be neglected. Additionally, the analyzed device contains the AlGaN layer which is **unintentionally doped**. This leads to the assumption that doping-induced comparing to the polarization induced charge in the 2DEG is negligible. Still, in order to verify this assumption, the 2DEG model will be derived taking into account the doping of the AlGaN layer. When the 2DEG (V_{gs}) model is obtained, the influence of doping will be quantified and therefore, concluded if it can be neglected or not.

The cross-section of the device that will be modelled in this work is shown in Fig. 3.1.

Figure 3-1 Cross-section of the analyzed device showing the geometrical parameters

Table 3-1 Basic characteristics of the analyzed device

V_{ds} [V]	$I_{d,max}$ [A]	Measured V_{th} [V]	Substrate	Package
100V	27	-2	SiC	TO-220

Table 3-2 Geometrical parameters of the device

W_g [mm]	L_g [μm]	L_{sg} [μm]	L_{gd} [μm]	L_{fp} [μm]	t_{ox} [nm]	T_{gate} [nm]	d_{AlGaN} [nm]
120	2	2	4	1.5	80	100	24

Table 3-3 Physical properties of the AlGaIn/GaN heterostructure

m [%]	σ_{PZ} [C/m ²]	ϵ_a [C/(Vm)]	ϵ_g [C/(Vm)]	ΔE_c [V]	μ_{LF} [m ² /Vs]	v_{SAT} [cm/s]	E_c [V/cm]	N_d [1/m ³]
24	0.01	8.3×10^{-11}	8.6×10^{-11}	0.328	1000	2.78	150 $\times 10^3$	10^{22}

Table 3-4 Additional parameters of the device

ϕ_{mi} [V]	ϕ_m [V]	ϵ_{ox} [C/(Vm)]	R_{S_CM} [mΩ]	R_{D_CM} [mΩ]
3	1.152	6.2×10^{-11}	32	32

The Table 3.1 presents the basic characteristics of the device (the voltage rating, the package, the substrate etc), the Table 3.2 gives the values of the geometrical parameters, Table 3.3 shows the physical properties of the AlGaIn/GaN heterojunction while Table 3.4 presents some additional parameters of the device that will be used in the analysis.

The starting point in the analysis of the 2DEG density control by the Schottky gate is the application of the Gauss law for charge conservation at the AlGaIn/GaN heterojunction, considering that device is in the equilibrium (Fig. 3.2). Furthermore, the application of the Poisson's equation for AlGaIn and GaN layer is necessary (observing the energy band-diagram from Fig. 3.3 when V_{gs}

voltage is applied), in order to obtain the values of the electric field at the heterojunction: $E_{a,int}$ for the AlGa_N side and $E_{g,int}$ for the Ga_N side. Finally, the application of Fermi-Dirac's statistics is required in order to establish the relation between the Fermi-level voltage and the two lowest energy sub-band levels in the quantum well. This is particularly important for the precise modelling of the 2DEG density control in the area of gate voltages close to the threshold.

3.1.1. Gauss law for charge conservation at the AlGa_N/Ga_N heterojunction

The energy band-diagrams of an AlGa_N/Ga_N HEMT in equilibrium and in charge control regime when the gate voltage is applied are shown in Fig. 3.2 and 3.3. In equilibrium, the 2DEG density formed in the quantum well comes from the built-in polarization field and doping of the AlGa_N layer, N_d . The polarization-induced sheet density, n_{PZ} , is strongly dependent on the Aluminum mole fraction, m , in the AlGa_N layer. For the analyzed structure with $m=24\%$, n_{PZ} is calculated using the methodology from [Ambacher 1999].

Figure 3-2 Energy band-diagram in the equilibrium.

$$\overset{\rightarrow\rightarrow}{\oint_{S_{Gauss}}} DdS = Q_{free} \quad (3.1)$$
$$\int_{S_{1Gauss}} \vec{D}_1 ds + \int_{S_{2Gauss}} \vec{D}_2 ds = Q_{free} \quad (3.2)$$
$$D_1 = \varepsilon_a E_{a,int} \quad (3.3a)$$

In (3.3 a, b), $E_{a,int}$ and $E_{g,int}$ are the intensities of the electric field vectors. Taking into consideration the directions of the electric displacement vectors (with respect to the vectors of the Gauss surface) and replacing (3.3 a, b) into (3.2), the following equation is obtained:

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Since S_1 is equal to the S_2 , the previous equation can be written as

$$-\varepsilon_a E_{a,int} - \varepsilon_g E_{g,int} = -qn_{pZ} \quad (3.5)$$

3.1.2. Poisson's equation for GaN layer

In order to determine the relation between the value of the electric field at the GaN/AlGaIn interface, $E_{g,int}$, and the 2DEG sheet density, it is necessary to solve the Poisson's equation in GaN layer, observing the energy band-diagram from Fig. 3.3.

The relation between the electric field E_g in GaN layer and the potential v_g is given by

$$E_g = -\frac{dv_g}{dy} \quad (3.6)$$

Since $dv_g(y)/dy > 0$, the electric field in GaN layer is negative with the intensity equal to $E_{g,int}$ at the heterojunction. If the assumed width of the depletion region in GaN layer is equal to w_g (Fig. 3.3) the following boundary conditions for the E_g are obtained:

$$E_g(y = d_{AlGaIn}) = -E_{g,int} \quad (3.7a)$$

$$E_g(y = d_{AlGaIn} + w_g) = 0 \quad (3.7b)$$

The Poisson's equation gives the relation between the derivative of the electric field in GaN layer and the existing charge distribution in this layer. If the density of ionized donors due to unintentional background doping of GaN layer is neglected, the Poisson's equation for this layer becomes:

$$\frac{dE_g}{dy} = \frac{qn_{free,g}}{\varepsilon_g} \quad (3.8)$$

In (3.8), the $n_{free,g}$ is the concentration of free electrons. Integration of (3.8) between the boundaries of the depletion region in GaN layer gives:

$$\int_{d_{AlGaIn}}^{d_{AlGaIn}+w_g} dE_g = \frac{q}{\varepsilon_g} \int_{d_{AlGaIn}}^{d_{AlGaIn}+w_g} n_{free,g} dy \quad (3.9)$$

Using the boundary conditions (3.7 a, b) in (3.9), it is obtained

$$E_{g,int} = \frac{q}{\epsilon_g} n_{2DEG} \quad (3.10)$$

In (3.10), n_{2DEG} is the 2DEG sheet density at the GaN/AlGaN interface.

3.1.3. Poisson's equation for the AlGaN layer

Assuming that AlGaN layer is fully depleted of free electrons, taking into consideration density of doping charge, N_d , the Poisson's equation can be written as

$$\frac{d^2 v_a}{dy^2} = \frac{q N_d}{\epsilon_a} \quad (3.11)$$

where v_a is the potential inside the AlGaN layer. The relation between the electric field E_a and the potential is

$$E_a = -\frac{dv_a}{dy} \quad (3.12)$$

Observing the band diagram in the charge control regime shown in Fig. 3.3, it can be seen that the boundary conditions for v_a are:

$$v_a(0^+) = -V_{gs} + \varphi_m \quad (3.13a)$$

$$v_a(d_{AlGaN}^-) = \Delta E_C - \frac{E_F(V_{gs})}{q} \quad (3.13b)$$

where φ_m is the Schottky barrier height at the gate/AlGaN junction, ΔE_C is the height of the quantum well while E_F is the energy of the Fermi-level calculated with respect to the bottom of the well. It is worth noticing that Fermi level depends on the applied V_{gs} .

The electric field at the AlGaN/GaN heterojunction is equal to

$$E_{a,int} = -\frac{dv_a(y)}{dy} \big|_{y=d_{AlGaN}^-} \quad (3.14)$$

If (3.11) is being integrated from the point $y=y^*$ in the AlGaN layer to the point $y=d_{AlGaN}^-$, the following equation is obtained

$$E_a \big|_{y=y^*} - E_{a,int} = \frac{q N_d}{\epsilon_a} (d_{AlGaN} - y^*) \quad (3.15)$$

When (3.12) is substituted in (3.15), it is obtained:

$$-\frac{dv_a}{dy^*} = E_{a,int} + \frac{qN_d}{\varepsilon_a}(d_{AlGaN} - y^*) \quad (3.16)$$

Integration of (3.16) from $y^*=0^+$ to $y^*=d_{AlGaN}$, gives

$$v_a(0^+) - v_a(d_{AlGaN}) = E_{a,int}d_{AlGaN} + \frac{qN_d d_{AlGaN}^2}{2\varepsilon_a} \quad (3.17)$$

Applying the boundary conditions (3.13 a, b) in (3.17) we obtain the electric field at the AlGaN/GaN heterojunction:

$$E_{a,int} = \frac{-V_{gs} + \varphi_m - \Delta E_C + \frac{E_F(V_{gs})}{q} - \frac{qN_d d_{AlGaN}^2}{2\varepsilon_a}}{d_{AlGaN}} \quad (3.18)$$

Finally, replacing (3.18) and (3.10) into (3.5) we obtain

$$n_{2DEG}(V_{gs}) = n_{PZ} + \frac{\varepsilon_a}{qd_{AlGaN}}(V_{gs} - \varphi_m + \Delta E_C - \frac{E_F(V_{gs})}{q} + \frac{qN_d d_{AlGaN}^2}{2\varepsilon_a}) \quad (3.19)$$

The previous equation can be written in the following form

$$n_{2DEG}(V_{gs}) = \frac{\varepsilon_a}{qd_{AlGaN}}(V_{gs} - V_{th} - \frac{E_F(V_{gs})}{q}) \quad (3.20)$$

where V_{th} presents the effective threshold voltage

$$V_{th} = \varphi_m - \Delta E_C - \frac{qn_{PZ}d_{AlGaN}}{\varepsilon_a} - \frac{qN_d d_{AlGaN}^2}{2\varepsilon_a} \quad (3.21)$$

Using the values from Table 3.1, the equation (3.21) gives $V_{th} = -2.077V$.

In order to see if the doping charge density, N_d , has a significant influence on the threshold voltage, this density was set to 0 and the threshold was recalculated. The obtained value of -2.072V showed **that influence of unintentional doping on the threshold of the device is lower than 1%**. Furthermore, (3.19) provides the possibility to calculate the contribution of the unintentional doping to the 2DEG sheet density and compare it to the polarization charge density, n_{PZ} . Using the values from Table 3.2 and 3.3, the doping contribution n_D is calculated from (3.19):

$$n_D = \frac{N_d d_{AlGaN}}{2} \quad (3.22)$$

Using the values from Table 3.2 and 3.3, the obtained value for n_D is $1.2 \cdot 10^{14} \text{ 1/m}^2$. Comparing to $n_{PZ} = 6.26 \cdot 10^{16} \text{ 1/m}^2$, it is negligible.

Since the influence of unintentional doping on threshold voltage and 2DEG density is negligible, it can be left out from further calculations of I-V

characteristics. Additionally, the input capacitance dependence on the gate-source voltage will not be affected by N_d , since it is dominantly determined by 2DEG(V_{gs}). Therefore, N_d can be neglected in the calculation of $C_{iss}(V_{gs})$. Finally, parasitic capacitances C_{gd} , C_{gs} and C_{ds} in the subthreshold regime, dominantly depend on the amount of undepleted 2DEG below the field-plate and in the source/ drain drift regions. Since this undepleted value is also determined by 2DEG(V_{gs}), it is not expected to have a significant influence of N_d on total gate-drain, gate-source and drain-source charge. Additionally, as it will be shown in Chapter 5, the $C_{gd}(V_{ds})$ has a high gradient around V_{ds} when vertical charge depletion below the field-plate ends. The influence of the doping charge in AlGaIn layer could be manifested through a bit smoother $C_{gd}(V_{ds})$ transition around the vertical depletion boundary. Nevertheless, due to aforementioned high-gradient around this boundary, doping will not have significant influence on the estimation of total gate-to-drain charge (which corresponds to the surface below the $C_{gd}(V_{ds})$ curve). Therefore, it will not affect the efficiency estimation of the converter, as it will be shown in Chapter 4 and 5. It can be concluded that doping charge of unintentionally doped AlGaIn layer can be neglected in further calculations of this model.

3.1.4. Fermi-Dirac's statistics for calculation of sub-band occupation

In order to obtain the complete dependence of the 2DEG sheet density on the applied gate-to source voltage from (3.20), it is necessary to obtain the relation between the Fermi level, E_F , and applied gate-to-source voltage, V_{gs} . In order to obtain that, it is necessary to apply Fermi-Dirac's statistics which relates the occupation of the two lowest energy sub-bands to the position of the Fermi level:

$$n_{2DEG} = Dk_B T \left[\ln \left(1 + e^{\frac{(E_F - E_0)}{k_B T}} \right) + \ln \left(1 + e^{\frac{(E_F - E_1)}{k_B T}} \right) \right] \quad (3.23)$$

where $D = 4\pi m_{le}^* / h^2$ is the density of states for each sub-band, T is the temperature, m_{le}^* is the longitudinal effective mass of electron ($m_{le}^* = 0.22m_e$ with m_e as the electron mass), h is the Planck's constant, k_B is the Boltzmann's constant, E_F , E_0 and E_1 are the Fermi level energy and the energy of the first and the second subband, respectively.

The first and the second energy sub-band, E_0 and E_1 , are related to the sheet density as

$$E_0(eV) = \lambda_0 n_{2DEG}^{2/3} \quad (3.24a)$$

$$E_1(eV) = \lambda_1 n_{2DEG}^{2/3} \quad (3.24b)$$

where λ_0 and λ_1 are experimentally obtained coefficients, given in Table 3.1 [Manju, 2010].

In order to simultaneously solve equations (3.19) and (3.23) and determine n_{2DEG} dependence on V_{gs} , the methodology from [Rashmi 2002] is used. This methodology applies two different approximations of (3.23) for the gate-source voltages below and around the threshold (the first range) and higher than the threshold (the second range).

3.1.4.1. Region for V_{gs} below and around the threshold

When the Fermi level lies at the bottom of the quantum well, the device operates below the threshold and the value for E_F is equal to 0. The 2DEG sheet density that corresponds to this position of the Fermi level can be calculated from:

$$n_{2DEG0} = Dk_B T \left[\ln \left(1 + e^{\frac{-\lambda_0 n_{2DEG0}^{2/3}}{k_B T}} \right) + \ln \left(1 + e^{\frac{-\lambda_1 n_{2DEG0}^{2/3}}{k_B T}} \right) \right] \quad (3.25)$$

Using the corresponding values from Table 3.1, the obtained value for n_{2DEG0} is 3.8×10^{15} .

When the device is in a subthreshold regime, the Fermi level is well below the energy levels E_0 and E_1 . For $E_F \ll E_0, E_1$, $e^{(E_F - E_0)/k_B T} \ll 1$ and $e^{(E_F - E_1)/k_B T} \ll 1$. Therefore, using the approximation $\ln(1 + x) \cong x$ for $-1 < x < 1$, it is obtained:

$$n_{2DEG}^I = Dk_B T [e^{(E_F - E_0)/k_B T} + e^{(E_F - E_1)/k_B T}] \quad (3.26)$$

Near the threshold, the contribution of the level E_1 can be safely ignored. Therefore, as the Fermi level approaches the E_0 , the 2DEG sheet density can be presented as

$$n_{2DEG}^I = Dk_B T e^{\frac{E_0 - E_F}{k_B T}} \quad (3.27)$$

If the sheet density n_{2DEG0} that corresponds to $E_F=0$ is also approximated by the contribution only from the E_0 level

$$n_{2DEG0} = Dk_B T e^{\frac{E_0}{k_B T}}, \quad (3.28)$$

the equation (3.27) can be written as

$$n_{2DEG}^I = n_{2DEG0} e^{\frac{E_F}{k_B T}} \quad (3.29)$$

In order to obtain the 2DEG sheet density in this region of operation, it is necessary to solve the Fermi level dependence on the gate-source voltage. Since the Fermi level in this region of V_{gs} lies only a few tens of $k_B T$ above the bottom of the quantum well, the MacLaurin series of exponential function in (3.29), gives

$$n_{2DEG}^I \cong n_{2DEG0} (1 + \frac{E_F}{k_B T}) \quad (3.30)$$

By equating (3.30) and (3.29), the following equation for $E_F(V_{gs})$ in this region of operation is obtained:

$$E_F^I(V_{gs}) = \frac{q \epsilon_a k_B T (V_{gs} - V_{th} - \frac{q d_{AlGaIn} n_{2DEG0}}{\epsilon_a})}{q^2 d_{AlGaIn} n_{2DEG0} + \epsilon_a k_B T} \quad (3.31)$$

By substituting (3.31) in (3.29), the 2DEG sheet density dependence on V_{gs} in the range of gate-source voltages below and around the V_{th} is obtained:

$$n_{2DEG}^I(V_{gs}) = n_{2DEG0} e^{\left(\frac{q \epsilon_a (V_{gs} - V_{th} - \frac{q d_{AlGaIn} n_{2DEG0}}{\epsilon_a})}{q^2 d_{AlGaIn} n_{2DEG0} + \epsilon_a k_B T} \right)} \quad (3.32)$$

The equation (3.32) is valid in the range $V_{gs} \leq V_{gs1}$, where V_{gs1} is equal to:

$$V_{gs1} = V_{th} + \frac{k_B T n_{2DEG0} (\epsilon_a + 2D q^2 d_{AlGaIn})}{q \epsilon_a (2D k_B T - n_{2DEG0})} \quad (3.33)$$

For analyzed transistor, V_{gs1} obtained from (3.33) is equal to -1.88V.

3.1.4.2. Region for V_{gs} higher than the threshold

In the operating region above the threshold, the Fermi level is several $k_B T$ above the bottom of the quantum well, leading to the large values of n_{2DEG} . Using the approximation $E_F \gg E_0, E_1$ in (3.25), the sheet density in this region of V_{gs} can be presented as:

$$n_{2DEG}^{II} = D k_B T \left(\frac{E_F - E_0}{k_B T} + \frac{E_F - E_1}{k_B T} \right) \quad (3.34)$$

Therefore, the Fermi level in this region is equal to:

$$E_F = \frac{n_{2DEG}^I + E_0 + E_1}{2D} \quad (3.35)$$

Using (3.24a, b) and approximation that $\sqrt[3]{n_{2DEG}^I{}^2} \ll n_{2DEG}^I$ for large values of n_{2DEG} , equation (3.35) becomes

$$E_F \cong \frac{n_{2DEG}^I}{2D} \quad (3.36)$$

Substituting (3.34) in (3.20), the 2DEG density in this region is obtained

$$n_{2DEG}^I = \frac{2\varepsilon_a q D}{(\varepsilon_a + 2q^2 D d_{AlGaN})} (V_{gs} - V_{th}) \quad (3.37)$$

The equations (3.32) and (3.37) provide the analytical model for 2DEG density dependence on the applied gate-source voltage shown in Fig. 3.4.

Figure 3-4 2DEG sheet density dependence on the applied V_{gs}

Comparing to the COMSOL simulation, the obtained analytical dependence shows good agreement.

3.2. The model for the output I-V characteristics

The obtained 2DEG sheet density dependence on the applied gate-to-source voltage is necessary for obtaining the model for the output characteristics of a HEMT, $I_d(V_{ds}, V_{gs})$. The drain current in the channel can be modelled by the following equation [Manju 2010]:

$$I_d = q W_g v_{DRIFT}(|E_x|) n_{2DEG}(V_{gs}, V_c(x)) \quad (3.38)$$

In the previous equation, the $|E_x|$ is the intensity of the lateral electric field in the channel, $V_c(x)$ is the voltage drop in the channel calculated with respect to the source-end under the gate and $v_{DRIFT}(|E_x|)$ is the electron drift velocity in the channel (Fig. 3.5). It is worth noticing that due to the presence of the voltage drop $V_c(x)$, the 2DEG sheet density in the channel depends on the position in the channel (Fig. 3.6).

Figure 3-5 Cross-section of the device showing drift and contact resistances.

The drift velocity of electrons is defined as

$$v_{DRIFT}(|E_x|) = \mu(|E_x|)|E_x| \quad \text{for } |E_x| \leq E_c \quad (3.39a)$$

$$v_{DRIFT} = v_{SAT} \quad \text{for } |E_x| > E_c \quad (3.39b)$$

where $\mu(|E_x|)$ presents the field-dependent mobility of electrons while E_c is the critical value of the lateral electric field for which the device enters the saturation region of operation. Similarly, v_{SAT} presents the drift velocity of electrons in the saturation regime.

3.2.1. The linear region of operation

The model that is used for the field-dependent mobility in the linear region of operation, $\mu(|E_x|)$, is given by the following equation:

$$\mu(|E_x|) = \frac{\mu_{LF}}{1 + \frac{|E_x|}{E_C}} \quad (3.40)$$

where μ_{LF} is the low field mobility of the 2DEG. The corresponding values for μ_{LF} , E_C and v_{SAT} are given in Table 3.3, while the relation between the potential $V_c(x)$ in the channel and the intensity of the lateral electric field, $|E_x|$ is

$$|E_x| = \frac{dV_c(x)}{dx} \quad (3.41)$$

Figure 3-6 COMSOL Simulation of the 2DEG distribution along the channel, when different V_{ds} is applied.

As it was previously mentioned, the 2DEG sheet density in the channel when the device is conducting current will depend on the position in the channel. Since the output characteristics are defined for gate-to-source voltages well above the threshold value, the linear approximation of the 2DEG dependence on V_{gs} will be used.

If the voltage drop $V_c(x)$ is included in the equation (3.37), it is obtained

$$n_{2DEG}(V_{gsi}, V_c) = \frac{2\varepsilon_a q D}{(\varepsilon_a + 2q^2 D d_{AlGaIn})} (V_{gsi} - V_{th} - V_c(x)) \quad (3.42)$$

or

$$n_{2DEG}(V_{gsi}, V_c) = A_1 (V_{gsi} - V_{th} - V_c(x)) \quad (3.43)$$

where

$$A_1 = \frac{2\varepsilon_a q D}{(\varepsilon_a + 2q^2 D d_{AlGaIn})} \quad (3.44)$$

In (3.43), the V_{gsi} presents the intrinsic gate-source voltage which is defined as the voltage between the gate electrode and the source-end under the gate (Fig. 3.5). The intrinsic model for the output characteristics of a HEMT will be derived for the part of the device which does not include drift, contact and metallization resistances.

3.2.1.1. Intrinsic model

By replacing (3.39a), (3.40), (3.41) and (3.43) into (3.38), it is obtained:

$$I_d = qW_g \frac{\mu_{LF}}{1 + \frac{1}{E_c} \frac{dV_c(x)}{dx}} \frac{dV_c(x)}{dx} A_1 (V_{gsi} - V_{th} - V_c(x)) \quad (3.45)$$

Integrating equation (3.45) from $x=0$ which corresponds to $V_c=0$, to $x=L_g$ which corresponds to $V_c=V_{dsi}$, it is obtained:

$$I_d = \frac{qW_g \mu_{LF} A_1}{\left(L_g + \frac{1}{E_c} V_{dsi}\right)} \left((V_{gsi} - V_{th}) V_{dsi} - \frac{V_{dsi}^2}{2} \right) \quad (3.46)$$

where V_{dsi} presents the intrinsic drain-source voltage (from drain-end under the gate to the source-end under the gate). Equation (3.46) presents the intrinsic model of the drain current in the linear region of operation.

3.2.1.2. Extrinsic model

In order to obtain an extrinsic model that takes into account source and drain drift resistances, R_{S_DRIFT} and R_{D_DRIFT} , as well as source and drain contact and metalization resistances, R_{S_CM} and R_{D_CM} , the intrinsic gate-source and drain-source voltages will be presented in the following way:

$$V_{dsi} = V_{dse} - R_{SDRIFT}I_d - R_{SCM}I_d - R_{DDRIFT}I_d - R_{DCM}I_d \quad (3.47a)$$

$$V_{gsi} = V_{gse} - R_{SDRIFT}I_d - R_{SCM}I_d \quad (3.47b)$$

By presenting the total source and drain resistances as:

$$R_{STOT} = R_{SDRIFT} + R_{SCM} \quad (3.48a)$$

$$R_{DTOT} = R_{DDRIFT} + R_{DCM} \quad (3.48b)$$

the equations (3.47a, b) can be presented as

$$V_{dsi} = V_{dse} - R_{STOT}I_d - R_{DTOT}I_d \quad (3.49a)$$

$$V_{gsi} = V_{gse} - R_{STOT}I_d \quad (3.49b)$$

The values for drain and source resistances due to contacts and metalization process, R_{S_CM} and R_{D_CM} , are provided by the manufacturer and given in Table 3.4, while the source and drain drift resistances, R_{S_DRIFT} and R_{D_DRIFT} , will be modelled in the following section.

The substitution of (3.49 a, b) into (3.46) gives:

$$I_d^2 C_1 + I_d C_2 + C_3 = 0 \quad (3.50)$$

where

$$C_1 = \left(\frac{R_{D,TOT} + R_{S,TOT}}{E_C} + qW_g\mu_{LF}\frac{A_1}{2}(R_{STOT}^2 - R_{DTOT}^2) \right) \quad (3.51a)$$

$$C_2 = \left(A_1 V_{th} (R_{D,TOT} + R_{S,TOT}) q W_g \mu_{LF} + A_1 q W_g \mu_{LF} (R_{D,TOT} + R_{S,TOT}) V_{dse} - \right. \\ \left. A_1 q W_g \mu_{LF} R_{STOT} V_{dse} - A_1 q W_g \mu_{LF} (R_{D,TOT} + R_{S,TOT}) V_{gse} - \left(L_g + \frac{V_{dse}}{E_C} \right) \right) \quad (3.51b)$$

$$C_3 = \frac{A_1 q W_g \mu_{LF}}{2} (2 V_{gse} V_{dse} - 2 V_{th} V_{dse} - V_{dse}^2) \quad (3.51c)$$

Solving (3.50) and using (3.51a, b, c) gives the extrinsic model for the drain current in the linear region of operation:

$$I_d = \frac{-C_2 - \sqrt{C_2^2 - 4 C_1 C_3}}{2 C_1} \quad (3.52)$$

3.2.2. The saturation region

3.2.2.1. Intrinsic model

Since the saturation region is not the region of interest in a switching application, it will be modelled in a simple way by considering the saturation current constant for V_{ds} higher than the saturation voltage, V_{dsi}^{sat} . Using (3.39b) in (3.38), it is obtained:

$$I_{dsat} = q W_g v_{SAT} n_{2DEG} (V_{gsi}, V_{dsi}^{sat}) \quad (3.53)$$

or

$$I_{dsat} = q W_g v_{SAT} A_1 (V_{gsi} - V_{th} - V_{dsi}^{sat}) \quad (3.54)$$

3.2.2.2. Extrinsic model

In order to obtain the extrinsic model that can be compared to the experimental characteristics of the device, the equations (3.49a, b) are replaced into (3.54):

$$I_{dsat} = q W_g v_{SAT} A_1 (V_{gse} - V_{th} - V_{dse}^{sat} + R_{DTOT} I_{dsat}) \quad (3.55)$$

Solving (3.55) gives the extrinsic model for the drain current in the saturation region:

$$I_{dsat} = \frac{qW_g v_{SAT} A_1 (V_{gse} - V_{th} - V_{dse}^{sat})}{(1 - qW_g v_{SAT} A_1 R_{TOT})} \quad (3.56)$$

Since the drain current needs to be continuous at V_{dse}^{sat} , substituting $V_{dse} = V_{dse}^{sat}$ into (3.52) and equalizing (3.52) and (3.56), gives the values for V_{dse}^{sat} voltages.

3.2.3. Drift resistance model

In order to complete previously obtained extrinsic model for the drain current in a linear and saturation region of operation, it is necessary to model source and drain drift resistances, R_{S_DRIFT} and R_{D_DRIFT} . The first step towards this is the COMSOL simulation of the electric potential along the channel, when the device is conducting current (Fig. 3.7).

From the curves shown in Fig. 3.7, it can be seen that for lower drain-to-source voltages (up to 8V), the electric potential can be treated as the linear function of the position along the channel. Since the drain current is continuous and equal in every point between the source and drain electrodes, the resistances in source and drain drift areas can be modeled as constant resistances. For higher V_{ds} (when the device operates in saturation region), the slope of the potential in the area below the field plate starts to deviate from the linear. However, since the saturation region is not the region of interest, R_{S_DRIFT} and R_{D_DRIFT} will be modeled as constants. In this way, the model will be significantly simplified, yet accurate enough in the operating region of interest.

The drift resistances can be modelled as sheet resistances, using the following equations:

$$R_{D_DRIFT} = \frac{L_{gd}}{q\mu_L F W_g n_{S0}} \quad (3.57a)$$

$$R_{S_DRIFT} = \frac{L_{gs}}{q\mu_L F W_g n_{S0}} \quad (3.57b)$$

The value of the 2DEG sheet density in the source and drain drift areas, n_{S0} , will be treated as constant value (independent on the applied drain-source and gate-source voltages). Observing the simulation results from Fig. 3.6, it can be seen that this approximation is completely valid in the areas between the drain contact and the field-plate edge as well as in the region between the source

contact and source-end under gate. The only region where the 2DEG density changes with the change in V_{gse} and V_{dse} is below the field-plate extension of the gate electrode. The simulations in Fig. 3.6 for different gate-source voltages, showed that this density varies from -12% for $V_{gse}=-2V$ to +22% for $V_{gse}=1V$, with respect to the nominal value of $4.5 \cdot 10^{16} \text{ 1/m}^2$. In order to simplify the model for R_{D_DRIFT} and R_{S_DRIFT} , these variations will be neglected.

Due to the aforementioned simplifications, n_{s0} can be obtained using the methodology from Section 4.2.1 that will model vertical depletion of the 2DEG under the field-plate. This depletion process will be modelled for the conditions that keep the device below the threshold ($V_{gse}=-3V$), while V_{dse} is being changed from zero to the breakdown value. Since n_{s0} is treated as the uniform 2DEG in the drain and source drift regions, it can be equalized to the 2DEG density below the field-plate, before process of vertical depletion starts. Therefore, n_{s0} corresponds to the value obtained from Fig. 4.5 for drain-source voltage equal to zero. Observing the curve from Fig. 4.5, the value of $n_{s0}= 4.4 \cdot 10^{16} \text{ 1/m}^2$ is obtained. The analytical model for vertical depletion process will be derived and analyzed in detail in Section 4.2.1.

Comparing the obtained analytical value for n_{s0} to the COMSOL simulation result which predicts the value of $4.5 \cdot 10^{16} \text{ 1/m}^2$, the deviation of only 2.3% is observed. Finally, by substituting the modelled value for n_{s0} into (3.57a, b) and using the values of the corresponding parameters from the Table 3.2 and 3.3, the values of 47.4 and 23.7 m Ω for R_{D_DRIFT} and R_{S_DRIFT} are obtained.

Figure 3-7 Simulation of the electric potential along the channel.

3.3. Experimental verification of the model for I-V output characteristics

3.3.1. Verification of the threshold voltage of the device

The threshold voltage of the device can be directly measured by measuring the input capacitance dependence on the applied gate-to-source voltage, since this capacitance will have a high increase when the device reaches the threshold. From previously obtained $n_{2DEG}(V_{gs})$ dependence, the input capacitance can be modelled in the following way:

$$C_{ISS}(V_{gs}) = qW_gL_g \frac{dn_{2DEG}(V_{gs})}{dV_{gs}} + C_{ISS,sub} \quad (3.58)$$

where $C_{ISS,sub}$ is the value of the input capacitance in the subthreshold region for $V_{ds} = 0V$. This value is equal to 490pF and will be modelled and calculated in the next chapter.

Comparison of the model for $C_{ISS}(V_{gs})$ given by (3.58) and the measurement is shown in Fig. 3.8. It can be seen that non-linear dependence of the 2DEG sheet density on the applied V_{gs} has been modelled precisely, giving the correct value for the effective threshold of the device (-2V).

3.3.2. Verification of the output I-V characteristics

Since the complete extrinsic model for the drain current in the linear and saturation region has been developed, it can be compared to the experimentally obtained output characteristics of the device. The output characteristics were measured for V_{gse} from -1.5 to 0.5V, using the step of 0.5V. The comparison between the measured curves and the complete extrinsic model is shown in Fig. 3.9, while Fig. 3.10 enlarges the comparison in the linear region of operation.

Figure 3-8 Input capacitance dependence on V_{gs} –model versus measurements.

Figure 3-9 Extrinsic model for the output characteristics versus measurements.

Figure 3-10 *Extrinsic model versus measurements in the linear region of operation*

Observing these two figures, it can be seen that very good agreement between measured and predicted values exists in a linear part of the output characteristics, while the deviation increases with the increase in drain-to-source voltage in the saturation region. This was expected, since very simple model for the saturation current was applied, in order to simplify the complete model in the region which is not the one of interest. This region could be improved by implementing the model for channel length modulation from [Ahn 1994], which would make it significantly more complex.

The dependence of the on-resistance on the extrinsic gate-source voltage for two different values of the drain current was measured and presented in Fig. 3.11. Comparing to the analytical model, very good agreement was obtained in the higher range of V_{gse} where the device operates in the linear region of operation while the deviation increases in the lower range of gate-source voltages. This was expected since the device approaches the saturation region as the V_{gse} decreases for the constant drain current which was not modelled precisely, since this is not the operating region of interest. Furthermore, the power loss of a high-frequency buck converter (presented in Chapter 5) will use

the average value of the R_{on} obtained from the modelled curves shown in Fig. 3.10.

Figure 3-11 Model versus measurements for the on-resistance dependence on V_{gse} .

Finally, the transfer characteristic of the device was measured and modelled, for extrinsic drain-source voltage equal to 5V (Fig.3.12). It can be seen that the highest deviation between the model and the measurement is around 33%. However, this deviation will not influence the estimation of the power losses in a high-frequency buck converter, as it will be shown in the Chapter 5.

3.4. Summary and conclusions

The starting point of the model for the output characteristics was determination of the 2DEG sheet density dependence on the applied gate-source voltage, when drain-source voltage is equal to zero. This dependence was obtained by applying Poisson's equation for AlGa_N and GaN layers, together with the Gauss law for charge conservation at the AlGa_N/GaN heterojunction and Fermi-Dirac's statistics for the relation between the Fermi-level and the first two sub-

bands in the quantum well [Manju 2010]. The analytical model showed good agreement with the Comsol simulation results.

Figure 3-12 Model versus measurements for the transfer characteristic of the device.

Furthermore, this 2DEG model was used for obtaining the intrinsic and extrinsic models of the output characteristics of the device. In order to complete the extrinsic model, it was necessary to calculate the drift resistances in the gate-source and gate-drain drift areas. These resistances were calculated as sheet resistances, using the value for the 2DEG sheet density obtained from the model for vertical depletion. The vertical depletion model will be presented and analyzed in more detail in Section 4.2.1.

Finally, the obtained curves for extrinsic model showed very good agreement with the experimental characterization of the device, especially in the linear region of operation. Therefore, on-resistance which is crucial for determination of the conduction losses in the converter has been precisely modelled.

Additionally, the extrinsic model for the transfer characteristic of the device showed good agreement with the measurements, providing the forward transconductance dependence on the applied gate-source voltage. Furthermore,

modelled value for the threshold voltage was confirmed by the measurement of the input capacitance dependence on V_{gs} . Therefore, all of the necessary parameters for the power loss analysis were modelled and experimentally verified.

Chapter4. The proposed physics-based model for input, output and reverse capacitance of the device in the subthreshold regime

4. The proposed physics-based model for input, output and reverse capacitance of the device in the subthreshold regime

4.1. Introduction

The input, output and reverse (Miller's) capacitance of a switching device determine the switching power losses and limit the switching speed. Therefore, the key point of a device design optimization for high-frequency application is obtaining the physics-based model for these capacitances and their non-linear dependence on the applied drain-to-source voltage. The proposed modelling methodology is based on the analysis of gate-source, drain-source and gate-drain (Miller's) capacitance separately. The cross-section of the device that will be modelled is shown in Fig. 4.1 while the corresponding geometrical and physical parameters are given in Table 3.1, 3.2, 3.3 and 3.4.

Figure 4-1 Cross-section of the AlGaIn/GaN HEMT with the gate field-plate structure

The first capacitance that will be modelled is the Miller's capacitance, C_{gd} , which determines the duration of the plateau time in gate-to-source driving signal and therefore directly influences the switching losses. As it was shown in Chapter 2 analyzing the State Of the Art in physics-based models of GaN

HEMTs, the Miller's capacitance of a GaN HEMT without the field-plate structure already has been analyzed and modelled. Since the type and geometry of a field-plate highly influence the non-linearity of this capacitance, the proposed capacitance models cannot be used in the case of structure from Fig. 4.1.

In principle, the Miller's capacitance modelling demands solving of 2D Poisson's equation for the potential inside the depleted region in AlGaIn layer (Fig. 4.1). In order to avoid Finite Element Analysis Tools and obtain a simplified analytical model that can be used in design optimization algorithms, the proposed methodology is based on the approximation of the charge depletion in two separated directions: perpendicularly (vertically) and laterally with respect to the channel. The vertical depletion takes place in the part of the channel which is directly below the field-plate while the lateral extensions of the depleted area separately exist around the drain-side gate edge and the field-plate edge in the channel. The portions of the capacitance that correspond to each depletion process need to be analytically modelled and calculated. The complete model for $C_{gd}(V_{ds})$ will be obtained by summing these portions in the corresponding intervals of V_{ds} where these charge depletions exist.

On the other hand, the origin of gate-source and drain-source capacitance will be found in the fringing between the corresponding electrodes and their extensions through the undepleted 2DEG in the channel. As it will be shown, these capacitances are very little or not at all dependent on the applied V_{ds} .

4.2. The model for the Miller's capacitance in the subthreshold regime

In order to make the first step in identifying the aforementioned charge depletions that need to be analytically modelled, the 2DEG distribution in the channel when the device is turned-off was simulated (Fig. 4.2 and 4.3). The different 2DEG densities correspond to the conditions when gate-source voltage is kept below the threshold (at the value of -3V) while drain-source voltage is being varied from 0 to 60V. Simulation results show that significant amount of the 2DEG leftover directly under the field plate is being depleted as V_{ds} increases up to approximately 14V. On the other hand, Fig. 4.3 shows that for V_{ds} with higher values, only small lateral extension of the depletion area around the field-

plate edge exists. This suggested that two directions of the charge density variation could be distinguished:

1. y-direction which is referred to the variation in the 2DEG density in one fixed point along the channel
2. x-direction which is referred to the extension of the depletion area laterally (Fig. 4.2 and 4.3).

Figure 4-2 Simulation of 2DEG depletion process under the field-plate for V_{ds} up to 20V.

From the simulation results presented in Fig. 4.2 and 4.3, two ranges of V_{ds} can be distinguished: the Range I which covers the values up to approximately 14V where both vertical and lateral depletion of the 2DEG exist and the Range II for V_{ds} higher than 14V where only lateral extension of the depletion area exists.

The modelling of vertical depletion is based on the methodology used for obtaining the 2DEG density dependence on the applied V_{gs} (Chapter 3), taking V_{gd} for the voltage that controls the depletion process. The structure that is analysed is Metal Insulator-Semiconductor HEMT (MISHEMT) and the analytical model is obtained by applying Poisson's equations for AlGaN and GaN layers, together with the Gauss law for charge conservation at the oxide/AlGaN and AlGaN/GaN heterojunctions.

Figure 4-3 Simulation of 2DEG depletion process under the field-plate for V_{ds} up to 60V

On the other hand, the lateral extensions of the depletion area around the drain-side gate edge and the field plate edge are modelled separately, applying conformal mapping technique from [Si 2013]. Since the approach from [Si 2013] was developed for AlGaIn/GaN HEMT without the field-plate structure, it was necessary to make the modifications of this methodology, using the approximations that will be clearly elaborated in the following section.

4.2.1. The analytical model for the vertical depletion under the field plate

In order to obtain the analytical model for 2DEG depletion process in y-direction, the following methodology is proposed. Since V_{gs} is kept constant at the value just below the threshold while V_{ds} is being varied, the depletion process can be analyzed as if the 2DEG under the field plate is being controlled by drain-to-gate voltage, V_{dg} . The V_{gs} voltage that keeps the device in the off state is marked as V_{gs}^* and is equal to -3V in this analysis.

The following analysis is based on the energy band-diagram of the MISHEMT structure shown in Fig. 4.4. The reference point for the $v_a(y)$ potential is set to the bottom of the quantum well ($v_a(w_a^+) = 0$) as well as the position of the Fermi level voltage, E_F , for the complete range of V_{dg} . In this way, the analysis is

significantly simplified by avoiding the Fermi-Dirac's statistics shown in Chapter 3. This simplification is justified since the values of the applied V_{dg} are significantly higher than $E_F(V_{gd})$ [Khandelwal 2011].

Figure 4-4 Energy band-diagram of the MISHEMT structure.

The AlGaIn layer of the analyzed device is unintentionally doped which implies that doping density of charge in this layer can be neglected. Accordingly, the Poisson's equation for the AlGaIn layer becomes the Laplace equation:

$$\frac{d^2 v_a}{dy^2} = 0 \quad (4.1)$$

The boundary conditions for the potential $v_a(y)$ are $v_a(0^+) = V_{dg} + \phi_{mi}$ and $v_a(w_a^-) = \Delta E_c$. The electric field value at the AlGaIn/GaN heterojunction is equal to

$$E_{a,int} = -\frac{dv_a(y)}{dy} \Big|_{y=w_a^-} \quad (4.2)$$

where $w_a = t_{ox} + d_{AlGaIn}$. If (4.1) is being integrated from the point $y=y^*$ in the AlGaIn layer to the point $y=w_a^-$ together with (4.2) it gives

$$E_{a,int} = -\frac{dv_a(y)}{dy} |_{y=y^*} \quad (4.3)$$

The equation (4.3) shows that vertical component of the electric field inside the AlGaIn layer is constant which was expected due to negligence of the doping charge. Integration of (4.3) from $y=t_{ox}^+$ to $y=w_a^-$ gives

$$v_a(t_{ox}^+) - v_a(w_a^-) = E_{a,int}(w_a - t_{ox}) \quad (4.4)$$

Substituting the boundary condition for $v_a(w_a^-)$ in (4.4) the electric field $E_{a,int}$ is obtained:

$$E_{a,int} = \frac{v_a(t_{ox}^+) - \Delta E_C}{(w_a - t_{ox})} \quad (4.5)$$

From the band-diagram shown in Fig. 4.4, $v_a(t_{ox}^+)$ can be determined as

$$v_a(t_{ox}^+) = V_{dg} + \phi_{mi} - E_{ox}t_{ox} \quad (4.6)$$

where E_{ox} is the value of the homogeneous electric field inside the Si_3N_4 . This field is also homogeneous since the dielectric charge has been neglected.

In order to obtain the value of E_{ox} , the Gauss law is applied to the surface at the $\text{Si}_3\text{N}_4/\text{AlGaIn}$ heterojunction (Fig. 4.4). In order to simplify the analysis, the following assumptions were made. The polarization field in AlGaIn layer was neglected, since it is strongly reduced by the field that originates from the positive surface states and negative 2DEG. Furthermore, the density of the surface-states positive charge will be treated as approximately equal to the density of surface polarization negative charge. Since the dielectric charge is neglected as well, the E_{ox} is obtained as

$$E_{ox} = \frac{E_{a,int}\epsilon_a}{\epsilon_{ox}} \quad (4.7)$$

Combining (4.5), (4.6) and (4.7), the vertical component of the electric field inside the AlGaIn layer is being obtained:

$$E_{a,int} = \frac{V_{dg} + \phi_{mi} - \Delta E_C}{(w_a - t_{ox})(1 + \frac{\epsilon_a t_{ox}}{\epsilon_{ox}(w_a - t_{ox})})} \quad (4.8)$$

In order to obtain the dependence of the 2DEG sheet density under the field plate on the applied V_{dg} , it is necessary to solve the Poisson's equation for GaN layer:

$$\frac{dE_g}{dy} = \frac{qn_{free,g}}{\epsilon_g} \quad (4.9)$$

where $n_{free,g}(y)$ and E_g are the concentration of free electrons and the electric field in GaN layer, respectively. Assuming that depletion area width in GaN layer is w_g , extending from the $y=w_a^+$ at the interface to the $y=w_a+w_g$, the electric field E_g satisfies the following boundary conditions:

$$E_g(y = w_a^+) = -E_{g,int} \quad (4.10a)$$

$$E_g(y = w_a + w_g) = 0 \quad (4.10b)$$

Applying these boundary conditions and integrating (4.9) between the boundaries of the depletion region in GaN layer, the electric field at GaN/ AlGaN heterointerface is obtained

$$E_{g,int} = \frac{q}{\epsilon_g} n_{2DEG,FP} \quad (4.11)$$

where $n_{2DEG,FP}$ is the density of the 2DEG under the field plate.

Finally, in order to complete the obtaining of $n_{2DEG,FP}(V_{dg})$, it is necessary to apply the Gauss law for charge conservation at the AlGaIn/GaN heterojunction. Observing the Gauss surface S_{2Gauss} , it is obtained:

$$\oint_{S_{Gauss}} \vec{D} d\vec{S} = Q_{free} \quad (4.12)$$

or

$$\int_{S_{1Gauss}} \vec{D}_1 d\vec{S} + \int_{S_{2Gauss}} \vec{D}_2 d\vec{S} = Q_{free} \quad (4.13)$$

where Q_{free} is the free charge enclosed by the Gauss surface while D_1 and D_2 are the vectors of the electric displacement at the AlGaIn/ GaN, respectively (Fig. 4.4). The intensities of these vectors are:

$$D_1 = \epsilon_a E_{a,int} \quad (4.14a)$$

$$D_2 = \epsilon_g E_{g,int} \quad (4.14b)$$

where, $E_{a,int}$ and $E_{g,int}$ are the intensities of the electric field vectors. Assuming that heterojunction is in the equilibrium, providing the 2DEG sheet density equal to the polarization charge density and replacing (4.14a, b) into (4.13), the following equation is obtained:

$$-\varepsilon_a E_{a,int} S - \varepsilon_g E_{g,int} S = -q n_{PZ} S \quad (4.15)$$

or

$$-\varepsilon_a E_{a,int} + q n_{PZ} = \varepsilon_g E_{g,int} \quad (4.16)$$

In (4.15) and (4.16), n_{PZ} is the sheet density of the 2DEG in equilibrium, equal to the polarization charge sheet density, σ_{PZ}/q .

Finally, by replacing (4.8) and (4.11) into (4.16), the expression for the vertical depletion of the 2DEG under the field plate is obtained

$$n_{2DEG,FP}(V_{dg}) = n_{PZ} - \frac{\varepsilon_a(V_{dg} + \varphi_{mi} - \Delta E_C)}{q(d_{AlGaIn} + \frac{\varepsilon_a}{\varepsilon_{ox}} t_{ox})} \quad (4.17)$$

Replacing $V_{gd} = V_{gs}^* - V_{ds}$ in (4.17), the $n_{2DEG,FP}(V_{ds})$ dependence is obtained and shown in Fig. 4.5. The analytical expression for drain-source voltage which determines the completion of vertical depletion and the end of Range I, V_{ds}^I , is equal to:

$$V_{ds}^I = V_{gs}^* - \varphi_{mi} + \Delta E_C + \frac{\sigma_{PZ}(d_{AlGaIn} + \frac{\varepsilon_a}{\varepsilon_{ox}} t_{ox})}{\varepsilon_a} \quad (4.18)$$

By substitution of the corresponding values, equation (4.18) gives V_{ds}^I equal to 11V (Fig. 4.5) while the value obtained with the Comsol simulation was 14V. Furthermore, the obtained analytical value of the 2DEG density for $V_{ds} = 0V$, n_{s0} , is equal to $4.35 \times 10^{16} \text{ m}^{-2}$ which is 20% lower than the value obtained by the Comsol simulation. Overall, these deviations are not high enough to significantly influence the calculation of the C_{gd} portion due to vertical depletion.

Since the vertical depletion of the 2DEG under the field plate has been analytically modelled, the part of C_{gd} caused by it can be calculated. The corresponding part will be marked as $C_{gd,y}^I$ and can be calculated as:

$$C_{gd,y}^I(V_{ds}) = q L_{fp} W_g \frac{dn_{2DEG,FP}}{dV_{ds}} \quad (4.19)$$

Substitution of (4.17) into (4.19) gives

$$C_{gd,y}^I(V_{ds}) = L_{fp} W_g \frac{\varepsilon_a}{(d_{AlGaIn} + \frac{\varepsilon_a}{\varepsilon_{ox}} t_{ox})} \quad (4.20)$$

For the analyzed structure with parameters from Table 3.2, 3.3 and 3.4, the obtained value for $C_{gd,y}^I$ is 113.9pF.

Figure 4-5 2DEG vertical depletion under the field plate

4.2.2. Model for the lateral extension using conformal mapping technique

In order to complete the analytical model for $C_{gd}(V_{ds})$, it is necessary to model the dependence of the lateral extension of the depletion area in the channel on the applied drain-source voltage.

As it was shown in Fig. 4.2 and 4.3, for $V_{ds} \leq 11V$ the lateral extension of the depletion area exists only around the drain-side gate-edge while the area around the field-plate edge remains unchanged. On the other hand, for $V_{ds} > 11V$, the gate side depletion region does not extend and the main source of C_{gd} is found in the lateral extension of the channel depletion area around the field-plate edge.

This behavior can also be observed through the Comsol simulation of the lateral component of the electric field in the channel (Fig. 4.6). Analyzing the different field distributions, it can be seen that for V_{ds} between 10 and 20V, the peak of the electric field around the drain-side gate edge saturates, causing the increase in

the electric field distribution around the field-plate edge. Therefore, these lateral extensions will be marked as $b^I(V_{ds})$ and $b^{II}(V_{ds})$ since they correspond to the Range I and II of drain-source voltage. The portions of Miller's capacitance caused by these depletion extensions, $C_{gd,x}^I$ and $C_{gd,x}^{II}$, can be calculated as:

$$C_{gd,x}^{I/II} = qW_g n_{s0} \frac{\partial b^{I/II}(V_{ds})}{\partial V_{ds}} \quad (4.21)$$

where n_{s0} is previously obtained analytical value for the 2DEG sheet density for $V_{ds}=0$. The $b^I(V_{ds})$ and $b^{II}(V_{ds})$, can be obtained separately, using the method proposed in [Si 2013].

Figure 4-6 Simulation of the lateral electric field along the channel

The methodology from [Si 2013] was developed for AlGaIn/GaN HEMT without the field plate structure where only one peak of the electric field exists and the corresponding extension around the drain-side gate edge. In the case of HEMT that contains the field-plate which is long enough to have two separate peaks of the electric field (like in the Fig. 4.6), this methodology can be applied for the calculation of each extension separately. Still, it is necessary to apply some modifications, which will be discussed in detail in this section.

The mathematical model for determination of $b^I(V_{ds})$ is shown in Fig. 4.7. It is important to highlight that this calculation neglected the influence of the field-plate extension of the gate electrode (as it can be seen from the model presented in Fig. 4.7). This simplification can be justified by the fact that in this range of V_{ds} , the influence of the field-plate is dominantly seen through the vertical depletion of the 2DEG that was previously modelled and taken into account.

Therefore, the lateral extension of the depletion area can be decoupled from the vertical depletion process.

In order to obtain $b^l(V_{ds})$ it is necessary to solve 2D Poisson's equation for potential inside the depletion region in AlGaIn layer (Fig. 4.7).

$$\nabla^2 v_a = 0 \quad (4.22)$$

Figure 4-7 Applied physical model for extension of the depletion area around the drain-side gate edge.

It can be observed that (4.22) is a Laplace equation, which was expected since AlGaIn layer is not doped.

In order to solve (4.22), the following boundary conditions are used. The assumption that positive polarization charge density at the AlGaIn/GaN interface is equal to the 2DEG density in the undepleted region, n_{s0} , gives the first boundary condition for $y=d_{AlGaIn}$:

$$\frac{dv_a}{dy}(y = d_{AlGaIn}) = -\frac{qn_{s0}}{\epsilon_g} \quad (4.23)$$

The second boundary condition for $y=0$ and $x < b^l$ follows from the assumption about the equality of the positive surface states density and the negative polarization charge density. Therefore, the net charge concentration is zero at the surface of AlGaIn layer and application of Gauss law gives the following:

$$\frac{dv_a}{dy}(x < b^l, y = 0) = 0 \quad (4.24)$$

Furthermore, the electric field outside the depletion region is negligible which gives the third boundary condition at the edge of the depletion area:

$$\frac{dv_a}{dx}(x=0) = 0 \quad (4.25)$$

Finally, the gate is at the potential of $V_{gs}^* = -3V$ which presents the fourth boundary condition.

The boundary conditions given by (4.23)-(4.25) are shown in Fig. 4.8.

Figure 4-8 Applied physical model with the boundary conditions in the initial plane, before mapping transformations.

In order to avoid FEA tools for solving 2D equation (4.22), the conformal mapping transformations from [Si 2013] are applied. In this way, the geometry from the initial z -plane shown in Fig. 4.8 is being transformed into the one in w -plane shown in Fig. 4.9. The transformed sheet density distribution, $n_{s0}'(x')$, is obtained by the transformation of the boundary conditions and is equal to

$$n_{s0}'(x') = \frac{d_{AlGaIn}(c+1)\sinh(\pi x')}{\sqrt{((c+1)\cosh(\pi x') - (c-1))^2 - 4}} \quad (4.26)$$

where $c = \cosh(\pi b(V_{ds})/d_{AlGaIn})$ while $b(V_{ds})$ is

$$b(V_{ds}) = \begin{cases} b^I(V_{ds}), & V_{ds} \leq V_{ds}^I \\ b^{II}(V_{ds}), & V_{ds} > V_{ds}^I \end{cases} \quad (4.27)$$

The unit for $b^I(V_{ds})$ and $b^{II}(V_{ds})$ is nm. The details about the conformal mapping transformations can be found in [Si, 2013].

Figure 4-9 Applied physical model with the boundary conditions after conformal mapping transformations

Since the transformed geometry from Fig. 4.9, contains the gate electrode as the conduction plane, the image charge method can be applied for obtaining the potential inside the depletion region for Range I of V_{ds} , $v_a^I(x_0', y_0')$. Comparing to the methodology from [Si 2013] that neglected the potential of the gate electrode, the following analysis will take it into account. In order to do that, the potential $v_a^I(x_0', y_0')$ will be calculated using the principle of superposition.

This potential is obtained as

$$v_a^I(x_0', y_0') = v_{a1}(x_0', y_0') + v_{a2}^I(x_0', y_0') \quad (4.28)$$

where $v_{a1}(x_0', y_0')$ is the potential that originates only from the sheet density $n_{s0}'(x')$, considering that the conduction plane is at zero volts, while $v_{a2}^I(x_0', y_0')$ is the potential that originates only from the conduction plane in the absence of $n_{s0}'(x')$. The superposition is shown in Fig 4.10.

The dependence $v_{a1}(x_0', y_0')$, was derived in [Si, 2013] while $v_{a2}^I(x_0', y_0')$ is obtained as the potential in the area near the conduction plane of $V_{gs}^* = -3V$ referring to the mapped point of the source electrode, $D(x_{DW}, 1)$ (Fig. 4.7, 4.9 and 4.10).

Figure 4-10 The principle of superposition for determination of $v_a^I(x_0', y_0')$

Using the expression from [Si, 2013] for $v_{a1}(x_0', y_0')$, the potential $v_a^I(x_0', y_0')$ becomes:

$$v_a^I(x_0', y_0') = \int_0^{+\infty} \frac{qn_{s0}'(x')}{2\pi\epsilon_a} \ln \left(\frac{(x'-x_0')^2 + (1+y_0')^2}{(x'-x_0')^2 + (1-y_0')^2} \right) dx' + V_{gs}^*(1-y_0') \quad (4.29)$$

In order to obtain the relation between the extension of the depletion area and the applied drain-source voltage, $b^I(V_{ds})$, it is necessary to calculate (4.29) in the point $B(x_B', y_B')$ that corresponds to the mapped point of the drain electrode.

In the w-plane, the point B has the coordinates: $x_B' = 0$ $y_B' = \frac{1}{\pi} \text{acosh}(\frac{3-c^I}{1+c^I})$ where $c^I = \cosh(\pi b^I(V_{ds})/d_{AlGaIn})$. Replacing x_B' and y_B' into (4.29), the parameter c^I and therefore b^I could be obtained as a function of V_{ds} . However, the parameter c^I is in the integral part of the equation (4.29) which makes it difficult for direct extraction. Therefore, the equation (4.29) was calculated for different values of c^I and this relation is shown in the lower part of the curve in Fig. 4.11. The wanted dependence $c^I(V_{ds})$ and therefore $b^I(V_{ds})$ are finally obtained by reading the values of c^I for a particular value of V_{ds} . Range I ends when V_{ds} becomes equal to V_{ds}^I . The value $b^I(V_{ds}=V_{ds}^I)$ will be marked as b_1 .

Figure 4-11 The obtained dependence of the lateral extension around the gate edge and the field plate edge on the applied V_{ds}

In order to obtain $b''(V_{ds})$ which corresponds to the lateral extension of the depletion area around the field-plate edge towards drain electrode, the physical model from Fig. 4.12 will be used.

Figure 4-12 Applied physical model for the extension of the depletion area around the field-plate edge.

Similarly to the previous calculation, $b^{II}(V_{ds})$ will be found independently on $b^I(V_{ds})$, since the length of the field-plate is sufficiently high to separate them. Comparing to the methodology used for obtaining $b^I(V_{ds})$, the presence of the Si_3N_4 dielectric with the voltage drop V_{ox} should be taken into account. This is necessary since the dielectric is found between the AlGaIn layer and the gate electrode, which is used as the conduction plane in the image charge method.

The analysis of device structure along the y-direction (used for vertical depletion modelling), gives the $V_{ox}(V_{ds})$ dependence shown in Fig. 4.13. Observing this dependence, it can be seen that before vertical depletion is completed (for $V_{ds} < V_{ds}^I$), the voltage drop inside the oxide depends on the applied V_{ds} meaning that image charge method would have different potentials of the conduction plane for each value of V_{ds} . But, since the lateral extension of the depletion area around the field-plate edge exists only for $V_{ds} > 11\text{V}$ when vertical depletion is completed, the V_{ox} used in the calculation of $b^{II}(V_{ds})$ will have a constant value of 13.54V.

Therefore, the potential $v_a^{II}(x'_0, y'_0)$, is equal to

$$v_a^{II}(x'_0, y'_0) = \int_0^{+\infty} \frac{qn'_{s0}(x')}{2\pi\epsilon_a} \ln \left(\frac{(x'-x'_0)^2 + (1+y'_0)^2}{(x'-x'_0)^2 + (1-y'_0)^2} \right) dx' + (V_{gs}^* - V_{ox})(1 - y'_0) \quad (4.30)$$

Figure 4-13 The oxide voltage drop dependence on the applied V_{ds}

Calculating (4.30) in the mapped point of the drain electrode, the dependence of $b_{tot}(V_{ds})=b_1+b^{II}(V_{ds})$ is obtained and shown in the upper part of the curve from Fig. 4.11. The total lateral extension is equal to the sum of b_1 and b^{II} , because for $V_{ds}>V_{ds}^I$, the extension b_1 around the gate edge already exists. Therefore, in order to obtain the extension only around the field-plate edge, $b^{II}(V_{ds})$, it is necessary to read the value for $b_{tot}(V_{ds})$ from Fig. 4.11 and then subtract b_1 from this value.

It is worth noticing that $\log_{10}(c^{I/II})$ is used in the curve representation in Fig. 4.11, since $c^{I/II}$ is a *cosh* function on $b^{I/II}$. Furthermore, V_{ds} is scaled with $\varepsilon_a/qd_{AlGaIn}n_{S0}$. In this way, the obtained curve provides easily readable points from which required $b^I(V_{ds})$ and $b_{tot}(V_{ds})$ can be obtained. As it was aforementioned, the lateral extension around the field-plate edge, $b^{II}(V_{ds})$ is obtained as $b^{II}(V_{ds})=b_{tot}(V_{ds})-b_1$, where $b_1=b^I(V_{ds}=V_{ds}^I)$.

Finally, by substituting $b^I(V_{ds})$ and $b^{II}(V_{ds})$ into (4.21), the parts of Miller' capacitance caused by lateral extension of the depletion area around the drain-side gate edge (for $V_{ds}<V_{ds}^I$) and the field-plate edge (for $V_{ds}>V_{ds}^I$) are be obtained.

4.2.3. The analytical model for fringing capacitance between gate and drain connecting pads

In order to complete the model for the Miller's capacitance, it is necessary to model the fringing capacitance between the pads that connect all gate and drain fingers in the multi-finger layout, $C_{gd_top_top_pad}$ (Fig. 4.14). This capacitance can be obtained applying the model from [Bansal 2006] that calculates the fringing between the top surfaces of two sufficiently long metal lines:

$$C_{gd_top_top_pad}(V_{ds}) = \varepsilon_g \frac{W_{pad_gd} \ln(1 + \frac{2W_{pad_gd}}{S_{pad_gd}})}{(W_{pad_gd} \pi + (H_{pad_gd} + T_{pad_gd}) \ln(1 + \frac{2W_{pad_gd}}{S_{pad_gd}}))} \quad (4.31)$$

where $W_{pad_gd}=194.7\mu\text{m}$, $S_{pad_gd}=965.3\mu\text{m}$, $H_{pad_gd}=0$ (the height difference between the pads) and $T_{pad_gd}=100\text{nm}$ (the height of the pads). These values are obtained from the Nomarski microscope image shown in Fig. 4.14.

Calculating (4.31) using previously obtained values of the corresponding parameters, the obtained value for $C_{gd_top_top_pad}$ is 9pF.

Figure 4-14 The top view of the multi-finger layout of the device

Finally, the complete model for the Miller's capacitance can be presented as:

$$C_{gd}(V_{ds}) = \begin{cases} C_{gd,y}^I + C_{gd,x}^I(V_{ds}) + C_{gd_top_top_pad}, & V_{ds} \leq V_{ds}^I \\ C_{gd,x}^{II}(V_{ds}) + C_{gd_top_top_pad}, & V_{ds} > V_{ds}^I \end{cases} \quad (4.32)$$

The obtained analytical model is shown in Fig. 4.15, clearly distinguishing the Range I and II of V_{ds} .

4.3. The analytical model for drain-to-source capacitance in the subthreshold regime

Drain-to-source capacitance contains of different fringing capacitances among which the highest one is caused by fringing between the undepleted 2DEG in the gate-source and gate-drain drift regions (Fig. 4.16).

Figure 4-15 The analytical model for the Miller's capacitance in the subthreshold regime

Figure 4-16 The physical origin of C_{ds} capacitance

The spacing between these undepleted areas is equal to the gate length for $V_{ds} \leq V_{ds}^I$ or to the sum of the gate length and the length of the field plate for $V_{ds} > V_{ds}^I$. As V_{ds} changes from 0 to the breakdown rating of 100V, the length of

the drift area that contains the 2DEG is decreased for $b^{II}(V_{ds})$ as it was shown in the previous section. Using the analytical model from [Bansal 2006] for the calculation of the “top-top” fringing capacitance between the undepleted 2DEG in the gate-source and gate-drain regions, it is obtained:

$$C_{ds_top_top}(V_{ds}) = \epsilon_g \frac{L_{gs} \ln(1 + \frac{2L_{gs}}{S_1})}{(L_{gs}\pi + (H_1 + S_1) \ln(1 + \frac{2L_{gs}}{S_1}))} \quad (4.33)$$

where $H_1=0$ (the height difference between the electrodes), $T_1=2nm$ (the approximation of the 2DEG height) while S_1 is equal to

$$S_1 = \begin{cases} L_g + b^I(V_{ds}), & \text{for } V_{ds} \leq V_{ds}^I \\ L_g + L_{fp} + b^{II}(V_{ds}), & \text{for } V_{ds} > V_{ds}^I \end{cases} \quad (4.34)$$

Similarly to the model for the Miller’s capacitance, the non-negligible fringing capacitance exists between the pads that connect all drain and source fingers (Fig. 4.14). This capacitance, $C_{ds_top_top_pad}$, can be calculated using (4.31) with the values of geometrical parameters determined from the microscope photo of the multifinger layout: $S_{pad_ds}=1160\mu m$, $T_{pad_ds}=T_{pad_gd}$, $W_{pad_ds}=W_{pad_gd}$ and $H_{pad_ds} = H_{pad_gd}$. For this multifinger layout, it is equal to 7.9pF.

Finally, the $C_{ds}(V_{ds})=C_{ds_top_top}(V_{ds})+C_{ds_top_top_pad}$ is shown in Fig. 4.17. Using previously obtained model for $C_{gd}(V_{ds})$, $C_{oss}(V_{ds})$, is calculated and also shown in Fig. 4.17.

Figure 4-17 The analytical model for the drain-source and the output capacitance

4.4. The analytical model for gate-to-source capacitance in the subthreshold regime

Gate-to-source capacitance also needs to be analytically modelled in order to obtain the complete model for input capacitance of the device. This capacitance contains of different fringing capacitances which do not depend on V_{ds} , since the 2DEG concentration in the source drift area doesn't change with drain-to-source voltage (Fig. 4.2 and 4.3).

The cross-section of the device which shows different parts of C_{gs} is given in Fig.4.18. Different portions of fringing between the electrodes will be analytically modelled and calculated by distinguishing the fringing between the top and top, top and sidewall, sidewall and bottom of the electrodes and applying the methodology from [Bansal 2006] for each of them.

As it can be seen in Fig. 4.18, the fringing capacitance between the bottom of the gate electrode and the top of the undepleted 2DEG in the source drift region is marked as $C_{gs_bottom_top}$, and can be calculated as

$$C_{gs_bottom_top} = \epsilon_a L_g \frac{\ln(1 + \frac{2L_g}{S_2})}{L_g \pi + (d_{AlGaN} + T_1) \ln(1 + \frac{2L_g}{S_2})} \quad (4.35)$$

Figure 4-18 The physical origin of C_{gs} capacitance

In the previous equation, T_1 is the height of the 2DEG (estimated to 2nm) while S_2 is the lateral distance between the 2DEG layer and the gate electrode. Theoretically, this distance is zero but in order to apply (4.35), the value of $S_2=2nm$ was used. Using the values from Table 3.2 and 3.3 for ϵ_a , L_g and d_{AlGaN} , the value $C_{gs_bottom_top}=184.7pF$ is obtained.

The capacitance between the sidewall of the gate electrode and the top of the undepleted 2DEG is marked as $C_{gs_sw_top}$ and also can be calculated by applying the model from [Bansal 2006]. Since the gate electrode is passivated using Si_3N_4 , the lines of the fringing field are contained in Si_3N_4 and AlGaN layers. However, since the total height of the gate electrode is $T_{gate}+t_{ox}=180nm$ while the thickness of AlGaN layer is only 24nm, the ϵ_{ox} will be used in the model for this capacitance. Additionally, the dielectric constant of Si_3N_4 is only 1.34 times higher than the constant of AlGaN so the expected error of not taking into consideration two materials in the fringing area is quite small. In this way, the analysis of this fringing capacitance is not additionally complicated and the model from [Bansal 2006] can be directly applied:

$$C_{gs_sw_top} = \frac{2}{\pi} \epsilon_{ox} \ln \left(\frac{d_{AlGaN} + T_{gate} + t_{ox} + \sqrt{S_2^2 + (T_{gate} + t_{ox})^2} + 2d_{AlGaN}(T_{gate} + t_{ox})}{S_2 + d_{AlGaN}} \right) \quad (4.36)$$

Calculation of (4.36) gives $C_{gs_sw_top}=107pF$.

The third part of gate-to-source capacitance that presents the fringing through AlGaN layer between the bottom of the gate electrode and the sidewall of the source, $C_{gs_top_sw}$ (Fig. 4.18) can be calculated similarly to $C_{gs_sw_top}$, using different values that correspond to this geometry:

$$C_{gs_top_sw} = \frac{2}{\pi} \epsilon_a \ln \left(\frac{d_{AlGaN} + \sqrt{L_{gs}^2 + d_{AlGaN}^2}}{L_{gs}} \right) \quad (4.37)$$

Calculating (4.37) it is obtained that this capacitance is quite small: $C_{gs_top_sw}=0.6pF$.

The fourth part of C_{gs} is the plate capacitance between the sidewall of the source and the sidewall of the gate electrode, $C_{gs_sw_sw}$, which can be calculated as $C_{gs_sw_sw}=\epsilon_{ox} \times W_g \times (T_{gate}+t_{ox})/L_{gs}$. The obtained value of 0.7pF is negligible. This capacitance exists between gate and drain electrodes as well, but has the order of 10^{-13} and was completely neglected.

Finally, the multifinger layout of the device causes additional capacitance due to fringing between the areas that connect all gate and source fingers. In this multifinger configuration, these areas are placed quite close to each other, causing a significant portion of C_{gs} (Fig. 4.19). Using the parameters marked on Fig. 4.19, this capacitance can be calculated as top-top fringing capacitance, applying the corresponding model from [Bansal 2006]:

$$C_{gs_multifinger} = \epsilon_a W_{gs_finger} \frac{\ln(1 + \frac{2W_{gs_finger}}{S_{gs_finger}})}{W_{gs_finger}\pi + (H_{gs_finger} + T_{gs_finger})\ln(1 + \frac{2W_{gs_finger}}{S_{gs_finger}})} \quad (4.38)$$

In (4.38), T_{gs_finger} is the height of the pad that connects gate/source fingers and is approximated to the value of T_{gate} while H_{gs_finger} is the height difference between these pads and is equal to zero. Using the values for $W_{gs_finger}=29.1\mu m$ and $S_{gs_finger}=4.55\mu m$ from Fig. 4.19, equation (4.38) gives $C_{gs_multifinger}=69.2pF$.

The sum of previously obtained capacitances gives the total gate-source capacitance equal to 362.2pF. The complete analytical model for input capacitance of the device, $C_{iss}(V_{ds})=C_{gd}(V_{ds})+C_{gs}$ is shown in Fig. 4.20.

Figure 4-19 Fringing between gate and source finger-connecting pads

Figure 4-20 *The analytical model for the input capacitance.*

4.5. Experimental verification of the proposed capacitance model

In order to verify the proposed physics-based model, the experimental characterization of the device was done. The HEMT was kept in the subthreshold regime by applying the $V_{gs} = -3V$. The reverse (C_{gd}), output (C_{oss}) and input (C_{iss}) capacitances were measured for V_{ds} varied from 0 to 100V. The frequency and the amplitude of the small signal used for the excitation in the measurement were 1MHz and 25mV respectively. The comparison between the proposed analytical model and the curves obtained from the measurement is shown in Fig. 4.21, 4.22 and 4.23.

Speaking of switching application that requires devices rated for $V_{ds}=40V$, the modelled and the measured value of gate-to-drain charge can be obtained as the area under each of the curves from Fig. 4.21 and are equal to 2.02nC and 2.37nC respectively. This gives 14.7% of the deviation between the modelled and the measured value of gate-to-drain charge.

Using the same approach, the modelled and the measured values for the output and the input charge can be obtained. The output charge, Q_{oss} , for

$V_{ds}=40V$ and $V_{gs}=-3V$, has the measured value of $3.51nC$ while the model predicts $3.12nC$, giving the deviation of 11.2% . Speaking of input charge, Q_{iss} , the measured and the modelled values are $17.31nC$ and $16.42nC$, respectively, giving the deviation of only 5.2% .

Figure 4-21 *The analytical model versus measurements for the Miller's capacitance.*

Figure 4-22 *The analytical model versus measurements for the output capacitance*

Figure 4-23 *The analytical model versus measurements for the input capacitance*

4.6. Summary and conclusions

In this chapter, a novel technique for analytical modelling of input, output and reverse capacitance of a GaN HEMT with the field-plate structure has been proposed. For each of the device capacitances (Miller's, gate-to-source and drain-to-source), the physical origin has been found and the corresponding analytical model for capacitance dependence on the applied drain-source voltage has been derived.

The proposed model for Miller's capacitance is based on the approximation of the charge depletion in two separate directions: vertically (perpendicularly) and laterally with respect to the channel. In this way, FEA tools that are necessary for solving 2D Laplace equation in AlGaN and GaN layers have been avoided and fully analytical models for vertical and lateral depletion process have been obtained. It was found that **the non-linearity of the Miller's capacitance dominantly depends on the design of the field-plate structure**. Since the field-plate extension determines the breakdown voltage of the device, the obtained model can be used for the estimation of the trade-off between the breakdown voltage rating of the device and the amount of gate-to-drain charge. Together with the analytical model for the electric field in the

channel (which will be presented in the Chapter 6 of this thesis), this capacitance model will provide the analytical equations necessary for the optimization of the field-plate design for the target breakdown voltage. The optimization will be based on the minimization of the Miller's charge, in order to decrease the duration of the plateau time in the gate-source signal and therefore minimize the switching losses in the converter. Comparison between the modelled and experimentally obtained value for gate-to-drain charge showed the deviation of 14.7%. As it will be shown in the next chapter, this deviation will not influence the power loss estimation in the buck converter, up to 20MHz of switching frequency.

Speaking of **drain-source and gate-source capacitances**, it has been found that these capacitances **are dominantly caused by fringing between the corresponding electrodes and their extensions through the 2DEG in the source and drain drift regions**. While drain-source capacitance has a weak dependence on the applied V_{ds} , gate-source capacitance is completely independent on the drain-source voltage, since the concentration of the 2DEG in the source drift area doesn't change. The analysis of the multifinger layout of the device **showed that significant amount of this capacitance is caused by the fringing between the gate and source pads that connect all gate and source fingers**.

The proposed capacitance model made some clear directions in the device design optimization for high-frequency switching application. Since the field-plate design can be optimized separately by gate-to-drain charge minimization for a given breakdown voltage, the rest of the design parameters that determine gate-source and drain-source capacitance together with the switching on-resistance can be optimized by the power losses minimization in the topology of interest.

**Chapter5. Verification of the
power loss model of a high-
frequency buck converter together
with the precision of the proposed
physics-based model**

5. Verification of the power loss model for a high-frequency buck converter together with the precision of the proposed physics-based model

5.1. Power loss model of a high-frequency buck converter

The electrical (power loss) model is a crucial part of the optimization loop presented in Fig.5.1. It can be used for losses calculation in a certain topology or for the device design optimization from the application point of view. This process is described by the block diagram in Fig. 5.1 where starting from the device itself and following the blocks in the counter clockwise direction, the overall efficiency of the chosen topology is being estimated. Alternatively, starting from a certain application and following the same blocks in the clockwise direction, the device design is being optimized by power losses minimization. In both cases, precise power loss model of the topology of interest presents a necessary link between the device and its physical characteristics on one hand and its application on the other.

Figure 5-1 The block scheme of a device design optimization

Basically, the loss models can be classified into three categories. The first one are the physics-based models used for Finite Element Analysis which are very precise but time consuming [Cheng 2005, Bowman 1999]. The second type are the behavioral models for simulation programs such as PSPICE and Simplorer where device is usually described by some key parameters. These models are widely used since they provide good trade-off between the accuracy and simulation time [Wang 2008, Pagano 2006]. The third type are the analytical models, based on different equivalent circuits during the switching transitions. Analytical models [Zhang 2011, Bai 2004, Eberle 2009, Sagneri 2009, Ren 2006, Rodriguez 2009] are the fastest among the aforementioned types but their accuracy can be the major problem, especially at high switching frequency and low output power. The power loss model that was used in this work is a hybrid analytical-behavioral power loss model for high-frequency and low load buck converter, proposed and verified in [Diaz 2012].

The proposed approach provides a transistor model that can be used for fast calculation of the power losses by numerical solving of a set of differential equations (specific for each topology) or by direct application in a circuit simulator such as PSPICE or Simplorer. In this work, the model was implemented into Simplorer simulation tool.

The applied model is developed for a simplified buck converter, focusing on the transistors losses and neglecting the losses in the magnetic components and capacitors. The complete model of the switch is shown in Fig. 5.3 while the schematic circuit of the modelled synchronous buck converter is shown in Fig. 5.2. Due to high-frequency operation, the parasitic inductances of the transistor's package, L_d , L_g and L_s were taken into account together with the parasitic inductance of the PCB layout, L_{pcb} . Parasitic resistances of the package were also taken into account.

The main assumption of the model is that load behaves as a current source i.e. that inductor used in the experimental prototype has been designed in a way that provides a DC output current. In that way, the core losses and the wire AC losses are removed from the converter losses.

In the proposed modelling approach, the non-linear dependence of the device capacitances on drain-to-source voltage can be measured or read from the datasheet and fitted as a polynomial function.

Furthermore, the relationship between the drain current and gate-source voltage is modelled as a piece by piece linear curve:

$$i_{channel} = \begin{cases} 0, & v_{gs} < V_{th} \\ g_{m1}(v_{gs} - V_{th}), & V_{th} < v_{gs} < V_a \\ I_0 + g_{m2}(v_{gs} - V_a), & v_{gs} > V_a \end{cases} \quad (5.1)$$

where g_{m1} , g_{m2} , V_{th} and V_a should be measured or estimated from the datasheet.

Figure 5-2 Schematic circuit of the modeled synchronous buck converter

Figure 5-3 The complete model of the switch

It is important to notice that forward transconductance is modelled taking into account its dependence on gate-to-source voltage, using two different values.

Additionally, the following parameters were taken into account: the input voltages of the drivers, V_{dr} and V_{dr2} , the dead times between the control

signals, turn-on and turn-off impedances of the drivers as well as the body-diode forward voltage drop (V_d), reverse recovery charge, Q_{rr} , gate resistance R_g , inductor DC resistance, R_{dc} and finally the average value of the on-resistance of the switch, R_{dson} . The complete model with its implementation and validation can be found in [Diaz 2012].

5.2. High-frequency buck converter for ET and EER, using GaN HEMTs

As explained in the Introduction of this thesis, the target application for GaN device in this work is a high frequency buck converter aimed to be applied as an Envelope Amplifier in Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) transmission techniques. In both techniques, Envelope Amplifier behaves as a dynamic power supply of a Radio Frequency Power Amplifier (RFPA), which operates in a linear mode in ET (Class A, B or AB) and non-linear mode in EER (Class C, D, E or F).

Speaking of efficiency enhancement using ET technique, it was demonstrated that application this type of a transmitter provides significantly higher efficiency comparing to the linear RFPA that is supplied from a constant power supply. However, EER technique provides even higher efficiency values, due to highly efficient non-linear RFPA. Nevertheless, the linearity of the signal transmission can be an issue in EER, since it depends on the bandwidth of an envelope amplifier and the time alignment of the envelope and phase modulation [Kenington 2000, Vasic 2010]. Approximately, in order to achieve the RF signal's bandwidth of 1MHz in EER, it is necessary to provide three to five times higher bandwidth of the envelope. This requires 20MHz for the minimum switching frequency of the converter. Since GaN HEMTs are characterized by significantly lower capacitances than their Si counterparts, they are considered to be excellent candidates for this type of application.

5.2.1. Experimental prototype of a HF buck converter

With the aim of verification of presented power loss model, together with the precision of the proposed physics-based model, the prototype of a high-frequency buck converter was built, using modeled AlGaN/GaN HEMT for the main switch and STPS20L25CT diode from ST microelectronics for the freewheeling diode. The RF inductor 144-02J12L from Coilcraft was used as

filter inductor. The driving circuit was designed using EL7155 commercially available driver from Intersil together with ISO721 isolation chip that received signal generated in Spartan 3 FPGA board. Since the analyzed switch has the threshold voltage of -2V, the gate signal levels were set to -5V for the off-state and 0V for the on state of the device. The converter operated in open loop, with the following specifications:

- Input voltage of 24V
- The load resistance of 6Ω
- The switching frequency of 7, 15 and 20MHz.

Since the analyzed GaN HEMT has a TO-220 package, estimated values for L_d , L_g and L_s were 1, 1, 6nH respectively while additional parasitic inductance of a high frequency loop due to PCB layout was estimated to 5nH. The photo of the modelled switch is shown in Fig. 5.4 while the prototype of the converter is presented in Fig. 5.5. The measured and simulated waveform at the input of the LC filter at 20MHz of switching frequency is shown in Fig. 5.6.

The overall efficiency of the converter, including the driving losses, was measured at switching frequency equal to 7, 15 and 20MHz, providing different output power levels by changing the duty cycle values. The measurements were done in this manner since Radio Frequency Power Amplifier behaves as the resistive load, while the envelope tracking is performed by the duty cycle modulation. The efficiency measurements at each of the aforementioned switching frequencies are shown in Fig. 5.7.

Figure 5-4 Modeled AlGaIn/GaN HEMT in a TO-220 package

Figure 5-5 *The prototype of a high-frequency buck converter using analyzed GaN HEMT as the main switch*

5.2.2. Simulation results using experimentally obtained HEMT characteristics

In order to verify the power loss model, measured curves for $C_{gd}(V_{ds})$, $C_{oss}(V_{ds})$ and $C_{iss}(V_{ds})$ from Fig. 4.21, 4.22 and 4.23 were fitted and implemented into Simplorer schematic. Furthermore, according to (5.1), forward transconductance dependence on gate-to-source voltage was fitted using two different values, extracted from the measured curves in Fig. 3.10. The obtained values for parameters from (5.1) are $V_{th}=-1.9V$, $V_a=-1.5V$, while $I_0=3A$, $g_{m1}=7.5A/V$ and $g_{m2}=8.5A/V$. Furthermore, the average value for the on-resistance of the switch using measured I-V curves from Fig. 3.10 was estimated to $183m\Omega$. Moreover, using the datasheet, the output capacitance of a Schottky diode was estimated to $C_{diode}=0.6nF$ and this value was used in the simulation. The driver voltage levels were equalized to the ones used in experimental measurements: $-5V$ for the OFF state and $0V$ for the ON state. The obtained simulated efficiencies at 7, 15 and 20MHz of switching frequency, together with the measured efficiency curves are shown in Fig. 5.8.

Figure 5-6 The measured and simulated waveform at the input of LC filter at 20MHz of switching frequency

Figure 5-7 The overall efficiency measurements at 7, 15 and 20MHz of switching frequency

Observing simulated curves that used measured characteristics of a HEMT, it can be seen that good agreement with the measured efficiency curves was obtained at each switching frequency. Especially important result is a good agreement at 20MHz in a low range of the output power, since these are the target operating conditions of the converter. Therefore, the power loss model was verified and can be used in a further device design optimization for this application.

Figure 5-8 The overall efficiency of the converter at 7, 15 and 20MHz of switching frequency: measurements vs simulations that used measured device characteristics.

5.2.3. Simulation results using modelled HEMT characteristics

Since the power losses model has been verified through the efficiency simulations that employed experimentally obtained characteristics of the HEMT, the next step was precision verification of the proposed physics-based model. In order to do that, the same simulations have been performed only using modelled characteristics for the I-V curves and the capacitances, shown in Fig. 3.10, 4.21, 4.22 and 4.23.

Simulated efficiency curves that used modelled characteristics of the switch, at 7, 15 and 20 MHz of switching frequency, are shown in Fig. 5.9.

Figure 5-9 The overall efficiency of the converter at 7, 15 and 20MHz of switching frequency: measurements vs simulations that used modeled device characteristics.

Comparing these simulations to the measurements and previous simulations which used experimental characteristics of the device, it can be observed that very good agreement is obtained, showing the discrepancy towards higher values of P_{out} , i.e. towards higher values of the output current. This result was expected due to the imprecision of 14.7% in the model of total gate-to-drain charge, Q_{gd} . (Section 4.5) Since Q_{gd} defines the duration of Miller's "plateau" time in gate-source signal, the precision in Q_{gd} estimation will highly influence the precision of switching loss estimation. Since the switching losses are directly proportional to the product of the output current and Miller time, the influence of 14.7% will dominantly be seen in higher range of the output current. Nevertheless, the obtained discrepancies are quite small and acceptable from the application point of view: 4% at 25W and 15MHz and 3% at 12.5W and 20MHz. Also, a deviation of 4% can be seen at 20MHz for very small output power of 2W. Overall, observing the complete curves from Fig. 5.9 it can be concluded that precision of the proposed physics-based model is high enough.

Therefore, the proposed model can be used in the device design optimization process.

5.2.4. Simulation results using constant Miller's capacitance

As it was explained in the Introduction of this thesis, the absence of analytical models for the capacitances of AlGaIn/GaN HEMTs with the field-plate structure, complicates the estimation and conclusions about the precision of the methodology proposed in this work. As explained in Section 2.3.2, the only analytical model for capacitances of this structure was found in [Ahsan, 2016]. Since this model is a surface-potential based model, it contains complex, unified expression for Fermi-level dependence on the gate voltage that demands iterative numerical solving. Therefore, this model is not suitable for implementation into the optimization algorithm and was not analyzed in terms of precision. In order to more thoroughly examine the precision of the methodology proposed in our work, the additional simulations were made.

Since precise estimation of gate-to-drain charge is crucial for precise calculation of switching losses, the additional simulations were performed using constant values for Miller's capacitance in the complete range of V_{ds} . The values used for this purpose are: $C_{gd}=130pF$ (which corresponds to the C_{gd} value in the Range I of V_{ds}), $C_{gd}=11.8pF$ (which corresponds to the C_{gd} value in the Range II of V_{ds}), and finally $C_{gd}=C_{gd,eq}=40pF$ which is the value obtained from the approximate calculation of the energy in the capacitor:

$$E_{C_{gd}} = \frac{1}{2} C_{gd,eq} V_{max}^2 \quad (5.2)$$

In (5.2), $V_{max}=24V$, while $E_{C_{gd}}$ was obtained as $E_{C_{gd}} = \int_0^{V_{max}} C_{gd}(V_{ds}) V_{ds} dV_{ds}$, using the modelled characteristic for $C_{gd}(V_{ds})$. The comparison between additionally simulated efficiency curves for switching frequency of 7MHz is shown in Fig. 5.10, together with measured efficiencies and previously simulated efficiency curves when modelled and experimentally measured $C_{gd}(V_{ds})$ dependence was used.

Observing the curves from Fig. 5.10, it can be seen that very good agreement exists between the measurements and the simulations obtained when modelled $C_{gd}(V_{ds})$, measured $C_{gd}(V_{ds})$ and $C_{gd,eq}$ is used. Maximum discrepancy of 3% for P_{out} lower than 7W is obtained between the curves that used modelled and measured $C_{gd}(V_{ds})$, showing very good loss estimation

when proposed model for Q_{gd} is used. Additionally, the curve obtained using $C_{gd,eq}$ showed very good agreement, implying that equivalent capacitor value calculated from (5.2) can also be used for precise loss calculation. On the other hand, simulations that used constant C_{gd} equal to the value of this capacitance in the Range I or II of V_{ds} , showed significantly higher discrepancies: 10% for $C_{gd} = 130pF$ and 5% for $C_{gd} = 11.8pF$, in almost entire range of V_{ds} . Since the calculation of the energy in the capacitor also demands non-linear $C_{gd}(V_{ds})$ dependence, we conclude that proposed non-linear model for $C_{gd}(V_{ds})$ is necessary for precise loss estimation in a high-frequency buck converter.

Figure 5-10 The simulations at 7MHz using constant values for Miller's capacitance.

5.3. The TO-220 package influence on the overall efficiency of the converter

The important issue when speaking of device optimization for high-frequency switching application certainly is the device package. In our case, the existing TO-220 package is highly inappropriate for high-frequency application, due to

high values of parasitic inductances in drain, gate and source: L_d , L_g and L_s respectively. Therefore, it is important to analyze how much the package of the device penalizes the efficiency of the converter at high switching frequency.

Using previously presented and verified power loss model, the same design of the device was simulated using DirectFET package for the device. This package was chosen due to significantly lower values for L_d , L_g and L_s [Ji 2013]. The comparison between the overall efficiency of the converter when new (DirectFET) and old (TO-220) package is used, at 20MHz of switching frequency is shown in Fig. 5.11. It can be seen that high difference in the efficiency was obtained, implying that replacement of TO-220 package is necessary when optimization of the switching device for this application is performed.

Figure 5-11 The additional efficiency simulations at 20MHz of switching frequency: old (TO-220) and new (DirectFET) package

5.4. The influence of the Schottky diode capacitance on the overall efficiency of the converter

After power loss model and proposed physics-based model were verified, the total loss breakdown was calculated for P_{out} of 8W and switching frequency of 20MHz. The loss breakdown is shown in Fig. 5.12.

Figure 5-12 The total loss breakdown at $P_{out}=8W$ and $f_{SW}=20MHz$

Observing the loss breakdown from Fig. 5.12, it can be seen that losses due to output capacitance of a freewheeling Schottky diode, $C_{diode}=0.6nF$, present 30% of total losses at 20MHz and output power of 8W. If C_{diode} is reduced from 0.6 to 0.1nF and previously presented DirectFET package is used, the simulations from Fig. 5.13 are obtained. It can be seen that, due to significant efficiency improvement especially in a low range of the output power, synchronous buck configuration will be preferable topology when optimized design of the device is tested.

Figure 5-13 The efficiency simulations for different capacitances of the Schottky diode at 20MHz of switching frequency.

5.5. The simulations and experimental measurements of 64QAM signal of 1MHz of Large Signal Bandwidth

In order to verify the power loss model together with proposed physics-based model for variable signal at the output of the converter, 64QAM signal with 1MHz of large signal bandwidth was generated, using the switching frequency of approximately 20MHz. The experimental prototype is shown in Fig. 5.5 and was described in detail in Section 5.2. It is worth reminding that load resistance in this type of measurement is kept constant and equal to 6Ω , while the envelope is generated using different values of the duty cycle, generated by Spartan 3 FPGA board. Generated signal is shown in Fig. 5.14.

Measured efficiency for generated signal with the average output power equal to 5.4W and Peak to Average Power Ratio (PAPR) of 10.5dB is 38.2 %. The average output power was measured by measuring the output voltage during one sequence of the envelope signal and calculating the total energy during this time period. The average power was obtained as this total energy divided by the time duration of the sequence.

Figure 5-14 Generated 64QAM signal with 1MHz of large signal bandwidth

Finally, the overall efficiency of the converter was estimated using previously proposed power loss model. Using the probability density for the envelope voltage V_{out} from [Vasic 2010], $p(V_{out})$, the efficiency was calculated for each value of the output voltage (which is in the range from 0 to 24V), $\eta(V_{out})$. Finally, the average efficiency of the signal was obtained as

$$\eta_{64QAM} = \frac{1}{V_{max}} \int_0^{V_{max}} \eta(V_{out}) p(V_{out}) dV_{out} \quad (5.3)$$

where V_{max} is equal to the input voltage of 24V. The obtained value $\eta_{64QAM}=38.8\%$ is in a very good agreement with the measured value.

5.6. Conclusions

In this chapter, **experimental verification of the power loss model of a high-frequency buck converter was performed, together with verification of the precision of proposed physics-based model of the device.**

The measurements of the overall efficiency of the converter at 7, 15 and 20MHz of switching frequency showed very good agreement with the simulations that used experimentally obtained characteristics of the analyzed

device. In this way, **power loss model was verified. Furthermore, good agreement was obtained between the simulations that used modelled characteristics of the device and the measurements**, showing slightly higher discrepancies in the higher range of the output power, which was expected due to deviation of 14.7% in the model for gate-to-drain charge. Still, **the obtained maximum discrepancies of 4% at 25W and 15MHz and 3% at 12.5W and 20MHz are quite small and acceptable from the application point of view.** Therefore, **the proposed physics-based model proved to be precise enough for further design optimization of the device design.**

Furthermore, the penalization of the efficiency due to TO-220 package of the device was addressed. **When compared to DirectFET package, TO-220 penalizes the converter efficiency up to 17% at 20MHz of switching frequency.** Additionally, the losses due to high value of the output capacitance of the freewheeling diode were analyzed. Observing the total loss breakdown at 8W and 20MHz it has been established that diode losses present 30% of total losses, implying that **synchronous buck configuration should be used when optimization of the device is performed.**

Finally, the power loss model and physics-based model were verified when 64QAM signal with 1MHz of large signal bandwidth was generated, switching at 20MHz. Measured efficiency for the generated signal with the average output power equal to 5.4W and Peak to Average Power Ratio (PAPR) of 10.5dB, was 38.2 % which is in a very good agreement with predicted value of 38.8%.

Chapter6. The proposed optimization of a GaN HEMT design using previously developed physics-based model

6. The proposed optimization of GaN HEMT design using previously developed physics-based model

6.1. Variation of design parameters and its influence on the total efficiency of the converter

Since the physics-based model for input, output and reverse capacitance of a GaN HEMT with the field-plate structure has been obtained and verified, together with the model for output characteristics of the device, it can be used for device design optimization for application in high-frequency buck converter. In order to make some starting directions for optimization process and observe how each parameter influences the overall efficiency of the converter, the following analysis has been performed.

As it can be seen from the analysis presented in Chapter 3, parameters such as Aluminum mole fraction, m , and the thickness of $\text{Al}_m\text{Ga}_{(1-m)}\text{N}$ layer, $d_{\text{AlGa}}N$, dominantly influence the on-state properties of the device by determining the 2DEG density dependence on the gate voltage. It is important to highlight that these two parameters depend on each other due to technological constraints for growth of pseudomorphic Al-containing GaN alloys. Higher Al mole fraction in $\text{Al}_m\text{Ga}_{(1-m)}\text{N}$ layer increases the lattice mismatch to GaN, which is accommodated by increased strain in the film. **This decreases the critical thickness** for growth of pseudomorphic Al-containing GaN alloys, above which stress in the film is released by formation of strain relaxation and therefore reduction in piezoelectric polarization (formation of dislocation). One of the models that provides the relation between m and maximum thickness of AlGa N layer, $d_{\text{AlGa}}N$ is the model from [Fischer 1994]. This model was compared to experimentally obtained structures in [Ambacher 2000] and it was shown that partly relaxed structures (structures with dislocations) lie slightly above the m - $d_{\text{AlGa}}N$ curve of this model (i.e. for higher values of critical thickness $d_{\text{AlGa}}N$). This is shown in Fig. 6.1. Therefore, this model can be used for determination of maximum thickness of AlGa N layer, since experimentally obtained results demonstrated that even higher values for $d_{\text{AlGa}}N$ thickness can be used. Since increase in m increases the 2DEG sheet density for the same gate-source voltage, higher values of m decrease the on-resistance of the device, while having negligible influence on the capacitive part. Therefore, from the point of view of our application, the goal is to increase m up to the technological

boundary, choosing d_{AlGaN} according to the Fischer model curve from Fig. 6.1. Since the relaxation factor starts to increase for $m > 35\%$ independently on the d_{AlGaN} , $m = 35\%$ will be the chosen value in our optimized design. Accordingly, the corresponding value for d_{AlGaN} will be set to 20nm which is the value read from the Fischer curve in Fig. 6.1. Three different $n_{2\text{DEG}}(V_{\text{gs}})$ curves that correspond to the initial structure with $m = 24\%$, $d_{\text{AlGaN}} = 24\text{nm}$ and two different structures obtained using the curve from Fig. 6.1 are shown in Fig. 6.2.

Figure 6-1 The relation between Al mole fraction, m and maximum thickness of AlGaN layer, d_{AlGaN} , which does not introduce strain relaxation and dislocations in AlGaN/GaN heterostructure.

Figure 6-2 2DEG dependence on V_g for different m - d_{AlGaN} designs

The $I_d(V_{gs}, V_{ds})$ curves that correspond to the geometry from Table 3.2, using $n_{2DEG}(V_{gs})$ curves from Fig. 6.2 are shown in Fig. 6.3. The decrease of on-resistance can be clearly observed for the structures with increased m comparing to the initial structure with $m=24\%$.

Furthermore, variation in the field plate thickness and length influences the off-state properties of a HEMT by changing its Miller's capacitance dependence on V_{ds} while parameters such as gate width and length, gate-to-source and drain-to-source spacing significantly affect both- turn-on and turn-off properties.

Regarding the field plate design, the first parameter that we can vary and observe its influence on the overall efficiency of a buck converter is the thickness of the dielectric Si_3N_4 , which will be marked as t_{ox} . This variation directly influences the process of vertical depletion of the 2DEG leftover under the field plate (described in Section 4.2.1). Applying the same methodology, from (4.18) we obtain the values for the “knee” drain-to-source voltage in $C_{gd}(V_{ds})$ curve, V_{ds}^I , while (4.20) directly calculates the part of C_{gd} caused by this depletion –

$C_{gd,y}^{I_{gd,y}}$. Different $C_{gd}(V_{ds})$ that correspond to 25 and 50% of increase/ decrease in Si_3N_4 thickness (with respect to the nominal value of 80nm), are presented in Fig. 6.4. When these curves are implemented into power loss model of a high frequency buck converter from the previous section, we obtain the efficiency curves shown in Fig. 6.5.

Figure 6-3 $I_d(V_{ds}, V_{gs})$ characteristics for different m - $d\text{AlGaIn}$ designs

Observing the curves from Fig. 6.4, it can be seen that for lower values of insulator thickness, knee voltage shifts towards lower values of V_{ds} , while maximum value of C_{gd} increases. Nevertheless, the decrease in the thickness results in higher efficiency of the buck converter, since the total amount of gate-to-drain charge that corresponds to the area under the $C_{gd}(V_{ds})$ is lower. From the curves shown in Fig. 6.5, it can be seen that application of 40 and 120nm thick Si_3N_4 gives approximately 6% of efficiency difference in the whole range of output power, at 10MHz of switching frequency.

Figure 6-4 The Miller's capacitance for different insulator thickness

Figure 6-5 Estimated overall efficiency of a buck converter for different field plate thickness at 10MHz

The length of the field-plate length is the next parameter that can be varied. This value also influences the Miller's capacitance of the device, but comparing to the previous variations with the field plate thickness, the knee

voltage of C_{gd} curve remains the same while the capacitance value in the Range I of V_{ds} is being changed. Equation (4.20) was used in the calculation of $C_{gd,y}^I$ for field plate lengths of $0.75\mu\text{m}$ and $2.25\mu\text{m}$, which corresponds to decrease/increase of 50% with respect to the nominal value of $1.5\mu\text{m}$. Similarly to the previous analysis for different field plate thickness, the amount of $C_{gd,x}^I$ and $C_{gd,x}^{II}$ due to lateral electric field remains unchanged. The obtained $C_{gd}(V_{ds})$ curves are presented in Fig. 6.6. It can be clearly seen that by increase of L_{fp} , the Miller's capacitance due to vertical charge depletion below the field-plate increases. On the other hand, the increase in L_{fp} will decrease the overall drain-to-source charge due to larger distance between source and drain drift regions and lower fringing capacitance between them (Fig. 4.16, Fig. 6.7.)

Figure 6-6 Miller's capacitance for different field plate length.

Figure 6-7 Drain-to-source capacitance for different field plate lengths.

Simulation results for different field-plate lengths are shown in Fig. 6.8.

Figure 6-8 Estimated efficiency of a buck converter for different field plate lengths at 10MHz.

It can be seen that variation in gate-to-drain charge dominantly influences the efficiency of the converter. This was expected since gate-to-drain charge determines the duration of the plateau in gate-source signal and therefore highly influences the switching losses in the converter. Efficiency difference between the curves is more visible in the range of higher output currents (higher duty cycle values) since the switching losses are directly proportional to the product of the output current and Miller time.

Regarding the design of the gate electrode, as it was already mentioned, it influences both – the turn-off and turn-on properties of a HEMT. Increase/decrease in the gate length for 50% with respect to the nominal value of $2\mu\text{m}$, will provide less or more drain current for the same V_{gs} and V_{ds} (Fig 6.9). On the other hand, this parameter strongly influences the part of C_{gs} due to fringing between gate and source electrodes. Following the analysis from Section 3.2 and 4.4, we obtain the corresponding values for average R_{on} and total C_{gs} (Table 6.1).

Figure 6-9 Output characteristics for different gate lengths.

Table 6-1 Different gate-length designs

L_g [μm]	$R_{on_average}$ [$\text{m}\Omega$]	C_{gs_tot} [pF]
1	176	317
2	187	343
3	203	354

Simulations of transistor designs that correspond to the values from Table 6.1, give the efficiency curves shown in Fig. 6.10. It can be seen that efficiency values in the low output power range (up to 10W) do not change significantly, while difference of approximately 4% is seen for P_{out} higher than 40W. Since both – on-resistance and input capacitance of the device were changed, simulations at 10MHz of switching frequency showed dominance in variation of conduction losses.

Figure 6-10 Estimated overall efficiency of a buck converter for different gate lengths at 10MHz.

Finally, the gate width of the transistor will be varied and its influence on the overall efficiency of a high frequency buck converter will be observed. As it can be seen from the analysis in Section 3.2 and 4.2.1, the variation of this

parameter directly influences the output characteristics of the device together with the part of C_{gd} due to vertical depletion under the field plate, $C_{gd,y}^I$. Since the method from [Bansal, 2006], that was used for calculation of fringing capacitance between gate-source and drain-source electrodes, assumes that gate width is much larger than the length of all three electrodes, a variation in the gate width will not affect these capacitances. From the same reason, conformal mapping technique together with image charge method, used for calculation of $C_{gd,x}^I$ and $C_{gd,x}^{II}$, will not be affected by the variation in the gate width. Different $C_{gd}(V_{ds})$ curves that correspond to the values from Table 6.2 are shown in Fig. 6.11, while the output characteristics for these three designs are presented in Fig. 6.12. Simulation results at 10MHz are shown in Fig. 6.13.

Table 6-2 Different gate-width designs

W_g [mm]	$R_{on_average}$ [m Ω]	C_{gdy} [pF]
60	293	48.15
120	187	92.2
180	131	144.45

Figure 6-11 Miller's capacitance for different gate widths.

Figure 6-12 Output characteristics for different gate lengths.

Figure 6-13 Simulated efficiency curves for different gate width at 10MHz

Observing simulated efficiency curves from Fig. 6.13, it can be seen that the design with the highest value for gate width provides the highest efficiency in the $P_{out} > 46W$ range, while penalizes the efficiency in the low range of the output power. These results were expected observing the values for R_{on} and C_{gd} from the Table 6.2. Comparing to this design, the shortest gate width provides maximum of 3% of efficiency increase in the low power range (up to 19W) and penalizes the efficiency for higher values of P_{out} due to significantly higher R_{on} .

6.2. The analysis of the breakdown voltage rating and its dependence on the field-plate design

As previously stated, the application of field-plate structure increases the breakdown voltage of a GaN HEMTs since it causes the second peak of the electric field in the channel (Fig. 6.14), thus reducing the maximum electric field.

Up to date, the most common methods for design and analysis of GaN HEMTs with one or multiple field-plate structure are the Finite Element Analysis (FEA) simulations [Kalmakar 2001]. Although FEA simulations are quite useful for field-plate design optimization for a given breakdown voltage, their drawback is necessary fitting of the design equations to the simulated data curves, which makes the optimization valid only for the simulated structure. Therefore, FEA cannot be used for the complete design optimization of the device. On the other hand, the physical models implemented into FEA simulation software are quite complex and time consuming. Therefore, they are not suitable for incorporation into iterative optimization tool, when optimizing the device design for a target application.

In order to optimize the design of a switching device for a given breakdown voltage, it is necessary to obtain an analytical model for the breakdown voltage dependence on the design parameters.

The breakdown mechanisms in AlGaIn/GaN HEMTs are quite complex and still investigated topic. Since the detailed breakdown analysis is out of the scope of this thesis, the typical breakdown scenario related to impact ionization occurrence will be considered. Since the impact ionization in each material occurs when the peak values of the electric field are close to the critical values (specific for each material), the breakdown voltage of the device will be defined **as drain-to-source voltage for which, the channel electric field comes close to the critical value for GaN material, 3MV/cm, with a predefined margin.**

6.2.1. Some general relations between the field-plate design and channel electric field

As it was shown in Section 4.2 when Miller's capacitance was modelled, the first peak of the electric field in the channel saturates when vertical depletion of the 2DEG ends. Furthermore, for V_{ds} values higher than V_{ds}^I , the second peak around the field-plate edge starts to increase. Equation (4.18) determined V_{ds}^I , from previously obtained model for vertical depletion. Observing (4.18) it can be seen that parameters which determine this voltage are Aluminum mole fraction of the AlGaIn layer, m , thickness of the AlGaIn layer, d_{AlGaIn} , permittivity and thickness of the oxide below the field-plate extension, ϵ_{ox} and t_{ox} . On the other hand, the length of the field-plate extension does not affect this value. If we choose Si_3N_4 for the insulator below the field-plate, the $V_{ds}^I(t_{ox})$ is shown in Fig. 6.16 for two compositions of m and d_{AlGaIn} . It can be seen that for both structures, as t_{ox} increases, the V_{ds}^I value increases, giving the higher value of the peak around the gate edge. The increase in this value decreases the peak of the electric field around the field-plate edge providing a higher breakdown voltage of the device. Consequently, with increase in t_{ox} , the gate-to-drain charge increases and efficiency of a converter drops (Fig. 6.4 and 6.5). Basically, this represents the major trade-off when designing devices that contain the field-plate: **higher t_{ox} gives a higher breakdown voltage but higher gate-to drain charge.**

As it was calculated in Section 4.2, V_{ds}^I for the analyzed structure with $m=24\%$ and $d_{AlGaIn}=24\text{nm}$ that employs Si_3N_4 with the thickness of $t_{ox}=80\text{nm}$ is equal to 11V. The corresponding COMSOL simulation of lateral electric field distribution was shown in Fig. 4.6.

In order to examine the precision of eq. (4.18) used for V_{ds}^I calculation, the same AlGaIn/GaN structure with 100nm thick SiO_2 used for the field-plate insulator material was simulated. The obtained distribution of the lateral electric field in the channel is shown in Fig. 6.17. Using the corresponding value for ϵ_{ox} of SiO_2 together with $t_{ox}=100\text{nm}$, eq. (4.18) gives $V_{ds}^I = 27\text{V}$. This value is in a good agreement with simulation results from Fig. 6.17, since the peak around the field-plate edge starts to increase for V_{ds} between 20 and 30V.

Figure 6-16 The dependence of V_{ds}^I on the oxide thickness for two compositions of m and d_{AlGaN}

Figure 6-17 COMSOL simulation of lateral electric field in the channel, for insulator SiO_2 with the thickness $t_{ox}=100$ nm

Regarding the length of the field-plate, the additional simulations of electric field in the channel were made. The simulated structure contained the same parameters as given in Table 3.2 and 3.3, except for the length of the field-plate extension. The simulations for values of L_{fp} equal to 1 and 2 μm are shown in Fig. 6.18 and 6.19.

Figure 6-18 COMSOL simulation of lateral electric field in the channel for $L_{FP}=1\mu\text{m}$

Figure 6-19 COMSOL simulation of lateral electric field in the channel, for $L_{FP}=2\mu\text{m}$

Observing the field distributions from Fig. 6.18 and 6.19, it can be seen that length of the field-plate does not influence V_{ds}^I since the peak values of channel electric field remain the same in both cases. The same conclusion is made analyzing the equation (4.18). The only influence of the field-plate length can be observed through the distance between the lobes of the field distribution. Since our analytical model for lateral extension of the depletion area around both edges was based on the assumption that two separate lobes exist, the length of the field-plate electrode will have the minimum value for which the proposed methodology can be applied. This will be important limitation in the design optimization.

Therefore, two conclusions about the design of the field-plate for a given breakdown voltage can be made:

1. The field-plate material and thickness determine the peak values of the electric field in the channel, therefore, determining the breakdown voltage of the device.
2. The field-plate length must have sufficiently high value in order to apply the approximation of two separate lobes of the electric field in the channel, for a target breakdown voltage of the device. Otherwise, the methodology from Section 4.2 cannot be used.

6.2.2. The analytical model for lateral component of the electric field in the channel

In order to determine the electric field in the channel and relate its peak values to the design of the field-plate, the methodology based on [Si, 2013] can be used.

The methodology from [Si, 2013] determined the analytical model for surface electric field and its peak value around the drain-side gate edge, analyzing the AlGaIn/GaN HEMT without the field-plate structure. The same conformal mapping transformations can be used for determination of a channel electric field of an AlGaIn/GaN HEMT that contains the field-plate extension of the gate electrode.

As it was previously mentioned, the simulations from [Karmalkar 2005] showed that electric field in the channel has the peak magnitudes almost the same as their x-component (Fig. 6.15). At the peak point, simulations showed $(E_y/E_x) < 25\%$. Since the resultant magnitude of the field, E , is given by:

$$E = \sqrt{E_x^2 + E_y^2} \approx E_x \left(1 + \frac{1}{2} \frac{E_y^2}{E_x^2}\right) \approx E_x \quad (6.1)$$

the contribution of E_y to E is <3%. Therefore, the channel electric field will be approximated by its lateral component, since the values of interest are the peak values of the field.

The approximation of the total electric field in the channel by its lateral component is very important in order to apply the boundary condition at AlGaIn/GaN interface:

$$E_x^{AlGaIn} = E_x^{GaN} \quad (6.2)$$

Since the methodology from Section 4.2.2 determined the electric potential inside AlGaIn layer, the peak of electric field at AlGaIn/GaN interface, E_x^{AlGaIn} , can be obtained. Therefore, using (6.2), the peak of the electric field in the GaN channel, E_x^{GaN} , can be modeled and calculated for each value of V_{ds} .

The analysis in Section 4.2.2 determined the potential inside AlGaIn layer as a function of geometrical parameters in w-plane, for both ranges of V_{ds} :

$$v_a(x'_0, y'_0) = \begin{cases} v_a^I(x'_0, y'_0), & V_{ds} \leq V_{ds}^I \\ v_a^{II}(x'_0, y'_0), & V_{ds} > V_{ds}^I \end{cases} \quad (6.3)$$

In (6.3), $v_a^I(x'_0, y'_0)$ and $v_a^{II}(x'_0, y'_0)$ are given by (4.29) and (4.30). These potentials correspond to the potential inside the depleted AlGaIn layer before and after vertical depletion of 2DEG is finished. Therefore, these potentials are related to increase of the electric field around the gate edge and the field-plate edge, respectively.

The mathematical models used for determination of the electric field peaks around the drain-side gate edge and the field-plate edge are identical to the ones used in Section 4.2.2 and are shown in Fig. 6.20 and 6.21. The point E presents the point where the peak E_x^{AlGaIn} takes place.

In order to calculate the peaks around the gate edge and field-plate edge, we give the first-order Taylor expansion of potential v_a near this point:

$$v_{aE} = v_a(x'_E, y'_E) + \left. \frac{\partial v_a}{\partial x'_0} \right|_{E(x'_E, y'_E)} x'_E + \left. \frac{\partial v_a}{\partial y'_0} \right|_{E(x'_E, y'_E)} y'_E \quad (6.4)$$

where x'_E and y'_E are the coordinates of the point E in the w-plane.

Figure 6-20 The depletion region around the drain-side gate edge with corresponding points of interest: z-plane (left) and w-plane (right)

From Fig 6.20 and 6.21 left, it can be seen that point E in the z-plane has the coordinates:

$$x_E = b^{I/II} - \xi \quad (6.5a)$$

$$y_E = d_{AlGaN} \quad (6.5b)$$

where $b^{I/II}$ is the extension of the depletion area around the gate edge/field-plate edge, while ξ is a small positive number representing the distance to gate edge/field-plate edge.

Figure 6-21 The depletion region around the field-plate edge with corresponding points of interest: z-plane (left) and w-plane (right)

The extension $b^{I/II}$ depends on the applied V_{ds} as it was derived in Section 4.2.2 and shown in the Fig. 4.11.

Observing the complex z -plane, the point E has the following representation:

$$z_E = (b^{I/II} - \xi) + id_{AlGaN} \quad (6.6)$$

In order to obtain x_E' and y_E' , it is necessary to map the point E from z -plane to w -plane, using the conformal mapping transformations from Fig. 6.22.

Figure 6-22 Procedures of conformal mapping technique: (a) original z -plane, (b) z_1 -plane, (c) z_2 plane and (d) final w -plane

Observing these transformations, we obtain:

$$w_E = \frac{1}{\pi} \cosh^{-1}(z_{2E}) \quad (6.7)$$

where z_{2E} is equal to:

$$z_{2E} = \frac{-2 \cosh\left(\frac{\pi(b^{I/II}-\xi)}{d_{AlGaN}}\right) - \cosh\left(\frac{\pi b^{I/II}}{d_{AlGaN}}\right) + 1}{\cosh\left(\frac{\pi b^{I/II}}{d_{AlGaN}}\right) + 1} \quad (6.8)$$

Having in mind that parameter c was defined as $c = \cosh(\pi b^{I/II}/d_{AlGaN})$ (Section 4.2.2), equation (6.7) can be written as:

$$w_E = \frac{1}{\pi} \cosh^{-1} \left(\frac{-2 \cosh\left(\frac{\pi(b^{I/II}-\xi)}{d_{AlGaN}}\right) - c + 1}{c + 1} \right) \quad (6.9)$$

In order to obtain real and imaginary part of w_E , x_E' and y_E' the following identity will be used:

$$\cosh^{-1}(x) = \ln(x + \sqrt{x^2 - 1}) \quad (6.10)$$

Equation (6.10) can be written as:

$$\cosh^{-1}(x) = \ln \left(-1 \left(-x - \sqrt{x^2 - 1} \right) \right), \quad (6.11)$$

giving the following :

$$\cosh^{-1}(x) = \ln(e^{i\pi}) + \ln \left(-x - \sqrt{x^2 - 1} \right) \quad (6.12)$$

Substitution of (6.12) into (6.7) gives:

$$w_E = i + \frac{1}{\pi} \ln \left(-z_{2E} - \sqrt{z_{2E}^2 - 1} \right) \quad (6.13)$$

Therefore,

$$y_E' = 1 \quad (6.14)$$

while substitution of (6.8) into (6.13) gives:

$$x_E' = \frac{1}{\pi} \ln \left(\frac{3c - 1 - \frac{2\pi\xi}{d_{AlGaN}}\sqrt{c^2 - 1} - 2 \sqrt{2c^2 - 2c + \frac{\pi\xi}{d_{AlGaN}}\sqrt{c^2 - 1}(1 - 3c) + (c^2 - 1)\frac{\pi^2\xi^2}{d_{AlGaN}^2}}}{c + 1} \right) \quad (6.15)$$

From (6.14) and (6.15) it can be seen that mapped coordinates of the point E in the channel are a function of c (which depends on V_{ds}) and ξ .

Since the coordinates x_E' and y_E' are determined as a function of V_{ds} , we will solve (6.4) in order to obtain the potential v_a around the point E and, therefore, the electric field near this point.

The first term in (6.4) can be calculated directly from (6.3), (4.29) and (4.30), using (6.14) and (6.15) for y_E' and x_E' , respectively:

$$v_a(x_E', 1) = \begin{cases} \int_0^{+\infty} \frac{qn'_{S0}(x')}{2\pi\epsilon_a} \ln\left(\frac{(x'-x_E')^2+4}{(x'-x_E')^2}\right) dx', & V_{ds} \leq V_{ds}^I \\ \int_0^{+\infty} \frac{qn'_{S0}(x')}{2\pi\epsilon_a} \ln\left(\frac{(x'-x_E')^2+4}{(x'-x_E')^2}\right) dx', & V_{ds} > V_{ds}^I \end{cases} \quad (6.16)$$

The second term in (6.4) can be obtained by calculating a derivative of (6.3) with respect to the x_0' :

$$\frac{\partial v_a(x_0', y_0')}{\partial x_0'} = \begin{cases} \int_0^{+\infty} \frac{qn'_{S0}(x')}{\pi\epsilon_a} \frac{(x'-x_0')}{(x'-x_0')^2+(1+y_0')^2} \frac{4y_0'}{(x'-x_0')^2+(1-y_0')^2} dx', & V_{ds} \leq V_{ds}^I \\ \int_0^{+\infty} \frac{qn'_{S0}(x')}{\pi\epsilon_a} \frac{(x'-x_0')}{(x'-x_0')^2+(1+y_0')^2} \frac{4y_0'}{(x'-x_0')^2+(1-y_0')^2} dx', & V_{ds} > V_{ds}^I \end{cases} \quad (6.17)$$

Equation (6.17) around the point E($x_E', 1$) becomes:

$$\left. \frac{\partial v_a(x_0', y_0')}{\partial x_0'} \right|_{E(x_E', 1)} = \begin{cases} \int_0^{+\infty} \frac{4qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{((x'-x_E')^2+4)(x'-x_E')} dx', & V_{ds} \leq V_{ds}^I \\ \int_0^{+\infty} \frac{4qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{((x'-x_E')^2+4)(x'-x_E')} dx', & V_{ds} > V_{ds}^I \end{cases} \quad (6.18)$$

Therefore, the second term of (6.4) is equal to:

$$\left. \frac{\partial v_a(x_0', y_0')}{\partial x_0'} \right|_{x_E'} = \begin{cases} \left(\int_0^{+\infty} \frac{4qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{((x'-x_E')^2+4)(x'-x_E')} dx' \right) x_E', & V_{ds} \leq V_{ds}^I \\ \left(\int_0^{+\infty} \frac{4qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{((x'-x_E')^2+4)(x'-x_E')} dx' \right) x_E', & V_{ds} > V_{ds}^I \end{cases} \quad (6.19)$$

Similarly to the calculation of the second term, the third term in (6.4) can be obtained by calculating a derivative of (6.3) with respect to the y_0' . Around the point E($x_E', 1$) it is equal to:

$$\left. \frac{\partial v_a(x_0', y_0')}{\partial y_0'} \right|_{E(x_E', 1)} = \begin{cases} \int_0^{+\infty} \frac{qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{(x'-x_E')^2+4} dx' - V_{gs}^*, & V_{ds} \leq V_{ds}^I \\ \int_0^{+\infty} \frac{qn'_{S0}(x')}{\pi\epsilon_a} \frac{1}{(x'-x_E')^2+4} dx' - (V_{gs}^* - V_{ox}), & V_{ds} > V_{ds}^I \end{cases} \quad (6.20)$$

which gives the third term in (6.4):

$$\left. \frac{\partial v_a(x'_0, y'_0)}{\partial y'_0} \right|_{E(x'_E, 1)} y'_E = \begin{cases} \left(\int_0^{+\infty} \frac{qn'_{s0}(x')}{\pi \epsilon_a} \frac{1}{(x' - x'_E)^2 + 4} dx' - V_{gs}^* \right) y'_E, V_{ds} \leq V_{ds}^I \\ \left(\int_0^{+\infty} \frac{qn'_{s0}(x')}{\pi \epsilon_a} \frac{1}{(x' - x'_E)^2 + 4} dx' - (V_{gs}^* - V_{ox}) \right) y'_E, V_{ds} > V_{ds}^I \end{cases} \quad (6.21)$$

From (6.21) we conclude that the third term in (6.4) has different forms in Range I and II of V_{ds} , i.e. around the gate edge and the field-plate edge. Nevertheless, the electric field calculated as the derivative of (6.4) with respect to the ξ , will be the same in both Ranges of V_{ds} .

Substituting (6.21), (6.19) and (6.16) into (6.4), the first-order Taylor expansion of potential v_a around the point $E(x'_E, 1)$ is obtained. Numerical calculation of indefinite integrals finally gives v_{aE} as a function of $b^{I/II}(V_{ds})$ and ξ .

The lateral component of the electric field near the point $E(b^{I/II-\xi}, d_{AlGaIn-})$, $E_{xE}^{AlGaIn-}$, can be calculated as:

$$E_{xE}^{AlGaIn-} = -\frac{dv_{aE}(x_E)}{dx_E} = \frac{dv_a(x_E)}{d\xi} \quad (6.22)$$

since $x_E = b^{I/II-\xi}$.

Finally, by calculation of derivative (6.22), the electric field at $y = d_{AlGaIn-}$ is obtained as a function of $b^{I/II}(V_{ds})$ and the parameter ξ . For a particular V_{ds} voltage, the value for b is read from previously obtained dependence shown in Fig. 4.11. Since ξ represents a small distance from the gate edge (which can be arbitrarily chosen), the value of 1nm will be used for the calculation of the electric field peak value. Furthermore, if the goal is to obtain the complete distribution of the field in the channel, the value for ξ can be increased and, for each value of ξ , the corresponding value of the field can be calculated. In our analysis, only the peak value of the field is of interest, since we are modeling the breakdown voltage of the device.

The peak values of the electric field in the channel that correspond to V_{ds} from 10 to 60V, obtained using the proposed analytical approach, are shown in Fig. 6.23. In order to make comparison with simulation results, the electric field distributions obtained using COMSOL are also shown in the same figure. Observing simulated and analytically obtained peak values, it can be seen that highest error of 43% exists for $V_{ds}=20V$. This was expected, since for the value of 20V we are just entering the Range II of V_{ds} where we consider to have only a lateral depletion. Basically, we will have the highest imprecision of the proposed model exactly around the V_{ds}^I since this is the value for which vertical depletion ends and only lateral depletion remains, according to our simplification of the 2D problem into two 1D directions. As we move more deeply in the Range II (towards higher and higher values of V_{ds}) or more deeply in the Range I

(towards lower values of V_{ds}), the precision of the model will be higher since the correlation between the vertical and lateral depletion significantly decreases. This was confirmed through the comparison between the simulation results and the analytical solution, shown in Fig. 6.23. Since the goal of this analysis is to make the analytical relation between the breakdown voltage of the device and the field-plate design, we can say that precision of the proposed methodology is sufficient enough for V_{ds} around the maximum value. From Fig. 6.23, it can be seen that for $V_{ds}=60V$, this error is 2%. Although the breakdown voltage of the analyzed device is around 100V, COMSOL simulation for this voltage was not feasible. Therefore, the comparison between the analytical and simulated peak of the electric field for V_{ds} equal to the breakdown voltage is not given. Analytically obtained value of the electric field peak for $V_{ds}=100V$ is 1.98 MV/cm. Since the critical electric field for GaN material is around 3MV/cm, the value of 2MV/cm will be used for the maximum allowable electric field value in further design optimization process. This will provide a sufficient safety margin and will conform to the design guidelines of the existing device.

Figure 6-23 COMSOL simulation of lateral electric Vs analytically obtained values

6.3. The optimization algorithm

6.3.1. The optimization of a field-plate design

As it was shown in the previous sections, the design of a field-plate dominantly influences Miller's capacitance of a device and determines the breakdown voltage. Since the analytical models for peaks of the electric field in the channel together with the model for $C_{gd}(V_{ds})$ were obtained, the optimization of a field-plate design can be done separately from the other parameters of the device, by minimization of gate-to-drain charge.

As it was concluded in Section 6.2.1, the thickness and material used for the insulator below the field-plate extension, determine the peak values of the electric field in the channel. Since decrease in t_{ox} decreases total gate-to-drain charge (Fig. 6.4), minimum oxide thickness will be chosen, for a target breakdown voltage. The breakdown will be defined for the conditions when peak of the electric field in the channel (around the gate edge or the field-plate edge) reaches the value of 2MV/cm.

In order to avoid the breakdown in the insulator material, it is necessary determine the minimum insulator thickness that can be reached. Since each material has its own dielectric constant, the obtained minimum values for insulator thickness will be different for different materials used below the field-plate. Therefore, **the material will be chosen in order to have lower $Q_{gd,y}^I$ (gate-to-drain charge caused by vertical depletion of the 2DEG below the field-plate) for conditions when electric field in the material is maximum.** This analysis can be done separately from further optimization of t_{ox} and L_{fp} values and it will be presented in the following section.

6.3.1.1. Determination of a field-plate material

Speaking of materials used for the insulator below the field-plate extension in AlGaIn/GaN HEMTs, SiO₂ and Si₃N₄ are the most common ones. Both materials have critical electric field around 11MV/cm, but different dielectric constants, which implies different values for V_{ds}^I and $C_{gd,y}^I$ for the same insulator thickness, according to the equations (4.18) and (4.20). Therefore, the first step in the determination of the optimum field-plate design will be a determination of the insulator material which provides lower $Q_{gd,y}^I$ when the insulator thickness is

set to the minimum value t_{ox_min} in order to avoid the breakdown in the insulator material.

The analysis that was performed in Section 4.2.1 when vertical depletion of the 2DEG under the field-plate was modeled, gives the following two conditions for oxide thickness, t_{ox} .

The first condition can be presented as:

$$n_{2DEG,FP}(V_{ds} = 0) > 0 \quad (6.23)$$

This condition ensures that when the devices is in the OFF state and applied V_{ds} is equal to 0V, the thickness of the oxide is high enough to provide the existence of the undepleted 2DEG below the field-plate. From (4.17) it is obtained:

$$n_{PZ} - \frac{(-V_{gs}^* + \varphi_{mi} - \Delta E_C)}{q(d_{AlGaN} + \frac{\epsilon_a}{\epsilon_{ox}} t_{ox})} > 0 \quad (6.24)$$

Therefore, **the first condition for t_{ox}** becomes:

$$t_{ox} > \frac{\epsilon_{ox}}{\sigma_{PZ}} (-V_{gs}^* + \varphi_{mi} - \Delta E_C) - \frac{\epsilon_{ox}}{\epsilon_a} d_{AlGaN} \quad (6.25)$$

In the previous equation, σ_{PZ} , φ_{mi} and ΔE_C present the polarization charge sheet density, gate-insulator barrier height and quantum well height in the device, while V_{gs}^* presents the gate-source voltage necessary to keep the device in the OFF state. As shown in Section 3.1, σ_{PZ} and ΔE_C are only a function of Aluminum mole fraction, m , while V_{th} and therefore V_{gs}^* is a function of m and AlGaN thickness, d_{AlGaN} (Fig. 6.2, eq. 3.19). Therefore, observing the parameters from previous equation, it can be seen that if the heterostructure with predefined values for m and d_{AlGaN} is chosen, the dielectric constant ϵ_{ox} dictates the minimum value for t_{ox} .

The second condition for minimum oxide thickness is related to the breakdown in the oxide, when V_{ds} is equal to maximum voltage. From (4.5), (4.6) and (4.7), we obtain the following equation for the electric field in the insulator:

$$E_{ox} = \frac{\epsilon_a(V_{ds} - V_{gs}^* + \varphi_{mi} - \Delta E_C)}{\epsilon_{ox}(d_{AlGaN} + \frac{\epsilon_a}{\epsilon_{ox}} t_{ox})} \quad (6.26)$$

Since the value for critical electric field is equal to 11MV/cm for both materials, we can set the condition for t_{ox_min} that will provide $E_{ox}=10\text{MV/cm}$ for

the target voltage rating $V_{ds}=40V$. Using these values in (6.26), we obtain **the second condition for the insulator thickness**:

$$t_{ox} > \frac{(40V - V_{gs}^* + \phi_{mi} - \Delta E_C)}{10MV/cm} - d_{AlGaN} \frac{\epsilon_{ox}}{\epsilon_a} \quad (6.27)$$

In order to demonstrate how the insulator material selection can be performed, we will observe the example of heterojunction with $m=35\%$ and $d_{AlGaN}=20nm$. These values of Aluminum mole fraction together with AlGaN layer thickness give $\sigma_{PZ(m=35\%)}$ and $\Delta E_{C(m=35\%)}$ equal to $0.0154C/m^2$ and $0.504V$ while the needed value for V_{gs}^* is equal to $-4V$ (Fig. 6.1). As it was previously mentioned, common insulator materials are SiO_2 and Si_3N_4 , with dielectric constants equal to:

$$\epsilon_{ox}^{SiO_2} = 3.9 \quad (6.28a)$$

$$\epsilon_{ox}^{Si_3N_4} = 7.5 \quad (6.28b)$$

Substituting the values for $\sigma_{PZ(m=35\%)}$ and $\Delta E_{C(m=35\%)}$ together with (6.28a, b) into (6.25), we obtain **the first condition for t_{ox}** for both materials:

$$t_{ox}^{SiO_2} > 11.1nm \quad (6.29a)$$

$$t_{ox}^{Si_3N_4} > 21.3nm \quad (6.29b)$$

while substituting the same values into (6.27), we obtain the second condition:

$$t_{ox}^{SiO_2} > 38.1nm \quad (6.30a)$$

$$t_{ox}^{Si_3N_4} > 30.4nm \quad (6.30b)$$

Observing the obtained values from (6.29a, 6.30a) and (6.29b, 6.30b) we conclude that:

$$t_{ox_min}^{SiO_2} = 38.1nm \quad (6.31a)$$

$$t_{ox_min}^{Si_3N_4} = 30.4nm \quad (6.31b)$$

In order to have round numbers for oxide thickness (since this is preferable from the technological point of view), the values of $t_{ox_min}^{SiO_2}=40nm$ and $t_{ox_min}^{Si_3N_4}=35nm$ will be used in the following calculations.

Now, when minimum oxide thickness for each material has been determined, the equations (4.18) and (4.20) can be used for calculation of V_{ds}^I and $C_{gd,y}^I/(W_g L_{fp})$. The obtained values for V_{ds}^I are:

$$V_{ds}^{I, SiO_2} = 9.66V \quad (6.32a)$$

$$V_{ds}^{I, Si_3N_4} = 2.38V \quad (6.32b)$$

while the corresponding curves for scaled $C_{gd,y}^I/(W_g L_{fp})$ are shown in Fig.6.24. Since the vertical depletion is the dominant source of Miller's capacitance, the curves from Fig. 6.24 will be used for estimation of total gate-to-drain charge for both materials. By calculating the surface below each of the curves, it is obtained:

$$Q_{gd}^{SiO_2}/(L_{fp} W_g) = 6.897 \text{ mC/m}^2 \quad (6.33a)$$

$$Q_{gd}^{Si_3N_4}/(L_{fp} W_g) = 3.12 \text{ mC/m}^2 \quad (6.33b)$$

Observing the values given by (6.33 a, b) it is concluded that Si_3N_4 provides lower gate-to-drain charge. Therefore, Si_3N_4 will be used for the insulator material below the field-plate.

Figure 6-24 Miller's capacitance due to vertical depletion of the 2DEG below the field-plate: SiO_2 (blue) and Si_3N_4 (red)

6.3.1.2. The algorithm of a field-plate design optimization for a chosen oxide material

After the material for the insulator below the field-plate is chosen, the optimization of a field-plate design in terms of thickness and length can be performed.

Speaking of insulator thickness value, it was shown that this value influences only Miller's capacitance of the device (Section 6.1). As it can be seen from the curves shown in Fig. 6.4, lower t_{ox} causes lower gate-to-drain charge and higher efficiency of a high-frequency buck converter (Fig. 6.5). Therefore, this value needs to be minimized having in mind the boundary conditions from the previous section.

Therefore, the optimization algorithm starts from t_{ox_min} obtained in the previous section and calculates the peaks of the electric field in the channel around the gate edge and the field-plate edge, for V_{ds} being changed from 0 to V_{ds_max} . If we comply with the condition that peaks of the electric field are lower than the critical value set to 2MV/cm for entire range of V_{ds} , the starting t_{ox_min} can be chosen for the final insulator thickness. If not, the thickness should be increased and the whole procedure should be repeated.

Speaking of field-plate length value, it was demonstrated that lower L_{fp} also decreases gate-to-drain charge (Fig. 6.6) but slightly increases drain-to-source charge (Fig. 6.7). Nevertheless, the simulations of a high-frequency buck converter showed that change in Q_{gd} dominantly influences the overall efficiency of a converter (Fig. 6.8). Therefore, L_{fp} should be minimized.

When analyzing the boundary condition for minimization of the field-plate length, it can be concluded that L_{fp} must be sufficiently long in order to have two separate lobes of the electric field, since the proposed modeling methodology is based on this assumption. Previously obtained values for t_{ox} and ϵ_{ox} fixed the value for V_{ds}^I (the drain-source voltage that defines the end of Range I). Therefore, the lateral extension of the depletion area around the gate edge for $V_{ds}=V_{ds}^I$, $b_1=b(V_{ds}^I)$, (Fig. 6.25) can be calculated, using the curve shown in Fig 4.11. For drain-source voltages higher than V_{ds}^I , this lateral extension around the gate-edge remains unchanged while the extension around the field-plate edge starts to increase. As it was explained in Section 4.2.2., for $V_{ds}>V_{ds}^I$, the total value of the lateral extension for a particular V_{ds} voltage, $b_{tot}(V_{ds})$, can be read from Fig. 4.11. Since this total extension includes b_1 together with the extension around the field-plate edge, $b^{II}(V_{ds})$, the dependence $b^{II}(V_{ds})$ can be obtained as

$b^{II}(V_{ds})=b_{tot}(V_{ds})-b_1$. If b_2 is equal to $b^{II}(V_{ds_max})$, we can approximately calculate $L_{fp,min}$ as (Fig. 6.25):

$$L_{fp,min} = b_1 + b_2 \quad (6.34)$$

where

$$b_1 = b^I(V_{ds}^I) \quad (6.35a)$$

$$b_2 = b^{II}(V_{ds,max}) \quad (6.35b)$$

Figure 6-25 The lateral component of the electric field in the channel for $V_{ds} = V_{ds,max}$: determination of $L_{fp,min}$ and $L_{gd,min}$

Observing the field distribution from Fig. 6.25, it can be seen that length of the field-plate is defined by the portion of the lateral extension of the depletion area, contained in the **inner lobes of the electric field distribution**. These extensions are lower than the values b_1 and b_2 . Nevertheless, by taking the complete values b_1 and b_2 , in the calculation of the field-plate length, we will obtain more simple solution with additional safety margin. Finally, in order to obtain the field-plate length which is suitable for technological manufacturing, we will add Δ_1 (Fig. 6.26).

Finally, the gate-drain length should be minimized as well, in order to minimize the drain drift resistance of the device. This value can be obtained as a sum of previously calculated $L_{fp,min}$ and the complete extension of the electric field distribution, b_2 , analogically to the calculation of $L_{fp,min}$ (Fig. 6.25). Finally, Δ_2 will be added in order to obtain a round number for $L_{gd,min}$, suitable for technological manufacturing of the device.

The complete algorithm of the field-plate design optimization together with determination of the optimum $L_{gd,min}$ is shown in Fig. 6.26. As we already explained, we start the optimization process by choosing the material for the insulator below the field-plate that will provide minimum gate-to drain charge. Using this ϵ_{ox} together with the minimum thickness obtained in the previous section, we calculate V_{ds}^I . If the peak values of the electric field around the gate edge (for $V_{ds} < V_{ds}^I$) are lower than $E_{crit}=2\text{MV/cm}$ (in our approximation), then we continue the analysis for $V_{ds} > V_{ds}^I$. If not, we have to choose the material again, since the increase in t_{ox} will only increase V_{ds}^I and therefore, will increase the peak value of the field around the gate edge. When we enter the range $V_{ds} > V_{ds}^I$, we repeat the same analysis. Nevertheless, if we have $E_{peak2} > E_{crit}$ for $V_{ds} > V_{ds}^I$, we can increase t_{ox} . In this way, we will increase V_{ds}^I and the peak of the electric field around the gate edge, therefore decreasing the peak value around the field-plate edge.

6.3.2. Optimization of remaining parameters

The remaining parameters that will be optimized are: Aluminum mole fraction, m , thickness of AlGa_N layer, d_{AlGaN} , the length of the gate electrode, L_g , gate-to-source distance, L_{gs} and finally, the width of the gate electrode, W_g .

Among these parameters, m and d_{AlGaN} , depend on each other in order to have AlGa_N layer that will not provide many dislocations when grown on GaN buffer [Ambacher 1999, Ambacher 2002]. The boundaries for these parameters will be chosen according to the literature [Ambacher 2002], in order to comply with basic technological requirements for manufacturing high-quality AlGa_N/GaN heterojunction. Using the analysis from [Ambacher 2002], it was concluded that increase in m demands decrease in d_{AlGaN} in order to avoid strain relaxation in Al_mGa_(1-m)N layer (Fig.6.1).

Section 6.1 showed **how variation in each of these parameters influences the overall efficiency of a high-frequency buck converter**. If m is increased while decreasing d_{AlGaN} (according to the Fig. 6.1), the sheet density of the 2DEG in the channel is increased for the same gate-source voltage (Fig. 6.2). At the same time, the threshold voltage of the device shifts towards more negative values. Since higher 2DEG density for the same V_{gs} values means lower source and drain drift resistance, the increase in m is desirable from the point of view of conduction losses. While on-resistance is being decreased with higher m and correspondingly lower d_{AlGaN} , capacitive characteristics remain the same.

Therefore, increase of m and decrease of d_{AlGaN} is desirable in order to minimize total losses in the converter.

Figure 6-26 The algorithm of the field-plate design optimization

Furthermore, decrease in L_g demonstrated decrease in on-resistance and gate-to-source charge, but increase in drain-to-source charge. The simulations of a high-frequency buck converter at 10MHz of switching frequency showed that lower values for L_g give higher efficiency of the converter i.e that gate length should be decreased.

Moreover, decrease in L_{gs} provides lower source drift resistance and therefore lower on-resistance, lower C_{ds} due to shorter extension of the undepleted 2DEG in the source drift region (Fig. 4.16) and lower C_{gs} from the same reason (Fig. 4.18). Therefore, minimum possible value for L_{gs} should be chosen. Due to the scaling issues, L_{gs} will be chosen to be equal to the value of L_g [Piedra 2012].

6.3.2.1. Gate width optimization and current rating of a switching device

The width of the gate electrode, W_g , is the parameter that defines the current rating of the device. Therefore, in order to determine the boundary for this parameter, additional analysis should be performed.

As demonstrated in Section 6.1, the decrease in gate width decreases Miller's charge but increases the on-resistance of the device. The converter simulations at 10MHz showed that in the low range of the output power, lower values of W_g provide higher efficiency of the converter. This leads to a conclusion that at frequencies higher than 10MHz, in the low range of P_{out} , variation in Miller's charge will dominantly influence power losses in the converter. Since low-power and high switching frequency are the target operating conditions of the converter, it is concluded that W_g should be decreased. Since W_g determines the current rating of the device, this value should be decreased to the boundary which ensures that device is able to turn-on/off properly. From the point of view of current rating, this means that device needs to take over full load current during the turn-on/off transition.

Observing the operating conditions of the Envelope Tracking buck converter from Chapter 5, it can be seen that for duty cycle being changed from 0-100%, the output voltage changes from 0 to 24V. Since RFPA is emulated by a 6Ω resistor, the load current changes from 0 to 4A. In order to set the current rating of our optimized device with an additional safety margin, 6A will be the chosen current rating of our optimized device.

In order to properly turn-on/off the high-side switch in a buck converter, it is necessary to provide the ability of taking over the full load current when gate-source voltage becomes equal to the plateau voltage. The plateau voltage can be approximately calculated as [Fairchild, 2014]:

$$V_{gs,plateau} = V_{th} + \frac{I_{out}}{g_m} \quad (6.36)$$

where V_{th} is the threshold voltage of the device, I_{out} is the load current and g_m is the transconductance of the device in the V_{gs} range around the threshold. The waveforms of $V_{gs}(t)$, $V_{ds}(t)$ and $I_d(t)$ during the hard-switching turn-on are shown in Fig. 6.27.

As it was previously shown, the Aluminum mole fraction, m and thickness of AlGaIn layer, d_{AlGaIn} determine the $n_{2DEG}(V_{gs})$ and therefore, the threshold voltage of the device, V_{th} . In order to minimize the on-resistance of the device, m was maximized to the technological boundary of 35%, while d_{AlGaIn} was correspondingly decreased to 20nm in order to avoid formation of defects (Fig. 6.1). Observing $n_{2DEG}(V_{gs})$ from Fig. 6.2, it can be seen that V_{th} of our optimized device is -2.8V.

Figure 6-27 The turn-on waveforms of a hard-switching device

In order to obtain minimum possible W_g that provides 6A of current rating when $V_{gs}=V_{gs,plateau}$, it is necessary to have corresponding $I_d(V_{gs}, V_{ds})$ output characteristics that provide 6A of drain current for operating point $V_{gs}=V_{gs,plateau}$ and $V_{ds}=24V$ (V_{ds} is equal to 24V since that is the input voltage of the converter). This can be determined from the I - V model from Chapter 3.

Applying this methodology, the obtained value for $W_{g,min}$ is 60mm. The obtained $I_d(V_{gs})$ is shown in Fig. 6.28. Using this curve, transconductance for V_{gs} slightly higher than the threshold is estimated to 15.4S.

Figure 6-28 The $I_d(V_{gs})$ dependence, for $V_{ds}=24V$

Using this value in (6.36), the obtained plateau value, $V_{gs,plateau}$ is -2.4V. The obtained $I_d(V_{gs}, V_{ds})$ characteristics of the optimized design are shown in Fig. 6.29, especially emphasizing the curve for $V_{gs}=V_{gs,plateau}=-2.4V$. It can be seen that drain current value for $V_{gs}=V_{gs,plateau}$ and $V_{ds}=24V$, corresponds to previously set value for current rating of the device (6A).

Figure 6-29 The $I_d(V_{gs}, V_{ds})$ characteristics for optimized design of the device: the turn-on process of the device

6.3.2.2. The optimization of the remaining parameters – the summary

From the presented analysis, the direction of each parameter variation that leads to minimization of the power losses in the buck converter can be obtained. This is summarized in Fig. 6.30.

Since the total loss breakdown from the previous section, showed that losses due to output capacitance of a free-wheeling diode present a significant portion of the total losses at 20MHz of switching frequency, the loss minimization should be performed in configuration of a synchronous buck converter. Furthermore, due to significantly higher values for parasitic inductances, the initial TO-220 package will be replaced by DirectFET package of the device. Therefore, the parasitic source, drain and gate inductances will be

reduced from $L_s^{\text{TO-220}} = 6\text{nH}$, $L_g^{\text{TO-220}} = 1\text{nH}$ and $L_d^{\text{TO-220}}=1\text{nH}$ to $L_s^{\text{DirectFET}} = 0.09\text{nH}$, $L_g^{\text{DirectFET}} = 0.09\text{nH}$ and $L_d^{\text{DirectFET}}=0.44\text{nH}$ [Ji 2013]. The DirectFET package of a commercially available MOSFET from IR is shown in Fig. 6.31.

Figure 6-30 The summary of each parameter influence on the total efficiency of the converter

Figure 6-31 The DirectFET package of a commercially available Si MOSFET

6.4. The optimized HEMT design with the field-plate structure and obtained efficiency curves

Applying previously presented algorithms, the design of a GaN HEMT with a field-plate structure has been optimized for application in high-frequency buck converter, presented in detail in Chapter 5.

As it was explained in the previous section, the design of the field-plate extension of the gate electrode was optimized independently from the other parameters, by minimization of gate-to-drain charge for a given breakdown voltage of 40V.

By following the block diagram from Fig. 6.26, and using $E_{crit}=2\text{MV/cm}$ (as explained in Section 6.2.2), the parameters from Table 6.3 and 6.4 for optimized field-plate structure are obtained.

These parameters provide $C_{gd}(V_{ds})$ shown in Fig. 6.32. The total gate-to-drain charge was decreased from to 2.3675nC in the initial design of the device to 0.4502nC in the optimized design of the device.

Table 6-3 Optimized Field-Plate design: vertical depletion parameters

$V_{ds,max}$ [V]	Material	$t_{ox,min}$ [nm]	V_{ds}^I [V]	E_{peak1} [MV/cm]	E_{peak2} [MV/cm]
40	Si ₃ N ₄	25	1.3	0.6	1.52

Table 6-4 Optimized Field-Plate design: lateral depletion parameters

b_1 [nm]	b_2 [nm]	Δ_1 [nm]	Δ_2 [nm]	$L_{fp,min}$ [um]	$L_{gd,min}$ [nm]
35.5	128.3	86.2	121.7	0.25	0.5

When the field-plate structure was optimized independently on the rest of the parameters, the optimization of the device design was continued using the conclusions from Fig. 6.30. As previously explained, Aluminum mole fraction, m , together with AlGa_N thickness, d_{AlGaN} were set to the technological boundaries that provide an AlGa_N/Ga_N heterojunction of a good quality [Ambacher 2002]. The chosen values for m and d_{AlGaN} are 35% and 20nm, respectively.

Figure 6-32 Miller's capacitance for optimized design in comparison to the nominal design

Furthermore, gate length L_g was minimized according to the previous analysis. The boundary for the minimization process was 250nm, in order to avoid short channel effects that were not taken into consideration in the I-V model [Fjeldly book 1997]. Additionally, gate-source distance was selected to be equal to the gate length due to scaling demands [Piedra 2012].

Finally, the gate width, W_g , was minimized in order to minimize power losses in the converter but keeping the necessary current rating of the device. The minimum gate width that provided the target current rating of 6A was $W_g=60\mu m$ which is 50% lower than the value in the initial design. In order not to change the 1mm width of one finger, the number of fingers was set to 60 in the optimized design. The final values for the parameters of the optimized (new) design in comparison to the parameters of the initial (old) design are given in Table 6.5 and 6.6. The output and input capacitances for both designs are shown in Fig. 6.33 and 6.34, respectively.

Table 6-5 General and technological parameters of the optimized (new) and nominal (old) design

	m [%]	d_{AlGaN} [nm]	V_{th} [V]	Field plate	Number of fingers
NOMINAL(OLD) DESIGN	24	24	-2	Si₃N₄	120
OPTIMIZED (NEW) DESIGN	32	32	-4.5	Si₃N₄	60

Table 6-6 Geometrical parameters and on-resistance of the optimized (new) and nominal (old) design

	L_g [μm]	L_{sg} [μm]	L_{gd} [μm]	L_{fp} [μm]	t_{ox} [nm]	W_g [mm]	R_{on_av} [mΩ]
NOMINAL(OLD) DESIGN	2	2	4	1.5	80	120	189
OPTIMIZED (NEW) DESIGN	0.25	0.25	0.5	0.25	25	60	83
THE DIFFERENCE [%]	87.5	87.5	87.5	83.3	75	50	56

Figure 6-33 Output capacitance for optimized design in comparison to the nominal design

Figure 6-34 Input capacitance for optimized design in comparison to the nominal design

Since the power loss model was verified in a configuration of a simple buck converter, the first simulations that compared the performance of the optimized to the nominal device design were performed in this configuration, using old and new device design in a DirectFET package. The freewheeling diode used in the simulations was the diode used in the experimental verification in the previous section. The comparison of the simulated efficiency curves at 20MHz of switching frequency is shown in Fig. 6.35, while the total losses breakdown for the output power equal to 23W is shown in Fig. 6.36.

Figure 6-35 The overall efficiency of a simple buck converter at 20MHz, using *optimized (new)* and *initial (old)* design of the device

Observing the efficiency curves from Fig. 6.35, it can be seen that optimization of the device design (together with the new package) provided only around 5% of efficiency increase in the complete range of the output power. This was expected due to high output capacitance of the freewheeling diode (equal to 0.6nF) which caused high diode losses at 20MHz of switching frequency. From the total loss breakdown for 23W of the output power, it can be seen that in the converter with the initial device design, diode loss present 40% of the total losses.

Figure 6-36 The total losses breakdown at 20MHz and 23W of the output power – comparison of the optimized (new) and initial (old) design in the simple buck configuration

If the topology is changed into synchronous buck converter and the same simulations are performed, the efficiency curves shown in Fig.6.37 are obtained.

Figure 6-37 The overall efficiency of a synchronous buck converter at 20MHz, using *optimized (new)* and *initial (old)* design of the device

It can be seen that the efficiency of the converter was increased more than 20% in the low range of the output power. Observing the total loss breakdown shown in Fig. 6.38, it can be seen that for $P_{out}=20W$, total losses are decreased for 80% in synchronous buck configuration. The switching losses that presented 81% of the total losses were decreased for 76% due to highly improved capacitance characteristics of the device.

Figure 6-38 The total losses breakdown at 20MHz and 20W of the output power – comparison of the optimized (new) and initial (old) design in the synchronous buck configuration

Since the target voltage rating of the optimized device is 40V which is substantially lower than the initial voltage rating of 100V, the question that can be raised is if the field-plate structure is needed at all. In order to give an answer to this question, the additional simulations were made using the optimized structure without the field-plate extension of the gate electrode.

6.5. The optimized design without the field-plate structure and simulated efficiency curves

As it can be concluded from previously presented physics-based model of the device, the absence of field-plate structure will decrease the gate-to-drain charge and increase drain-to-source charge. On the other hand, the I-V characteristics and the gate-to-source charge will not be influenced.

In order to see if the same optimized design but without the field-plate extension can be used for our application, it is necessary to calculate the peak of the electric field around the gate edge for $V_{ds}=40V$. This was done using the methodology presented in Section 6.2.2. The obtained value is equal to 1.910942 MV/cm while the total extension of the depletion area that corresponds to this peak value is $b_1=163.5nm$. Observing the value of 2MV/cm that was set to the critical value for the peak of the electric field, we can say that the same optimized design without the field-plate extension can be used in our topology.

Applying the capacitance model from Section 4.2, 4.3 and 4.4, the following dependencies for $C_{gd}(V_{ds})$, $C_{ds}(V_{ds})$, $C_{oss}(V_{ds})$ and $C_{iss}(V_{ds})$ are obtained. The gate-to-drain charge is decreased due to the absence of vertical depletion below the field-plate which causes lower value of Miller's capacitance in the Range I of V_{ds} (Fig. 6.39).

Figure 6-39 Miller's capacitance for optimized design with and without the field-plate structure

Figure 6-40 Drain-to-source capacitance for optimized design with and without the field-plate structure

Figure 6-41 C_{oss} for optimized design with and without the field-plate structure

Figure 6-42 Input capacitance for optimized design with and without the field-plate structure

When optimized design without the field-plate structure was used for high-side and low-side switches in a synchronous buck converter, using the DirectFET package and the same simulation conditions as in the previous analysis, the efficiency curve at 20MHz is obtained and shown in Fig. 6.43. Comparing these values to the efficiency obtained when design with the field-plate is used, it can be seen that approximately the same efficiencies of the converter are obtained in a higher range of the output power. On the hand, in the low P_{out} range, the design with the field-plate provides slightly higher efficiencies (only 1-2%). This can be explained by the trade-off between Q_{gd} and Q_{ds} of these two designs. Since the switching losses are proportional to the product of the output current and Miller time, higher Q_{gd} will have more visible influence on the efficiency values in the higher range of the output current i. e. in the higher range of the output power. In our converter, the influences of higher Q_{gd} and lower Q_{ds} are quite similar in a higher P_{out} range, giving approximately the same efficiency values. As we move to the lower output current values, the influence of higher Q_{ds} becomes slightly dominant over Q_{gd} , and the design with the field-plate gives slightly higher efficiencies. Overall, we conclude that in our application, the optimized design with the field-plate

structure provides better solution since it gives better electric field distribution and higher robustness of the device, without penalization of the converter's efficiency.

Figure 6-43 Estimated efficiency of a synchronous buck converter at 20MHz of switching frequency, using optimized design with and without the field-plate.

6.6. Summary and conclusions

In this chapter, the optimization of an AlGaN/GaN HEMT design for application in high-frequency buck converter has been presented. As an introduction to the optimization procedure, the parameters of the device were varied and the corresponding designs were simulated, using the power loss model from the previous Chapter. In this way, it has been clearly shown how each of the parameters influences capacitances and on-resistance of the device, and through them, the overall efficiency of the converter.

In order to be able to optimize the design for a target breakdown voltage, **an analytical model for the peak of the electric field in the channel was developed** and presented. In this way, the design of the field-plate was directly related to the breakdown voltage of the device. Having in mind that field-plate design dominantly influences Miller's charge in the device, the optimization of

the field-plate in terms of material, thickness and length has been performed independently on the other parameters of the HEMT, by minimization of the gate-to-drain charge for a breakdown voltage of 40V. The detailed block diagram of this optimization procedure has been presented and explained.

Since the initial design of the device contained TO-220 package which has high values for parasitic inductances, it was replaced by DirectFET package. Additionally, it was shown that freewheeling diode in a simple buck configuration caused 40% of the total losses at 20MHz of switching frequency, due to high value of the output capacitance. **Therefore, the simple buck was replaced by synchronous buck configuration.**

Furthermore, the rest of the parameters of the device were optimized independently, by minimization of the power losses in the synchronous buck converter. These parameters are: Aluminum mole fraction, m , thickness of AlGa_N layer, d_{AlGaN} , gate length and width, L_g and W_g , and gate-to-source distance, L_{gs} . Among them, m and d_{AlGaN} are dependent on each other, due to necessity to obtain the AlGa_N/Ga_N heterojunction which will not provide many dislocations in the channel. Additionally, the value for L_{gs} was set to be equal to the obtained value for the gate length in order to comply with scaling rules.

Using the optimized design with DirectFET package in a synchronous buck converter, simulations showed efficiency increase of **20% in the low range of the output power**, at 20MHz of switching frequency, when compared to the nominal design with the same package. The total loss breakdown showed that **switching losses that presented 81% of the total losses were decreased for 76% due to highly improved capacitance characteristics of the device.**

Finally, in order to examine if the field-plate structure was necessary for the target breakdown voltage of 40V, the peak of the electric field around the gate edge was calculated, using the proposed analytical model. It has been established that the peak value for $V_{ds}=40V$ is equal to the 1.910942 MV/cm which is close to 2MV/cm (the maximum allowed value according to our design rules), while the design with the field-plate provided two peaks of 0.6 and 1.52MV/cm. **Therefore, the same design without the field-plate can be used in our application but it has lower robustness when compared to the design that contains the field-plate.** Furthermore, the proposed capacitance model showed that optimized design without the field-plate extension has lower gate-to-drain charge but higher drain-to-source charge, which eventually gave approximately the same efficiency values at 20MHz of switching frequency. Therefore, we conclude that using the **design with the field-plate structure, we obtain more robust solution from the point of view of electric field**

distribution and breakdown characteristics and approximately equal efficiency of the converter.

Chapter7. Summary and future work

7. Summary and future work

7.1. Thesis summary and contributions

The topic of this thesis is a **physics-based analytical modelling of AlGaIn/GaN HEMTs that contain gate field-plate structure and device design optimization of these devices for application in high-frequency switching converters.**

The process of design optimization requires precise, non-complex, analytical, physics-based model of the device. Analyzing State Of the Art in this type of models for AlGaIn/GaN HEMTs, it was concluded that previous works were mainly focused on HEMTs **without field-plate structure**, while **the only proposed model for this type of devices was surface-potential based model, characterized with high complexity** and computationally intensive numerical simulations [Ahsan, 2016]. Since the **field-plate extension of the gate electrode crucially influences the capacitive part of the device**, the analytical model for input, output and reverse capacitance is **highly different from the ones proposed in SOA for devices without the field-plate**. Therefore, the derivation of a novel, physics-based model for non-linear dependence of these capacitances on the applied drain-source voltage, when the device is in the subthreshold regime, is the first contribution of this thesis.

The methodology that was used for Miller's capacitance modelling is **based on the approximation of the 2-Dimensional charge depletion by two 1-Dimensional depletions** that can be treated and modelled independently. The charge that is being depleted as the drain-source voltage is being increased from zero to the breakdown voltage, while gate-source voltage is kept below the threshold, is the 2DEG leftover in the gate-drain drift area directly below the field-plate. The first 1-D depletion is addressed as vertical depletion, since the charge depletion is caused by the electric field component perpendicular to the channel. The second 1-D depletion of the same 2DEG leftover charge, is addressed as lateral depletion, since it is caused by the electric field component parallel to the channel. This lateral depletion takes place around the drain-side gate edge and the field-plate edge, while vertical depletion exists directly below the field-plate. The analysis showed that in the range of drain-source voltages from zero to the particular value, vertical depletion exists together with lateral depletion around the drain-side gate edge. Furthermore, for drain-source voltages higher than the "boundary" value, it was found that only the lateral

depletion around the field-plate edge exists. After each of the charge depletions and corresponding V_{ds} ranges were identified, they were analytically modelled.

Since **vertical depletion** presents the channel charge control by the applied drain-source voltage while gate-source voltage is kept constant, this depletion process was modelled as 2DEG charge control by gate-drain voltage in a MISHEMT structure. The general methodology used for charge-control models of HEMT structure was applied, using Poisson's equations and Gauss law for charge conservation. In this way, fully analytical model for 2DEG sheet density dependence on the applied drain-source voltage was obtained, **directly giving the dependence of this part of Miller's capacitance on the applied V_{ds}** . Additionally, this analytical model provided the value for V_{ds} when vertical depletion below the field-plate ends and lateral depletion around the field-plate edge begins.

Regarding the **lateral depletion** process, in order to obtain fully analytical relation between the extension of the depletion region and the applied drain-to-source voltage, several conformal mapping transformations of the original geometrical model were performed. Afterwards, the image charge method together with the principle of superposition were applied, providing the dependence of the depletion area extension on the drain-source voltage, and therefore, the drain-source voltage dependence of the corresponding part of Miller's capacitance.

Regarding the **drain-source capacitance**, the analysis showed that **this capacitance primarily originates in the fringing between the extension of drain and source electrodes** through the drain and source drift areas. The applied modelling methodology was based on the analytical calculation of fringing capacitance between two sufficiently long metal lines. Because the width of these lines changes after vertical depletion is completed, and consequently the extension of the drain electrode is decreased for the length of the field-plate, **drain-source capacitance will be affected by drain-source voltage**. However, **comparing to Miller's capacitance, the variation of drain-source capacitance values with drain-source voltage is significantly smaller**.

The origin of gate-source capacitance was also identified in the **fringing between the electrodes**. Since variation in drain-source voltage does not affect the extension of the source electrode through the source drift region, **the gate-source capacitance is found to be completely independent on the applied V_{ds}** . It is worth noticing that a **significant portion of gate-source capacitance was found in the fringing between fingers of gate and source electrodes, due to the multifinger layout of the device**.

In order to examine the precision of the obtained capacitance model, the experimental characterization of the device was performed. The highest discrepancy was equal to 14.7% and it was found between the modelled and the measured value for gate-to-drain charge. In order to examine if this value as well as the precision of the complete capacitance model is acceptable from the point of view of design optimisation for high-frequency switching applications, the additional simulations were performed. The efficiency of a high-frequency buck converter at 7, 15 and 20MHz of switching frequency was simulated, using modelled and experimentally measured capacitance curves. Very good agreement between the efficiency curves was obtained, showing maximum deviation of 4% at 15MHz for P_{out} higher than 25W, and 3% at 20MHz for P_{out} higher than 12W. Taking into consideration that target application of the device is a converter that needs to generate high Peak-to-Average power ratio signals while operating at high switching frequency, the obtained results are highly acceptable. **Therefore, the precision of the proposed capacitance model is proved to be high enough for device design optimization.**

Furthermore, the prototype of a high-frequency buck converter was implemented, using the analyzed AlGaN/GaN HEMT as the main switch. Measured efficiency curves at 7, 15 and 20MHz of switching frequency showed very good agreement with simulations that used modelled and experimentally obtained capacitance characteristics. **Good agreement was obtained even at 20MHz in the low range of the output power.** In this way, **the power loss model together with proposed capacitance model were experimentally verified.**

In order to additionally examine the influence of the proposed capacitance model on the overall efficiency of a high-frequency buck converter, the simulations that employed constant values for $C_{gd}(V_{ds})$ were performed. The applied values were: $C_{gd,I}=130pF$ which is the capacitance value in the range of V_{ds} where vertical and lateral depletions exist, $C_{gd,II}=11.8pF$ which is the capacitance value in the range of V_{ds} where only lateral extension around the field-plate edge exists, and $C_{gd}=C_{gd_{eq}}=40pF$ which is the value obtained from the approximate calculation of the energy in the capacitor. The energy in the capacitor was calculated using modelled characteristic for non-linear $C_{gd}(V_{ds})$ dependence. The reference efficiency curve in the following comparison will be the curve obtained when measured $C_{gd}(V_{ds})$ was implemented. **Simulations at 7MHz showed that implementation of constant value for Miller's capacitance equal to $C_{gd,I}$ and $C_{gd,II}$ causes higher discrepancies in the efficiency estimation in the complete range of P_{out} , comparing to the curve obtained when modelled $C_{gd}(V_{ds})$ was used.** These discrepancies are equal to 10% and 5% for $C_{gd,I}$ and $C_{gd,II}$ respectively while modelled $C_{gd}(V_{ds})$ showed 3% of deviation only in the range

of $P_{out} < 7W$. Furthermore, the implementation of $C_{gd,eq}$ showed good agreement in the whole range of the output power. This additionally emphasized the necessity for non-linear $C_{gd}(V_{ds})$ model, in order to precisely estimate power losses in the converter.

Observing the obtained results it is found that **proposed methodology provides much better results comparing to power loss calculation that does not take into account non-linear $C_{gd}(V_{ds})$ dependence**. Since only one, complex, surface-potential based capacitance model for devices with the field-plate is found in the SOA [Ahsan 2016], it **can be concluded that methodology proposed in this thesis provides model that is suitable for design optimization process, with sufficiently high level of accuracy**.

After the verification of the novel capacitance model, the optimization of the device design was performed. In order to optimize the design for a target breakdown voltage of 40V, it was necessary to obtain the analytical relation between the channel electric field and the applied drain-source voltage. **Since the peaks of the channel field can be approximated by the peaks of the field's lateral component, this analytical relation was derived using the methodology similar to the one that determined the lateral extension of the depletion area in the channel**. This analytical relation between the electric field in channel and applied V_{ds} presents **the second contribution of the thesis**.

Before the optimization of the device was performed, the influence of initial TO-220 package of the device on the overall efficiency of the converter was examined. **Simulations showed that this package highly penalizes the efficiency at 20MHz of switching frequency, and therefore needs to be substituted with different one, that contains lower values for parasitic inductances**. Therefore, DirectFET was chosen for the package of the optimized device. **Additionally, simulations showed that due to high value of the output capacitance of the Schottky diode used in the simple buck configuration, losses due to this capacitance present 30% of total losses at P_{out} of 8W and switching frequency of 20MHz**. Therefore, **the simple buck converter was replaced by synchronous-buck configuration**.

The third contribution of this thesis is the design optimization of the device. Since previous analysis showed that **design of a field-plate dominantly influences Miller's charge while determining the breakdown voltage** of the device, the **field-plate design was optimized separately** from the other parameters of the HEMT. The field-plate thickness, length and insulator material were obtained by minimization of gate-to-drain charge for the target breakdown voltage of 40V. Since gate-to-drain distance is directly related to the

field-plate length and electric-field distribution for $V_{ds}=40V$, this parameter was also obtained as a result of this optimization code.

In order to continue the optimization of the design, efficiency simulations using proposed model were performed, by changing the values of the following parameters: Aluminum mole fraction, m , thickness of AlGaN layer, d_{AlGaN} , gate width and length, W_g and L_g and gate-to-source distance, L_{gs} . The obtained efficiency curves showed that m and d_{AlGaN} should be increased and decreased, respectively, while minimizing W_g , L_g and L_{gs} . The boundary for minimization of the gate width is the target current rating of the device (6A). The number of fingers was scaled down according to the obtained gate width, while keeping the same width of 1mm per finger.

Using DirectFET package and synchronous-buck converter, the optimized design of the device was simulated at switching frequency of 20MHz and compared to the nominal design in the same package and the same topology. **The efficiency curves showed more than 20% of efficiency increase in the low range of the output power.** The total loss breakdown for $P_{out}=20W$ at the same switching frequency, showed that **total losses were decreased for 80%.** **The switching losses that presented 81% of the total losses were decreased for 76% due to highly improved capacitance characteristics of the device.**

Since the initial device was designed for a breakdown voltage of 100V, it was important to examine if the field-plate structure was necessary for the target breakdown voltage of 40V. If the field-plate is removed and other parameters kept as in the optimized design, the peaks of the electric field still lie below the critical design values, meaning that the field-plate is not necessary. The field-plate removal causes decrease in gate-to-drain charge but increase in drain-source charge, due to higher fringing capacitance between drain and source electrodes. These changes gave approximately the same efficiency values at 20MHz of switching frequency. **It can be concluded that using the field-plate structure, more robust solution is obtained, giving approximately equal efficiency of the converter.**

7.2. Future work

Several topics and research lines could be addressed in the area of modelling and optimization of AlGaN/GaN HEMTs.

Since the proposed capacitance model is fully analytical and based on Poisson's equations, Gauss law, conformal mapping transformations and image

charge method, it would be possible to apply the same modelling methodology for different AlGaIn/GaN devices such as HEMTs with multiple gate and source field-plate structures, AlGaIn/GaN MISHEMTs as well as for normally-off HEMTs with the recessed gate or gate-insulated transistors. After identifying the origins of different capacitive parts, vertical and lateral depletion models together with the fringing capacitance models could be applied in the aforementioned structures. If the models show acceptable precision, they could be used for further optimization of these devices for different switching applications.

Since proposed physics-based model is not temperature dependent, the future work could provide the upgrade in terms of thermally dependent model for capacitances of a HEMT with a field-plate structure.

Finally, the multifinger layout of the device could be additionally analyzed and optimized. Different structures such as fractal structures could be used instead of conventional comb structure that was used in the analyzed device. This could additionally decrease the fringing capacitances between the fingers and improve the optimized design of the device.

7.3. Publications

During the work on this thesis, the following papers are published:

- [P1] Cucak, D., Vasic, M., Garcia, O., Oliver, J.A., Alou, P., Cobos, J.A., Wang, A., Horcajo, S., Romero, F. and Calle, F., Forthcoming. Physics-based analytical model for input, output and reverse capacitance of a GaN HEMT with the field-plate structure. *IEEE Transactions on Power Electronics*. DOI: <http://dx.doi.org/10.1109/TPEL.2016.2569404>
- [P2] Cucak, D., Vasic, M., Garcia, O., Oliver, J.A., Alou, P. and Cobos, J.A., 2016. Optimization of a Gallium Nitride HEMT design for a high frequency DC-DC converter application. *ETG-Fachbericht-CIPS 2016*.

- [P3] Cucak, D., Vasic, M., Garcia, O., Bouvier, Y., Oliver, J., Alou, P., Cobos, J.A., Wang, A., Martin-Horcajo, S., Romero, F. and Calle, F., 2014, September. Physical model for GaN HEMT design optimization in high frequency switching applications. In *2014 44th European Solid State Device Research Conference (ESSDERC)* (pp. 393-396). IEEE. DOI: <http://dx.doi.org/10.1109/ESSDERC.2014.6948843>
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- [P5] Cucak, D., Vasic, M., García, O., Oliver, J., Alou, P. and Cobos, J.A., 2014. Filter Design Methodology and Application of GaN HEMTs in High-Frequency DC/DC Converter. *IETE Journal of Research*, 60(3), pp.240-248. DOI: <http://dx.doi.org/10.1080/03772063.2014.914696>
- [P6] Cucak, D., Vasic, M., Garcia, O., Oliver, J., Alou, P., Cobos, J.A., 2013 March. Application of GaN FET in 1MHz large signal bandwidth power supply for radio frequency power amplifier. In *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* (pp. 664-671). IEEE. DOI: <http://dx.doi.org/10.1109/APEC.2013.6520281>
- [P7] Cucak, D., Vasic, M., Garcia, O., Oliver, J., Alou, P., Cobos, J.A., 2013 July. Application and Modelling of GaN HEMT in 1MHz Large Signal Bandwidth Power Supply for Radio Frequency Power Amplifier. In *Seminario Anual*

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- [P8] Cucak, D., Vasic, M., Garcia, O., Oliver, J.A., Alou, P. and Cobos, J.A., 2012, March. Application of eGaN FETs for highly efficient Radio Frequency Power Amplifier. *ETG-Fachbericht-CIPS 2012*.
- [P9] Čučak, D., Vasić, M., García, O., Oliver, J.A., Alou, P. and Cobos, J.A., 2011, September. Optimum design of an envelope tracking buck converter for RFPA using GaN HEMTs. In *2011 IEEE Energy Conversion Congress and Exposition* (pp. 1210-1216). IEEE. DOI: <http://dx.doi.org/10.1109/ECCE.2011.6063914>
- [P10] Cucak, D., Vasic, M., Garcia, O., Oliver, J., Alou, P., Cobos, J.A., 2011 July. High Efficiency Envelope Tracking Buck Converter for RFPA using GaN HEMTs. In *Seminario Anual de Automatica, Electronica Industrial e Instrumentacion (SAAEI)*, (pp. 113-118).

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