RESEARCH ARTICLE

Evolution of silicon bulk lifetime during III–V-on-Si multijunction solar cell epitaxial growth

Elisa García-Tabarés , John A. Carlin , Tyler J. Grassman , Diego Martín , Ignacio Rey-Stolle and Steven A. Ringel

ABSTRACT

The evolution of Si bulk minority carrier lifetime during the heteroepitaxial growth of III–V on Si multijunction solar cell structures via metal-organic chemical vapor deposition (MOCVD) has been analyzed. In particular, the impact on Si lifetime resulting from the four distinct phases within the overall MOCVD-based III–V/Si growth process were studied: (1) the Si homoepitaxial emitter/cap layer; (2) GaP heteroepitaxial nucleation; (3) bulk GaP film growth; and (4) thick $GaAs_yP_{1-y}$ compositionally graded metamorphic buffer growth. During Phase 1 (Si homoepitaxy), an approximately two order of magnitude reduction in the Si minority carrier lifetime was observed, from about 450 to $\leq$1 μs. However, following the GaP nucleation (Phase 2) and thicker film (Phase 3) growths, the lifetime was found to increase by about an order of magnitude. The thick $GaAs_yP_{1-y}$ graded buffer was then found to provide further recovery back to around the initial starting value. The most likely general mechanism behind the observed lifetime evolution is as follows: lifetime degradation during Si homoepitaxy because of the formation of thermally induced defects within the Si bulk, with subsequent lifetime recovery due to passivation by fast-diffusing atomic hydrogen coming from precursor pyrolysis, especially the group-V hydrides (PH_3, AsH_3), during the III–V growth. These results indicate that the MOCVD growth methodology used to create these target III–V/Si solar cell structures has a substantial and dynamic impact on the minority carrier lifetime within the Si substrate.

KEYWORDS

III–V on silicon; GaAsP/Si; heteroepitaxy; MJSC; metamorphic growth; minority carrier lifetime; bottom subcell

1. INTRODUCTION

Multijunction solar cells (MJSCs) based on III–V compound semiconductors are of great interest for lowering the cost of solar energy because of their extraordinary solar energy conversion efficiencies that can exceed 40% under solar concentration. They are also the mainstay technology for space photovoltaics because of the advantageous specific power parameters—W/m^2 and W/kg. There is likewise great interest in merging III–V MJSCs with Si substrates, which would replace the conventional, and more costly, Ge and GaAs substrates currently used for MJSC technology. The successful attainment of III–V/Si hybrid MJSCs would thereby link the already demonstrated efficiency potential of III–V semiconductor multijunction architectures with the low cost, large area, and wide availability of Si substrates, helping to reduce the cost of solar electricity toward levels that hold promise to become competitive with conventional sources. Additionally, depending upon the method of integration, the Si substrate itself could participate as an important power producing subcell in such an arrangement.

Interest in III–V/Si photovoltaics (PV), at varying levels of magnitude, goes back many years, but scientific advances over the past decade or so, as well as modern PV economics, have ignited a significant surge in attention

and activity in this area [1–7]. While there are a number of approaches for achieving such materials integration, of current particular interest for the formation of ideal multijunction structures is the growth of metamorphic III–V materials on Si by way of GaP nucleation and compositionally graded $GaAs_yP_{1-y}$ buffer layers [2,8,9]. The vast majority of the effort in this direction has concentrated on the optimization of the heteroepitaxial growth of III–V compounds on Si, ranging from the GaP nucleation layer and $GaAs_yP_{1-y}$ graded buffer to ideal GaAsP and GaInP upper subcells [2,9–11], with the primary goal being the minimization of crystal defects (e.g., antiphase domains, stacking faults, and threading dislocations). To this end, good quality metamorphic III–V materials and devices have indeed been reported, demonstrating great promise toward the achievement in the goal of III–V/Si solar cells [2,10]. However, little to no work has focused on the Si, which plays a key role as not only a growth substrate but also as an active bottom subcell, and the potential impact upon it with respect to these III–V heteroepitaxial processes.

In conventional Si PV, it is well-established that the bulk minority carrier lifetime (τ) is not a fixed, intrinsic material property, but rather strongly depends on the thermal history and processing environment in which the solar cell is manufactured [12]. It is thus worthy of note, then, that a wide range of ambient environments can be present within a metal-organic chemical vapor deposition (MOCVD) environment—the generally accepted industry standard for large-scale III–V epitaxy. This includes not only conditions required for the growth of the aforementioned III–V materials but also the formation of the Si bottom junction itself. While the Si p-n junction can certainly be formed via traditional *ex-situ* diffusion-based methods [13,14], *in-situ* formation within the MOCVD reactor, such as via the previously reported method of n-type homoepitaxial emitter growth on a p-type substrate [15,16], which would reduce the total number of process steps, is of great interest. To this end, a strong influence of the MOCVD environment on minority carrier lifetime during one type of *in situ* Si junction formation (i.e., *in situ* diffusion) has already been previously reported by the authors [17].

Therefore, because the Si minority carrier lifetime will not only govern the performance of the Si bottom subcell but in turn will also impact the entire multijunction device and its optimal design [18], it is important to fully understand the impact of the MOCVD processing on Si lifetime. Despite the achievement of high-quality III–V layers integrated on Si substrates, the impact of these steps on the Si bulk lifetime has not been explored to date. Accordingly, in this paper, we report the results of a systematic study in which the individual phases of the MOCVD based III–V/Si heteroepitaxial process have been examined with respect to their impact on the p-type Si minority carrier lifetime. The growth process was found to heavily influence the p-Si bulk lifetime, with a massive reduction observed following the first phase (Si homoepitaxy) and a stepwise, full recovery during the subsequent III–V heteroepitaxial phases. This lifetime evolution was attributed to a dynamic defect formation and passivation mechanism that is directly related to the III–V/Si growth process.

2. EXPERIMENTAL METHODS

An Aixtron 3 × 2 close-coupled showerhead MOCVD system (AIXTRON SE, Herzogenrath, Germany), with a graphite susceptor, was used for all epitaxial growths in this work. The substrates used were p-type (B-doped, 1–5 $\Omega \cdot$cm) float-zone (Fz) Si(100), intentionally misoriented 6° toward <011>. The native oxide on the as-received Fz-Si substrates was removed via etching in an fluorhydric acid (HF) solution prior to loading into the reactor. The effectiveness of this simple chemical clean with respect to preparing silicon wafers for III–V heteroepitaxy, as compared with more time-consuming methods like the Radio Corporation of America (RCA) Standard Cleaning or Ishizaka–Shiraki processes, was previously reported by the authors [17]. The overall process used for the epitaxial III–V/Si and Si subcells has been previously reported [15,16] and is described briefly here, noting the four major phases. Phase 1 is the growth of the homoepitaxial Si emitter, which was conducted at 760°C using a dilute SiH_4 source (typically used for n-type doping of III–V compounds) with a growth rate of ~5 Å/min; this essential step also serves to bury any residual surface contamination, namely carbon, which can lead to non-ideal GaP nucleation, and is thus unavoidable. Phase 2 is the atomic layer epitaxy (ALE) GaP nucleation [16], performed at 450°C, yielding approximately 6 nm of total GaP growth and a total growth time (i.e., precursor exposure) of around 2.5 min. Phase 3 consists of standard (i.e., non-pulsed) GaP growth at 550°C to a total GaP thickness of 250 nm and a growth time of 30 min. For both Phase 2 and 3, triethylgallium (TEGa) and tertiarybutylphosphine (TBP) were used as Ga and P sources, respectively. Phase 4, the final step in the process used for this study, is the growth of step-graded metamorphic $GaAs_yP_{1-y}$ buffer layers at 725°C, terminating at a composition of $GaAs_{0.7}P_{0.3}$. For the present study, the total buffer thickness (including a thick terminal composition cap layer) was 3.2 µm, with an aggressive grading rate of 1% misfit per µm and total growth time of 110 min. In this case, trimethylgallium (TMGa) was the Ga source, while arsine (AsH_3) and phosphine (PH_3) were used as the group-V precursors.

To track the evolution of the bulk Si minority carrier lifetime throughout the growth process, multiple samples were produced after the four different process phases described earlier. Before performing minority carrier lifetime measurements, all III–V epitaxial material was removed via etching in a $HCl:HNO_3$ solution. Moreover, at least 1 µm of Si surface material was also stripped away to ensure a clean surface. The etched sample was then passivated in a 0.05 M quinhydrone–methanol solution bath [19]. To verify the reproducibility of the lifetime measurements, especially with respect to the quinhydrone passivation quality, as-received Si reference samples were processed (etching and passivation) and measured in parallel with

the target samples. Bulk minority carrier lifetime of the p-type Si was measured at 300 K by photoconductance decay with a Sinton WCT-120 tool (Sinton Consulting Inc., Boulder, CO, USA), which has a lower end detection limit of approximately 1 μs. Generally, the lifetime measurements used a photocarrier injection level, Δn, of 10^{15} cm^{-3}, but for very low lifetime values, (i.e., <10 μs) the injection level was necessarily reduced to 10^{14} cm^{-3}.

3. RESULTS AND DISCUSSION

3.1. Process-dependent minority carrier lifetime

Table I presents the bulk Si lifetime data as measured after the four different phases of the III–V/Si epitaxial process described in Section 2, with data from the as-received wafer included for comparison. For Phase 1, the homoepitaxial Si emitter growth, two different layer thickness, and thus growth times, were considered: 20 nm (40 min) and 90 nm (180 min). It is here, Phase 1, where one of the key results of this work is observed. That is, a massive degradation of more than two orders of magnitude of the minority carrier lifetime appears to occur over the course of the homoepitaxial Si emitter growth. Given that a lifetime reduction from 432 to only 6 μs was observed for even the relatively short growth period (40 min), the apparent rate of degradation is quite rapid. An additional 140 min (70 nm) of growth reduces the lifetime further to 1 μs. However, because this is actually the lower limit for the instrumentation being used, it is possible that the actual lifetime of the 90 nm emitter sample is even lower. Regardless, the low lifetime values observed in both cases are clearly detrimental to PV performance.

Nonetheless, as shown in the remainder of Table I, while the Si homoepitaxy was found to yield a drastic lifetime reduction, it was also found that the III–V MOCVD growth process (Phases 2–4) does exactly the opposite, providing an equally drastic overall lifetime recovery. However, the observed recovery process is less straightforward. After Phase 2, the GaP nucleation step, the lifetime was found to have increased by at least an order of magnitude, to about 30 μs, despite the very short duration (2.5 min), low-temperature (450°C) GaP ALE process. Continued "bulk" GaP MOCVD growth for 30 min at 550°C (Phase 3) provided about another factor of two improvements. The most substantial and remarkable Si lifetime recovery back to around its as-received value then occurred in Phase 4, the long (110 min), high-temperature (725°C) $GaAs_yP_{1-y}$ buffer growth.

These results indicate that the MOCVD growth methodology used to create these target III–V/Si solar cell structures, with a focus on elimination (or at least minimization) of structural defects, actually has a substantial and dynamic impact on the minority carrier lifetime within the Si substrate. It is fortuitous that the sequential effects, as a function of the four deposition phases outlined earlier, return the Si lifetime to its starting value. The following sections focus on the likely degradation and recovery mechanisms associated with each phase of the growth process.

Table I. Average minority carrier lifetime for float-zone (Fz)-Si wafers after III–V heteroepitaxy. All epitaxial material and some wafer surface material have been removed to enable direct measurement of the Si bulk lifetime. An as-received Fz wafer is included for comparison (Phase 0). A maximum standard deviation of 7.5% was measured for these samples.

Phase	Temperature (°C)	Growth time (min)	Precursor species	Δn (cm^{-3})	τ (μs)
0	—	—	—	10^{15}	432
1	760	40	H_2, SiH_4	10^{14}	6
1	760	180	H_2, SiH_4	10^{14}	1
2	450	2.5	H_2,TBP, TEGa	10^{15}	30
3	550	30	H_2,TBP, TEGa	10^{15}	72
4	725	110	H_2, PH_3, AsH_3,TMGa	10^{15}	467

3.2. Lifetime degradation and recovery mechanisms

3.2.1. Phase 1: lifetime degradation.

Neglecting the small contribution of SiH_4 to the process atmosphere—the SiH_4 partial pressure is very low (~4.4×10^{-3} mbar) because the associated source is normally used for III–V doping, making large flows unavailable—the homoepitaxial emitter growth is very similar to annealing under pure H_2 (within an MOCVD environment), which has been previously reported to produce a rapid degradation of the Si lifetime [17]. This prior work by the authors was able to narrow the possible mechanisms for this degradation down to three, which due to the process similarity, should also apply to the present case observed during the high-temperature (760°C) Si homoepitaxial growth (Phase 1). Namely, these potential degradation mechanisms are (1) the in-diffusion of some lifetime-killing impurity associated to the MetalOrganic Vapor Phase Epitaxy (MOVPE) process (e.g., Zn, a typical p-type dopant used in MOVPE that could back-diffuse from the reactor vacuum system); (2) the in-diffusion of transition metals (e.g., Cu, Fe, and Ni) coming from heated parts of the MOVPE reactor; or (3) the formation of crystal defects as a result of the thermal treatment of the wafer.

With respect to the first possibility, an important feature of an extrinsic diffusion mechanism is that any such impurity should show a decreasing concentration with depth into the wafer, provided that the diffusivity is not such that the diffusion front can extend deep enough so as to produce an effectively homogeneous distribution throughout the entire wafer thickness. High impurity/defect concentration near the wafer surfaces can produce an effective bulk lifetime reduction, similar to that seen with high surface recombination velocities [18]. Therefore, if the lifetime

degradation observed here is the result of some in-diffused impurity species, then removal of sufficient material from the wafer surfaces (where the concentration of the impurity would be highest) should result in an effective bulk lifetime recovery.

Table II presents the results of just such an experiment where a chemical etch (CH_3COOH:HNO_3 : HF) was used to uniformly remove over 20 µm of surface material from lifetime-degraded Si wafers, with a comparison of pre-etch and post-etch minority carrier lifetimes, τ_i and τ_f, respectively. Prior to etching, the p-type Fz-Si wafers were submitted to lifetime-killing, high-temperature (830°C) anneals in H_2 ambient of either 2 min or 30 min, as well as different pre-anneal treatments (with and without HF oxide etching). As seen in Table II, the degraded bulk minority carrier lifetimes were found to remain constant after etching, if not even slightly lower, suggesting that lifetime degradation is indeed a bulk effect rather than a surface-induced effect. The very minor differences (i.e., slightly lower post-etch values) may be related to the passivation quality, which could be slightly impacted because of increased surface roughness resulting from the deep etch.

In order to verify these results, the diffusion profiles of the most likely impurity of concern for the MOCVD-based anneals shown in Table II, Zn, have been calculated using a simple Fickian diffusion model and are presented in Figure 1. Zn was considered as the most likely candidate because it is a typical p-type dopant in III–V semiconductors, and thus traces could be present in many MOCVD environments. Zn is also a fast-moving impurity with strong lifetime-killing effects in Si; concentrations as low as $10^{13}\,cm^{-3}$ are capable of ruining minority carrier lifetime [20]. A Zn-in-Si diffusivity (at 830°C) of $4\times10^{-9}\,cm^2/sec$ [21] and a constant surface impurity concentration (Cs) were used. It has been reported that, under some circumstances, the diffusion of Zn in Si deviates from the standard error function (erfc) profile and follows a kick-out diffusion mechanism [22]. However, according to the same work, the erfc profile always represents the most intense diffusion for wafer thicknesses below 500 µm. As such, a Zn erfc profile should then establish a working upper-limit "worst case" scenario for the situation under consideration here. As such, the calculated final impurity concentrations (Cf_i), given in Figure 1, are higher than if they were calculated by a kick-out diffusion profile.

Table II. Minority carrier lifetime comparison before (τ_i) and after (τ_f) etching the Si wafer. The estimated removed thickness from each side of the wafer, Δt, according to wafer weight measurements is included in the last column.

Sample	Cleaning	Treatment	τ_i (µs)	τ_f (µs)	Δt/side (µm)
A	HF	2 min 830°C 100 mbar H_2	60	54	22.5
B	HF	30 min 830°C 100 mbar H_2	5	5	25.6
C	None	30 min 830°C 100 mbar H_2	9	7	23.0

According to the calculated diffusion profiles in Figure 1(a), samples B and C, which underwent long, high-temperature anneals, yield post-etch near-surface impurity concentrations, C_f^B and C_f^C, respectively, of about half the starting concentration. Because the impact of such a relatively small concentration change on the Shockley–Read–Hall (SRH) recombination lifetime is also relatively small, as indicated by Figure 1(b), the results from samples B and C are effectively inconclusive because of the lack of sufficient sensitivity. Sample A, on the other hand, which received a considerably shorter anneal, should be much more telling. The calculated impurity concentration at the etch point, C_f^A (22.5-µm deep), is reduced by nearly 50× compared with the initial surface concentration. Such a difference in Zn concentration should induce an approximately equally large change in SRH lifetime [20], as shown in Figure 1(b), making Sample A the more sensitive test case. Nonetheless, just as with samples B and C, no difference was observed between the lifetimes measured for the pre-etched and post-etched measurements (i.e., $\tau_i \approx \tau_f$) for sample A. Finally, for a degree of independent verification with respect to the potential in-diffusion of Zn, a sample of Fz-Si, which received the same chemical clean as the pre-epitaxy samples, was annealed in an ultra-high vacuum molecular beam epitaxy chamber at 700°C for 60 min. This system—consisting on a sample holder made of molybdenum and tantalum and a baking plate made of sapphire—with an idle chamber pressure of $\leq 3\times10^{-10}$ mbar has never made use of Zn. Nonetheless, the anneal resulted in a similar degradation of the minority carrier lifetime to a value of 8 µs.

These results indicate that there is likely no depth dependence in the lifetime-killing recombination sites, but rather suggests a fully homogeneous distribution of defects or impurities (i.e., $C_s \approx C_f$). This then effectively rules out the case of relatively slow diffusers (e.g., Zn), but does not necessarily rule out the potential for fast diffusers (e.g., Fe), which tend to yield uniform concentration distributions in the absence of any kind of gettering effect, or the possibility of thermally induced crystal defects.

Regarding Fe contamination, injection-level dependent recombination lifetime measurements [23] of as-received, lifetime degraded, and lifetime recovered samples, after light soaking, indicate that Fe is indeed present in bare silicon wafers; but it has been found that it is most likely not the limiting source of lifetime degradation. This suggests that either the influence of other recombination centers cannot be neglected or other factors—such as atomic H as will be commented in the succeeding paragraphs—are having a key role in the FeB → Fei dissociation dynamics. Accordingly, results with respect to Fe are currently inconclusive and consequently, further investigations with DLTS are ongoing to clarify this topic.

Taken together, these results strongly indicate against an in-diffused impurity mechanism as the cause of the observed Phase 1 lifetime degradation. Instead, the more likely mechanism is that the thermal treatments experienced by these samples—both H_2-annealed (Table II) and

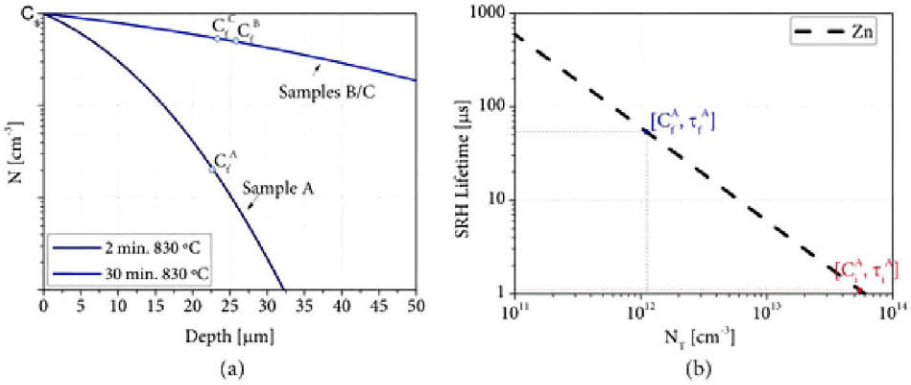

Figure 1. (a) Calculated diffusion profiles of Zn in Si for annealing times and temperatures as applied to samples A and B (C) described in Table II. An arbitrary constant surface impurity concentration (Cs) was considered. The data points indicate the anticipated final surface impurity concentration (Cfi) after performing the chemical etch for each sample from Table II (i = A, B, C). (b) Evolution of the Si Shockley–Read–Hall (SRH) recombination lifetime as a function of the Zn concentration according to Colleti [20]. The final concentration (CfA)—calculated from tfA— and the initial concentration (CiA)—expected to be in the order of 50 times higher than CfA according to Figure 1(a) for Sample A, which showed the largest potential change in impurity concentration—have been plotted to quantify the variation in terms minority carrier lifetime (tiA vs tfA). According to this model, tiA should be in the range of 1 μs; being significantly lower than the actual value (60 μs).

homoepitaxial Si (Table I)—is leading to the formation of either extrinsic or intrinsic defects [24]. Examples of such extrinsic defects are the formation of complexes with low pre-existing concentrations of C and/or O (such as thermal donors) or extended defects (such as the well-known swirls); while point defects (e.g., in-diffused vacancies) are examples for intrinsic defects.

In this sense, such defects and their deleterious effect on the minority carrier lifetime have been widely reported. For example, the formation of oxide precipitates during thermal treatment is accompanied by the nucleation of extended lattice defects, which become recombination centers by attracting and concentrating otherwise low-density impurities present in the wafer bulk [24]. Of course, extended defects can also be produced as a result of the mechanical stress during the thermal process [24]. In this sense, Wang *et al.* [25] reported that the formation of swirl defects is conditioned by the cooling rate of the sample after being submitted to a high-temperature annealing. In this respect, they stated that slow cooling rates (~1°C/sec) for a dislocation-free, swirl-free crystal is critical for obtaining high minority carrier lifetimes, avoiding the formation of lattice micro-defects related to fast cooling rates [25]. Moreover, the agglomeration of intrinsic defects can result in the formation of so-called swirl defects, which can act as nucleation centers for oxygen precipitation, degrading the minority carrier lifetime [24]. In a different study, Usami *et al.* [26] reported a correlation between lifetime degradation and formation of vacancies and V-O complex defects on swirls-containing crystals. On the contrary, lifetime degradation in swirls-free crystals was related to the formation of tiny defects, dispersed along the crystal, generated during the crystal growth as a result of the suppression of swirl defect generation [26]. In all cases, these defects act as recombination centers producing lifetime degradation.

Separately, Graff and Pieper [27] explained the variation in lifetime observed at room temperature after specimens were quenched from high temperature by assuming reactions between impurities and intrinsic defects, or just as a result of intrinsic defects, which act as recombination centers. One example of this are vacancies, which become frozen-in during quenching and can react with residual impurities present on interstitial sites, yielding recombination centers. Moreover, vacancies can also act as recombination centers themselves [27].

Heating and cooling rates of no more than 1°C/sec were employed for this work, which should allow for sufficient thermal equilibration and prevention of excessive defect freeze-in. However, unlike in conventional diffusion-based cell production, where optimized emitter and/or back-surface field (BSF) formation processes provide beneficial defect gettering, these epitaxial structures received no such treatment. Therefore, the degradation observed here is considered as effectively anomalous mainly because it is not being automatically mitigated by the cell formation process. Future epitaxial process development should be able to take this issue into account.

3.2.2. Lifetime recovery during phases 2–4.

According to Table I, a progressive lifetime recovery is observed during the III–V epitaxial steps, Phases 2–4. This lifetime recovery is most consistent with a passivation mechanism where the previously formed (in Phase 1) recombination center defects are effectively mitigated. The most likely source of this effect is that of H passivation through the in-diffusion of atomic H. Atomic H is an extremely fast interstitial diffuser in Si [21], capable of penetrating deep into (or even entirely through) the wafer at the process conditions employed during the III–V epitaxy steps (Phases 2–4).

The role of atomic H as a versatile passivation agent has been widely reported in the literature [12,28–33]. In particular, its effect on neutralizing recombination centers in Si has been well-studied. For example, the suppression of swirl defect formation by H doping has been reported by several authors [34,35]. Moreover, it has been reported that hydrogenation of metallic impurities in Si wafers can yield a significant reduction in associated trap states, with reported reductions for interstitial Fe of a factor of 5 [32] and up to nearly two orders of magnitude for Zn [28,36]. Similarly, Ammerlaan [28] and Stolz *et al.* [36] reported the passivation of a range of both acceptors (B, Al, Ga, Be, and Zn) and donors (P, As, and Sb) by the formation of stable acceptor-H and donor-H complexes. Similarly, Karzel *et al.* demonstrated the beneficial effect of hydrogenation (by means of atomic H) on the improvement of the average effective bulk minority carrier lifetime in multicrystalline Si [30], and Ulyashin *et al.* reported the lifetime improvement via H-passivation of dangling bonds within bulk structural defects in single-crystal Si [12]. Therefore, it is very likely that, regardless of the specific source of the lifetime degradation, atomic H can act as an effective passivant, yielding a recovery of the minority carrier lifetime.

The observed lifetime recovery during the growth of the III–V layers (Phases 2–4) suggests a link to the introduction of the group-III and/or group-V precursors into the reactor chamber. Additionally, the differing extents of recovery—approximately an order of magnitude through Phases 2 and 3, and another order of magnitude through Phase 4—suggests a dependence upon the identities of the precursor species themselves and/or the associated growth temperature for the different phases. Phases 2 and 3 utilized TEGa and TBP as the Ga and P precursors, respectively, which should provide a small amount of available atomic H [37]; Phase 4 utilized TMGa [38] and PH_3/AsH_3, the latter of which (i.e., group-V hydrides) should provide substantially more atomic H, especially at the higher (725°C) growth temperature [39]. Although the SiH_4 used for the homoepitaxial Si in Phase 1 would also be expected to yield some atomic H, the combination of process temperature (760°C) and pressure (150 mbar) actually favors the formation of H_2 [40]. Additionally, note that dissociation of H_2 itself at such temperatures, without some catalyzing or reactive species, has also been reported to be disfavored [41].

The presence of P-based precursors also suggests some potential similarity to the recovery observed during high-temperature PH_3 annealing, as previously described by the authors [17]. However, it is important to point out that this prior work demonstrated significant levels of P in-diffusion because of the high (≥800°C) annealing temperatures and direct exposure to the Si surface, thereby likely offering some degree of defect gettering; no significant P diffusion is found for the lower temperature epitaxial GaP/Si case presented here [15]. Interestingly, a small amount (~5×10^{17} cm^{-3}) of group-V species (As and P) was indeed found to incorporate via background doping during the homoepitaxial Si growth [15], indicating that their presence alone is insufficient to yield lifetime recovery.

To further investigate the likelihood of an atomic H passivation mechanism, a final set of experiments was conducted, the results of which are presented in Table III. Here, 250 nm GaP-on-Si wafers were produced following Phases 1–3, as described previously. These samples were cleaved into pieces and subjected to a range of anneals within the MOCVD reactor under different precursor ambients (PH_3 and AsH_3) and temperatures (from 550 to 725°C). In this sense, by increasing the annealing temperature, a more effective pyrolysis of the corresponding hydride is expected, and consequently higher doses of H will be applied. The as-grown material (i.e., unannealed) is denoted as sample B. In this case, the Si substrates used were high-quality Czochralski (Cz) wafers, with the same nominal doping and resistivity, as well as a similar as-received minority carrier lifetime (sample A), as the Fz wafers used in the prior measurements. Note that the Phase 3 lifetime measured in sample B here is also similar to that seen for the Fz results shown in Table I.

The item of note is the result observed for Sample C, which received a 90 min 725°C anneal in PH_3. This anneal was found to provide more than an order of magnitude increase in the lifetime, yielding a recovery back to (and even slightly higher than) the as-received value for the Cz substrate, similar to that seen with the Fz-Si after Phase 4 growth (Table I). First, this sample, along with Samples A and B, suggests no impact of the wafer type (Cz versus Fz) on the lifetime degradation and the recovery mechanisms for this process. Second, and more importantly, this result supports the conclusion of H-passivation as the source of lifetime recovery. As noted earlier, previous investigation of potential P-diffusion into Si across the GaP/Si interface via annealing under these same conditions (725°C, PH_3/H_2 ambient, 120 min) revealed to appreciable diffusion profile, as measured by secondary ion mass spectroscopy (SIMS) [15] leaving H-passivation as the only likely contender.

Consistent with the hypothesis of lifetime recovery due to atomic H-passivation and reduced pyrolysis kinetics of the group-V hydrides at lower temperatures (thus yielding

Table III. Average minority carrier lifetime for Czochralski (Cz) Si wafers after III–V heteroepitaxy. All epitaxial material and some wafer surface material have been removed for measuring the bulk lifetime. An as-received Cz wafer was included for comparison.

Phase	Temperature (°C)	Growth time (min.)	Precursor species	Δn (cm^{-3})	t (μs)
A	—	—	—	10^{15}	444
B	550	30	H_2,TBP, TEGa	10^{14}	40
C	725	90	H_2, PH_3	10^{15}	475
D	650	90	H_2, PH_3	10^{15}	165
E	650	90	H_2, AsH_3	10^{15}	336
F	600	90	H_2, AsH_3	10^{15}	370
G	550	90	H_2, AsH_3	10^{15}	279

a lower dose of atomic H), when decreasing the PH_3 annealing temperature from 725 to 650°C (Sample D), the degree of lifetime recovery is also reduced, down to 165 µs, only about 4× greater than the initial (Phase 3) value. Elucidation of whether this PH_3-based recovery is limited by a lack of available atomic H or the result of the lower temperature is not possible because of the limited range of PH_3 flows available in the MOCVD reactor used for this work. Therefore, to further examine this effect, an AsH_3 anneal under identical conditions, Sample E (650°C, 90 min), was also performed. The AsH_3 anneal resulted in an ~8× increase in lifetime over the initial value, which double that observed under PH_3 (Sample D). In fact, a similar degree of recovery was observed for AsH_3-based anneals all the way down to 550°C. At such lower temperatures, the likelihood of any group-V diffusion into the Si is effectively eliminated, further supporting the H-passivation mechanism.

The difference in magnitude of recovery observed for the two different species at 650°C is worth some examination. Because these anneals were completed at the same temperature, the difference suggests that the passivation is not limited by temperature but rather the availability of atomic H, which is likely related to the relative pyrolysis kinetics and/or thermodynamics of the two hydride species. That is, AsH_3 dissociates at the surface more readily than PH_3 [39] because of its reduced molecular bond strength; AsH_3 (H_2As-*H*) has a significantly lower bond dissociation energy (for removal of the first H), 3.31 eV, versus that of PH_3 (H_2P-*H*), 3.64 eV [42]. Based on a simple thermal Boltzmann analysis, this would suggest a difference in atomic H supply from the two hydride species of two to three orders of magnitude for the range of annealing temperatures examined here, reasonably consistent with the difference in lifetime recovery observed for the AsH_3 (Sample E) versus the PH_3 (Sample D) annealing at 650°C. This same analysis also suggests strong temperature dependence for the supply of atomic H, and thus lifetime recovery, which would be consistent with the behavior observed for the PH_3 annealing at 725 and 650°C. Of course, such a simplistic analysis ignores the more complex chemical realities in such a reactive system—for example, the detailed reaction pathways on the GaP and $GaAs_yP_{1-y}$ surfaces of interest (as opposed to mere thermal "cracking") will strongly impact the actual reaction/dissociation kinetics—as evidenced by the relative lack of temperature dependence of the AsH_3 anneals (Samples E–G). It is also worth noting that a weak trend in the AsH_3 could exist, but is obscured by small errors in the lifetime measurement because of, for example, the quality of the quinhydrone surface passivation, although care was taken to ensure that all samples received identical preparation. Of note is the fact that the AsH_3 anneals were found to cause the GaP surface to roughen significantly, which was not observed for PH_3 or even pure H_2 annealing and is presumably due to As-P displacement. The roughening effect was also found to track with increasing annealing temperatures; 725°C AsH_3 annealing effectively resulted in the complete decomposition of the GaP film (thus its lack of inclusion here). As such, it may be possible that the excess strain in the GaP had some secondary impact on the underlying Si.

Finally, while H-passivation is effective for yielding a recovered lifetime, the question of longevity and stability deserves some attention. In this respect, although the passivation offered by atomic H has been reported to be indefinitely stable at lower temperatures [43], it is important to highlight that if the H supply is interrupted and the temperature is still high enough to break the associated bonds, dehydrogenation can occur [30], and lifetime will be again degraded. Accordingly, post-growth device processing must be designed and carried out using a limited thermal budget in order to avoid the depassivation of the recombination center defects. It is fortuitous, then, that the typical thermal budget for III–V-based device processing is generally low enough (≤450°C) to satisfy this requirement. Accordingly, the passivation of the atomic H is expected to remain stable during III–V/Si solar cell processing and application.

4. IMPACT OF SILICON BULK MINORITY CARRIER LIFETIME ON SOLAR CELL PERFORMANCE

In order to quantitatively assess the impact of the minority carrier lifetime evolution observed on the electrical performance of a bottom cell working in a III–V/Si MJSC, we have simulated its J_{SC}, V_{OC}, and FF at 1 sun (AM1.5D) as a function of the Si bulk lifetime. The study presented in this work has been carried using Silvaco TCAD [44], with which we have previously obtained reasonably accurate numerical simulations for conventional III–V MJSCs [45]. We have considered a Si homoepitaxial (i.e., abrupt junction) Si emitter of 90 nm with a doping concentration of $N_D = 10^{18}\,cm^{-3}$ and a 300-µm-thick base. GaP nucleation (which also serves as a heteroface window layer) and $GaAs_yP_{1-y}$ compositionally graded buffer layers have been added to the top of the Si junction. As we will focus on the bottom cell performance, no tunnel junctions or upper III–V cell structures have been included; the terminal III–V structure has been simplified to a 2.5-µm-thick $GaAs_{0.7}P_{0.3}$ layer.

The aim of simulating the complete multilayer structure is to account for the complex optical behavior of the +10 nucleation, buffer and top-cell upper layers, rather than simply applying a cut-off wavelength to the spectrum. By doing so, the light propagation through the layered structure is calculated, which has a great influence in the quantum efficiency (QE) of the bottom cell, as is seen in Figure 2. From the simulated internal QE (IQE), the 2.7-µm-thick $GaAs_{0.7}P_{0.3}$ (top cell + buffer) is found to absorb all the radiation for wavelengths up to 675 nm, according to its 1.78 eV direct gap. It is also clear that there is substantial room for improvement in the Si subcell infrared response because of the absence of any BSF,

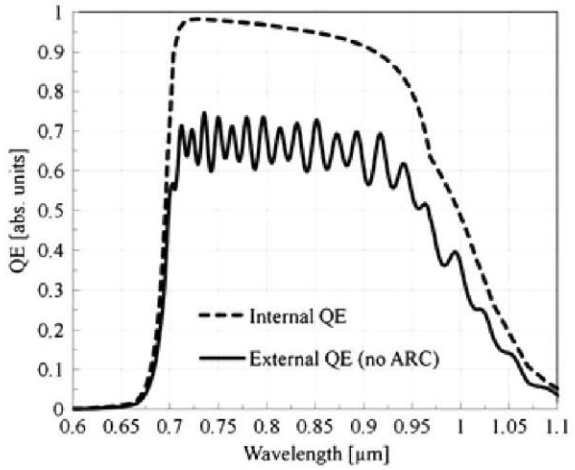

Figure 2. Simulated internal quantum efficiency (IQE) and external QE (EQE) of the Si bottom cell (i.e., with no back-surface field and GaP/Si interface recombination velocity of 10E6 cm/s). Recall that the simulated cell structure includes the GaP nucleation/window, GaAsyP1-y compositionally graded buffer, and $GaAs_{0.7}P_{0.3}$ top layers. No anti-reflecting coating (ARC) or rear reflector was included in the simulated structure.

passivation strategy, or optical reflector at this first stage. The simulated external QE (EQE) shows the well-known oscillations because of the resonant cavity effect in the quasi-transparent upper layers. The average EQE value is relatively low because no anti-reflecting coating has been included in the structure. More details about the simulation strategy can be found elsewhere [18].

With the aim of getting rid of the surface recombination component, and hence, to fully assess the effect of the minority carrier lifetime on the solar cell performance, Si subcell was simulated considering the presence of a non-passivated 1-μm thick, full-area BSF (doped at a theoretically ideal $N_A = 10^{20}\,cm^{-3}$) and considering a moderate GaP/Si interface recombination velocity of 10^2 cm/s. Contour plots for this simulation series are presented in Figure 3. Correspondingly, Table IV shows the evolution of Si bulk lifetime during the growth of the III–V structure

Table IV. Simulated performance metrics for a Si bottom cell—with a low interface recombination velocity and considering the presence of a back-surface field—with respect to specific bulk Si lifetime values measured at different phases of the III–V/Si epitaxial process. A base doping level of $N_A = 2 \cdot 10^{15}\,cm^{-3}$ was used.

τ_b (μs)	J_{SC} (mA/cm^2)	V_{OC} (mV)	FF (%)
1.0	10.19	475	78.75
72	13.94	558	81.13
467	14.27	611	81.15

and its simulated impact on the bottom cell performance for this scenario. Parameters in the table were calculated considering a base doping of $N_A = 2 \cdot 10^{15}\,cm^{-3}$, to reproduce the experimental conditions of this study (i.e., the doping level of the wafers included in the experimental section was $N_A = 2 \cdot 10^{15}\,cm^{-3}$).

Figure 3 and Table IV show that under these conditions (i.e., presence of a BSF and moderate recombination velocities), J_{SC} and V_{OC} are not being limited by the recombination at the surfaces, instead becoming limited by the minority carrier lifetime in the Si bulk. As a result, any processes contributing to a recovery of minority carrier lifetime would produce a corresponding increase in the PV performance of the Si bottom cell (and, accordingly, the full multijunction device into which it will be integrated).

As an example, Table IV evidences that the increase of the bulk lifetime that is produced during the growth of the GaAsP buffer layer in the experimental samples (i.e., moving from 72 to 467 μs) is shown to have a deep impact on the bottom cell electrical performance, especially on its V_{OC} and J_{SC}. Moreover, the base minority carrier lifetime has important repercussions on the internal quantum efficiency of the Si bottom cell, as evidence (Figure 4), observing a clear degradation of this parameter as the lifetime becomes lower.

However, it is important to highlight that despite the evolution of bulk lifetime along the different phases involved in the growth of the III–V/Si structure has reported to deeply affect the performance metrics of the silicon

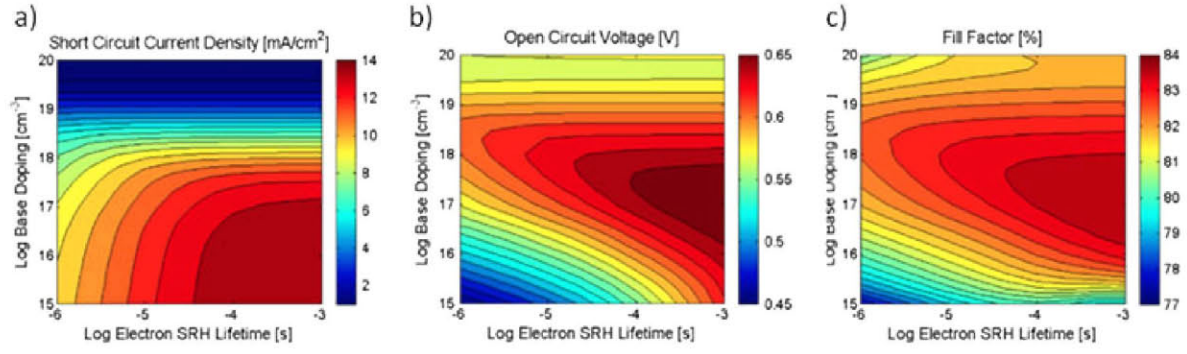

Figure 3. Contour plots of Si bottom cell performance metrics as a function of base doping and minority carrier (electron) lifetime. (left) Short circuit current density (JSC); (center) open circuit voltage (VOC); (right) fill factor (FF).

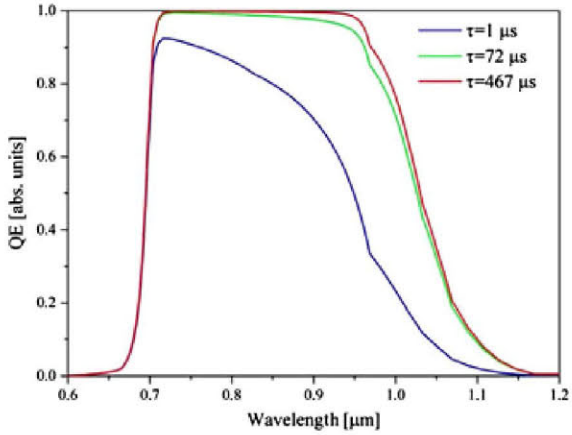

Figure 4. Simulated IQE of the Si bottom cell (i.e. with BSF and GaP/Si interface recombination velocity of 10E2 cm/s) for each lifetime value included in Table IV. Recall that the simulated cell structure includes the GaP nucleation/window, GaAsyP1-y compositionally-graded buffer, and GaAs0.7P0.3 top layers. No ARC or rear reflector was included in the simulated structure.

bottom cell (Table III), the improvement of the J_{SC} with the minority carrier lifetime is only guaranteed until a certain point; that is to say, there is a lifetime value beyond which an increase on lifetime does not pay back in an improvement of the short circuit current (~500 μs for this particular IRV). Consequently, the increase of the lifetime beyond this point does not provide much improvement of the solar cell performance. In this sense, we can confirm that the minority carrier lifetimes obtained after the growth of the GaAsP-graded buffers are sufficiently high for obtaining a high-quality solar cell. Increasing this value will not have important repercussions on the solar cell PV behavior when having a recombination velocity of 10^2 cm/s at the GaP/Si interface.

While, in reality, subcell design optimization with respect to actual realized materials properties (minority carrier lifetime, front and back recombination velocity, etc.) would help to improve the performance under the conditions considered here, the trends observed are nonetheless valid and provide strong motivation for focusing on not only lifetime recovery in the epitaxial process but also recombination velocity in the device structures where possible.

5. CONCLUSIONS

The evolution of the Si bulk minority carrier lifetime during key phases in the fabrication of an MOCVD-grown III–V-on-Si epitaxial structure has been analyzed. A two order of magnitude reduction in p-type Si lifetime during Si homoepitaxy, followed by a complete recovery over the course of subsequent III–V heteroepitaxy, was observed. On the one hand, it was suggested that the lifetime degradation (observed in Step 2) is related to the activation of recombination centers. The precise nature of such recombination centers has not yet been unequivocally determined. Remaining possible degradation mechanisms include contamination by fast-diffusing recombination species, such transition metals (e.g., Fe) or the formation of thermally induced crystalline defects, such as swirls, point defects or complexes with typical pre-existing atoms of C and/or O. Fortuitously, a stepwise lifetime recovery is observed during the subsequent III–V (GaP, $GaAs_yP_{1-y}$) heteroepitaxy. This important recovery is most likely a result of passivation of the thermally generated recombination centers by means of atomic H, generated through the pyrolysis of precursor species during the III–V growth. This recovery mechanism was confirmed by the observation of lifetime recovery after annealing low-lifetime GaP/Si samples at different temperatures in an AsH_3 ambient. Ultimately, the phenomena described herein—the substantial and dynamic impact on the bulk minority carrier lifetime within the Si substrate, both degradation and recovery, as a direct result of the III–V heteroepitaxial process—has wide-reaching consequences for III–V/Si PV and will need to be accounted for in the development of future production processes.

In order to assess the importance of having a high minority carrier base lifetime in the overall PV performance of the associated Si bottom cell, the TCAD simulations, as a function of the Si bulk lifetime, were performed. When sufficiently low recombination velocities were considered (by adding a BSF and reducing the IRV at the GaP/Si interface), the cell performance shifted to be bulk recombination limited, making the lifetime recovery discussed herein a key component for yielding high-performance cells, showing special importance on J_{SC}, V_{OC} and IQE.

In summary, it was observed that minority carrier lifetime of the Si substrates evolves during the processes needed to manufacture a hybrid III–V/Si MJSC. Such evolution may imply processes with deleterious effects on the lifetime that, if not recovered, will have a detrimental impact on the Si bottom cell performance. Therefore, designing processes that promote the recovery of the lifetime during the growth of the III–V structure is a must to support the production of high-performance multijunction III–V/Si solar cells.

ACKNOWLEDGEMENTS

Some of the experiments in this work were carried out during a research stay of Ms Elisa García-Tabarés at the Nanotech West Lab of The Ohio State University. We acknowledge the strong support of the staff at OSU and the financial support of the Universidad Politécnica de Madrid for her stay. This work was supported by FP7 Program of the European Union through project NGCPV (283798), by the Spanish Ministerio de Economía y Competitividad through project with reference TEC2012-37286. It was also supported by the Department of Energy under the FPACE program (DE-EE0005398) and the Ohio Office of Technology Investment Third Frontier program.

REFERENCES

1. Andre CL, Carlin JA, Boeckl JJ, Wilt DM, Smith MA, Pitera AJ, Lee ML, Fitzgerald EA, Ringel SA. Investigations of high-performance GaAs solar cells grown on Ge-$Si_{1-x}Ge_x$-Si substrates. *IEEE Transactions on Electron Devices* 2005; **52**(6): 1055–1060.
2. Geisz JF, Olson JM, Romero MJ, Jiang CS, Norman AG. Lattice-mismatched GaAsP solar cells grown on silicon by OMVPE. *IEEE 4th World Conference on Photovoltaic Energy Conversion*, Waikoloa, HI, USA, 2006.
3. Grassman TJ, Brenner MR, Rajagopalan S, Unocic R, Dehoff R, Mills M, Fraser H, Ringel SA. Control and elimination of nucleation-related defects in GaP/Si(001) heteroepitaxy. *Applied Physics Letters* 2009; **94**(23): 2321061–2321063.
4. Ringel SA, Carlin JA, Andre CL, Hudait MK, Gonzalez M, Wilt DM, Clark EB, Jenkins P, Scheiman D, Allerman A, Fitzgerald EA, Leitz CW. Single-junction InGaP/GaAs solar cells grown on Si substrates with SiGe buffer layers. *Progress in Photovoltaics: Research and Applications* 2002; **10**(6): 417–426.
5. Schöne J, Dimroth F, Bett AW, Tauzin A, Jaussaud C, Roussin JC. III-V solar cell growth on wafer-bonded GaAs/Si-substrates. *IEEE 4th World Conference on Photovoltaic Energy Conversion*, Waikoloa, HI, USA, 2006.
6. Tanabe K, Watanebe K, Arakawa Y. III-V/Si hybrid photonic devices by direct fusion bonding. *Scientific Reports* 2012; **2**: 349.
7. Bolkhovityanov YB, Pchelyakov OP. GaAs epitaxy on Si substrates: modern status of research and engineering. *Physics-Uspekhi* 2008; **51**: 437–456.
8. Grassman TJ, Brenner MR, Carlin AM, Rajagopalan S, Unocic R, Dehoff R, Mills M, Fraser H, Ringel SA. Toward metamorphic multijunction GaAsP/Si photovoltaics grown on optimized GaP/Si virtual substrates using anion-graded $GaAs_yP_{1-y}$ buffers. *34th IEEE Photovoltaic Specialists Conference* (*PVSC*), Philadelphia, PA, USA, 2009.
9. Hayashi K, Soga T, Nishikawa H, Jimbo T, Umeno M. MOCVD growth of GaAsP on Si for tandem solar cell application. *Proceedings of the 24th IEEE Photovoltaics Specialist Conference*, Hawaii,USA, 1994.
10. Grassman TJ, Brenner MR, Gonzalez M, Carlin AM, Unocic RR, Dehoff RR, Mills MJ, Ringel SA. Characterization of metamorphic GaAsP/Si materials and devices for photovoltaic applications. *IEEE Transactions on Electron Devices* 2010; **57**(12): 3361–3369.
11. Roesener T, Döscher H, Beyer A, Brückner S, Klinger V, Wekkeli A, Kleinschmidt P, Jurecka C, Ohlmann J, Volz K, Stolz W, Hannappel T. MOVPE growth of III-V solar cells on silicon in 300 mm closed coupled showerhead reactor. *25th European Photovoltaic Solar Energy Conf. and Exhibition*, Valencia, Spain, 2010.
12. Ulyashin A, Simoen E, Cernel L, De Wolf S, Dekkers H, Beaucarne G, Poortmans J, Rafí JM, Claeys C. Effective lifetime of minority carriers in silicon: the role of heat- and hydrogen plasma treatments. *8th High Purity Silicon Conference*, Oslo, Norway, 2004.
13. García-Tabarés E, Martín D, García I, Rey-Stolle I. Understanding phosphorus diffusion into silicon in a MOVPE environment for III–V on silicon solar cells. *Solar Energy Materials and Solar Cells* 2013; **116**(0): 61–67.
14. García-Tabarés E, García I, Martín D, Rey-Stolle I. Influence of PH_3 exposure on silicon substrate morphology in the MOVPE growth of III–V on silicon multijunction solar cells. *Journal of Physics D: Applied Physics* 2013; **46**(44): 4451041–4451047.
15. Grassman TJ, Carlin JA, Galiana B, Yang F, Mills MJ, Ringel SA. MOCVD-grown GaP/Si subcells for integrated III-V/Si multijunction photovoltaics. *IEEE Journal of Photovoltaics* 2014; **4**(3): 972–980.
16. Grassman TJ, Carlin JA, Galiana B, Yang L-M, Yang F, Mills MJ, Ringel SA. Nucleation-related defect-free GaP/Si(100) heteroepitaxy via metal-organic chemical vapor deposition. *Applied Physics Letters* 2013; **102**(14): 1421021–1421024.
17. García-Tabarés E, Rey-Stolle I. Impact of metal-organic vapor phase epitaxy environment on silicon bulk lifetime for III–V-on-Si multijunction solar cells. *Solar Energy Materials and Solar Cells* 2014; **124**(0): 17–23.
18. Martin D, Garcia-Tabares E, Rey-Stolle I. Numerical simulation and experimental facts about bottom-cell optimization for III-V on silicon multijunction solar cells. *IEEE 39th Photovoltaic Specialists Conference* (*PVSC*), Tampa, Florida, USA, 2013.
19. Takato H, Sakata I, Shimokawa R. Surface passivation of silicon substrates using quinhydrone/methanol treatment. *Proceedings of 3rd World Conference on Photovoltaic Energy Conversion* Osaka, Japan, 2003.
20. Coletti G. *Impurities in silicon and their impact on solar cell performance*. Utrecht University: Utrech, 2011.
21. Bracht H. Diffusion mechanisms and intrinsic point-defect properties in silicon. *MRS Bulletin* 2000; **25**(06): 22–27.
22. Grünebaum D, Czekalla T, Stolwijk NA, Mehrer H, Yonenaga I, Sumino K. Diffusion and solubility of zinc in dislocation-free and plastically deformed silicon crystals. *Applied Physics A* 1991; **53**(1): 65–74.
23. Macdonald DH, Geerligs LJ, Azzizi A. Iron detection in crystalline silicon by carrier lifetime measurements

for arbitrary injection and doping. *Journal of Applied Physics* 2004; **95**(3): 1021–1028.
24. Susi E. Recombination mechanisms in crystalline silicon: bulk and surface contributions. *International Journal of Photoenergy* 1999; **1**: 1–9.
25. Wang TH, Ciszek TF, Schuyler T. Micro-defect effects on minority carrier lifetime in high purity dislocation-free silicon single crystals. *Solar Cells* 1988; **24**(1–2): 135–145.
26. Usami A, Fujii Y, Monoka K. The effect of swirl defects on the minority carrier lifetime in heat-treated silicon crystals. *Journal of Physics D: Applied Physics* 1977; **10**(6): 899–909.
27. Graff K, Pieper H. Carrier lifetime measurements for process monitoring during device production. In *Lifetime Factors in Silicon*. American Society for Testing and Materials: Baltimore, 1980.
28. Ammerlaan CAJ. Hydrogen. In *Silicon Evolution and Future of a Technology*, Sieffter P, *et al.*, (eds). Springer: Germany, 2004.
29. Hallam BJ, Wenham SR, Hamer PG, Abbott MD, Sugianto A, Chan CE, Wenham AM, Eadie MG, Xu G. Hydrogen passivation of B-O defects in czochralski silicon. *Energy Procedia* 2013; **38**(0): 561–570.
30. Karzel P, Frey A, Fritz S, Hahn G. Influence of hydrogen on interstitial iron concentration in multicrystalline silicon during annealing steps. *Journal of Applied Physics* 2013; **113**(11): 1149031–1149039.
31. Kazmerski LL. Investigation of impurity neutralization and defect passivation in polycrystalline silicon solarcells. *MRS Online Proceedings Library* 1987; **106**: 1505–1508.
32. McLean K, Morrow C, Macdonald D. Activation energy for the hydrogenation of iron in p-type crystalline silicon wafers. *IEEE 4th World Conference on Photovoltaic Energy Conversion*, Waikoloa, HI, USA, 2006.
33. Pearton S, Corbett J, Stavola M. Shallow impurity passivation by atomic hydrogen. In *Hydrogen in Crystalline Semiconductors*. Springer: Berlin Heidelberg, 1992.
34. Ciszek TF. Copper decoration and X-ray topography of point defects in dislocation-free silicon crystals grown under various conditions. *Semiconductor Silicon*, 1973.
35. Wang TH, Ciszek TF, Schuyler T. Charge carrier recombination centers in high-purity, dislocation-free, float-zoned silicon due to growth-induced microdefects. *Journal of Crystal Growth* 1991; **109**(1–4): 155–161.
36. Stolz P, Pensl G, Grünebaum D, Stolwijk N. Hydrogen passivation and thermal reactivation of zinc double acceptors in silicon. *Materials Science and Engineering B* 1989; **4**(1–4): 31–34.
37. Li SH, Larsen CA, Buchan NI, Stringfellow GB, Kosar WP, Brown DW. Study of tertiarybutylphosphine pyrolysis using a deuterated source. *Journal of Applied Physics* 1989; **65**(12): 5161–5165.
38. Jacko MG, Price SJW. The pyrolysis of trimethyl gallium. *Canadian Journal of Chemistry* 1963; **41**: 1560–1567.
39. Stringfellow GB. *Organometallic Vapor-Phase Epitaxy: Theory and Practice*. Stringfellow GB (ed). Academic Press, Inc.: San Diego & London, 1989: pages.
40. Cavallotti C, Masi M. Semiconductors and semimetals. In *Silicon Epitaxy*, Crippa D *et al.* (eds). Academic Press Inc., 2001.
41. Jones R, Coomer BJ, Goss JP, Hourahine B, Resende A. The interaction of hydrogen with deep level defects in silicon. *Solid State Phenomena* 1999; **71**: 173–248.
42. Luo Y-R, Cheng J-P. Bond dissociation energies in polyatomic molecules. In *CRC Handbook of Chemistry and Physics*, Haynes WM (ed). CRC Press/Taylor and Francis: Boca Raton, FL, USA, 2014–2015.
43. Pearton SJ. Neutralization of deep levels in silicon. In *Hydrogen in Semiconductors*, Pankove JI, *et al.* (eds). Academic Press, Inc.: San Diego, 1991.
44. Silvaco TCAD Manuals, (2014) http://www.silvaco.com/products/tcad/.
45. Baudrit M, Algora C. Modeling of GaInP/GaAs dual-junction solar cells including tunnel junction. *33rd IEEE Photovoltac Specialist Conference*, San Diego, California, USA, 2008.