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Improvement of performance and reliability of
GaN-based high electronmobility transistors
(HEMTs) using high-k dielectrics

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Abstract

GaN-based high electron mobility transistors (HEMTs) have been studied extensively in last decades due to its promising potential in high power, high frequency and high temperature applications, thanks to the attractive properties of GaN, such as wide band gap (3.4 eV), high critical electric field (> 3 MV/cm) and high saturation velocity. However, there are still some drawbacks, such as high leakage current, current collapse and trapping effects as well as devices stability at harsh environments. In this thesis work, the development of MOS-HEMTs (metal-oxide-semiconductor HEMTs) using high-k dielectrics and the assessment of their thermal, electrical and under irradiation stabilities have been discussed in order to provide solutions to the aforementioned issues.

Firstly, some critical steps of the devices processing, including MESA isolation and gate dielectric deposition were optimized. A good device isolation is necessary to avoid undesired leakage currents among the devices. In this case, a dry etching using ICP-RIE technique was used, and we have achieved devices with smooth surface, vertical profile as well as low leakage current by optimizing the plasma mixture. The best results come from the $\text{Cl}_2/\text{BCl}_3 = 10:1$ composition.

Afterwards, we have fabricated and characterized conventional and MOS-diodes, as well as HEMTs and MOS-HEMTs using Al_2O_3 , HfO_2 and ZrO_2 on different kinds of heterostructures (HS), such as AlGaIn/GaN , AlInN/GaN and $\text{GaN}/\text{AlInN}/\text{GaN}$. The differences among the three kinds of dielectrics on AlGaIn/GaN are very small, the dielectrics have decreased the leakage current, off-state drain current by over 10^4 , and increased the on/off ratio by 10^3 , decreased the current collapse and trapping effects in the devices, especially HfO_2 . For the dielectrics on AlInN/GaN HS, the leakage current decreased by 10^3 by Al_2O_3 and HfO_2 , and the highest on/off ratio was up to 10^5 in the ZrO_2 MOS-HEMTs. Regarding the dielectrics on $\text{GaN}/\text{AlInN}/\text{GaN}$ HS, the leakage current decreased by more than 10^7 , and the on/off ratio was increased to 10^6 in the case of HfO_2 MOS-HEMTs compared with the conventional HEMTs.

Based on the results from the comparison among the various MOS devices, another optimization technique aimed to improve the effects of dielectrics on the HS was done by pre-cleaning using KOH solution. The devices were fabricated on AlGaIn/GaN HS with HfO_2 dielectric. The results show that the pre-deposition cleaning using KOH can help reduce the trapping effects in the devices by cleaning the C related defects. The tests with short thermal annealing proved that KOH cleaning have improved the devices stability and improve the on/off ratio.

The effects of thermal cycle tests on the devices including AlGaIn/GaN HEMTs, AlInN/GaN HEMTs and $\text{HfO}_2/\text{GaN}/\text{AlInN}/\text{GaN}$ MOS HEMTs were studied, and the trapping center in the devices were analyzed to be O complex (O_N) and O vacancy (V^-).

The irradiation effects on the AlInN/GaN conventional and MOS devices with HfO₂ using H⁺ and He⁺ were analyzed. The results showed that the effects of He⁺ irradiation on the devices is much stronger than H⁺, and the higher the ion fluence, the more the damaged on the devices. Results also showed that the MOS-HEMTs are more stable than the conventional HEMTs after irradiation, due to the buffering effects of the dielectric layer.

The H⁺ irradiation on the previously fabricated devices showed that the MOS-Ds with all dielectrics are less affected by the proton irradiation than the SDs. However, in the case of AlInN/GaN and GaN/AlInN/GaN HS, the ZrO₂ MOS-Ds showed I_{rev} and I_{for} decrease after irradiation. This was explained by the improvement of isolation in the GaN buffer layer and Ni void formation within the interface. Then the DC characteristics change of the HEMTs and MOS-HEMTs after irradiation were studied. For the AlGaN/GaN and GaN/AlInN/GaN HS, the MOS-HEMTs with HfO₂ and Al₂O₃ showed very small decrease on the $I_{D,max}$, $g_{m,max}$ and V_{th} , especially HfO₂, the change is negligible. For the AlInN/GaN HS, the DC characteristics degradation of MOS-HEMTs with ZrO₂ is negligible, together with the leakage current decrease in the MOS-Ds, it is the best option for further studies under irradiation environments.

Then the effects of electrical stress on the AlGaN/GaN HEMTs and MOS-HEMTs with HfO₂ were studied. Results showed that there was critical point of gate drain voltage at about 33 V in the conventional HEMTs. Different from the previous discussion before, this critical voltage mostly probably due to the properties of the heterostructure: the crystallographic defects due to inverse piezoelectrical properties or hot electron induced traps. This was not observed in the MOS-HEMTs, implying the improvements of the MOS-HEMTs with HfO₂ dielectric layers

Finally, another new dielectric material Gd₂O₃ is studied. The thermal stability of the devices during a short thermal annealing, step thermal cycle process and long term thermal process, have been studied. The Gd₂O₃ MOS-HEMTs had a low gate leakage current and stable DC behaviour during the long thermal test. In contrast, the conventional HEMTs showed permanent degradation after a one-day thermal storage at 500°C, featured by an increased gate leakage current and on-resistance, reduced maximum drain current, maximum transconductance and gate lag ratio. In addition, we also concluded that a soft thermal annealing process enhanced the thermal stability of the MOS-HEMTs with Gd₂O₃ dielectric. Therefore, MOS-HEMTs using Gd₂O₃ dielectric with improved stability are well qualified candidates for high temperature applications compared with conventional HEMTs. Also, results during the thermal cycle tests have shown that the MOS-HEMTs were less influenced by temperature due to the protection of dielectric layer under the gate, and the trapping effects on the devices surface or in the channel interface were mitigated by the Gd₂O₃ dielectric layer.

Resumen

Los transistores de alta movilidad electrónica (HEMT, por sus siglas en inglés) basados en GaN han sido ampliamente estudiados en las últimas décadas debido a su prometedor potencial en aplicaciones a alta potencia, alta frecuencia y alta temperatura, gracias a las únicas propiedades que posee el GaN, como son su ancha banda prohibida (3.4 eV), alto campo eléctrico crítico (> 3 MV/cm) y elevada velocidad de saturación. Sin embargo, todavía presenta algunos inconvenientes, tales como una alta corriente de fugas, colapso de corriente y efectos de atrapamiento de carga, además de problemas de estabilidad en condiciones desfavorables que limitan la fiabilidad de los dispositivos y su alto potencial. En este trabajo de tesis doctoral, se han desarrollado dispositivos HEMT con puerta aislada, comúnmente denominados MOSHEMT (metal-aislante-semiconductor HEMT) haciendo uso de materiales aislantes de puerta de alta constante dieléctrica (k) y se ha evaluado su estabilidad térmica, eléctrica y bajo irradiación, con objeto de proporcionar soluciones a los problemas anteriormente mencionados. En primer lugar, algunos de los pasos críticos del proceso de fabricación de los dispositivos basados en GaN se han optimizado, como son el aislamiento eléctrico entre dispositivos (denominado aislamiento MESA) y el depósito de dieléctricos de puerta. Conseguir un buen aislamiento del dispositivo es necesario para evitar corrientes indeseables de fugas entre dispositivos. En este caso, se ha hecho uso de un ataque seco, mediante la técnica de ICP-RIE, y se han conseguido dispositivos con una superficie lisa, perfiles verticales y baja corriente de fugas tras optimizar los gases del plasma. Los mejores resultados se obtuvieron con una mezcla de Cl_2/BCl_3 con una composición de 10: 1.

Posteriormente, hemos fabricado y caracterizado diodos convencionales y diodos MOS, así como HEMTs y MOSHEMTs utilizando Al_2O_3 , HfO_2 y ZrO_2 en diferentes tipos de heteroestructuras, tales como AlGaIn/GaN , AlInN/GaN y $\text{GaN}/\text{AlInN}/\text{GaN}$. Las diferencias entre los tres tipos de dieléctricos de puerta sobre AlGaIn/GaN son muy pequeñas, los dieléctricos han reducido la corriente de fugas por la puerta, la corriente de drenador en estado apagado en un factor de más de 10^4 , un aumento de 10^3 en la relación de corriente encendido/apagado (ON/OFF) de, y una reducción del colapso de corriente y los efectos de carga atrapada en los dispositivos, especialmente con HfO_2 . Para los dieléctricos sobre AlInN/GaN , la corriente de fuga disminuyó en un factor de 10^3 en el caso de usar Al_2O_3 y HfO_2 , y la mayor relación ON/OFF era de hasta un 10^5 en los MOSHEMTs con ZrO_2 . En cuanto a los dieléctricos sobre $\text{GaN}/\text{AlInN}/\text{GaN}$, la corriente de fuga disminuyó en más de 10^7 y la relación ON/OFF aumentó a 10^6 en los MOSHEMTs con HfO_2 , respecto a HEMTs. Basándose en estos resultados, se realizó otra optimización mediante el uso de un tratamiento superficial basado en KOH previo al depósito de dieléctrico con objeto de mejorar los efectos de los dieléctricos en las heteroestructuras. En este caso, los dispositivos MOSHEMT se fabricaron en heteroestructuras AlGaIn/GaN con HfO_2 de dieléctrico

de puerta. Los resultados muestran que la limpieza usando KOH previa al depósito de HfO_2 puede ayudar a reducir los efectos de carga atrapada en los dispositivos gracias a la limpieza de los defectos relacionados con resto de C en superficie. Los procesos de recocido térmico corto demostraron que la limpieza de KOH mejora la estabilidad de los dispositivos y la relación ON/OFF.

Los efectos de ciclos térmicos se han evaluado en los dispositivos HEMT sobre $\text{AlGaIn}/\text{GaInN}$ y $\text{AlInN}/\text{GaInN}$, así como los MOSHEMTs sobre $\text{AlInN}/\text{GaInN}$ con HfO_2 obtenido que los complejos de oxígeno (O_N) y vacantes de oxígeno (V^-) actúan como centros de captura de carga.

Además, se han analizado los efectos de la irradiación con protones (H^+) y helio (He^+) en los dispositivos convencionales sobre heteroestructuras $\text{AlInN}/\text{GaInN}$ y MOS con HfO_2 . Los resultados mostraron que los efectos de He^+ irradiación son mucho más acusados que con H^+ , y a mayor fluencia de iones, mayor es el más daño causado en los dispositivos. Los resultados también mostraron que tras la irradiación los MOS-HEMTs son más estables que los HEMT convencionales, debido a los efectos de amortiguación de la capa dieléctrica. La irradiación con H^+ en los dispositivos previamente fabricados mostraron que a los diodos MOS (MOS-Ds) con todos dielectrics les afecta menos la irradiación de protones que a los SDs convencionales. Sin embargo, en el caso de $\text{AlInN}/\text{GaInN}$ y $\text{GaInN}/\text{AlInN}/\text{GaInN}$, el ZrO_2 MOS-Ds mostró una disminución en la corriente inversa (I_{rev}) y en la corriente directa (I_{for}) tras la irradiación. A continuación, se estudió el cambio de las características en DC de los HEMT y MOS-HEMT después de la irradiación. En el caso de $\text{AlGaIn}/\text{GaInN}$ y $\text{GaInN}/\text{AlInN}/\text{GaInN}$, los MOS-HEMTs con HfO_2 y Al_2O_3 mostraron una pequeña reducción en los valores de $I_{\text{D,max}}$ y $g_{\text{m,max}}$, especialmente usando HfO_2 , para el cuál el cambio es insignificante. En el caso de $\text{AlInN}/\text{GaInN}$, las características de salida en DC apenas mostraron cambios en los MOS-HEMTs con ZrO_2 , junto con la disminución de la corriente de fuga en el MOS-Ds, presentado un comportamiento muy estable bajo irradiación.

A continuación, se estudiaron los efectos de estrés eléctrico en los HEMT de $\text{AlGaIn}/\text{GaInN}$ y MOS-HEMT con HfO_2 . Los resultados mostraron que había un voltaje crítico entre drenador y puerta, aproximadamente en 33 V en los HEMT convencionales. A diferencia de la discusión anterior, este voltaje crítico se debe probablemente a las propiedades de la heteroestructura: los defectos cristalográficos debidos al campo piezoeléctrico inverso, o a trampas inducidas por electrones calientes. Esto no se observó en los MOS-HEMTs, lo que implica las mejoras de los MOS-HEMTs con HfO_2 . Finalmente, se ha estudiado otro nuevo material dieléctrico, Gd_2O_3 . Se ha analizado la estabilidad térmica de los dispositivos durante un recocido térmico corto, un proceso de ciclo térmico escalonado y un proceso térmico a largo plazo. Los MOS-HEMTs con Gd_2O_3 presentaron una baja corriente de fuga por la puerta y un comportamiento estable en DC durante el test térmico de larga duración. En cambio, los HEMTs convencionales mostraron degradación permanente después de un almacenamiento

térmico de un día a 500°C, caracterizado por un aumento de la corriente de fugas por la puerta y en la resistencia de entrada, la reducción en la máxima corriente de drenadorje, máxima transconductancia y la relación de retardo de puerta (conocido por “gate lag”). Además, también se ha llegado a la conclusión de que un proceso de recocido térmico suave mejora la estabilidad térmica de los MOS-HEMTs con Gd_2O_3 dieléctrica. Por lo tanto, los MOS-HEMTs utilizando Gd_2O_3 presentan una mejor estabilidad térmica, por lo que son firmes candidatos para aplicaciones a alta temperatura, a diferencia de los dispositivos convencionales. Además, los resultados durante las pruebas del ciclo térmico han demostrado que a los MOS-HEMTs les afecta menos el estrés térmico debido a la protección de la capa dieléctrica bajo el metal de puerta, y los efectos de carga atrapada en la superficie de los dispositivos o en la intercara del canal que son mitigados con la capa dieléctrica de Gd_2O_3 .

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List of abbreviations

2DEG	two dimensional electron gas
AFM	atomic force microscope
AlGaN	aluminum gallium nitride
AlInN	aluminum indium nitride
AlN	aluminum nitride
ALD	atomic layer deposition
CYCLE	thermal cycle test
DT	direct tunneling
FET	field effect transistor
FNT	Fowler-Nordheim tunneling
GaAs	gallium arsenide
GaN	gallium nitride
GLR	gate lag ratio
H21	transmission hybrid parameters
HEMTs	high electron mobility transistors
HPS	high pressure sputtering
HT	high temperature
ICP	inductively coupled plasma
InN	indium nitride
LONG	long thermal test
MAG	maximum available gain
MOS	metal oxide semiconductor
MOCVD	metal organic chemical vapor deposition
MSG	maximum stable gain
PAE	power added efficiency
PFE	Poole-Frenkel emission
RIE	reactive ion etching
RF	radio frequency
RMS	root mean square
RT	room temeprature
RTA	rapid thermal annealing
SE	Schottky emission
SEM	scanning electron microscopr
Si	silicon

STA	short thermal annealing
STEM	scanning transmission electron microscope
TAT	trap assisted tunneling
TFE	thermonic-field emission
TLM	transmission line method
U	unilateral gain
XRD	X-ray diffraction

List of notations

C	capacitance at $V=0$
E_C	conduction band edge
E_g	bandgap
E_T	trapping activation energy
E_V	valance band edge
g_m	transconductance
$g_{m,max}$	maximum transconductance
h	Planck constant
I_{DS}	drain current
$I_{D,max}$	maximum drain current
I_{for}	forward leakage current
I_{GS}	gate current
I_{rev}	reverse leakage current
j_n	electron current density
k_B	Boltzmann constant
L_G	gate length
L_{GD}	distance between gate and drain
L_{GS}	distance between source and gate
m_e^*	electron effective mass
N_A	acceptor-like traps density
N_C	conduction band density of state
n_s	charge density
R_C	contact resistance
R_{sheet}	sheet resistance
R_{ON}	on-resistance
R_{semi}	semiconductot resistance
R_T	total resistance
V_{BR}	breakdown voltage
V_{DS}	drain voltage
V_{GS}	gate voltage
$V_{DS,Q}$	quiescent drain voltage
$V_{GS,Q}$	quiescent gate voltage
V_{th}	threshold voltage

$I_{G,off}$	off-state gate current
I_{OFF}	off-state drain current
W_G	gate width
μ	electron mobility
ϕ_b	Schottky barrier height
Φ_M	metal work function
χ	electron affinity energy
ϵ_0	vacuum dielectric constant
ϵ_r	relative dielectric constant
σ_n	electron capture cross-section
ΔE_C	conduction band discontinuity

Chapter 1 Introduction

1.1 State of the art

The growing demand for high efficient, high power, high frequency and high temperature applications leads to the rise of wide bandgap compound semiconductors, such as silicon carbide (SiC) [1]–[3] and gallium nitride (GaN) [4]–[13], which are the most promising alternatives to silicon (Si) or gallium arsenide (GaAs). In particular, GaN is a good candidate for most of the applications due to its low price, high breakdown voltages (up to 200 V) [14]–[16], high saturation electron velocity [7], [17]–[19], good thermal conductivity [20]–[22], low parasitic capacitances, low turn-on resistance [23]–[26], and high cut off frequencies [27]–[29]. The highlight of the key properties of GaN compared with other semiconductors are shown in Figure 1-1.

Figure 1-1 GaN material merits compared to Si and GaAs [30]

GaN-based devices were firstly reported in 1990 for its potential in optoelectronic applications, such as blue/ultra-violet (UV) light emission diodes (LEDs), long lifetime violet laser diodes, UV detectors, and so on [3], [31]–[33]. In 1993, the first GaN-based transistor was demonstrated by Khan *et al.* [34], who used a thin layer of AlGaIn on top of the GaN epitaxy, with a highly conductive channel formed at the interface. Since then, a tremendous progress has been made in GaN-based high electron mobility

transistors (HEMTs) to achieve mature commercial products, in particular RF electronics, demanding high efficient RF power amplifiers for wireless applications, radar transmitters, satellites, etc., and power electronics, including DC-DC converters, power supplies, etc. [14], [35]–[38]. A summary of different application areas of GaN-based devices is shown in Figure 1-2.

Figure 1-2 Main applications of GaN-based devices

The advantages of the GaN materials enable the devices to operate at higher voltages with lower on-resistances than Si or GaAs materials, together with high power and high efficiency, make them popular for commercial productions and manufactures [14], [35]–[38]. High voltage switches operating at voltages as high as 10 kV can be designed for power conversion purposes [24], [39]–[41]. High frequency power amplifiers covering the microwave frequency spectrum (300 MHz–300 GHz) [6], [10], [42], [43] can be used for wireless and radar communications.

However, the raise of the power and frequency levels in these devices (up to 40 W/mm [44] and 265 GHz [45]) gave rise to serious challenges for the surface and interface management of the devices and their short/long term reliability under high temperature, electrical stress and heavily irradiated situations. The most relevant issues are the presence of high leakage currents, trapping effects and current collapse that strongly degrades the off-state of the transistor, decreasing both the ON/OFF current ratio and the breakdown voltage of the device [46].

In order to reduce gate leakage currents in HEMTs, several researchers have tried to use a metal-oxide-semiconductor HEMT (MOS-HEMT), by adding a thin dielectric layer between the gate metal and the semiconductor. Different gate dielectrics have been used on AlGaIn/GaN-based MOS-HEMTs,

such as SiO₂ [47]–[50], Al₂O₃ [50]–[54], HfO₂ [55]–[57], Gd₂O₃ [58]–[61], Y₂O₃ [62]–[64], or TiO₂ [65]. Besides, gate insulator has also been widely studied to mitigate the trapping phenomena [48], [55], [66]. Therefore, the use of a dielectric under the gate or in-between source and drain area, could be a good solution to both reduce the device leakage current and mitigate the current collapse.

1.2 Motivation

AlGaIn/GaN MOS-HEMTs using SiO₂ as gate dielectric is one of the most common approaches. These devices show a decrease in the gate leakage current of more than six orders of magnitude with 13 nm SiO₂ [50] and an increase in breakdown voltage to about 810 V with 23 nm SiO₂ [49]. However, one problem caused by using SiO₂ is that the SiO₂ thickness is usually high around 15-25 nm, which will enlarge the distance between gate contact and 2DEG channel. This will limit the scaling of gate length due to short channel effect in the HEMTs [67]. And there are some other problems as well, such as the reliability of the devices at high temperature, mainly because the gate leakage current increased rapidly with increasing temperature from 25°C to 200°C [48].

Considering the problems caused by the SiO₂, the most efficient approach is to use alternative materials with dielectric constant higher than that of SiO₂, which is called high-k materials or high-k dielectrics. The high-k gate oxides can decrease the leakage current without increasing the gate to channel distance, thus the drain current and output power will not change too much.

MOS-HEMTs with high-k dielectrics, such as Al₂O₃, HfO₂, Y₂O₃ and TiO₂, have shown promising results. For example, forward leakage current decreased about 6 orders of magnitude [52] and ON/OFF ratios of about 10⁹ [68] were observed on the MOS-HEMTs using 16 nm Al₂O₃. Threshold voltage instability of the Al₂O₃ based MOS-HEMTs has also been studied, which was attributed to acceptor-like deep states at Al₂O₃/GaN interface [53]. MOS-HEMTs using HfO₂ have shown about five orders of magnitude decreased gate leakage current compared with conventional HEMTs [57]. MOS-HEMTs using Y₂O₃ have proven to stand a high breakdown field to 10.7 MV/cm [64]. MOS-HEMTs using TiO₂ have showed ON/OFF ratios of about 4.5×10⁵ [65]. Most recently, MOS-HEMTs with Gd₂O₃ thin layers deposited by either molecular beam epitaxy [58] or electron-beam evaporation [59] have shown low leakage current densities and low dispersion effects by preventing surface damage on GaN or AlGaIn/GaN heterostructures. Therefore, Gd₂O₃ thin layer is also proven to be a promising candidate for gate dielectric on GaN-based MOS-HEMTs.

Concerning the thermal stability of the MOS HEMTs with high-k dielectrics, to the best of our knowledge, little work has been done to analyse the thermal stability of high-k based MOS-HEMTs and it needs to be investigated deeply. In particular on the transport mechanisms and thermal behaviours of the AlGaIn/GaN MOS-HEMTs using high-k dielectrics as the gate oxide.

Another important application field of GaN-based devices is aerospace. GaN based HEMTs have a good tolerance under irradiation. Several researchers have studied the irradiation effects on AlGaIn/GaN-based HEMTs at different energies and fluences both experimentally [69]–[71] and by simulation [64][65]. For instance, it was observed that 5 MeV proton irradiation with $2 \times 10^{15} \text{ cm}^{-2}$ [71][74][75] or $5 \times 10^{15} \text{ cm}^{-2}$ [76][77] fluences can cause DC current and transconductance decrease by 10% to 30%, with a positive threshold voltage shift, due to the generation of defect centers at the AlGaIn/GaN interfaces.

However, only a few reports have been found about the effects of irradiation on MOS-HEMTs: Al_2O_3 [78], MgO or Sc_2O_3 [79], NbAlO [80]. A recent study of proton irradiation on $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs, with a fixed proton dose of $5 \times 10^{15} \text{ cm}^{-2}$ and varying the energy from 5 MeV to 15 MeV, showed that the degradation effects is over 95% after 5 MeV proton irradiation [78], whereas the degradation mechanisms of the devices are still under discussion. Therefore, it is important to study the effects of irradiation on the MOS devices, in order to find the suitable dielectrics that can not only reduce the leakage current but also improve the irradiation hardness that can further the application in aerospace or other conditions with high irradiations.

1.3 Objectives

The main objective of the thesis is to reduce the leakage current in the GaN-based HEMTs and improve the thermal, electrical and irradiation hardness stability using MOS-HEMTs with high-k gate dielectrics. In order to achieve this goal, we are going to fabricate the GaN-based conventional and MOS HEMTs, and try to improve some of the critical steps during the fabrication; then we will study the current transport mechanisms of the diodes. When devices with low leakage current are fabricated, we will try to study their stability after thermal stress, irradiation and electrical stress.

1.3.1 Fabrication of GaN-based MOS-HEMTs

The first and one of the most important thing to do is to learn and control all the steps of fabrication procedure of GaN-based HEMTs, as well as diodes and test structures, using both AlGaIn/GaN and InAlN/GaN heterostructures (HS). This is essential to know from our own experience the limitations and advantages of the GaN technology in order to propose and optimize the processing of MOS-HEMTs.

1.3.2 Improvement of critical steps of GaN-based HEMTs fabrication

As discussed before, leakage current is one of the problem that limit the performance of GaN-based HEMTs. There are basically three sources for the leakage currents:

(a) the isolation current among the devices:

In order to reduce this isolation current, it is required to make an optimization of the MESA etching process;

(b) the leakage current through the gate during operation:

It can be reduced with an appropriate insulator between the gate metal and the heterostructure; and

(c) the off-state drain current:

It requires a good gate control of the 2DEG to minimize this contribution, therefore, the distance between the gate metal and the channel should be as small as possible.

In addition, charge trapping effects limit seriously the performance of GaN-HEMTs, so it should be mitigated with a suitable dielectric layer [81], [82]. Therefore, the optimization of the fabrication process needs to take into account both the different sources of leakage currents and the trapping effects.

1.3.3 Current transport mechanisms in AlGaIn/GaN and AlInN/GaN-based MOS-Ds

GaN-based MOS-HEMTs will be used to reduce the leakage current, so that the 2DEG in the channel will be controlled by a MOS-D gate instead of a Schottky barrier gate. Therefore, different electron transport mechanisms come into play, and the dominant conduction process will depend on the insulator, the temperature and voltage ranges [62], [81], [83]–[86]. Therefore, understanding the transport mechanisms in the diodes and MOS-Ds over a wide range of gate bias and temperatures is necessary to effectively improve the technology.

1.3.4 Devices characterizations and reliability of MOS-HEMTs under harsh environments

GaN-based HEMTs show degradation due to inter-diffusion phenomenon of the gate metals to the AlGaIn surface after thermal stress [87], and due to displacement or ionization damages after radiation stress [88], [89]. However, MOS devices are good candidates to improve the device performance under harsh conditions [90].

Therefore, the study of the failure mechanisms of different GaN-MOS-HEMTs is the basis to improve the robustness of the devices after high temperature stress or irradiation environments.

1.4 Outline

After a brief summary of the state of the art, the motivation and objective of the work are presented in the introduction section (Chapter 1). Then, an overview of the fundamentals of GaN materials and GaN-based devices, in particular the GaN-based HEMTs operating principles, are described in Chapter 2.

Chapter 3 shows a description of, firstly, the basic heterostructures used in this thesis, and secondly, the main steps and the corresponding optimizations carried out in the processing of the HEMT and MOS-HEMT devices, including device isolation, ohmic contacts for the drain and source terminals, Schottky and isolated gate contacts, and dielectrics deposition.

From Chapter 4 to Chapter 7, the main results of the behavior of the fabricated MOS-HEMT devices, with different gate dielectrics between the source and the drain contacts, are described and discussed. Chapter 4 focuses in the comparison of the HEMTs and MOS-HEMTs working at room temperature (RT), as a function of the gate dielectric and the kind of heterostructure, either AlGaN/GaN or AlInN/GaN types.

In Chapter 5, the thermal stability of various conventional HEMTs and MOS-HEMTs with different gate dielectrics and heterostructures is assessed, firstly during a step thermal test and then after a long term thermal test.

In Chapter 6, the device stability after irradiation test is analyzed. Firstly, a comparison of the effects of H^+ irradiation and alpha particles (He^+) irradiation in MOS-HEMT with HfO_2 gate dielectric on AlInN/GaN heterostructure is discussed. Then the effects of proton (H^+) irradiation at 2 MeV on AlGaN/GaN conventional HEMTs is compared as a function of the H^+ fluence in the range from $1 \times 10^{13} \text{ cm}^{-2}$ to $1 \times 10^{16} \text{ cm}^{-2}$. Then, the effects of proton irradiation at two H^+ fluences (10^{13} cm^{-2} and 10^{15} cm^{-2}) is analysed in MOS-HEMTs with different gate dielectrics, as a function of the heterostructure: AlGaN/GaN, Ga/AlIn/GaN and AlInN/GaN.

In Chapter 7, the electrical stability of the HEMT and MOS-HEMT devices with HfO_2 is assessed after an off-state drain bias step stress up to 40 V.

Chapter 8 focuses on the results of MOS-HEMTs using Gd_2O_3 gate dielectric only under the gate. The thermal stability and the robustness under H^+ and He^+ irradiation is discussed and compared with the conventional HEMTs.

Finally, the main results are summarized in Chapter 9, and the details of the samples, the fabrication process, the fabrication techniques and the devices characterization are described in Appendixes A, B, C and D, respectively.

Chapter 2 Fundamentals of GaN-based HEMTs and high-k materials

2.1 Epitaxial growth of GaN

Due to the lack of bulk GaN substrates for its high price and small size, GaN is usually hetero-epitaxially grown on foreign substrates. A suitable substrate should have similar crystallographic and physical properties to GaN, such as lattice match, thermal conductivity, coefficient of thermal expansion (CTE) and available size. Lattice mismatch, thermal conductivity and CTE difference affects the growth and reliability of the material due to strain and stress between two different materials. The most commonly used substrates are sapphire, Si, SiC and diamond. The material properties of the possible substrates suitable for GaN epitaxy growth are listed in Table 2-1.

GaN and other III-nitrides can be grown on different substrates for different purposes. For example, Si is the cheapest substrate, but it has the highest lattice mismatch with GaN, however, this issue can be improved using a GaN buffer layer to ease the lattice mismatch between substrate and the high quality GaN layer. Sapphire is the most thermally and chemically stable substrate, while the CTE is the highest. SiC has the smallest lattice mismatch to GaN and high thermal conductivity, and diamond has the best thermal conductivity, however, both substrates are quite expensive.

Table 2-1 Substrates used for GaN epitaxy growth [91]

	GaN (bulk)	Si (111)	Sapphire	6H-SiC	Diamond (S. C.)
Size (``)	2	12	4	4	< 1
Lattice mismatch (%)	-	17	13	3.4	11.8
CTE (10^{-6} K^{-1})	5.59	3.59	7.5	4.2	1.18
Isolation ($\Omega \text{ cm}$)	$\geq 10^9$	10^4	-	$\geq 10^{11}$	$\geq 10^9$
Thermal conductivity ($\text{Wm}^{-1}\text{K}^{-1}$)	250	150	34	490	2200

GaN or III-Nitrides are most commonly grown using metal-organic chemical vapour deposition (MOCVD) [92], [93] or molecular beam epitaxy (MBE) [94]–[96]. MOCVD technique uses metal organic compounds (usually trimethyl-gallium/-aluminum/-indium (TMGa/Al/In)) as gas precursors for metal sources and hydrides (usually ammonia (NH_3)) for nitride source. Firstly, the precursors are mixed, then they are introduced to the reactor chamber with suitable injector arrangement, leading them to

the heated substrate. MBE is based on Ga, Al, In vapor beams and nitrogen provided by ammonia or N_2 passing through a RF plasma under ultra-high vacuum (UHV) conditions, encroached on a hot substrate.

2.2 GaN properties

The reason why GaN with a wurtzite crystal structure are so popular is that it has direct wide band gaps, high breakdown voltage and high mechanical and thermal stabilities [37], [97]. The wide band-gap enables devices to withstand high electric fields; direct band-gap allows devices for light emission or light detection applications; high charge density and mobility enables them for high frequency applications; and high mechanical/thermal stability combined with good thermal conductivity enables them for high temperature applications. A comparison of basic parameters among the most well-known materials is shown in Table 2-2.

Table 2-2 Comparison of the basic parameters for some competing semiconductors [37], [98]

	Si	GaAs	4H-SiC	GaN
Band-gap (eV)	1.11	1.43	3.26	3.42
Electron mobility ($cm^2V^{-1}s^{-1}$)	1350	6000	800	900
Hole mobility ($cm^2V^{-1}s^{-1}$)	450	330	120	300
Electron saturation velocity (cm/s)	1.0×10^7	2.0×10^7	2.0×10^7	2.5×10^7
Breakdown field (MV/cm)	0.25	0.35	2.0	3.5
Thermal conductivity ($Wcm^{-1}K^{-1}$)	1.5	0.46	4.9	1.7
Relative Dielectric constant	11.8	12.8	9.7	9.0

2.2.1 Lattice structure and energy band gap of GaN

GaN with wurtzite Ga-face structure is the most commonly used for III-N HEMTs, it is shown in Figure 2-1 [99]. It is a direct band-gap semiconductor with a wide band-gap energy of 3.42 eV at room temperature (RT). Ternary alloys such as AlGaIn, AlInN and InGaIn are usually used in the design of GaN-based devices, and the band-gap energy depends on the composition according to Vegard's law [100],

$$E_{g,A_xB_{1-x}N} = E_{g,AN}x + E_{g,BN}(1-x) - b_{A,B}x(1-x) \quad 2-1$$

where $E_{g,AN}$ and $E_{g,BN}$ are the band-gap energy of the two III-N compounds, $b_{A,B}$ is the bowing parameter of AN and BN. The band-gap energy at RT of AlN and InN are 6.2 eV and 0.65 eV, respectively. The bowing parameter is about 0.35 eV for AlGa_xN_{1-x}, 1.8 eV for InGa_xN_{1-x} [101] and in the case of AlInN, it depends on the composition [102].

Figure 2-1. Wurtzite structure of GaN (Ga-face) [99]

The temperature dependence of the semiconductors band gap energy is usually described using Varshni formula [103]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T + \beta} \quad 2-2$$

where $E_g(0)$ is the semiconductor band gap energy at 0 K, and α and β are specific parameters of the materials. The Varshni parameters α and β for wurtzite III-nitride semiconductors are shown in Table 2-3.

Table 2-3 Band gap energy at 0 K ($E_g(0)$), and Varshni parameters α and β [104][105]

Materials	$E_g(0)$ (eV)	α (meV/K)	β (K)
GaN	3.510	0.909	830
AlN	6.25	1.799	1462
InN	0.78	0.245	624

2.2.2 Polarizations

Polarization is the formation of dipole moments in response to external electric field. One unique property of III-nitrides is the strong spontaneous polarization along the c-axis of the growth direction in wurtzite structures (Figure 2-1). In fact, the in-plane symmetry causes the net polarization dipole inside a unit cell to vanish, leaving only a non-vanishing dipole along the c axis. In the ideal wurtzite structure, the atoms place in perfect tetrahedral sites and the ratio of the lattice constants in the [0001] direction (c_0), and in plane (a_0) is

$$\frac{c_0}{a_0} = \sqrt{\frac{8}{3}} = 1.633 \quad 2-3$$

However, due to relaxation in actual wurtzite crystals, these values differ from those in the ideal structure, and the spontaneous polarization is related with the deviation of the value from the ideal condition. The larger deviation the structure has, the higher spontaneous polarization P_{sp} the compounds show (Table 2-4). Therefore, the spontaneous polarization is even reinforced in actual wurtzite structures.

Table 2-4 Lattice constants for the III-nitrides [104]

Materials	c_0 (nm)	a_0 (nm)	$\frac{c_0}{a_0}$	P_{sp} (C/m ²)
GaN	0.5185	0.3189	1.626	-0.034
AlN	0.4982	0.3112	1.601	-0.090
InN	0.5703	0.3545	1.612	-0.042

The strain in the III-N semiconductor can induce piezoelectric polarization P_{pz} due to the change in the c_0/a_0 ratio [106], [107], and it can be calculated using [108]:

$$P_{PE} = 2 \left(\frac{a-a_0}{a_0} \right) \left(e_{31} - \frac{e_{33}C_{13}}{C_{33}} \right) \quad 2-4$$

where a is the deformation lattice constant, $2 \left(\frac{a-a_0}{a_0} \right)$ is the in-plane strain, e_{13} and e_{33} are the piezoelectric coefficients, C_{13} and C_{33} are the elastic coefficients. All these values of the relevant nitrides interesting for this work are shown in Table 2-5.

Table 2-5 C_{13} and C_{33} , e_{13} and e_{33} , P_{SP} and P_{PE} values of III-N compounds [104][108]

Materials	C_{13} (GPa)	C_{33} (GPa)	e_{13} (pm/V)	e_{33} (pm/V)	P_{sp} (C/m ²)
GaN	106	398	-1.6	3.1	-0.034
AlN	108	373	-2.1	5.4	-0.090
InN	92	224	-3.5	7.6	-0.042
Al _x Ga _{1-x} N	2x+106	-25x+398	-0.5x-1.6	2.3x+3.1	-0.056x-0.013
Al _x In _{1-x} N	16+92	149x+224	1.4x3.5	-2.2x+7.6	0.022x-0.042

The total polarization is the sum of the spontaneous and piezoelectric polarizations ($P_{tot} = P_{sp} + P_{pz}$). If the thicknesses of the layers are thin enough (around several nanometers), the high polarization field can induce large band bending over small distances, which is essential to the formation of the 2 dimensional electron gas (2DEG) in III-nitrids. Besides the polarization properties of the III-nitrides, the other physical properties of the materials are shown in Table 2-6.

Table 2-6 Properties of GaN, AlN and InN Wurtzite crystal structure [109]

	Unites	GaN	AlN	InN
Density	g/cm	6.15	3.23	6.81
Static dielectric constant		8.9	8.5	15.3
High-frequency dielectric constant		5.35	4.77	8.4
Energy gap (Γ Valley)	eV	3.39	6.2	1.89
Effective mass (Γ Valley)	m_e	0.20	0.48	0.11
Polar optical phonon energy	meV	91.2	99.2	89.0
Lattice constant, a(c)	Å	3.189 (5.185)	3.11 (4.98)	3.54 (5.70)
Electron mobility	cm ² /Vs	1000	135	3200
Hole mobility	cm ² /Vs	30	14	
Saturation velocity	cm/s	2.5×10^7	1.4×10^7	2.5×10^7
Peak velocity	cm/s	3.1×10^7	1.7×10^7	4.3×10^7
Peak velocity field	kV/cm	150	450	67
Breakdown field	V/cm	$> 5 \times 10^6$		
Light hole mass	m_e	0.259	0.471	

Thermal conductivity	W/cm-K	1.5	2	
Melting point	°C	2530	3000	1100

2.2.3 2DEG formation in AlGa(In)N/GaN heterostructures

The accumulation of polarization charge in the interface, together with the conduction band offset between GaN and AlGa(In)N leads to the formation of an triangular electronic quantum well.

The amount of polarization charge at the interface ($\sigma_{\text{interface}}$) depends on the polarization differences between the two layers (Figure 2-2), given by:

$$\sigma_{\text{interface}} = ((P_{sp, \text{ GaN}}) - (P_{sp, \text{ AlGa}} + P_{pz, \text{ AlGa}})) \quad 2-5$$

The total polarization fields in AlGaN/GaN epitaxy lead to a large concentration of positive sheet charges. Electrons would be attracted by the positive charges, causing the conduction band edge drops below the Fermi level, thus the electrons are confined at the hetero interface, as shown in Figure 2-3.

The confined electrons are quantized in two dimensions, leading to the formation of electrons on the GaN side of the interface, named 2DEG [108], [110]. In this way, high electron concentration and mobility can be achieved without additional doping. The charge density (n_s) is usually about $1 \times 10^{13} \text{ cm}^{-2}$.

Figure 2-2. Polarization induced sheet charge density and directions of the spontaneous and piezoelectric polarization in Ga- faced (a) relaxed and (b, c) strained AlGaIn/GaN heterostructures. [108]

Figure 2-3. Energy-band diagrams for AlGaN/GaN heterostructure, electrons flow into the GaN side, accumulate at the interface and form 2DEG [110]

AlInN/GaN heterostructure shows similar electrical properties to AlGaN/GaN, however it has the possibility of strain-free lattice-matched structure, by using $\text{Al}_{0.82}\text{In}_{0.18}\text{N}/\text{GaN}$ [111]–[114]. Moreover, E. Kohn *et al.* showed that using $\text{Al}_{0.815}\text{In}_{0.185}\text{N}/\text{GaN}$ HEMT a good thermal stability up to 1000°C can be achieved [113].

2.3 GaN-based HEMTs operating principles

The main feature of GaN-based HEMTs for high power and high frequency applications is the 2DEG, as discussed in chapter 2.2.3. A spontaneous polarization is present in both AlGaN and GaN layers, due to the intrinsic properties described in chapter 2.2.2. Due to the strain caused by lattice mismatch of GaN and AlGaN, there is piezoelectric polarization existing in the AlGaN layer, the total polarization fields in AlGaN/GaN epitaxy lead to a large concentration of positive sheet charges. Electrons are attracted by the positive charges, forming a 2DEG at the AlGaN/GaN interface.

Figure 2-4 Schematic configuration of AlGaN/GaN HEMTs.

A rough picture of the schematic configuration of this kind of AlGaIn/GaN HEMTs is shown in Figure 2-4. There are three terminals on the devices, the source (S), the drain (D) and the gate (G) contacts. The main geometry parameters are gate length (L_G), gate width (W_G), gate source distance (L_{GS}) and gate drain distance (L_{GD}).

There are two operational states of the devices: ON-state and OFF-state. When the gate bias is more positive than the threshold voltage, it is ON, allowing electrons flowing from the source ohmic terminal to the drain ohmic terminal continually. When the gate biased is less positive than the threshold voltage, it means that the negative bias is sufficient to deplete the electrons in the 2DEG under the gate terminal, causing a cut-off between the source and drain terminals. Most of the devices fabricated are normally-on devices, where negative voltages are needed to deplete the electrons from flowing [13].

2.3.1 Carrier mobility

In long channel HEMTs, electron density and mobility are the key factors in HEMTs designs. The conductivity of 2DEG channel is given by:

$$\sigma = qn_s\mu \quad 2-6$$

where q is the electron charge, n_s is the sheet charge density and μ is the electron mobility. The mobility depends on lattice temperature and ionized impurity concentration. The average carrier velocity (v) is proportional to the applied electric field (E) until it reaches to saturation drift velocity (v_{sat}) when the electric field is low:

$$v = \mu E \quad 2-7$$

2.3.2 DC characteristics

The basic operating parameters of HEMT for high-power operations are: maximum drain current ($I_{D,max}$), maximum transconductance ($g_{m,max}$), threshold voltage (V_{th}), power density (P_{out}) and . These parameters can be extracted from the output and the transfer characteristics (Figure 2-5).

Figure 2-5. DC (a) output and (b) transfer characteristics of a AlGaIn/GaN HEMTs.

The maximum drain current ($I_{D,max}$) can be expressed as [100]:

$$I_{D,max} = qv_{sat}n_s = \frac{\mu\epsilon W_G}{2L_G d}(V_g - V_T)^2 \quad 2-8$$

where W_G and L_G are the gate width and length, as shown in Figure 2-4, ϵ is the semiconductor dielectric constant and d is the distance of the gate to the 2DEG.

Transconductance (g_m) is a measure of the variation of the drain current with the gate voltage and it is related to the gain of the device. It can be expressed as:

$$g_m = \frac{\partial I_D}{\partial V_G} |_{V_D=Constant} = \frac{\mu\epsilon W_G}{L_G d}(V_g - V_T) \quad 2-9$$

Threshold voltage is defined as the value of the V_{GS} at which the channel conductivity is null, therefore it determines when the channel starts to conduct. It also can be expressed as:

$$V_{th} = \phi_B - \Delta E_C - \frac{qN_D}{2\epsilon}d^2 \quad 2-10$$

where ϕ_B is the gate Schottky-barrier height, and ΔE_C is the conduction band discontinuity between the two sides of the heterojunction, and N_D is the background doping of the GaN layer.

Power density is an evaluation of the output power of the devices. It can be defined as:

$$dP_{out} = \frac{I_{D,max}(V_{BD}-V_K)}{8} \quad 2-11$$

where V_{BD} is breakdown voltage and V_K is knee voltage.

a) Gate leakage current

Another important physical property of the devices is the gate leakage current (I_G). The smaller the leakage current, the less power loss there would be in the devices. The main conduction mechanisms

in AlGaN/GaN [115], [116], AlInN/GaN [117]–[119], Al₂O₃/AlGaN/GaN [115] and so on have been widely studied in order to know how electrons transport in the heterostructures. Those transport mechanisms of electrons include Schottky emission (SE), thermionic-field emission (TFE), Fowler-Nordheim tunneling (FNT), direct tunnelling, Poole-Frenkel emission (PFE), hopping conduction or trap assisted tunneling (TAT), ohmic contact, space charge limited conduction, ionic conduction, grain boundary limited conduction and so on [120]. The way to figure out the main electron transport mechanism in a certain heterostructure is by fitting the experimental results with the theoretical curves of each mechanism. A more detailed discussion is described in Appendix C.

b) Short channel effects

The most common approach to increase the operating frequency of GaN based HEMTs is to scale dimensions of the devices: shorten the gate length (L_G). However, when the L_G is shortened, the short channel effect is inevitable: when the gate length is reduced in HEMTs, the performance enhancement due to devices scaling is restricted [121]–[123]. However, this is not because the gate length is too short, it is a geometrical in nature, all commonly fabricated devices are inherently limited by the short channel effects [67]. The key factor is the aspect ratio (L_G/d), for the AlGaN/GaN HEMTs fabricated on SiC substrate with SiN passivation, short channel effects begin to dominate frequency behaviors after the aspect ratio is smaller than 15 [67]. Therefore, gate insulator using high-k dielectrics is necessary to prevent gate leakage current [123]. Other efforts have also been made including gate recessing to increase aspect ratio, the use of double heterojunction structure, insulation of the buffer layer with p-type dopant, inverted HEMTs based on N-polar orientation of wurtzite [123] and so on.

2.3.3 RF characteristics

The RF parameters of interest for power transistors are the unity current gain frequency (f_T), the maximum oscillation frequency (f_{max}), the output power (P_{out}), maximum available gain (MAG) and power added efficiency (PAE). f_T and f_{max} can be extracted from the small signal RF behavior of the HEMT, tested by means of S-parameters measurements [124], which are explained in Appendix C. GaN-based devices with 300 GHz f_{max} have been studied in 2010 [43], and with f_T from 205 GHz to 245 GHz has been studied [45], [125], [126].

2.4 GaN-based HEMTs failure mechanisms

Despite the improvements in material properties and device designs, the reliability and stability of GaN-based HEMTs is still a bottleneck to achieve competitive devices for practical applications [7], [83], [116], [127], [128]. Therefore, to evaluate the failure mechanisms and propose novel solutions is

a priority. Fig. 6 shows the critical areas which could cause degradation in the devices. The main failure mechanisms may be classified according to their origins in the following aspects:

- 1) the material, that includes crystalline defects and lack of uniformity;
- 2) the metallurgy, that includes ohmic contact degradation, gate sinking, electro migration, hydrogen contamination, and so on; and
- 3) the electrical behaviours that include current collapse, gate-lag effects, drain-lag effects, and self-heating [128].

Figure 2-6. Schematic cross section of an AlGaIn/GaN HEMT, identifying critical areas that can be subjected to degradation [7].

2.4.1 Material

During material growth, impurities and thermo-mechanical relaxations and strains could lead to defects in the semiconductor surface, heterostructure interface or buffer. They can act like scattering centers, causing reduction of electron mobility or charge in the 2DEG of the heterostructure.

2.4.2 Metallurgy

Ohmic contact metallization degradation is usually related to thermal stability. Gate sinking effects are related to gate metal diffusion to the semiconductor [129]. Purple plague is related to gold-aluminum reactions [128].

2.4.3 Electrical behaviors

a) *Trapping effects*

Current collapse is the difference of the current in the devices between DC and high frequency biased conditions [130]–[133]. The effect is mainly caused by trapped charges on the barrier surface, at the barrier/bulk interface and/or in the bulk semiconductor materials. Depending on the origin, we distinguish between:

1. Gate lag, corresponding to the traps located at the surface layer close to the gate, acting as a virtual gate, as shown in Figure 2-7 [15], [130], [134], [135].
2. Drain lag, corresponding to the electronic traps in the buffer layer.

Figure 2-7. Schematic visualizing the virtual gate effect, in which the gate electrons are captured by surface traps and cause an extension of the effective gate length

Pulsed I-V measurements at different bias conditions are usually conducted to identify the origin of the traps. Figure 2-8 shows the pulsed output characteristics at different quiescent points ($V_{ds,Q}$, $V_{gs,Q}$):

- (a) at $V_{ds,Q} = 0$ V and $V_{gs,Q} = 0$ V, where no trapping effects are detected and it is used as reference,
- (b) at $V_{ds} = 0$ V and $V_{gs} = -8$ V, the drain current is reduced due to gate lag,
- (c) at $V_{ds} = 15$ V and $V_{gs} = -8$ V.

the drain current is decreased due to both gate and drain lag. Therefore, pulsed IV measurements can be a good indicator of trapping phenomena responsible for devices' degradation.

Figure 2-8. Double pulsed I-V characterization of AlGaIn/GaN HEMTs

b) Self-heating effects

In the case of HEMTs designed for high power applications, the high currents may cause thermal lattice vibrations, leading to increasing channel resistance in the 2DEG and self-heating because of limitations in the power dissipation [136]–[139]. This channel temperature rise is usually located at the drain-edge of the gate, where the electric field is maximum [59][66][67].

2.5 GaN-based HEMTs under harsh conditions

2.5.1 Thermal stress

GaN-based HEMT has been considered as a suitable choice for high temperature operation due to its wide band gap. In fact, F. Medjdoub *et al.*, proved that the GaN-HEMT operation in the range of 1000°C may not be limited by the heterostructure properties [141]. However, the highest temperature at which conventional AlGaIn/GaN Schottky diodes and HEMTs can be working properly is not as high as 500°C [142]–[145]. One of the main causes of device failure at high temperature is the degradation of the gate contact on the devices. An increase of the gate and drain leakage current was observed after long thermal storage test, which could be related to inter-diffusion phenomenon of the gate metals to the AlGaIn surface or perhaps even diffusing through the AlGaIn layer [146]. On the other hand, the diffusion would lead to contact resistance rise and surface roughness increase [87], [129], [147]. Therefore, the thermal stability of the materials used for the fabrication of this kind of devices is a key factor in the devices reliability.

2.5.2 Electrical stress

Various electrical stress on the GaN-based HEMT has been studied [46], [148]–[155]. A schematic of different biasing conditions for AlGaIn/GaN HEMTs and bias stress protocols are shown in Figure 2-9. There are four most basic stress conditions for HEMTs: On-state stress, High-power state stress, OFF-state stress and $V_{DS}=0$ V state stress. The type of stress protocols are:

- 1) Step stress: the devices were biased with gradual increase at one terminal for a continuous time;
- 2) Step-stress-recovery: the devices were stressed at gradual increase biases for a certain time length, during the stress, the stress would be removed, waiting the devices to recovery;
- 3) Stress recovery cyclic stress loading: this process is similar to the step-stress-recovery, however, the stress bias was kept at one voltage.

Figure 2-9 Schematic of different biasing conditions for AlGaIn/GaN HEMTs and bias-stress protocols [156]

In the electrical stress studies, there is an important parameter called critical voltage, the critical voltage was about +25 V for the AlGaIn/GaN HEMTs [151], [153], [157]. The causes of the degradation may be due to hot electron trapping [46] and inverse piezoelectric effects [151], [158].

2.5.3 Irradiation

The large bandgap, large displacement energy and relatively high operating temperature make GaN-based HEMT good candidates for space applications [73], [159]. In this case, the robustness and reliability of the devices under irradiation environments is essential due to the difficulties of a direct maintenance of the devices during working operation. Previous research showed that proton or heavy-ion irradiation causes a reduction of drain current and increase in ON-resistance in the III-V HEMTs [78], [160], [161]. In the case of GaN, nitrogen is vulnerable to lattice displacement after

irradiation, which may lead to carrier density and mobility decrease [162]–[164]. Electron-hole pairs are generated due to Compton scattering [165], introducing deep level traps in the semiconductor bulk and interface. Several authors have shown that a way to improve the devices reliability is to use MOS structures and proper passivation to diminish the damage of irradiation [79], [80], [166].

Irradiation effects with different kinds of materials on AlGaIn/GaN HEMTs has widely been studied [71], [75], [76], [89], [167]–[171]. Proton irradiation with low energy (275 keV and 330 keV) and low dose ($4.5 \times 10^{12} \text{ cm}^{-2}$) at the backside of the samples has been studied [16]. Results show that defects in the 2DEG channel and AlGaIn layer would be created with 330 keV protons, the introduction of charged defects would cause a reduction in electric field at the gate edges, which would eventually cause a decrease in drain current and improvements in off-state drain breakdown voltage; and proton irradiation with 275 keV would cause defects at GaN buffer. Protons with similar energy (380 keV) but higher dose has also been studied [172], showing that protons irradiation with 380 keV and 10^{14} cm^{-2} dose had no effects on sheet electron density, instead it cause dramatic decrease in electron mobility of the heterostructure.

Influence of 1.8 MeV proton irradiation on the defect evolution and electrical degradation of GaN/AlGaIn HEMTs were studied [173]. Results and analysis on the modification of the atomic structure for both V_{Ga} and N_{Ga} defects in AlGaIn produces interstitials and vacancy-related defects (N_i , $V_{\text{Ga}}-V_N$ and V_{Ga}) as acceptors which has led to positive shifts in the threshold voltage.

Degradation of the devices after proton irradiation with energy of 3 MeV at various dose have also been studied [169], the cause of the degradation were explained by the acceptor-like defects (Ga vacancies) introduced by the proton irradiation.

MIS-HEMTs with NbAlO gate dielectric were investigated using 3 MeV proton irradiation at a fluence of 10^{15} cm^{-2} were studied [80]. Degradation in DC performance and a flat band voltage shift in the capacitance-voltage curve were observed in the irradiated devices, trap densities increased from $1.18 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ to $1.82 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ in MIS-HEMTs after irradiation.

5 MeV proton irradiation with dose up to $2 \times 10^{15} \text{ cm}^{-2}$ would cause severely damage to GaN lattice, which would cause a DC current decrease [74][75][71], irradiation with $2 \times 10^{14} \text{ cm}^{-2}$ dose would improve the drain breakdown voltage and critical voltage [75][71].

Effects of 5 MeV proton irradiation with dose under $5 \times 10^{15} \text{ cm}^{-2}$ on AlGaIn/GaN HEMTs with source field plate [76] showed significant reduction in drain current and transconductance, with a positive threshold voltage shift and improvement in off-state drain breakdown voltage, similar to the devices discussed before [16]. This is due to the generation of defect centers at AlGaIn/GaN interfaces.

AlGaIn/GaN HEMTs degradation study varying proton energy from 5 to 15 MeV at fixed proton dose ($5 \times 10^{15} \text{ cm}^{-2}$) has also been done, more damage on dc electrical properties was observed with smaller proton energies, caused by the energy dependent penetration depth of the protons. Protons with higher energy could penetrate deeper, which would create smaller number of defects at the active layer of the HEMTs with shallow depth [77].

Effects of irradiation on MOS-HEMTs have been studied [78], effects of proton irradiation energy (5 MeV, 10 MeV, or 15 MeV) on $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS-HEMTs with the fixed proton dose of $5 \times 10^{15} \text{ cm}^{-2}$ were studied. After the 5 MeV, 10 MeV and 15 MeV proton irradiation, MOS-HEMTs' saturation current at gate voltage of 1 V were reduced by 95.3, 68.3 and 59.8% and maximum transconductance were reduced by 88, 54.4, and 40.7% respectively.

High energy proton irradiation up to 17 MeV has also been studied [171], results show that low dose would cause no significant degradation in dc behaviors of the devices, and high dose of $2 \times 10^{16} \text{ cm}^{-2}$ would cause great decrease in drain currents and transconductances.

AlGaIn/GaN HEMTs dc properties degradation after irradiation with extremely high energy (40 MeV) protons at doses equivalent to decades in low-earth orbit have also been studied [161], deep electron traps would be created by the protons. And the damage caused by the irradiation could be restored by 70% using post-irradiation annealing.

Proton irradiation with 40 MeV at a dose of $5 \times 10^9 \text{ cm}^{-2}$ on AlGaIn/GaN HEMTs with MgO or Sc_2O_3 passivation have been studied [79], results show that the devices with passivation showed reduced forward and reverse bias current due to decrease in channel doping and introduction of generation-recombination centers after.

Effects of irradiation on dynamic on-resistance [174] and RF behaviors [175] of AlGaIn/GaN HEMTs have also been researched. Charge trapping effects would be increased in the devices after the irradiation through observation of large increase of dynamic on-resistance [174].

There were also plenty of research on the effects of irradiation using different kinds of particles, such as Total ionizing dose (TID) radiation (10 KeV X-ray irradiation) [176], neutron irradiation [4][177], ^{60}Co γ -rays irradiation [170], Gamma irradiation [168], and Ge^+ irradiation [178].

There were also investigation on irradiation effects on the reliability of AlInN/GaN HEMTs [89], the reliability of the devices have been improved by the proton irradiations.

2.6 High-k dielectrics

High-k dielectrics are dielectric materials with high dielectric constant. In Si industries, it is the alternative of SiO₂. The requirements for the high-k dielectric are that [179]:

1. It must have a high enough k that it will be used for a reasonable number of years of scaling,
2. The oxide is in direct contact with the Si channel, so it must be thermodynamically stable with it.
3. It must be kinetically stable, and be compatible with processing to 1000°C for 5 seconds.
4. It must act as an insulator, by having band offsets with Si of over 1 eV to minimize carrier injection into its bands.
5. It must form a good electrical interface with Si.
6. It must have few bulk electrically active defects.

And the high-k gate oxide can be explained with physical thickness and electrical thickness, the physical thickness is the real thickness of the dielectric, and the electrical thickness is the “equivalent oxide thickness” (EOT), it is the thickness of SiO₂ needed to provide the gate oxide capacitance density as the high-k oxide film [180].

$$\frac{\varepsilon_{SiO_2} \varepsilon_0}{EOT} = \frac{\varepsilon_{high-k} \varepsilon_0}{t_{high-k}} \quad 2-12$$

$$EOT = \frac{\varepsilon_{SiO_2}}{\varepsilon_{high-k}} t_{high-k} = \frac{3.9}{\varepsilon_{high-k}} t_{high-k} \quad 2-13$$

Where ε_0 is the relative dielectric constant, t_{high-k} is the thickness of the high-k dielectric, and ε_{SiO_2} and ε_{high-k} is the relative constant of SiO₂ and high-k dielectric, respectively.

For the GaN based devices, the high-k oxides are deposited externally, not a native oxide, they can be grown on any semiconductor. The key aspects of the oxides are [181]:

1. sufficient band offsets of over 1 eV to act as a barrier for both electrons and holes; and
2. stable in contact with the semiconductor.

The most commonly used high-k oxides are Al₂O₃ [52], [53], [182]–[188], Gd₂O₃ [189]–[196], HfO₂ [44]–[55], ZrO₂ [198], [208]–[211], and Y₂O₃ [62]–[64], [212], [213]. However, the comparison among them is difficult due to the different kind of techniques used for the deposits, such as molecular beam epitaxy (MBE) [214]–[216], plasma enhanced chemical vapor deposition (PECVD) [49], [217], [218], inductively-coupled plasma chemical vapour deposition (ICP-CVD) [219], [220], atomic layer deposition (ALD) [183], [206], [221]–[223] and high pressure sputtering (HPS) [190], [191], [224]–[226], as well as the kind of heterostructure. The physical properties of several dielectrics are shown in Table 2-7, highlighting those dielectrics that have been studied during this thesis.

Table 2-7 Comparison of relevant properties for high-k dielectrics [180], [181], [227].

Material	Dielectric constant (k)	Bandgap E_G (eV)	ΔE_C to GaN (eV)	Electron affinity (eV)
Al_2O_3	10	8.8	2.16 [69].	1.0
Gd_2O_3	11-20 [228]	5.8	1.9 [181].	2.4
Y_2O_3	12-18 [213]	6.0	1.97 [69]	2.0
HfO_2	17-20 [207], [229], [230]	6.0	1.09 [69]	2.4
ZrO_2	17-20 [229], [231], [232]	5.8	1.1	2.5

2.6.1 Al_2O_3

Al_2O_3 on Si or III-V structures have widely been studied [53], [68], [187], [233]. It has been used in the study of AlGaIn/GaN-based MOS devices to inhibit leakage problems. The most commonly used method to grow Al_2O_3 films is ALD [52], [53], [68], [221], which is the method that is used in the work, as explained in Appendix C.

2.6.2 HfO_2

Similar to Al_2O_3 , HfO_2 on Si or III-V structures have also been studied widely, it has been used in the study of AlGaIn/GaN-based MOS devices to inhibit leakage problems [39]–[46]. The HfO_2 films can be deposited using MBE [234], ALD [55], [206], [235], reactive sputtering [207], radio frequency sputtering [220] and so on. In our work, the dielectric was deposited using ALD, as explained in Appendix C.

During the HfO_2 deposition study, in order to optimize the fabrication procedure, we have made more experiments with different cleaning process before depositions. Researches show that the use of a surface treatment, such as KOH, was shown to be effective in reducing the gate leakage in different GaN-based devices [236], [237]. Two groups of devices were fabricated, one with organic cleaning, the same to what we have explained before; one group with 0.5 M KOH cleaning for 30 s. Afterwards, the same processing was taken on the devices.

2.6.3 ZrO₂

ZrO₂ on Si or III-V structures is a commonly used high k dielectric. The properties of ZrO₂ are quite close to that of HfO₂. It has been used in the study of AlGaIn/GaN-based MOS devices to inhibit leakage problems [39]–[46]. The ZrO₂ films can be deposited using MOCVD [209], ALD [208], reactive sputtering [232], e-beam evaporation [231], etc. In our work, the dielectric was deposited using ALD, the same to that used for Al₂O₃ and HfO₂.

2.6.4 Gd₂O₃

During the HEMT and MOS-HEMT fabrication processing, the samples were divided into two pieces after the ohmic metallization. As shown in Figure 3-6, One half piece of the sample was covered by photoresist and the other half was gate patterned using standard photolithography, as discussed in the previous section. Then the corresponding gate dielectric was deposited and the gate metals were evaporated. Afterwards, feed metals were deposited.

Chapter 3 Device fabrication and characterization

In this chapter, the experimental details of the fabrication and characterization of GaN-based HEMTs and MOS-HEMTs are depicted. First of all, the basic heterostructures used in the work are described (see also Appendix A). Then, the basic steps of the device fabrication and the corresponding optimizations are detailed. Finally, the electrical characterization techniques of the devices are presented. More details on processing, device fabrication and device characterization are given in appendixes B, C and D, respectively.

3.1 Heterostructures used in the work

The basic heterostructures used in the work are AlGaN/GaN and AlInN/GaN grown by MOCVD on silicon substrate. A detailed summary of the samples used in this thesis are described in Appendix A.

3.1.1 AlGaN/GaN heterostructures

Two kinds of AlGaN/GaN structure were used in the study, with and without a GaN cap layer. The Al content and the thickness of the AlGaN layer is 32% and 22 nm, respectively. The GaN layer is unintentionally doped, with a thickness of 0.1 μm . The GaN cap is usually 2 nm thick. The GaN cap is helpful in reducing reverse leakage current [238]. The other kind of AlGaN/GaN structure has Al content and the thickness of the AlGaN layer of 25% and 25 nm, respectively, the thickness of GaN buffer is 0.1 μm . The detailed description of the heterostructures we have used is shown in Appendix A.

3.1.2 AlInN/GaN heterostructures

Besides AlGaN/GaN epilayer, two kinds of AlInN/GaN heterostructure are used here, with and without a GaN cap. Lattice matched AlInN/GaN heterostructure grown on (111) silicon wafer by metal-organic chemical vapor deposition (MOCVD). The In content and the thickness of the AlInN layer is 17% and 10 nm, respectively. The GaN buffer layer is unintentionally doped, with a thickness of 0.6 μm . The beneficial effects of AlInN/GaN structure is that they are lattice match materials, there is no string in between the two layers, therefore, the carrier density and mobility are higher than those AlGaN/GaN heterostructures [141], [239]. Studies have shown that the GaN cap could help improved the off-state characteristics and dynamic on-resistance of the AlInN/GaN heterostructure [23]; therefore, we have studied the AlInN/GaN and GaN/AlInN/GaN heterostructures at the same time.

3.2 Device fabrication

The flow charts of the basic steps of the device fabrication processing are shown in Figure 3-1. It consists of a first surface cleaning, followed by the electrical isolation of the devices, the formation of the drain and source ohmic contacts, the gate Schottky contact and the passivation layer deposition. All the steps need a standard lithography and lift-off process which is described in Appendix B. In the following subsections some of the steps of the fabrication processing are described in detailed, in particular those that have been optimized during this thesis work.

Figure 3-1 Flow chart of the device fabrication process

3.2.1 Initial surface cleaning

During the device fabrication process, in order to remove native oxides residues or remains formed during wafer cutting on the semiconductor surface, it is important to do a surface cleaning on the samples before each procedure [240]. The standard cleaning procedure is organic cleaning: the samples are rinsed in acetone, isopropyl alcohol (IPA) solvent in ultrasonic for 10 minutes each, then cleaned with deionized water (DIW) and blown with dry N₂.

In the steps involving metal deposition, the samples have to be cleaned using diluted HF:H₂O (10:1) for 10 s right before metalization.

3.2.2 Lithography

Lithography is used in semiconductor device fabrication to transfer pre-designed patterns of a mask onto a wafer surface. Firstly, the wafer is covered with a thin photoresist layer. Then photoresist on the wafer is selectively removed, followed by dry etching, lift-off, ion implantation or metallization at the areas accordingly. Lithography can be performed using either optical or electron beam (e-beam).

In our work, we have been using optical lithography technique. The optical lithography system is introduced in Appendix B.

3.2.3 Electrical isolation

In order to keep the devices electrically isolated, a MESA etching or a implantation process [240] is usually carried out. In our work, MESA etching process was used. Firstly, a layer of PMMA photoresist, about 100 μm thick, was defined by photolithography to select some specific areas on the sample. Then, a Cl_2 -based dry etching using Inductively Coupled Plasma reactive ion etching (ICP-RIE) system was processed, as discussed in the following sections.

a) Dry etching

The commercial ICP-RIE system used during the study is described in Appendix C. Some the most commonly used plasmas during GaN-based heterostructures etching are Cl_2/Ar [241]–[243], Cl_2/BCl_3 [244]–[246] and Cl_2/CF_4 [247], [248]. However, the role of the different mixtures and the etching mechanisms are still under discussion.

In the ICP-RIE system, etch rate and etched surface roughness are functions of process parameters, such as the plasma mixing ratio, ICP/RIE powers, pressure and temperature. Moreover, the etching process also depends on the particular heterostructure, making comparisons even more difficult. In order to find out the most suitable etch condition especially the plasma mixture for our work, an optimization of the mesa etching was carried out on the same GaN/AlGaIn/GaN heterostructures using four different kinds of plasma mixtures, including 10 sccm Cl_2 with (a) 5 sccm Ar, (b) 1 sccm Ar, (c) 1 sccm BCl_3 and (d) 1 sccm CF_4 , and keeping the other parameters including power, DC bias, pressure, Cl_2 plasma flow and temperature constant.

Table 3-1 Basic dry etching parameters in GaN-based HEMTs

Process Parameters	Values
ICP power	40 W
RIE power	100 W
Pressure	5 mTorr
Temperature	25°C

Plasma 1	Cl_2 (10 sccm)
Plasma 2	Ar (5 sccm)/Ar (1 sccm)/ BCl_3 (1 sccm)/ CF_4 (1 sccm)

A summary of the parameters are shown in Table 3-1. Etch rates, surface roughness, etch profiles, and electrical properties of the etched heterostructures were systematically analysed. After etching, the PMMA layer was removed with acetone and isopropanol, followed by DI water and blow dry N_2 . Further cleaning by O_2 plasma was done to remove the photoresist residues. The etched step was measured using an Alpha-step profilometer, and the surface morphology and edge profile was analysed by JSM-5800 and Inspect F50 scanning electron microscope (SEM).

The etch rates of the GaN/AlGaN/GaN heterostructure as a function of the plasma composition are compared in Figure 3-2. In the case of Cl_2 -Ar plasma mixture, the etch rate slows down drastically by about 80% when the Ar ratio in the plasma mixture was decreased in the same proportion, from 5 to 1 sccm. This is consistent with the results from Rosli et al., where the etch rate increases with respect to the flow rates of Ar as long as it is smaller than 20 sccm [242]. Therefore, in the case of 1 sccm Ar, only a small rate (13.2 nm/min) was achieved during the primary etching process, and only 45 nm were etched. In this case, a second etching was performed and the resultant etching rate increased to near 50 nm/min.

Figure 3-2 Etch rate of the samples with different gas species and plasma mixtures

This significant change in the etch rate could be explained by the etch selectivity of the GaN cap and the AlGaN barrier caused by their different physical properties. According to the literature, the reaction of GaN and AlGaN with Cl_2 plasma follows two steps:

- (1) the bond breaking of nitrides: Ga-N and Al-N, and

(2) the binding of volatile chloride etch products, like GaCl_x and AlCl_x [249].

The bond strength of Al-N (11.5 eV/atom) is much larger than that of Ga-N (8.9 eV/atom) [250]. Thus, it is expected that the Cl_2 plasma breaks the Ga-N bond faster than the Al-N bond. On the other hand, the differences between the etch rate of the AlGaN and GaN layers are clearly observed when Ar composition is low in the plasma mixture (1 sccm), because the GaCl_x and AlCl_x etch products are removed slowly. However, using a large amount of Ar (5 sccm) in the plasma mixture, the different etch rate at AlGaN and GaN layers becomes less significant.

Figure 3-3 SEM photomicrograph showing mesa sidewall profiles etched with: Cl_2 (10 sccm) (a) 5 sccm Ar; (b) 1 sccm Ar; (c) 1 sccm BCl_3 and (d) 1 sccm CF_4

In the case of 1 sccm gas flows (Ar, BCl_3 and CF_4), the etch rate was slightly increased when BCl_3 is added to the Cl_2 plasma respect to the case of Ar. A similar result has been observed by adding CF_4 in the plasma composition, and no significant differences were observed in the etch rates between the samples using Cl_2/BCl_3 or Cl_2/CF_4 plasma.

Regarding the surface roughness and etch profiles, a smooth morphology and a near vertical sidewall profile was observed in the case of Cl_2/BCl_3 plasma etching (Figure 3-3(c)), in contrast to the Ar plasma compositions. However, with Cl_2/Ar plasmas (both 1 sccm and 5 sccm), some etch residues were found on the etched surface, possibly due to photoresist residues or etch by-products (Figure 3-3(a), (b)). The etch by-product could be due to the etch selectivity between GaN and AlGaIn due to the surface oxides of the heterostructure. As AlGaIn was oxidized during storage in air, the aluminum oxides may provide a self-mask effect [251]. As the bond strength of Al-O (21.2 eV/atom) is larger than that of Al-N and Ga-N, the etching of AlGaIn could be limited, while GaN was less influenced because Ga-O has a higher reactivity. This will cause increase in surface roughness and affect the electrical properties of the sample as well.

When BCl_3 is added in the plasma mixture, BCl_3 will react with oxygen to form some BCl_xO_y trimer gases, which is chemically inert and can be easily pumped out [249]. This will eliminate the etch selectivity of the heterostructure and improve the smoothness of the etched surface. A similar smooth surface was observed in the case of Cl_2/CF_4 plasma etching.

In order to compare the electrical properties of samples etched with the different plasma compositions, the isolation current (I_{iso}) between two adjacent mesas and the sheet resistance (R_{sheet}) of the 2DEG, calculated by means of the transmission line method (TLM) described in Appendix C), are shown in Figure 3-4. The lowest I_{iso} values correspond to the Cl_2/BCl_3 plasma composition, about 10 nA at 40 V. Similar range of values were observed by N. A. Moser *et al.* for the isolation current between neighboring devices without any treatment [252]. According to literatures, the isolation leakage current is dominated by surface states, and it shows that it can be further reduced to below 1 nA by other techniques like passivation.

Figure 3-4 (a) Isolation current, (b) sheet resistance (R_{sheet}) of the samples etched with different plasma mixtures

The R_{sheet} of the samples was evaluated before and after the etching. The results are shown in Figure 3-4 (b). Before the etching, the R_{sheet} was similar in all cases (around $300 \Omega/\square$), which is slightly underestimated due to measurement technique of the TLM structure without mesa isolation. After the mesa etchings, most of the samples has R_{sheet} close to the nominal value, except etching using Cl_2/CF_4 plasma, which is a 15% higher. It is worth noticing that the etching process using Cl_2/BCl_3 composition shows a smooth surface without increasing the R_{sheet} values.

Therefore, from these results it is concluded that the Cl_2/BCl_3 plasma etching is the best candidate to use during HEMTs' fabrication, as it shows a moderate high etching rate, smooth and vertical etch profile, no increase of the nominal R_{sheet} and the lowest isolation current.

3.2.4 Ohmic contacts formation (drain and source)

High quality ohmic metal with very low resistance, well-defined edge, smooth surface morphology and high thermal and mechanical stability are necessary at the drain and source contacts to achieve well performed HEMTs.

The ohmic contact mechanism in a metal-AlGaIn/GaN or GaN system can be explained by tunneling effect due to nitrogen vacancies caused during nitride formation at the metal-AlGaIn/GaN or GaN interface, which makes AlGaIn/GaN or GaN to behave as heavily doped material with a large semiconductor band bending, whose Fermi level shifts to the energy level of the nitrogen vacancies [253]–[255]. Thus the barrier width becomes very narrow, through which the electrons can flow via tunneling.

The formation of the ohmic contacts requires a rapid thermal annealing after metal deposition. The processing steps are described in detail in the following subsections, as well as in Appendix C.

a) *Metal deposition*

A Ti/Al based metal stack was used traditionally to achieve ohmic contacts on GaN/AlGaIn layers [254], [256]. The GaN at the metal/GaN interface became heavily doped during annealing. This is caused by the solid phase reaction between Ti and GaN forming TiN which may lead to N vacancy accumulation in GaN near the junction. Then, one of the most frequently used metal stack for ohmic contact: Ti/Al/Ni/Au scheme [147] is studied to improve the contact resistance. In this design, Ti/Al plays the role of the real contact, while Ni/Au is working as the protection cap to prevent the surface oxidation of the Al. A lot of work on different metal schemes Ti/Al/X/Au has been investigated, where

X can be titanium (Ti) [257], platinum (Pt) [258], molybdenum (Mo) [146], [259], [260] and so on. Each metal in the ohmic stack has its specific purpose:

1. The first layer of Ti adheres to the surface of the heterostructure, providing good stability. It melts with the native oxide on the AlGaIn surface and creates nitrogen vacancies by reacting with nitrogen atoms to form TiN on the AlGaIn layer, which in turn acts as n-type donor sites, increasing the doping concentration, and thus, enabling electrons to tunnel through the thin metal/semiconductor barrier with very small resistance.

2. The second layer, Al reacts with Ti to form an Al₃Ti layer, thus prevents the underlying Ti layer from oxidizing. It also serves as a dispersion barrier for the metals on top when they are forming schottky barrier.

3. Ni, Pt, Mo or other metals could prevent the Al from mixing up with the Au, because the mix would lead to a highly resistive layer.

4. Au is used as contact with the outside contact probe and so on, because it has a high conductivity.

The metallization scheme used in our process is typically 20 nm Ti / 120 nm Al / 40 nm Ni / 50 nm Au, deposited by e-beam evaporation (see Appendix C), that was optimized previously by Dr. Sara Martin Horcajo in ISOM [261].

b) Rapid thermal annealing

Rapid thermal annealing is necessary in GaN-based heterostructures to achieve ohmic behaviors by diffusing the metal toward the 2DEG region. Thermal annealing is usually in the range between 800°C to 900°C in N₂ atmosphere and it requires an optimization depending on the metal scheme. The Ti/Al/Ni/Au metal stack has been optimized with the best result at 865°C [262]. The RTA equipment used in the lab is described in the Appendix C.

c) Ohmic metal characterizations

In order to make sure the ohmic contact with small contact resistance is achieved, we have to check the ohmic contacts property before the next step. The test method used is the transmission line method (TLM). It contains a serial of ohmic contacts separated by various distances, as shown in Figure 3-5. Contact resistance (R_c) and sheet resistance (R_{sheet}) can be extracted, the detailed explanation is shown in Appendix D.

Figure 3-5 Typical arrangement for a TLM test pattern [263].

In the past, several kinds of ohmic metal stack has been used, the contact resistivity (ρ_c) is about $2.3 \times 10^{-6} \Omega \text{cm}^2$ with V-Ti/Al/Ni/Au contact scheme [264].

In our experiments, R_c measured on AlGaIn/GaN heterostructure ranges from $0.3 \Omega \text{mm}$ to $0.9 \Omega \text{mm}$, and the R_c on AlInN/GaN heterostructure are from $0.5 \Omega \text{mm}$ to $0.9 \Omega \text{mm}$, which belong to the state-of-the-art values.

3.2.5 Schottky contact formation (conventional gate)

In order to get a device with good pinch off, a good Schottky contact has to be formed. The main requirements for the Schottky contact are: low leakage current, low conductivity, high breakdown voltage, good thermal stability and reliability.

Some typical metals used as rectifying contacts in AlGaIn/GaN HEMTs and their work function are shown Table 3-2. From the table, we can see that Ni, Au, Pt and Pd are the most suitable metals for Schottky contacts.

Table 3-2 Schottky metal work-functions

Metal	Work function Φ_M (eV)
Ni	5.15
Au	5.10

Pt	5.65
Pd	5.12
Mo	4.6
W	4.55

Source: Periodic Table of Elements from EnvironmentalChemistry.com

Besides the quality of the gate contact, another important figure is the layout design of the contact. In order to achieve high current and high output power, multi-finger structures with T-shape and U shape has been widely studied. The drawback of the multi-finger devices is the high self-heating effects.

In our work, in order to emphasize the effects of dielectric on the devices, we have been using the same gate metal for all devices, HEMTs and MOS-HEMTs: Ni (50 nm)/Au (200 nm). The conventional and MOS HEMTs are T-shapes, with one or two fingers. The gate length (L_G) were from 1.2 μm to 5 μm , and the gate width (W_G) were from 50 μm to 300 μm , but the most often used devices are the ones with L_G of 1.2 μm , W_G of 50 μm and 100 μm .

a) Schottky metal characterizations

The most important requirements of the Schottky contacts are low reverse leakage current and good cut-off. During the study, square shape diodes were fabricated at the same time as the HEMTs. The leakage current density at reverse and forward biased conditions, as well as the capacitance-voltage properties, can be checked, and the electron transport mechanisms and the interface charges can be calculated. The details are discussed in Appendix D.

3.2.6 Gate dielectric deposition (insulated gate)

As we have discussed in section 2.6, for GaN based devices, the high-k oxides are deposited externally, not native oxides, they can be grown on any semiconductor. The most import requirements of the gate dielectric oxides are [181]:

1. sufficient band offsets of over 1 eV to act as a barrier for both electrons and holes; and
2. stable in contact with the semiconductor.

Al_2O_3 , HfO_2 , ZrO_2 and Gd_2O_3 was used during the study. The physical properties of several dielectrics are shown in Table 2-7. During the HEMT and MOS-HEMT fabrication processing, the samples were divided into two pieces after the ohmic metallization, one piece was designed for conventional devices, and the other half was fabricated with an oxide layer, as shown in Figure 3-6.

Figure 3-6 Flow chart of the Gd_2O_3 device fabrication process.

There are two designs in the work, one is with dielectric layer in between source and drain, the other is to deposit the dielectric layer solo under the gate.

For the first design, the dielectrics used are Al_2O_3 , HfO_2 and ZrO_2 , deposited using ALD technique. After the ohmic contact at the source and drain region were deposited and characterized, the devices were covered with a thin layer of the selected dielectric, about 5 nm. Then the gate metal would be deposited on the signed area. Afterwards, the feeds area designed to make contacts between ohmic metal and external measurement equipments were etched using $\text{HF}:\text{H}_2\text{O}$ (10:1) solution, and the feeds metals were deposited.

In the second design, the dielectric used is Gd_2O_3 , deposited using high pressure sputtering (HPS) technique at the designed gate region. The samples were covered by photoresist and gate patterned using standard photolithography, as discussed in the previous section. Then the corresponding gate dielectric was deposited and the gate metals were evaporated. Afterwards, feed metals were deposited.

a) ALD

ALD is a thin-film deposition technique with atomic scale precision growth, it deposits a film on the substrate layer by layer with a sequence of precursors (chemical reactants). The process is based on two fundamental mechanisms: chemisorption saturation process and sequential surface chemical reaction. The advantage of ALD comparing with the other deposition techniques is that it provides

excellent adhesion and low stress on the dielectric film due to the chemisorption of precursors with the surface. The detailed description of the procedure is shown in appendix C.

In this work, the dielectrics deposited using ALD were done by the CTECHnano in Bilbao, as described in Appendix C.

b) HPS

The HPS technique works in the pressure of mbar range, which lies between 2 and 3 orders of magnitude above conventional sputtering. It is a two-step procedure developed by colleagues from UCM [190], [225], [226]. Firstly, a thin metallic Gd film is sputtered by HPS using a metallic Gd target and a pure Ar atmosphere. Then, without extracting the sample from the system, the Gd_2O_3 films are *in situ* plasma oxidized, by adjusting gas composition and plasma parameters.

In this work, the dielectric was deposited using HPS in collaboration with the group of “Láminas delgadas y microelectrónica” in the facilities of the Facultad de Físicas (Universidad Complutense de Madrid), as described in Appendix C.

3.2.7 Passivation layer

A passivation layer protects the devices from physical damage and decreases the trapping effects. The most commonly used materials are Si_3N_4 , SiO_2 , and mixtures such as SiON [265]–[270]. The Si_xN_y layer is usually deposited using plasma enhanced chemical vapor deposition (PECVD) [271]. Firstly, the devices were deposited with a dielectric passivation layer of about 100 nm, then passivation layer on top of the metal contacts is selectively etched.

In this work, there is no passivation layer over the devices, so that we can focus on the effects of the gate dielectric layers.

3.3 Summary

In this chapter, the device fabrication procedures are explained step by step. Firstly, the cleaning procedures are explained. Then, the device isolation techniques and the optimized MESA etching process is described in detail. Afterwards, the ohmic metals for drain and source contacts in GaN-based HEMTs are described, which is Ti/Al/Ni/Au metal stack followed by a 870°C rapid thermal annealing. The requirements and characterization methods of the ohmic contacts using TLM are mentioned. Then the formation of Schottky gate contacts are discussed. Then, the gate dielectrics

used in this work, including Al_2O_3 , Gd_2O_3 , HfO_2 and ZrO_2 are explained, as well as the experimental procedure and the deposition techniques. Finally, the passivation step has also been briefly discussed.

Chapter 4 GaN-based MOS-HEMTs at room temperature with high-k dielectrics

In this chapter, the effects of different gate dielectrics (HfO_2 , Al_2O_3 , and ZrO_2) in MOS-HEMTs at RT are compared as a function of the heterostructure (AlGaN/GaN , AlInN/GaN and $\text{GaN}/\text{AlInN}/\text{GaN}$). The heterostructures used during the study is shown in Figure 4-1. For the MOS HEMTs with high-k dielectrics, the most usual observed phenomenal is leakage current decrease and V_{th} negative shift, and some $I_{\text{D,max}}$ and $g_{\text{m,max}}$ decrease.

Figure 4-1 Schematic cross section of the HEMTs discussed in this chapter

Al_2O_3 gate dielectric was chosen because it has the most experience as alternative of SiO_2 in history, it is easy to be deposited, and it has a dielectric constant of 10, and a large bandgap about 8.8 eV. HfO_2 is the second most popular material used as gate dielectric in the field, it has a higher dielectric constant, close to 25, and the bandgap is close about 6.0 eV. The other dielectric, ZrO_2 , was also chosen because it shows similar physical properties to HfO_2 , but it is not so widely studied.

The thickness of the gate dielectrics are 5 nm, which is the minimum thickness that was possible to deposit to have a homogeneous and good quality dielectric layer, being able to decrease the leakage current of the devices..

The effects of the dielectrics on the DC behaviors of the HEMTs are compared at RT. Afterwards, the effects of pre-deposition cleaning using KOH on the MOS devices are compared with the MOS devices with traditional organic cleaning, as well as a comparison of short thermal annealing (STA) are studied.

4.1 Effects of varying the heterostructure design

In the following work, the leakage current decrease by the dielectrics is investigated on the selected heterostructures used in the study. Different dielectrics, including HfO_2 , Al_2O_3 , and ZrO_2 , were deposited using ALD method, as the gate dielectric of MOS-HEMTs on different heterostructures (AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN). The gate dielectrics (HfO_2 , Al_2O_3 , and ZrO_2) with a thickness of 5 nm were deposited in the area between the source and the drain, right after the ohmic contacts formation, as described in chapter 3.

4.1.1 AlGaIn/GaN heterostructures

Before dielectric deposition, the R_c is $0.6 \pm 0.05 \Omega \cdot \text{mm}$, and the R_{sheet} is about $600 \Omega/\square$, checked using TLM, the carrier density (n_s) and mobility (μ) is $0.87 \times 10^{13} \text{ cm}^{-2}$ and $1100 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, from Hall measurements. When the sample is fully fabricated after dielectric deposition, the contact resistance increases to about $0.75 \pm 0.1 \Omega \cdot \text{mm}$, and the sheet resistance decreases to $510 \Omega/\square$.

Previous published results showed that the smallest I_{rev} of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS diodes was close to $1.6 \text{ nA}/\text{cm}^2$ with 15 nm Al_2O_3 [53], and the smallest $I_{\text{D,off}}$ value of MOS HEMTs with 20 nm Al_2O_3 was about $10 \text{ nA}/\text{mm}$ [185]; for the $\text{HfO}_2/\text{AlGaIn}/\text{GaN}$ MOS HEMTs, the smallest $I_{\text{D,off}}$ was about $0.1 \mu\text{A}/\text{mm}$ with 5 nm SiN_x and 25 nm HfO_2 [220]; and for the AlGaIn/GaN MOS HEMTs with 22 nm ZrO_2 , the I_{rev} was observed to be about $1 \text{ mA}/\text{mm}^2$ [209]. Besides $I_{\text{D,off}}$ and I_{rev} decrease in the MOS devices, V_{th} shift was the most commonly observed behaviors, and the interface trap was the most studied. In the following parts, we are going to compare the effects of Al_2O_3 , HfO_2 and ZrO_2 on the devices.

a) Schottky and MOS-Ds

The I-V characteristics of the AlGaIn/GaN Schottky diodes and MOS-Ds with Al_2O_3 , HfO_2 and ZrO_2 are shown in Figure 4-2. The smallest reverse current (I_{rev}) is in the Al_2O_3 MOS-Ds (MOS-D), which is about $1.0 \mu\text{A}/\text{cm}^2$, about 10^3 lower than in the Schottky diodes (SD). In the forward biased region, the smallest forward current (I_{for}) was $50 \mu\text{A}/\text{cm}^2$, corresponds to MOS-D with HfO_2 and ZrO_2 gate dielectrics. This leakage current value is about 10^2 lower than in the MOS-D with Al_2O_3 , and 10^7 lower than in the SD.

There is no publication with the same design as shown in this work, so I tried to compare the results with similar designs. The values of the ZrO_2 MOS-D, the I_{rev} decrease by 10^2 compared with the previous study with 22 nm ZrO_2 [209]. And the I_{rev} of HfO_2 MOS-D in the study is close to the results of the MOS-HEMTs with 5 nm SiN_x and 25 nm HfO_2 [220], which makes this result the best comparing with other close studies. However, for the Al_2O_3 based devices, our result is not the smallest comparing

with other studies, because the thickness is about 15-20 nm in the other cases, but this thickness will decrease the capacitance. Therefore, in this group of devices, HfO_2 shows the smallest I_{for} among the three kinds of dielectrics, and it is the best case so far compared with the other studies.

Figure 4-2 I-V properties of SD and MOS-Ds with Al_2O_3 , HfO_2 and ZrO_2 on AlGaIn/GaN HS

The CV characteristics (forward and reverse) at 1 MHz of the SD and MOS-D are shown in Figure 4-3. The SD and MOS-D were swept forwardly and reversely with a step of 0.1 V at the speed of ~ 0.3 s/step, from -8 V to 0 V (in the case of SD) and from -8 V to 6 V (in the case of MOS-D). In the case of SD, no hysteresis was observed and the threshold voltage (V_{th}) is -3.5 V (Figure 4-3 (a)). In the case of MOS-D, the plateau capacitance at 0 V decreased, and the V_{th} shifted negatively due to the additional dielectric layer between gate and the channel. No frequency dispersion was observed in the negative sweep region (not shown).

The carrier density slightly increased in the MOS-D compared with the SD, as show in Figure 4-3 (a). This is consistent with the lower R_{sheet} observed after the gate dielectric deposition in the MOS-HEMTs. From the capacitance value at 0 V, the relative dielectric constant of the dielectrics is estimated, resulting in 10, 17, and 17 for Al_2O_3 , HfO_2 and ZrO_2 , respectively. They are reasonable values as observed in other studies [272].

Figure 4-3 C-V characteristics of SDs and MOS-Ds at (a) negative sweep and (b) positive range on AlGaIn/GaN HS

In the case of the MOS-D in the negative bias, no hysteresis is observed for the HfO₂ and Al₂O₃ dielectrics, but the MOS-D with ZrO₂ showed a slight hysteresis of 0.1 V, it is related to slow mobile charges in the dielectric layer, and the charge density is calculated to be $1.2 \times 10^{11} \text{ cm}^{-2}$.

The interface state density of the devices were estimated using the conductance method [273]. Details of the method are summarized in Appendix D. The fitting of G_p/w is shown in Figure 4-4 (a), and the D_{it} and the relevant energy level are shown in Figure 4-4 (b). The SD showed a trap density of $1 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ located at energy level of 0.57 eV below the conduction band, that could lead to current collapse and device breakdown [274]–[276]. The HfO₂ and ZrO₂ MOS-D showed a similar trap density ($2.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $2.8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, respectively) at the same energy level of $0.41 \pm 0.1 \text{ eV}$, that could be due to native defects complexes [276]. In the case of Al₂O₃ MOS-D, the interface state density was slightly lower $1.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ located at energy level of 0.35 eV, that might be due to the carbon related defects in the AlGaIn/GaN epilayer [277].

A huge hysteresis was observed in the positive bias range of Al₂O₃ MOS-Ds (Figure 4-3 (b)), indicating the existence of slow mobile charges at the Al₂O₃/AlGaIn interface [278]. The ZrO₂ based MOS-Ds showed oxide capacitance decrease as the gate voltage increased, which was due to the presence of oxide/AlGaIn interface traps [279].

In general, the MOS-Ds with HfO₂ has the smallest I_{rev} and I_{for} among the three kinds of MOS-Ds, and it has the smallest interface state density and the smallest mobile charges in the oxide and interface traps, therefore, it is the best candidate for AlGaIn/GaN MOS-D.

Figure 4-4 (a) Conductance, G_p/w calculated for the different diodes, and (b) D_{it} and $E_c - E_T$ achieved from the fitting curves

b) HEMTs and MOS-HEMTs

Afterwards, DC and pulsed characterizations of the conventional HEMTs and MOS-HEMTs, with gate length (L_G) 3 μm , gate drain distance (L_{GD}) 5 μm and gate width (W_G) 100 μm , were carried out at RT. From the DC output characteristics at $V_{GS} = 1$ V shown in Figure 4-5, an increase in the $I_{D,max}$ was observed for all the MOS-HEMTs respect to the conventional HEMTs. In particular, the highest $I_{D,max}$ value corresponded to the MOS-HEMTs with HfO_2 with an increase up to 37% and 10% smaller R_{on} than the conventional HEMTs. The values of $I_{D,max}$, R_{on} , $g_{m,max}$ and V_{th} are shown in Figure 4-6.

Figure 4-5 (a) $I_D - V_{DS}$ and (b) $g_m - V_{GS}$ of HEMTs and MOS-HEMTs on AlGaIn/GaN HS

The transfer characteristics of the devices in Figure 4-5 (b) show that V_{th} shifted negatively, from -3.1 V in the conventional HEMTs to -5.1 V, -5.3 V and -5.6 V for HfO_2 , ZrO_2 and Al_2O_3 MOS-HEMTs,

respectively, in good agreement with the behaviour of the MOS-Ds. Figure 4-5 (b) shows the maximum transconductance of the MOS-HEMTs and HEMTs at $V_{DS} = 4.9$ V.

Figure 4-6 Values of (a) $I_{D,max}$, R_{ON} and (b) $g_{m,max}$, V_{th} in the HEMTs and MOS-HEMTs on AlGaIn/GaN HS

The differences of $g_{m,max}$ of the MOS HEMTs are shown in Figure 4-6 (b), the $g_{m,max}$ is about 12%-14% lower than the HEMTs. This is due to the further separation between the gate and the 2DEG channel with the presence of the additional oxide layer in the MOS-HEMTs, as expected and in agreement with the literature [50], [57], [280], [281].

Figure 4-7 I_D - V_{GS} of HEMTs and MOS-HEMTs at (a) $V_{DS} = 0.1$ V and (b) 10 V on AlGaIn/GaN HS

In addition, the off-state drain current densities is about 1×10^{-10} A/mm for all the MOS-HEMTs, which is 10^3 lower than the conventional HEMTs. Therefore, the on/off ratio is 10^9 for the MOS-HEMTs

regardless the gate dielectric, which is 10^3 higher in comparison to the conventional HEMTs ($\sim 10^6$), as shown in Figure 4-8 (a).

Figure 4-8 Values of (a) $I_{D,off}$, on/off and (b) GLR, DLR in the HEMTs and MOS-HEMTs on AlGaIn/GaN HS

Regarding the pulsed measurements, Figure 4-9 shows the I-V characteristics at $V_{GS} = 1$ V for the HEMTs and MOS-HEMTs at different quiescent points and the corresponding GLR and DLR. The gate lag was reduced significantly in the MOS-HEMTs, featured by a 120% increase of the GLR, from 0.40 to values close to 1. In particular, MOS-HEMTs with HfO_2 shows the highest GLR value (0.95) indicating a high reduction of the surface trapping effects respect to the conventional HEMTs and MOS-HEMTs with ZrO_2 . This is in good agreement with the results of capacitance of the MOS-D and SD.

The drain lag was also slightly improved in the MOS-HEMTs respect to the HEMTs. The highest DLR values are in the MOS-HEMTs with HfO_2 (0.63) and Al_2O_3 (0.68), about 50-58% higher than in the conventional HEMTs. The drain lag is mainly due to the traps in the buffer, or the virtual gate effects in the devices [282]. Therefore, the increase of the DLR in the HfO_2 and Al_2O_3 indicates that there are less trapping effects in the channel and less virtual gate effects, in good agreement with the smaller interface state density we have observed from the CV properties of the diodes.

Figure 4-9 Pulsed IV curves of (a) HEMTs and (b,c,d) MOS-HEMTs on AlGaIn/GaN HS

In summary, from the DC properties, the Al_2O_3 , HfO_2 and ZrO_2 in between source and drain on the AlGaIn/GaN HS have decreased the leakage current by almost 10^4 in MOS-Ds and the MOS-HEMTs, and increased the on/off ratio by 10^3 in the MOS-HEMTs than the conventional HEMTs. Also, there is improvement in GLR and DLR, particularly for HfO_2 MOS-HEMTs, which is in good agreement with a lower trap density estimated from the MOS-D.

Therefore, the gate dielectric layers in the HEMTs used during the work decreased the leakage current effectively. Furthermore, HfO_2 was the best candidate to mitigate the trapping effects in the AlGaIn/GaN HEMTs, hence improving the performance of the devices.

4.1.2 AlInN/GaN heterostructures

The R_c of the ohmic contacts and R_{sheet} of the 2DEG were $1.5 \, \Omega/\text{mm}$ and $400 \, \Omega/\square$, respectively. The $n_{2\text{DEG}}$ and μ were 1.2×10^{13} – $1.8 \times 10^{13} \, \text{cm}^{-2}$ and 700 – $1400 \, \text{cm}^2 \, \text{V}^{-1} \, \text{s}^{-1}$, respectively. After dielectric deposition, the R_c was about $0.9 \pm 0.1 \, \Omega/\text{mm}$, and the R_{sheet} was about $275 \pm 5 \, \Omega/\square$.

The previous published results showed that the smallest I_{rev} of $Al_2O_3/AlInN/GaN$ MOS HEMTs was close to 10 nA/mm with 10 nm Al_2O_3 [283]; for $HfO_2/AlInN/GaN$ MOS HEMTs, the smallest $I_{G,rev}$ was about 1 μ m/mm with 10 nm HfO_2 [198] ; and for $ZrO_2/AlInN/GaN$ MOS HEMTs with 10 nm ZrO_2 , the $I_{G,rev}$ was slightly smaller than 1 μ m/mm [198]. In the following parts, we are going to compare the effects of Al_2O_3 , HfO_2 and ZrO_2 on the $AlInN/GaN$ HS.

a) Schottky and MOS-Ds

The I-V characteristics of the $AlInN/GaN$ SDs and MOS-Ds are shown in Figure 4-10. Like those observed in the case of $AlGaN/GaN$, a decrease in the reverse and forward leakage current is observed in the MOS-Ds with respect to the SDs. However, the behavior of the dielectrics on the $AlInN/GaN$ HS is not as homogeneous as in the $AlGaN/GaN$ heterostructures. For the SD, I_{rev} was about 1 A/cm², and I_{for} was about 8 A/cm². In the case of MOS-D with ZrO_2 , the reverse gate current is about 0.2 A/cm², which is only 10 times lower than in the SD. In contrast, Al_2O_3 and HfO_2 showed about 10⁴ and 10³ lower I_{rev} than the SD, respectively. Moreover, Al_2O_3 and HfO_2 also showed the lowest leakage currents in the forward biased (I_{for}), around 5 μ A/cm², what is more than 10⁷ lower than the SD, and 10⁵ lower than the MOS-D with ZrO_2 .

Comparing with previous published results and with the other dielectrics used in this work, the MOS-D with HfO_2 showed the most promising results comparing with the Al_2O_3 MOS-D, though Al_2O_3 MOS-D showed slightly smaller I_{rev} than HfO_2 MOS-D.

Figure 4-10 I-V characteristics of SDs and MOS-Ds on $AlInN/GaN$ HS

The capacitance characteristics of the devices at 1 MHz are shown in Figure 4-11 (a). As expected, a capacitance decrease and negative threshold voltage shift were observed in the MOS-D compared

with the SD. The capacitance of Al₂O₃ based MOS-D was smaller than the other MOS devices; this is due to the fact that the dielectric constant of Al₂O₃ is smaller than that of HfO₂ and ZrO₂ [191]. From the decrease of capacitance, the dielectric constant of the gate dielectrics was estimated to be 7, 18, and 14 for Al₂O₃, HfO₂ and ZrO₂, respectively. The carrier density ($n_{2\text{DEG}}$) at 0 V in the AlInN/GaN devices is $\sim 10^{13}\text{cm}^{-2}$ which is higher than in the AlGaN/GaN, as expected from the theory (see chapter 2). Moreover, this value can be even higher with a suitable dielectric layer onto the AlInN, such as HfO₂ or ZrO₂, where $n_{2\text{DEG}}$ increased by 60% than SD (Figure 4-11 (a)). In contrast, the $n_{2\text{DEG}}$ of MOS-D with Al₂O₃ was like that of the SD. The threshold voltage shifts to negative values in all the MOS-D respect to the conventional SD, about -4.3 V in the case of HfO₂ and ZrO₂, and -2.8 V in the case of Al₂O₃, due to the insertion of the dielectric layer.

In the negative bias region, no hysteresis nor frequency dispersion was observed in the MOS-Ds, except for the MOS-D with ZrO₂ dielectric, which showed 0.2 V hysteresis, it could be related to mobile charges in the dielectric layer, and the density was calculated to be $2.5 \times 10^{11}\text{cm}^{-2}$.

Figure 4-11 C-V characteristics of SDs and MOS-Ds at (a) negative and (b) positive range on AlInN/GaN HS

The interface state density of the devices can be estimated using the conductance method (see Appendix D). The fitting of G_p/w is shown in Figure 4-12 (a), the D_{it} and the relevant energy level of the traps are shown in Figure 4-12 (b). The SD showed surface traps at 0.29 eV below the conduction band with a density of $2 \times 10^{12}\text{cm}^{-2}\text{eV}^{-1}$, which is comparable to that in the AlGaN/GaN SD. These traps are most likely dislocation related [284]. The HfO₂ and Al₂O₃ MOS-Ds showed similar types of oxide/AlInN interface traps at energy level of 0.08-0.09 eV, with a density of $3.9 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$ and $4.9 \times 10^{11}\text{cm}^{-2}\text{eV}^{-1}$, respectively. This kind of traps have been observed in AlInN/GaN devices by photocurrent method, they are likely interface states associated with nitrogen vacancies [285]. The

ZrO₂ MOS-Ds showed $6.4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ interface traps at 0.26 eV, which might be surface traps, similar to those observed in the SD.

In the case of positive bias voltage, there was no hysteresis observed in the HfO₂ or ZrO₂ MOS-D, indicating that there is very few interface states in the oxide/AlInN interface. However, there is a 1 V hysteresis observed in the Al₂O₃ MOS-D, demonstrating the existence of interface charges in the oxide/AlGaN region, the charge density is calculated to be $4.3 \times 10^{12} \text{ cm}^{-2}$.

Figure 4-12 (a) Conductance, G_p/w calculated for the different diodes, and (b) the $D_{it} - E_c - E_T$ achieved from the fitting curves

b) HEMTs and MOS-HEMTs:

DC and pulsed characterization of the conventional HEMTs and MOS-HEMTs, with gate length (L_G) 3 μm , gate drain distance (L_{GD}) 5 μm and gate width (W_G) 100 μm , were carried out at RT. From the DC output characteristics at $V_{GS} = 1 \text{ V}$ in Figure 4-13, the MOS-HEMTs with HfO₂ dielectric layer showed the highest $I_{D,max}$ and smallest R_{ON} respect to the conventional HEMTs, which is about 10% and 12% change, respectively. However, the behavior of the MOS-HEMTs with the other gate dielectrics was close to that of the conventional HEMTs. The values of $I_{D,max}$, R_{ON} , $g_{m,max}$ and V_{th} are shown in Figure 4-14.

Figure 4-13 (a) I_D - V_{DS} and (b) g_m - V_{GS} of AlInN/GaN and oxide-MOS-HEMTs at RT

The transfer characteristics of the devices (Figure 4-13 (b)) shows the $g_{m,\text{max}}$ of the MOS-HEMTs and HEMTs at $V_{DS} = 4.9$ V. The $g_{m,\text{max}}$ of the MOS-HEMTs is about 20% lower than that of the HEMTs, in a similar way with the AlGaIn/GaN MOS-HEMTs. And the V_{th} shifted negatively, from -6.0 V in the HEMTs to -8.4 V, -8.4 V and -10.5 V in Al_2O_3 , ZrO_2 and HfO_2 MOS-HEMTs, respectively. This is due to the further separation between the gate and the 2 DEG channel with the presence of the additional oxide layer in the MOS structure, and it has been widely observed in other AlInN MOS-HEMTs [198], [283], [286].

Figure 4-14 Values of (a) $I_{D,\text{max}}$, R_{ON} and (b) $g_{m,\text{max}}$, V_{th} in the HEMTs and MOS-HEMTs on AlInN/GaN HS

Regarding the off-state drain current (I_{OFF}) shown in Figure 4-15, I_{OFF} of the AlInN/GaN HEMTs was 10^3 higher than that of the AlGaIn/GaN HEMTs. This is likely due that the $n_{2\text{DEG}}$ in the AlInN/GaN HS is much high than AlGaIn/GaN HS, which makes the control of the charges in the channel more difficult. However, in the MOS-HEMTs with a thin layer of gate dielectric, the I_{OFF} values were reduced by 10 to

10^3 , with respect to the AlInN/GaN HEMTs. And the highest I_{ON}/I_{OFF} (10^6) was the MOS-HEMTs with ZrO_2 , in both linear ($V_{DS}=0.1$ V) and saturation ($V_{DS}=10$ V) regions, a detailed comparison of the I_{OFF} , on/off ratio are shown in Figure 4-16.

Figure 4-15 I_D - V_{GS} of AlInN/GaN and oxide MOS-HEMTs at (a) $V_{DS} = 0.1$ V and (b) 10 V at RT

To analyze the trapping effects in the HEMT and MOS-HEMT devices, pulsed measurements were also carried out. Figure 4-17 shows the pulsed I-V curves of the HEMTs and MOS-HEMTs at different quiescent points at $V_{GS} = 1$ V, and the corresponding GLR and DLR.

Figure 4-16 Values of (a) $I_{D,off}$, on/off and (b) GLR, DLR in the HEMTs and MOS-HEMTs on AlInN/GaN HS

The GLR increased in the MOS-HEMTs, from 0.68 to 0.76 (Al_2O_3 and HfO_2) and 0.85 (ZrO_2), indicating a high reduction of the surface trapping effects compared with the AlInN/GaN HEMTs, in good agreement with the results of the diodes. Drain lag was also improved in the MOS-HEMTs, like in the

case of AlGaIn/GaN HS. The highest DLR value (0.89) corresponded to MOS-HEMT with Al_2O_3 and HfO_2 , which is a 10% higher than in the conventional HEMTs, proving the effectiveness of the dielectrics.

Figure 4-17 Pulsed IV curves of (a) HEMTs and MOS-HEMTs on AlInN/GaN HS

In summary, AlInN/GaN had larger leakage current than AlGaIn/GaN devices, however, the use of a gate dielectric layer such as Al_2O_3 , HfO_2 and ZrO_2 in between source and drain on the devices, reduced both the gate leakage currents and the off-state drain current, mitigated the trapping effects successfully, compared with the AlInN/GaN HEMTs. Among them, the use of HfO_2 improved the output characteristics more than the other dielectrics though the on/off ratio of the devices were not as high as ZrO_2 MOS-HEMTs, so we get to the conclusion that that HfO_2 is the best candidate in AlInN/GaN HS, the same to the AlGaIn/GaN HS.

4.1.3 GaN/AlInN/GaN heterostructures

The R_c of the ohmic contacts and the R_{sheet} of the 2DEG were $0.8 \, \Omega \cdot \text{mm}$ and $480 \, \Omega/\square$, respectively, as calculated using TLM technique (see Appendix D). The $n_{2\text{DEG}}$ and μ were $1.1 \times 10^{13} \, \text{cm}^{-2}$ and 1030

$\text{cm}^2\text{V}^{-1}\text{s}^{-1}$, respectively. After dielectric deposition, the R_c was about $0.7\pm0.1\ \Omega\cdot\text{mm}$, and the R_{sheet} was about $500\pm10\ \Omega/\square$.

The previous published results showed that the smallest I_{rev} of $\text{Al}_2\text{O}_3/\text{GaN}/\text{AlInN}/\text{GaN}$ MOS HEMTs was close to $1\ \text{nA/mm}$ with $10\ \text{nm}\ \text{Al}_2\text{O}_3$ [287]; for $\text{GaN}/\text{AlInN}/\text{GaN}$ MOS HEMTs using HfZrO_2 , the $I_{G,\text{rev}}$ was decreased by 10^2 , about $10\ \mu\text{m/mm}$ [288]. In the following parts, we are going to compare the effects of Al_2O_3 , HfO_2 and ZrO_2 on the $\text{GaN}/\text{AlInN}/\text{GaN}$ HS.

a) SD and MOS-D

The I-V characteristics of the $\text{GaN}/\text{AlInN}/\text{GaN}$ SDs and MOS-Ds are shown in Figure 4-19 (a). The I_{rev} in the SD is about $10^3\ \text{A/cm}^2$, which is 10^3 higher than the SD in AlInN/GaN . However, using a gate dielectric, such as Al_2O_3 , HfO_2 , or ZrO_2 the I_{rev} values were reduced significantly. The lowest value ($5\times10^{-5}\ \text{A/cm}^2$) corresponded to MOS-Ds with Al_2O_3 .

In the forward biased, the I_{for} was as high as $2\times10^3\ \text{A/cm}^2$ in the $\text{GaN}/\text{AlInN}/\text{GaN}$ SD. However, this value was reduced with a proper gate dielectric. The lowest I_{for} values corresponded to MOS-Ds with Al_2O_3 and HfO_2 , around $10^{-5} - 10^{-6}\ \text{A/cm}^2$.

Figure 4-18 I-V properties of $\text{GaN}/\text{AlInN}/\text{GaN}$ SDs and oxide based MOS-Ds

The capacitance curves of the devices at $1\ \text{MHz}$ are shown in Figure 4-19. Similar to the C-V characteristics in AlGaN/GaN and AlInN/GaN , a lower capacitance and negative threshold voltage shift was observed in the MOS-D. From the decrease of capacitance, we estimated the dielectric constant to be 8, 14, and 14 for Al_2O_3 , HfO_2 and ZrO_2 , respectively, similar to those we have estimated previously. No hysteresis was observed in the negative bias range of the MOS-Ds, so there were no mobile charges at the AlGaN/GaN interfaces.

The threshold voltage shifted negatively in the three kinds of MOS-Ds, compared with the SDs, from -6 V of SD to about -12 V of ZrO₂ MOS-Ds, -9 V of Al₂O₃ MOS-Ds and -7 V of HfO₂ MOS-Ds. This negative shift was due to the introduction of the dielectric layer and the appearance of positive charges in the dielectric interface or the channel.

Figure 4-19 C-V properties of Schottky Diodes and oxide based MOS-Ds at (a) negative and (b) positive voltage.

The interface state density of the devices was calculated using the conductance method (see Appendix D for details). The fitting of G_p/w is shown in Figure 4-20(a), and D_{it} versus the relevant energy levels are shown in Figure 4-20 (b). The SD showed surface trap density of $2.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ at 0.28 eV below the conduction band, which is similar to the kind of traps observed in AlInN/GaN HS, most likely dislocation related [284]. The traps in the MOS-Ds were located at energy level of 0.22 eV – 0.26 eV under the conduction band, related to dislocations in the AlInN layer [287].

Figure 4-20 (a) Conductance, G_p/w calculated for the different MOS-Ds, and (b) the D_{it} and $E_c - E_{it}$ calculated from the fitting using the conductance method.

b) HEMTs and MOS-HEMTs

DC and pulsed characterization of the GaN/AlInN/GaN HEMTs and MOS-HEMTs were carried out at RT. From the DC output characteristics at $V_{GS} = 1$ V shown in Figure 4-21, R_{ON} in the MOS-HEMTs increased by 20% - 50%, $I_{D,max}$ in the Al_2O_3 and HfO_2 MOS-HEMTs decreased by 20% and 30% , compared with the GaN/AlInN/GaN HEMTs. In the case of ZrO_2 MOS-HEMTs, $I_{D,max}$ was not decreased, but V_{knee} shifted by $\sim +4$ V of the knee voltage. The values of $I_{D,max}$, R_{ON} , $g_{m,max}$ and V_{th} are shown in Figure 4-22.

Figure 4-21 I_D - V_{DS} of GaN/AlInN/GaN and oxide-MOS-HEMTs at RT

The transfer characteristics of the devices in Figure 4-21 (b) showed that V_{th} shifted negatively, from -6.0 V in the HEMTs to -7 V, -8 V and -10 V in the MOS-HEMTs with HfO_2 , Al_2O_3 and ZrO_2 , respectively. The $g_{m,max}$ of the MOS-HEMTs decreased by 16%~25% in the MOS HEMTs compared with the HEMTs.

Figure 4-22 Values of (a) $I_{D,max}$, R_{ON} and (b) $g_{m,max}$, V_{th} in the HEMTs and MOS-HEMTs on GaN/AlInN/GaN HS

In addition, the off-state drain current densities are shown in Figure 4-23. Like in the case of AlGaIn/GaN and AlInN/GaN heterostructures, the I_{OFF} was decreased in the MOS HEMTs by using the dielectric layers. In this case, the lowest I_{OFF} corresponds to HfO_2 (5×10^{-7} A/mm), with the highest on/off ratio (10^6), which is in accordance with the AlInN/GaN MOS-Ds with HfO_2 .

Figure 4-23 g_m - V_{GS} of GaN/AlInN/GaN and oxide-MOS-HEMTs at RT

The I-V pulsed characteristics are shown in Figure 4-24. For the HEMTs, GLR was 0.47, signifying high density of trapped charges on the GaN surface. However, the MOS-HEMTs using HfO_2 , ZrO_2 and Al_2O_3 dielectric layers reduced the current collapse drastically and the GLR values were much closer to 1, between 0.90 (for HfO_2) and 0.95 (for Al_2O_3). In addition, the DLR values were also improved, from 0.72 in HEMTs to 0.90 in the MOS-HEMTs, showing that the gate dielectrics also plays a significant role in the mitigation of the drain lag effects.

Figure 4-24 Pulsed IV curves of (a) HEMTs and (b, c, d) oxide based MOS-HEMTs at RT

In summary, the use of a gate dielectric layer such as Al_2O_3 , HfO_2 or ZrO_2 , at the source and drain region of the GaN/AlInN/GaN HS, is necessary to achieve devices with a low leakage current, high on/off ratio, and low charge trapping effects. From this study, we get to the conclusion that MOS devices with HfO_2 dielectric has better behavior than the other two kinds of dielectrics, featured by the lowest leakage current, the highest on/off ratio and the smallest trapping effects, as shown in Figure 4-25.

Figure 4-25 Values of (a) $I_{D,off}$, on/off and (b) GLR, DLR in the HEMTs and MOS-HEMTs on GaN/AlInN/GaN HS

4.2 Effects of varying the surface treatment before HfO_2 deposition

HfO_2 with relative dielectric constant of about 20, electron affinity of about 1.75-2.0 eV [289] and band gap of about 5.3 eV [203], has been proven to be effective in reducing the leakage current in Si, GaAs and GaN [201] based MOS devices. The study in the previous section demonstrated that among

the three kinds of dielectrics, HfO_2 is the most suitable dielectric on the three kinds of HS. During the procedure, we have used the traditional organic cleaning procedure, however, some previous works have shown that the gate leakage reduction can be improved using a surface treatment before dielectric deposition [236], [237], such as KOH. Therefore, a study on the effects of cleaning procedure using KOH solution before HfO_2 deposition was analyzed on AlGaIn/GaN MOS-HEMTs.

Two different kinds of cleanings are used, namely,

- a) “Organics”: based on acetone (5 min) + methanol (5 min) + deionized water (DIW), and
- b) “KOH”: with the same “Organics” cleaning and a KOH (0.5 mol/L) cleaning procedure at RT for 20 s, the parameters are chosen based on previous studies [207].

Both MOS-Ds and MOS-HEMTs are compared to conventional SDs and HEMTs.

4.2.1 Schottky diodes and MOS-Ds

The I-V characteristics of the GaN/AlGaIn/GaN SDs and HfO_2 based MOS-Ds are shown in Figure 4-26. The I_{rev} in MOS-Ds was about 10^4 lower than in the SD, regardless of cleaning procedure. However, the lowest I_{for} was observed in the MOS-D (KOH), with a value 10^6 smaller than the SD, and 10^4 smaller than the MOS-D (Organics). The Schottky barrier height was calculated to be close to 1.0 eV for both SD and MOS-Ds with different cleaning process. The ideality factor of the SD was far from 1, between 3 to 4.5, which is comparable with the results from the literature [290].

Figure 4-26 (a) I-V properties and (b) TAT fitting plots of HfO_2 based MOS-Ds (Organics and KOH)

In addition, the electron transport mechanisms were analyzed in both kinds of devices by measuring the I-V characteristics, as described in Appendix D. For the SD, the dominant electron transport

mechanism is Schottky emission (SE), whereas for the MOS-D (both Organics and KOH cleaned), it is trap assisted tunneling (TAT), with an activation energy of 0.31 eV and 0.57 eV, respectively, as shown in Fig. 4-19 (b). The energy level at 0.31 eV on the MOS-D (Organics) is likely due to C substituting N (C_N) [277]. Interestingly, C related traps were not observed in the MOS-D (KOH), proving that the KOH cleaning is effective to remove C on the GaN surface [291]. On the MOS-D (KOH), there were traps at energy level of 0.57 eV, often observed at the AlGaIn/GaN interface on the GaN side [274], [276], [292].

The capacitance-voltage curves and the carrier density of the diodes are shown in Figure 4-27. From the MOS-D, the dielectric constant of the HfO_2 was calculated to be 15, which is in agreement with the literature [207]. No hysteresis nor frequency dispersion was observed in all the diodes, SD or MOS-Ds. No V_{th} shift was observed in the MOS-D (KOH) with respect to the SD. However, a 0.4 V V_{th} positive shift was noted in the MOS-D (Organics), with respect to the SD or MOS-D (KOH). This indicated injection of electrons in the oxide bulk or in the oxide/epilayer interface, similar to those observed in Y_2O_3 based MOS-HEMTs [63], where V_{th} positive shift happened because of the presence of fixed oxide charges in the oxide bulk and the oxide/epilayer interface.

The charges density was estimated to be $5.5 \times 10^{11} \text{ cm}^{-2}$ using:

$$D_{it} = \frac{C_{ox} \cdot \Delta V_{th}}{q^2}$$

where C_{ox} is the HfO_2 capacitance, and ΔV_{th} is the V_{th} shift.

Figure 4-27 (a) C-V and (b) carrier density properties of SDs and HfO_2 based MOS-Ds

In order to further study the properties of the dielectric and the HfO_2 /GaN interface, the MOS-Ds were swept from -6 to 6 V with 0.1 V/step and 0.3 s/step (Figure 4-28 (a)). When positive gate bias

was applied, electrons accumulated at the AlGa_N layer, leading to an increase of capacitance to dielectric capacitance (C_{HfO_2}); however, no saturation of C_{HfO_2} was observed in our case.

Frequency dispersion was detected in the MOS-D (KOH), during the positive sweep range, though it was not observed in the negative voltage sweep, featured by an on-set voltage shift with frequency. According to [187], we have estimated the interface state density and the energy level associated with this dispersion. The trap energy calculated from CV sweep at 1 MHz and 600 KHz was 0.27 eV and 0.29 eV, the interface state density at the average energy level was $1.7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Based on the previous discussion on the electron transport mechanisms, we concluded that these traps are at the HfO₂/Ga_N interface, due to the linear dislocations in the heterostructure. The frequency dispersion of the CV-f curves in the MOS-D (Organics) was not clearly observed, so we could not use this method to identify the traps. Therefore, the interface states of the three kinds of devices was analyzed using the conductance method [32, 33].

Figure 4-28 C-V-f characteristics of the HfO₂ based MOS-Ds in Ga_N/AlGa_N/Ga_N at positive voltage

The interface density as a function of energy level calculated using the conductance method is shown in Figure 4-29. Similar to the discussion described before, the traps in the MOS-D (KOH) located at energy level of $0.56 \pm 0.01 \text{ eV}$. The trap energy level of the MOS-D (Organics) was $0.31 \pm 0.02 \text{ eV}$, similar to that estimated in the SD of 0.31-0.45 eV.

Figure 4-29 interface state density as a function of energy level in the diodes

4.2.2 HEMTs and MOS-HEMTs

The MOS-HEMTs (both Organics and KOH) showed a smaller maximum drain current ($I_{D,max}$) and higher on resistance (R_{on}) compared with the conventional HEMTs, as shown in Table 4-1. $I_{D,max}$ decreased by 11% and 9% in MOS-HEMTs with Organics and KOH cleaning, respectively (Figure 4-30 (a)). This can be explained by the $\sim 10\%$ R_c increase, measured after the feed contacts deposition in the MOS-HEMTs, possibly due to the HfO_2 remains between the ohmic contact and the feed metal.

Figure 4-30 (a) I_D - V_{DS} and (b) g_m - V_{GS} of AlGaIn/GaN and HfO_2 MOS-HEMTs at RT

Transconductance characteristics of the HEMT devices are shown in Figure 4-30 (b). There was about 4% decrease in $g_{m,max}$ in the MOS-HEMTs with respect to the HEMTs, and there was a +0.2 V positive V_{th} shift in the MOS-HEMTs (Organics), in good agreement with the C-V characteristics. This positive shift of V_{th} indicated that there were negative charges in the oxide bulk or oxide/GaN interface.

Figure 4-31 I_D - V_{GS} of AlGaIn/GaN and HfO₂ MOS-HEMTs at (a) 0.1 V and (b) 10 V

In addition, the off-state drain current of the MOS-HEMTs (at $V_G = -7V$) was about 1.0×10^{-7} A/mm regardless the surface cleaning, in good agreement with the results found in the diodes. The on/off ratio of the MOS-HEMTs (both Organics and KOH) is 10^7 , which is about 10^4 times higher than the conventional HEMTs (Figure 4-31 (b)). These results showed that the MOS-HEMTs reduced both the drain and gate leakage currents of the GaN/AlGaIn/GaN HEMTs, and increased on/off ratio of the devices, so they are good candidates for switching applications.

Table 4-1 $I_{D,max}$, R_{on} , $g_{m,max}$ and V_{th} values achieved from DC-IV measurements

	$I_{D, max}$ (A/mm)	R_{ON} (Ω .mm)	$g_{m, max}$ (mS/mm)	V_{th} (V)
Conv-HEMTs	0.56	6.9	114	-4.2
MOS-HEMTs (Organics)	0.47	8.6	110	-3.9
MOS-HEMTs (KOH)	0.51	8.7	112	-4.0

Pulsed I-V characteristics of the HEMT and MOS-HEMTs are compared in Figure 4-32. A large gate lag is observed in the HEMTs, with a GLR of 0.35. This value increased to 0.53 in the MOS-HEMTs (KOH), showing a reduction of the surface traps on the device by the dielectric layer. However, the change of the DLR among the devices was not significant, indicating that the traps in the GaN buffer layer was dominant and the dielectric between drain and source has almost no effect on the channel.

Figure 4-32 Pulsed IV curves of (a) GaN/AlGaIn/GaN HEMTs and (b, c) MOS-HEMTs with HfO₂

In summary, the use of HfO₂ gate dielectric in GaN/AlGaIn/GaN HEMTs showed a decrease of I_{rev} , I_{for} and $I_{D,off}$ by over 10^4 , increase of on/off ratio around 10^4 and reduction of surface trapping phenomena. In addition, the KOH based surface cleaning prior the HfO₂ layer deposition have improved the beneficial effects of the HfO₂ layer further, with smaller change in $I_{D,max}$ and $g_{m,max}$. Also, the pre-cleaning using KOH has proven to be effective in removing C related traps on the GaN surface.

4.3 Effects of post-thermal annealing of HfO₂

In various publications, the effect of short thermal annealing (STA) on MOS-HEMTs with Al₂O₃ [68], Y₂O₃ [213] and so on has been studied, it has been proven to be effective in removing bulk charges or interface charges, and improve the devices properties. Therefore, we have conducted a STA at 400°C on the HfO₂ MOS devices, on one hand, to check the effects of STA on the devices; on the other hand, to compare the thermal stability among conventional HEMTs, MOS-HEMTs (Organics) and MOS-HEMTs (KOH) after STA. During the study, STA was carried out in a hot oven at 400°C in N₂ atmosphere for 10 minutes. Here, we have chosen this temperature because it has been studied that the crystallization temperature of HfO₂ is about 400°C [294].

4.3.1 Schottky diodes and MOS-Ds

I-V characteristics at RT of the GaN/AlGaIn/GaN SDs and HfO₂ based MOS-Ds before and after the STA are shown in Figure 4-33 (a). Comparing the I_{rev} and I_{for} of the diodes before and after STA, we can see that after STA, I_{rev} decreased by 10^2 in SD, and by 10^1 in the MOS-Ds regardless of cleaning procedure; I_{for} increased by 10^1 in the SD and MOS-D (Organics), it decreased by 10^1 in the MOS-D (KOH). In general, MOS-D (KOH) showed the smallest I_{rev} and I_{for} after the STA, about 1.0×10^{-6} A/cm² and 2.0×10^{-6} A/cm², respectively. The main electron transport mechanism in the MOS-D (KOH) after the STA was still TAT, by shallow vacancies with activation energy of 0.18 eV under the conduction

band, instead of 0.57 eV before STA; for the MOS-D (Organics), the activation energy is about 0.38 eV instead of 0.31 eV, as shown in Figure 4-33(b). The traps at energy level of 0.17-0.24 eV were related to linear line defects due to the dangling bonds along dislocation cores [295], and those at energy level of 0.38 eV in the MOS-D (Organics) were likely due to HfO_2/GaN interface traps in the oxide side [188].

Figure 4-33 I-V properties of SD and MOS-Ds with HfO_2 before and after STA

The capacitance-voltage characteristics of the diodes before and after the STA are shown in Figure 4-34. Positive V_{th} shift was observed in all diodes, indicating surface traps in the devices. The trap density was estimated to be $0.8 \times 10^{13} \text{ cm}^{-2}$.

Figure 4-34 Capacitance-voltage curves of HfO_2 based MOS-Ds and SDs before and after STA.

The KOH MOS-Ds were swept from 0 to 6 V with a 0.1 V step, as shown in Figure 4-35. There is smaller on-set positive voltage shift and stretch-out in the MOS-Ds (KOH) after STA, indicating less interface state charge [187].

Figure 4-35 Positive C-V curves of MOS-Ds (KOH) before and after STA

After STA, the interface density at trapping centers of 0.24 eV was calculated to be $0.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, using the technique described in Ref. [187], which is also summarized in Appendix D. Based on the previous discussion on the electron transport mechanisms, we can conclude that these traps are at the $\text{HfO}_2/\text{epilayer}$ interface, due to the linear dislocations in the heterostructure.

Figure 4-36 interface state density as a function of energy level for the diodes

Similar to the situation in the devices before STA, the CV-f curves of the MOS-D (Organics) were not clearly observed. Therefore, we have studied the interface states of the three kinds of devices using conductance method [32, 33]. The interface density as a function of energy level is shown in Figure 4-37(a). The traps in the MOS-D (KOH) located at energy level of 0.5 eV, and the trap energy level of the MOS-D (Organics) is about $0.3 \pm 0.02 \text{ eV}$, and is about $0.35 \pm 0.03 \text{ eV}$ in the SD after STA.

4.3.2 HEMTs and MOS-HEMTs

IV characteristics of the HEMTs and MOS-HEMTs before and after the STA are shown in Figure 4-37 (a). After the STA, $I_{D,max}$ decreased and R_{ON} increased in all the devices. $I_{D,max}$ tended to similar values among all three kinds of HETMs, about 0.48 ± 0.1 A/mm. R_{ON} of the MOS-HEMTs (Organics and KOH) was $8.2 \Omega \cdot \text{mm}$, 15% smaller than the conventional HEMTs. The values of the main parameters before and after the STA are summarized in Table 4-2.

Figure 4-37 (a) I_D - V_{DS} and (b) g_m - V_{GS} curves of HfO_2 based MOS-HEMTs and conventional HEMTs before and after STA

Similar to $I_{D,max}$, the $g_{m,max}$ values for the three kinds of devices were practically the same, about 115 mS/mm. Different from CV results of the SD and MOS-Ds discussed before, the MOS-HEMTs (KOH) showed the smallest V_{th} shifted (0.1 V), the MOS-HEMTs (Organics) showed +0.3 V V_{th} shift, the same to the conventional HEMTs. This indicates that the defects with activation energy of 0.38 eV that were observed in the MOS-Ds (Organics), likely carbon related traps [277], located in the gate-drain region.

Table 4-2 Device parameters of the HEMTs and MOS-HEMTs (Organics and KOH) before and after STA

		$I_{d, max}$ (A/mm)	R_{ON} ($\Omega \cdot \text{mm}$)	$g_{m, max}$ (mS/mm)	V_{th} (V)
HEMT	As fab	0.56	6.9	114	-4.2
	After STA	0.47	9.7	115	-3.75
MOS-HEMTs (Organics)	As fab	0.47	8.6	110	-3.9
	After STA	0.49	8.2	117	-3.5
MOS-HEMTs (KOH)	As fab	0.51	8.7	112	-4.0
	After STA	0.49	8.2	115	-4.0

The transfer characteristics of the HEMTs before and after the STA in Figure 4-38 showed that the I_{OFF} decreased by 10, 10^2 times in the MOS-HEMTs (Organics) and MOS-HEMTs (KOH), in good agreement with the MOS-Ds. The highest on/off ratio after the STA (10^8) corresponded to the MOS-HEMTs (KOH), which was about 10^4 higher than the conventional HEMTs, similar to the values before the STA.

Figure 4-38 I_D - V_{GS} of HfO_2 based MOS-HEMTs and HEMTs before and after STA

Pulsed measurements were taken on the MOS-HEMTs (KOH and Organics) before and after the STA (Figure 4-39). The curves showed that GLR increased by 25%, indicating that there was less surface trapping effects in the HfO_2 MOS-HEMTs (KOH) after STA. This can be explained by the decrease of oxygen complex and Ga vacancies after STA.

Figure 4-39 Pulsed I_D - V_{DS} curves of HfO_2 based (a) MOS-HEMTs (Organics) and (b) MOS-HEMTs (KOH) before and after STA

From the discussion above, we can see that for the SD and conventional HEMTs, the I_{for} and I_{OFF} increased after STA, though I_{rev} decreased. However, in the MOS-HEMTs, I_{OFF} and on/off ratio did not change, and the GLR increased after STA, and in the MOS-D (KOH), the I_{for} did not increase as in the SDs and MOS-D (Organics), proving that the MOS devices with KOH cleaning has better thermal stability after STA, and the STA is helpful in reducing the trapping effects and improving the devices characteristics by removing C related defects in the MOS devices, especially the MOS-HEMTs.

4.4 Summary

In this part, conventional HEMTs fabricated on AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN heterostructures and the relevant MOS-HEMTs using Al_2O_3 , HfO_2 and ZrO_2 were characterized and compared. The gate dielectrics were deposited in between source and drain contacts using ALD technique, and the thickness of the dielectrics are 5 nm. Two kinds of devices (SD/MOS-Ds and HEMTs/MOS-HEMTs) were characterized. From the characterization results, it was observed that MOS devices (MOS-Ds and MOS-HEMTs) showed a significantly decreased gate leakage current, off-state current and increased on/off ratio compared the conventional devices, which is in accordance with our expectation.

Comparing MOS devices with the three kinds of dielectrics on each HS, for the AlGaIn/GaN HS, all three kinds of dielectric have effectively decreased the leakage current and off-state current by 10^3 , the surface trapping effects and buffer trapping effects have been improved in the MOS-HEMTs, especially the MOS-HEMTs with HfO_2 . In the case of AlInN/GaN HS, HfO_2 MOS-Ds showed the most decrease in I_{rev} and I_{for} , and the MOS-HEMTs showed the best output property and leakage current among the three kinds of MOS devices. In the case of GaN/AlInN/GaN HS, the MOS-Ds with HfO_2 decreased the leakage current and showed the lowest off-state current. Therefore, in general, HfO_2 gate dielectric is the most suitable for all three kinds of HS at RT.

During the study, $I_{D,max}$ and $g_{m,max}$ decrease as well as V_{th} negative shift has also been observed besides leakage current decrease and on/off ratio increase. This is because $I_{D,max}$ is reversely proportional to the distance between gate and 2DEG channel. With the introduction of dielectric layer, the distance was increased, therefore, the $I_{D,max}$ decreased. However, the decrease was different among the different cases, due that the electron mobility and carrier density was also changed by the introduction of the dielectric layer. This should be done by solving poisson equations using simulations.

Afterwards, an optimization of the device fabrication procedure by applying a pre-deposition cleaning using KOH solution before dielectric deposition was carried out. Considering the best condition of the previous results, we have used AlGaIn/GaN HS with HfO_2 as dielectric layer. By

comparing the leakage depression effects and output behaviors of the conventional devices, the MOS devices with normal organic cleaning and the MOS devices with KOH cleaning, we have observed that both MOS devices with organic and with KOH cleaning have decreased the I_{rev} , I_{for} as well as I_{OFF} by 10^4 , and increased the on/off ratio by 10^4 , however, the MOS-HEMTs with KOH cleaning has better output characteristics than the MOS-HEMTs with organic cleaning.

Then the MOS devices after short thermal annealing was characterized and compared, in order to study the effects of STA and to compare the thermal stability of the devices with organic and KOH cleaning. Results show that STA is helpful in reducing the trapping effects and improving the devices characteristics by removing C related defects. The devices with KOH cleaning has better thermal stability after STA than the other kinds of devices.

Chapter 5 Thermal stability of GaN-based (MOS-)HEMTs

In this chapter, the behavior of the fabricated devices working at elevated temperatures is assed. Firstly, the effects of a thermal cycle (TC), from RT to 425 °C (with 100 °C step), in the conventional HEMTs, and the corresponding transport mechanisms are discussed as a function of the heterostructure, including GaN/AlGaIn/GaN and AlInN/GaN. Also the transport mechanisms in the SD are discussed. Then, the effects of the TC will be analyzed in the GaN/AlInN/GaN MOS-HEMTs with a HfO₂ gate dielectric.

5.1 GaN/AlGaIn/GaN

5.1.1 Schottky diodes

The I-V characteristics of the devices presented in Figure 5-1 showed that the I_{rev} increased gradually with temperature in the devices. I_{rev} of diodes at 425°C gave a value at least 10^2 times higher than that at RT. In addition, I_{rev} decreased by almost to the initial values at RT after the thermal cycle, showing that the increase of I_{rev} caused by high temperature is not permanent.

Figure 5-1 I-V-T characteristics of the GaN/AlGaIn/GaN SDs during the thermal cycle test

The electron transport mechanism in the devices was analyzed as decribed in detail in Appendix D. From the I-V-T characteristics of the SD, the linear dependence $\ln(J/T^2) \sim \sqrt{E}$ is plotted in Figure 5-2 (a), and the value of the barrier height (ϕ_b) and the dielectric constant (ϵ_s) can be extracted from the intercept and the slope of the curve.

Figure 5-2 (a) SE plot of the forward I-V characteristics (b) FNT plot of the forward I-V characteristics at each temperatures for the GaN/AlGaIn/GaN SDs

The estimated ϵ_s and ϕ_b values at each temperature were evaluated at an electric field range lower than 1.1 MV/cm, and they were shown in **Error! Reference source not found.**. The estimated ϵ_s is far away from the theoretical value of the heterostructure, which shows that the SE is not the main electron transport mechanism in the study.

Table 5-1 Parameters extracted from Schottky Emission (< 1.1 MV/cm)

	slope	ϵ_s	intercept	ϕ_b
RT	-3.0×10^{-4}	1.6	0.67	0.67
125	-3.8×10^{-4}	0.99	0.83	0.83
225	-4.7×10^{-4}	--	1.0	1.0
325	-5.3×10^{-4}	--	1.2	1.2
425	-5.8×10^{-4}	--	1.3	1.3

At higher electric fields, the electric field curves showed another linear relationship with the electric field. The barrier height and dielectric constant of the heterostructure are also estimated and summarized in **Error! Reference source not found.**. In this case, the dielectric constant values are beyond reasonable for the AlGaIn/GaN material, thus SE is not dominant in these kind of devices.

Table 5-2 parameters derived from Schottky Emission (1.3~1.8 MV/cm)

	slope	ϵ_s	intercept	ϕ_b
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RT	-8.7e-6	--	0.33	0.33
125	-4.9e-6	--	0.4	0.4
225	-4.6e-6	--	0.47	0.47
325	-7.6e-6	--	0.55	0.55
425	-1.9e-5	--	0.67	0.67

Regarding the FNT, $\ln(J/E^2) \sim \frac{1}{E}$ can be plotted as a linear curve shown on Figure 5-2 (b). The values of ϕ_b can be extracted from the slope of the linear fit curve, as shown in **Error! Reference source not found..** The theoretical value of barrier height between AlGaIn/GaN and Schottky metal is about 1 eV, however the calculated barrier height shown in the table below are too small for the theoretical value, which proves that FNT is neither the electron transport mechanism in this case.

According to the FNT calculations, the trap energy level is at 0.2 eV at 1.2~1.6 MV/cm and 0.16 eV at 0.8~1.1 MV/cm, which will be discussed later as due to trap assisted tunneling.

Table 5-3 Parameters derived from FNT estimation

	1.2~1.6 MV/cm		0.8~1.1 MV/cm	
	slope	ϕ_b	Slope	ϕ_b
RT	-4.0×10 ⁶	0.22	-2.4×10 ⁶	0.16
125	-3.4×10 ⁶	0.2	-2.2×10 ⁶	0.15
225	-3.2×10 ⁶	0.2	-2.2×10 ⁶	0.15
325	-3.2×10 ⁶	0.2	-2.1×10 ⁶	0.15
425	-3.6×10 ⁶	0.2	-2.0×10 ⁶	0.14

Regarding the TFE, $\ln(J/E) \sim \frac{1}{E^2}$ can be plotted as a linear curve shown in Figure 5-3. The values of ϕ_b can be extracted from the intercept of linear fit of TFE current curve, as shown in **Error! Reference source not found..**

Figure 5-3 TFE plot of the forward I-V characteristics

According to calculations, the barrier height calculated from this conduction mechanism is increasing with temperature, and the values calculated from the TFE are very similar among the two electric field regions, which makes this emission method not dominant in the AlGaIn/GaN Schottky diodes.

Table 5-4 Parameters derived from TFE estimation

	1.8~2.0 MV/cm		2.1~3.1 MV/cm	
	intercept	ϕ_b	intercept	ϕ_b
RT	-18.4	0.48	-19	0.5
125	-16.5	0.57	-17.0	0.6
225	-15.6	0.67	-16.1	0.7
325	-15.2	0.79	-15.6	0.8
425	-15	0.9	-15.5	0.95

As discussed before, PFE curves could be linearly fitted with electric field, and the $\ln(J/E_{OX}) \sim \sqrt{E_{OX}}$ of the diodes is plotted in Figure 5-4 (a). The values of ϕ_b and the ϵ_s were extracted from the intercept and the slope of the curve, respectively, as shown in Table 5-5.

Figure 5-4 (a) PF emission plots and (b) TAT plots of the forward I-V characteristics at each temperature

The values show that with increasing temperature, the dielectric constant was close to the theoretical value of the heterostructure, and the effects of PFE becoming more dominant. At higher temperatures, the dielectric constant is no longer fitting the theoretical value. So we have to turn to trap assisted tunneling to search for the electron transport mechanism.

Table 5-5 parameters derived from PF Emission estimation(1 ~ 1.4 MV/cm)

	slope	ϵ_{OX}	intercept	ϕ_b
RT	2.0×104	28	-0.79	0.79
125	2.5×104	17	-0.9	0.9
225	3.1×104	13	-1.1	1.1
325	3.6×104	9	-1.2	1.2
425	4.5×104	6	-1.5	1.5

From 125°C to 225°C, the dominant current conduction mechanism is PFE in the electric field range from 1 to 1.4 MV/cm. However, electron transport mechanisms at the other temperatures and other electric field range still need to be discussed. Regarding the trap assisted tunneling effects in the devices, the electron curves can be plotted using $\ln J_{TAT} \sim \frac{1}{E_{OX}}$, as shown in Figure 5-4 (b). The trap energy level ϕ_t can be derived as a function of the temperature and electric field range, as shown in Table 5-6.

Table 5-6 parameters derived from TAT estimation

	1.1~1.5 MV/cm		0.8~1.1 MV/cm	
	slope	ϕ_b	Slope	ϕ_b
RT	-6.8×10^6	0.32	-4.2×10^6	0.24
125	-6.1×10^6	0.3	-4.1×10^6	0.24
225	-5.9×10^6	0.3	-4.0×10^6	0.23
325	-5.9×10^6	0.3	-3.9×10^6	0.23
425	-6.1×10^6	0.3	-3.8×10^6	0.22

In these cases, the trap activation energy was estimated to be 0.22~0.3 eV, and the TAT mechanisms could be related to shallow traps in AlGaIn/GaN heterostructure, activated by high electric field or high temperature, or acceptor like traps, such as oxygen related complexes like O_N [296].

The C-V characteristics in Figure 5-5 showed that there was no hysteresis in the diodes during the thermal cycle test. Therefore, no activation of traps were observed in the heterostructure. In addition, almost no V_{th} shift was observed during and after the thermal cycle. This shows that the thermally activated traps during the thermal cycle have no noteworthy effects on the electrical behavior of the devices.

Figure 5-5 C-V-T characteristics of the GaN/AlGaIn/GaN SDs during the thermal cycle test

5.1.2 HEMTs

The output characteristics of the devices (I_D - V_{DS} - T) at $V_{GS} = 0$ V (Figure 5-6) show that $I_{D,max}$ decreased with increasing temperature, as expected from the literature since the mobility of the electrons in the channel will be reduced with temperature. This is because that with the increasing temperature,

the thermal mobility of the electrons will be increased, leading to increase of disorder elastic collision among electrons, where the mobility in the direction of current flow decrease [140], [297]. The changes of electric properties in our study is that $I_{D,max}$ at 425°C was ~40% of the value at RT, which is similar to the $I_{D,max}$ decreases at 200°C (by ~40%) in SiO₂/AlGaIn/GaN grown on sapphire [298], showing that the intrinsic devices used in the study have good thermal stability.

Figure 5-6 I_D - V_{DS} - T curves of the HEMTs

The transfer characteristics of the devices at $V_{DS} = 10$ V during the thermal cycle test (I_D - V_{GS} - T) (Figure 5-6) show that $I_{D,OFF}$ of the HEMTs increased by 4 orders of magnitude (from 80 nA/mm at RT to 19 μ A/mm at 225°C, and to 0.2 mA/mm at 425°C).

Figure 5-7 I_D - V_{GS} - T curves of the HEMTs

In addition, the transconductance-gate voltage curves are shown in Figure 5-8. At 425°C, $g_{m,max}$ decreased by ~53% in HEMTs on average.

Figure 5-8 g_m - V_{GS} - T curves of the GaN/AlGaIn/GaN HEMTs

Threshold voltage V_{th} extracted from the g_m - V_G curves are shown in Figure 5-9Figure 8-21. V_{th} is about -4.0 V, and no shift is observed with the temperature. Therefore, the amount of thermally activated charges at the AlGaIn/GaN interface is very small.

Figure 5-9 V_{th} change with temperatures

The pulsed measurements were taken place at room temperature after the thermal cycle test. The I-V curves for different quiescent points are show in Figure 5-10. The DLR of the HEMTs are about 35% better than those of initial values at RT, though the GLR of the devices have decreased by 20%, indicating that the most damage happened at the surface of the conventional HEMTs, which make necessary the protection of the heterostructure layer.

Figure 5-10 Pulsed IV curves of the HEMTs (a) before and (b) after thermal cycle

In summary, the electrical characteristics of the GaN/AlGaN/GaN SD and HEMTs were analyzed during and after a TC from RT to 425°C. The dominant transport mechanism in the SD depends on the range of both the temperatures and the electric field ranges. It was deduced that PFE is the dominant transport mechanism in the electric field range of 1 to 1.4 MV/cm, from 125°C to 225°C, whereas it is TAT in the other temperatures and electric field ranges, with a trap activation energy of 0.22~0.3 eV. In the case of the HEMTs, a drop in the I_{dsmax} and g_{max} , and an increase of the I_{off} was observed as the temperature was higher. However, a recovery of the characteristics after the TC indicated no permanent degradation in the devices. In addition, the V_{th} was very stable during the TC showing that the Schottky contact was not damaged and was able to control the 2DEG also at a high temperature of 425°C.

5.2 AlInN/GaN-based conventional devices

Similar to those AlGaN/GaN-based devices, thermal cycle tests on the AlInN/GaN HEMT devices were also carried out. AlInN/GaN-based devices (diodes and HEMTs) were subjected to a thermal cycle test from RT to 425°C with increment of 100°C.

5.2.1 Schottky diodes

The I-V characteristics of the diodes presented in Figure 5-11 show that the I_{rev} did not change much with temperature until 325°C in the -4 V to 0 V region. In the forward biased region, the I_{for} increased gradually with temperature, and the change is within the range of one order of magnitude. The increase step of the I_{for} is about 0.14 A/cm² per 100°C. This is ~10 times smaller than the AlGaN/GaN Schottky diodes, which is about 2.5 A/cm² per 100°C, from our previous measurements.

Figure 5-11 I-V-T characteristics of the AlInN/GaN SDs during the thermal cycle test

C-V-T characteristics of the Schottky diodes are shown in Figure 5-12. In this case, a capacitance decrease (7%) and a positive shift in the V_{th} (+1 V) up to 425°C was observed during the TC. One of the possible reasons for the lower capacitance as the temperature increases is related to the piezo effects. GaN and AlInN are lattice match materials at room temperature; however, as temperature increases, the different temperature dependence of energy bandgap would lead to different bandgaps of GaN and AlInN at each temperature, and therefore to piezo effects, causing the decrease of charge density by 40% (from $12.7 \times 10^{12} \text{ cm}^{-2}$ at RT to $7.6 \times 10^{12} \text{ cm}^{-2}$ at 325°C), and finally leading to a decrease of capacitance. Another possible explanation is that the temperature dependence of dielectric constant of the AlInN would lead to the capacitance difference in the heterostructure.

Figure 5-12 C-V-T characteristics of the AlInN/GaN SDs during the thermal cycle test

Positive V_{th} shift is usually due to extra negative charges in the AlInN/GaN interface or in the GaN buffer. The higher the temperature, the more positive V_{th} shift in the SDs. This interface charge density increase was estimated to be about $0.5 \times 10^{12} \text{ cm}^{-2}$.

5.2.2 HEMTs

The DC output characteristics of the AlInN/GaN HEMTs as a function of the temperature are shown in Figure 5-13. The $I_{D,max}$ decreases with temperature, which is related to the lower mobility of the electrons in the channel with temperature, as in the GaN/AlGaIn/GaN heterostructure. However, in this case, the drop is much higher (up to 75% at 425°C) than in the GaN/AlGaIn/GaN HEMTs (up to 65% at 425°C). Also, the R_{ON} increased with temperature, up to 112.5% at 425°C. This is different from the expectation that the AlInN/GaN structure should have better thermal stability than the AlGaIn/GaN devices [239].

Figure 5-13 I-V-T characteristics of the AlInN/GaN HEMTs during the thermal cycle test

The transconductance curves of the HEMTs with temperature are shown in Figure 5-14. In this case, a positive shift in the V_{th} of +3 V and a decrease in the $g_{m,max}$ up to 52% were observed. Therefore, there are thermally activated charges or traps at the AlInN/GaN interface.

Figure 5-14 g_m - V - T characteristics of the AlInN/GaN HEMTs during the thermal cycle test.

In summary, the effects of a TC in the electrical characteristics of the AlInN/GaN SD and HEMTs have been analyzed. The results show no significant changes in the I_{rev} and I_{for} of the SD with temperature. However, the $I_{D,max}$ of the HEMTs decreased up to 75% at 425°C, which is much higher compared to the GaN/AlGaIn/GaN HEMT. Moreover, a large positive V_{th} shift (up to +3 V) with temperature indicates that the devices are not thermally stable in contrast to the GaN/AlGaIn/GaN HEMTs.

5.3 HfO₂/GaN/AlInN/GaN MOS devices

In this section, the effects of the TC (from RT to 425°C, with 100°C step) as well as the transport mechanisms, will be analyzed in the GaN/AlInN/GaN MOS-D and MOS-HEMTs with HfO₂ gate dielectric.

5.3.1 MOS-Ds

The I-V characteristics of the MOS-Ds during the thermal cycle, displayed in Figure 5-15, show that the leakage current is decreasing with increasing temperature. Moreover, after the whole thermal cycle process, the leakage current at RT is about 10^6 lower than the original value, which suggests that a thermal annealing is necessary after devices fabrication to enhance the leakage current reduction in these HfO₂ AlInN/GaN MOS-HEMTs.

Figure 5-15 I-V-T of the HfO₂/GaN/AlInN/GaN MOS-Ds during the thermal cycle test

From the I-V curves at different temperatures, the dominant electron transport mechanisms were evaluated in HfO₂/AlInN/GaN MOS-Ds, showing that Fowler–Nordheim tunneling (FNT) prevails at low electric fields, and trap assisted tunneling (TAT) at high electrical fields. In this case, the trap energy level is about 0.2~0.3 eV, likely due to shallow oxygen vacancy in the oxide which will form a negative O vacancy (V⁻) [115].

Figure 5-16 (a) FN plot and (b) TAT plot of the forward I-V characteristics

The CV properties of MOS-Ds are shown in Figure 5-17. Different from the other diodes, a negative V_{th} shift is observed with increasing temperatures, showing that a higher density of negative fixed traps are present in the HfO₂/GaN interface as the temperature increases. An estimation of the charge density from the V_{th} shift is about $-5.1 \times 10^{11} \text{ cm}^{-2}$ at 425°C.

Figure 5-17 C-V-T of the HfO₂/GaN/AlInN/GaN MOS-Ds during the thermal cycle test

Also, hysteresis in the CV curves appeared from 125°C; the hysteresis decreased with increasing temperature, which is related to oxide traps, and it is estimated to be about $1.1 \times 10^{11} \text{ cm}^{-2}$ at 125°C. In addition, a stretch out in the C-V curve at high temperatures was observed, likely due to the presence of interface trapped charges at the HfO₂/GaN interface, which is estimated to be $9 \times 10^{11} \text{ cm}^{-2}$ from 325°C using the conductance method.

5.3.2 MOS-HEMTs

The DC IV curves of the HfO₂/GaN/AlInN/GaN MOS-HEMTs during the TC are shown in Figure 5-18. Similar to the HEMT devices, $I_{D,max}$ was decreased up to 55% at 425°C, and R_{ON} increased as the temperature is higher, up to 138% at 425°C. However, the decrease of $I_{D,max}$ is smaller in the HfO₂/GaN/AlInN/GaN MOS-HEMTs than in the conventional HEMTs, in spite of the increase in R_{ON} is larger.

Figure 5-18 I-V-T of the HfO₂/GaN/AlInN/GaN MOS-HEMTs during the thermal cycle test

The transconductance of the $\text{HfO}_2/\text{GaN}/\text{AlInN}/\text{GaN}$ MOS-HEMTs during the TC is shown in Figure 5-19. The $g_{m,\max}$ decreases by 65%, but almost no V_{th} shift was observed, in contrast to conventional AlInN/GaN HEMTs. Therefore, the use of a HfO_2 gate dielectric can improve the thermal stability of the AlInN/GaN HEMTs.

Figure 5-19 g_m - V_g - T of $\text{HfO}_2/\text{GaN}/\text{AlInN}/\text{GaN}$ MOS-HEMTs during the thermal cycle test

In summary, the dominant electron transport mechanisms in the $\text{GaN}/\text{AlInN}/\text{GaN}$ MOS-D with HfO_2 depend on the electric field and temperature range. Fowler–Nordheim tunneling (FNT) dominates at low electric fields, and trap assisted tunneling (TAT) with the trap energy level at about 0.2~0.3 eV is the dominant electron transport mechanism at high electric fields. A lower permanent I_{rev} (up to 10^6) was achieved after the TC, indicating the convenience of using a thermal annealing after the HfO_2 deposition. Respect to the MOS-HEMTs, a decrease in the $I_{D,\max}$ and $g_{m,\max}$, as well as an increase of the R_{ON} was observed as the temperature increased. However, the drop was higher than the conventional AlInN/GaN HEMTs and reversible. Moreover, V_{th} was more stable in the MOS-HEMTs than the conventional HEMTs, leading to MOS-HEMTs with HfO_2 good candidates for high temperature applications.

5.4 Summary

In this chapter 5 we have discussed the thermal stability of the $\text{GaN}/\text{AlGaIn}/\text{GaN}$ and AlInN/GaN conventional devices and compared to that of $\text{HfO}_2/\text{GaN}/\text{AlInN}/\text{GaN}$ MOS devices during a step thermal cycle process, from RT to 425°C.

For the conventional devices, AlInN/GaN HEMTs showed a higher $I_{D,max}$ decrease and R_{ON} increase, as well as more V_{th} shift than the GaN/AlGaIn/GaN HEMTs.

For the HfO₂/GaN/AlInN/GaN MOS devices, results have shown that the HfO₂ dielectric layer is useful to reduce the degradation behaviour during the thermal cycle. The $I_{D,max}$, $g_{m,max}$ decrease and R_{ON} increase and V_{th} shift are much smaller than the conventional HEMTs. The electron transport mechanisms of the MOS structure are discussed, Fowler–Nordheim tunneling (FNT) and trap assisted tunneling (TAT) with the trap energy level at about 0.2~0.3 eV are the dominate electron transport mechanisms in the devices.

Chapter 6 Stability of GaN-based MOS-HEMTs after irradiations

In this chapter, the effects of ion irradiation on conventional and MOS devices are discussed. Firstly, some previous studies about the effects of irradiation on GaN based HEMTs and MOS HEMTs are summarized, as well as the irradiation environment, and the ion properties in this work were introduced. Afterwards, the effects of ion irradiation varying ions and fluences on AlInN/GaN HEMTs and MOS-HEMTs with HfO₂ are compared: the ions used during the study are protons (H⁺) and helium (He⁺), and the fluences are $1 \times 10^{13} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$. Subsequently, a series of irradiation (using H⁺ with a fluence of $1 \times 10^{15} \text{ cm}^{-2}$) on the previously fabricated HEMTs and MOS-HEMTs varying dielectric layer and HS (the group of devices discussed in Chapter 4: AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN HS and) was carried out.

6.1 Introduction

Irradiation effects of AlGaIn/GaN HEMTs with different kinds of coating materials have widely been studied [71], [75], [76], [89], [167]–[171]. Proton irradiation with low energy (275 keV and 330 keV) and low fluence ($4, 5 \times 10^{12} \text{ cm}^{-2}$) at the backside of the samples shows that defects in the 2DEG channel and AlGaIn layer would be created with 330 keV protons, which would cause a reduction in electric field at the gate edges, leading to I_D decrease and off-state drain breakdown voltage increase [16]. The effect of protons with similar energy (380 keV) but higher fluence (10^{14} cm^{-2}) has shown dramatic decrease in the electron mobility in the heterostructure [172]. Then proton irradiation with 1.8 MeV on GaN/AlGaIn HEMTs has shown that irradiation modifies the atomic structure in AlGaIn by producing vacancy-related defects (N_i , $V_{\text{Ga}}-V_N$ and V_{Ga}) as acceptors, leading to V_{th} positive shifts [173].

Effects of irradiation on MOS-HEMTs with Al₂O₃ have shown that the $I_{D,max}$ decreased by 95.3, 68.3 and 59.8% and $g_{m,max}$ were reduced by 88, 54.4, and 40.7%, after the 5 MeV, 10 MeV and 15 MeV proton irradiation with fluence of $5 \times 10^{15} \text{ cm}^{-2}$, respectively [78].

There are all kinds of ions in the atmosphere, in order to investigate the capability of the HEMTs and MOS-HEMTs for space applications, the effects of irradiation using all different kinds of particles should be studied, such as Total ionizing dose (TID) radiation (10 KeV X-ray irradiation) [176], neutron irradiation [4][177], ⁶⁰Co γ -rays irradiation [170], Gamma irradiation [168], and Ge⁺ irradiation [178].

In this work, we have chosen proton and helium as the irradiation particle, due that proton is the most widely studied, where we can compare the devices performance with other researches, and helium is the least used, where we can compare it with proton irradiation. The ion energy was chosen to be 2 MeV in order to achieve apparent effects of irradiation on the devices, but not to kill the

devices; and two irradiation fluences were used: 10^{13} cm^{-2} and 10^{15} cm^{-2} , in order to compare the effects of irradiation with those two kinds of ion fluences.

The irradiation tests were carried out in Centro de Micro Análisis de Materiales (CMAM) in the Universidad Autónoma de Madrid (UAM), using a 5 MV Cockroft-Walton tandem accelerator, as shown in Figure C-10. Prior to the irradiation, the homogeneity of the collimated beam was measured with a quartz reference sample. A picture of the irradiation area on the devices under infrared luminescence (IL) is shown in Figure 6-1 (a). According to TRIM simulations [299], the projected range of 2 MeV H^+ is 24.6 μm , and that of the 2 MeV He^+ is about 4.2 μm , as shown in Figure 6-1 (b).

Figure 6-1 (a) picture of the irradiation area on the devices under IL and (b) comparison of ion range of 2 MeV H^+ and He^+ simulation using TRIM

There are two kinds of mechanisms in the irradiation study, one is direct collision among the atoms [294], and the other is electron-phonon coupling which was studied using inelastic thermal spike model [300]. During the H^+ and He^+ irradiation on GaN based HEMTs, the most possible reaction is electron-phonon coupling with inelastic thermal spike model, because the depth of the H^+ and He^+ ions are more than 15 μm , which will make the collision impossible. However, the collision caused secondary electrons could couple with the electrons in the HS, which will lead to device degradation.

In this part, the comparison of ion irradiation on diodes and HEMTs are going to be discussed. The diodes are square-shape with length of 100 μm , and the HEMTs geometry is $L_G=1.2 \mu\text{m}$, $W_G=50 \mu\text{m}$, $L_{SD} = 5 \mu\text{m}$ and $L_{SG} = L_{GD} = 1.9 \mu\text{m}$.

6.2 Effects of H^+ and He^+ irradiation on AlInN/GaN HEMT and MOS-HEMT with HfO_2

There were many researches on the effects of irradiation on GaN-based devices using different kinds of particles, such as proton, total ionizing dose (TID) radiation (10 KeV X-ray irradiation) [176], neutron

irradiation [4], [177], ^{60}Co γ -rays irradiation [170], gamma irradiation [168], and Ge+ irradiation [178], however, the study of helium irradiation on the GaN based devices are rare.

In the following paragraphs the effects of irradiation with protons and heliums of 2 MeV with two fluences, $1 \times 10^{13} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$, are analyzed on AlInN/GaN and $\text{HfO}_2/\text{AlInN}/\text{GaN}$ devices, including diodes and HEMTs.

6.2.1 Schottky diodes and MOS-Ds

The IV characteristics of the diodes are shown in Figure 6-2, from the curves we can see that I_{rev} of the AlInN/GaN has decreased by 10^3 after $1 \times 10^{15} \text{ cm}^{-2}$ fluence He^+ irradiation, and the I_{rev} of $\text{HfO}_2/\text{AlInN}/\text{GaN}$ MOS-Ds has decreased by 10^5 after the $1 \times 10^{15} \text{ cm}^{-2}$ fluence helium irradiation. In the other cases, the I_{rev} of the SDs decreased by 5 times in the SDs, and the I_{rev} of the $\text{HfO}_2/\text{AlInN}/\text{GaN}$ MOS-Ds has on change. However, the current density of the $\text{HfO}_2/\text{AlInN}/\text{GaN}$ MOS-Ds increased in the voltage range from -5 V to 1 V.

Figure 6-2 IV characteristics of the (a) SDs and (b) HfO_2 based MOS-Ds before and after irradiation.

In general, the H^+ irradiation with $1 \times 10^{13} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$ fluence had negligible effects on the leakage current of the diodes, and the He^+ irradiation with a fluence of $1 \times 10^{15} \text{ cm}^{-2}$ will cause I_{rev} to decrease by 10^3 to 10^5 times in SDs and MOS-Ds, respectively.

Figure 6-3 CV characteristics of the (a) SDs and (b) MOS-Ds before and after irradiation

From the CV curves shown in Figure 6-3, the $\text{HfO}_2/\text{AlInN}/\text{GaN}$ MOS-Ds showed a negative V_{th} shift of -1 V after H^+ irradiation of $1 \times 10^{15} \text{ cm}^{-2}$ fluence. All the devices after $1 \times 10^{15} \text{ cm}^{-2}$ fluence He^+ irradiation showed capacitance decrease, CV curve stretchout and severe V_{th} positive shifts. The SDs showed the capacitance decrease to 4.7 pF, and positive V_{th} shift by +5 V. The MOS-Ds showed the capacitance decrease to 1.7 pF, and positive V_{th} shift by +1 V.

A possible explanation for the capacitance decrease is that the electron-phonon coupling in the channel has caused the dramatic decrease of the 2DEG density in the channel which lead to the capacitance decrease and dramatic positive V_{th} shift.

6.2.2 HEMTs and MOS-HEMTs

The output and transfer characteristic parameters of the conventional and MOS HEMTs after irradiations are shown in Figure 6-4. From the curves, we can see that the damage caused by $1 \times 10^{15} \text{ cm}^{-2}$ fluence H^+ irradiation is stronger than that by $1 \times 10^{13} \text{ cm}^{-2}$ fluence He^+ irradiation. The damage caused by $1 \times 10^{15} \text{ cm}^{-2}$ fluence He^+ irradiation was enormous. Comparing the irradiation harm on HEMTs and MOS-HEMTs, we can see that the effects of irradiation on the conventional HEMTs are much stronger than those on the MOS-HEMTs.

Figure 6-4 Change in the (a) $I_{D,max}$, R_{ON} , and (b) $g_{m,max}$ as a function of the ion type and fluence for both HEMTs and MOS-HEMTs.

Figure 6-5 showed the SRIM simulation of damage difference between 2 MeV H^+ and He^+ on GaN. From the image, we can see that at irradiation distance from 0 to 1 μm , the energy loss of phonon and recoil during He^+ irradiation is much larger than that during H^+ irradiation. Because, the energy loss is due to electron-phonon coupling or recoil collision, the more energy loss, the more damage it would cause on the devices. Therefore, the damage caused by He^+ would be much larger than H^+ with the same fluence. However, when H^+ fluence is 10^2 times larger than He^+ , the damage caused by H^+ has surpassed the damage caused by He^+ , as shown in Figure 6-4. This means that the effects of He^+ would be less than 100 times larger than that of effects of H^+ with the same fluence and same energy, however, the accurate analysis should be done using simulation techniques.

For the MOS HEMTs, the reason why it could inhibit the irradiation damage is that there is no electron in the dielectric layer, which makes it possible to perform as a buffer layer for the coupling between ions and the electrons.

Figure 6-5 SRIM study of damage for 2 MeV H^+ and He^+ on GaN

The DC and transconductance curves of the HEMTs and MOS-HEMTs after $1 \times 10^{15} \text{ cm}^{-2}$ fluence He^+ irradiation is shown in Figure 6-6. The $I_{D,max}$ decreased by more than 10^2 , and R_{ON} increased by 50 times. There is almost no difference between AlInN/GaN conventional HEMTs and the HfO_2 MOS-HEMTs. Therefore, the damage caused by irradiation would be in the AlInN/GaN channel or the GaN buffer layers. This result is different from previous results in [301], which showed that the irradiation caused degradation has no relationship with irradiation ions.

The V_{th} shifted positively to -0.2 V, inspiring the idea of normally-off HEMTs using high fluence He^+ irradiation. However, the problem would be that the $I_{D,max}$ and $g_{m,max}$ decreased too much.

Figure 6-6 IV and g_m characteristics of the HEMTs and MOS-HEMTs after $1 \times 10^{15} \text{ cm}^{-2}$ He^+ irradiation.

In summary, the influences of H^+ irradiation and He^+ irradiation on the AlInN/GaN conventional and MOS-HEMTs are discussed in this part. With the same ion fluence, the effects of He^+ irradiation were

stronger than those of H^+ irradiation. For the same ion, the higher the ion fluence, the more degraded the devices are. The damage caused by the ion irradiation can be explained by electron-phonon coupling using the inelastic thermal spike model. The influence of irradiation on MOS-HEMTs is smaller than those on the conventional HEMTs, due to the protection shielding effects of the dielectric layer. The most damage appeared after $1 \times 10^{15} \text{ cm}^{-2}$ fluence He^+ irradiation, the V_{th} shift to the positive side, which makes He^+ irradiation a potential way to fabricate normally-off devices.

6.3 Proton irradiation on MOS-HEMTs with high-k dielectrics

According to the results achieved from the previous section, we can see that H^+ irradiation with 10^{15} cm^{-2} fluence showed the most difference among conventional and MOS-HEMTs while the devices are working in the reasonable range. In this part, we are focusing on the effects of dielectric layer on the devices after irradiation. Therefore, we decided to use H^+ irradiation with energy of 2 MeV and fluence of 10^{15} cm^{-2} .

During this study, the groups of device we have discussed in chapter are going to be irradiated, characterized and compared, including AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN HEMTs and MOS-HEMTs with Al_2O_3 , HfO_2 and ZrO_2 . Before comparing the irradiation effects on the HEMTs, we are going to study the irradiation effects on the SDs and MOS-Ds first, as discussed below.

6.3.1 AlGaIn/GaN

Similar to chapter 4, we are going to study the effects of H^+ irradiation on AlGaIn/GaN based devices and MOS devices with three kinds of dielectrics including Al_2O_3 , HfO_2 and ZrO_2 . Previous results showed that MOS-HEMTs with Al_2O_3 after proton irradiation have the $I_{D,max}$ decreased by 95.3, 68.3 and 59.8% and $g_{m,max}$ were reduced by 88, 54.4, and 40.7%, after the 5 MeV, 10 MeV and 15 MeV proton irradiation with fluence of $5 \times 10^{15} \text{ cm}^{-2}$, respectively [78].

a) SDs and MOS-Ds

The IV characteristics of the AlGaIn/GaN-based SDs and MOS-Ds before and after the H^+ irradiation are shown in Figure 6-7. In the case of SD, I_{rev} increased by 10^3 , I_{for} did not change. In contrast, in the MOS-Ds, no significant change was observed in the I_{rev} after irradiation, but the I_{for} increased by 10 times in the case of ZrO_2 and Al_2O_3 , and by 10^2 times in the case of HfO_2 . It is worth noting that the I_{rev} values of the MOS-Ds were similar among the three kinds of dielectrics and they are 10^6 smaller than the I_{rev} values of the SD.

Figure 6-7 IV characteristics of the AlGaIn/GaN-based diodes (SD and MOS-D)(a) before and(b) after irradiation

The C-V characteristics and the carrier densities of the SD and MOSD are shown in Figure 6-8. All the devices showed a positive V_{th} shift after irradiation of +0.6 V for the SD, and higher for the MOSDs, +1.1 V, +1.3 V and +1.4 V, for Al_2O_3 , HfO_2 , and ZrO_2 , respectively.

Figure 6-8 CV properties of the AlGaIn/GaN based diodes (SD and MOS-Ds) (a) before and (b) after irradiation

The cause of V_{th} positive shift can be explained by the decrease of carrier density induced by electron trapping at defect sites [73]. Various studies have shown that there is V_{th} positive shift and carrier density decrease after irradiation [75], [76], [302]. The HfO_2 MOS-Ds showed the smallest n_s decrease. The carrier density decrease could be due to inelastic electron-phonon coupling as discussed in the previous section. [73], [303]–[305].

b) HEMTs and MOS-HEMTs

The output and the transfer characteristics of the HEMTs and MOS-HEMTs are shown in Figure 6-9. The DC IV and transconductance of the conventional HEMTs show that the proton irradiation caused great decrease of $I_{D,max}$ and $g_{m,max}$, by 64% ,and 55 %, respectively. In addition, a +0.4 V V_{th} shift was observed in the conventional HEMTs, in good agreement with the C-V characteristics of the SD.

However, the MOS devices showed a lower decrease of the parameters after irradiation, in comparison to the conventional HEMTs. For instance, the MOS-HEMTs with Al_2O_3 and HfO_2 showed a reduction of $I_{D,max}$ and increase of R_{ON} lower than 1%, and the decrease of $g_{m,max}$ is about 6% in the Al_2O_3 MOS-HEMTs. However, the ZrO_2 MOS-HEMTs showed 20% decrease of $I_{D,max}$ and 25% increase of R_{ON} . Respect to the V_{th} shift, there are positive shift in all the devices, it is similar to the V_{th} observed from CV properties. there are the most V_{th} shift in the ZrO_2 MOS-HEMTs (+ 1 V) and the smallest V_{th} shift in the Al_2O_3 and HfO_2 MOS-HEMTs.

Figure 6-9 (a) I_D and (b) g_m properties of the GaN/AlGaIn/GaN-based (MOS)HEMTs before and after irradiation

The smallest degradation occurred in the HfO_2 MOS-HEMTs and the most degradation occurred in the conventional HEMTs. Among the MOS-HEMTs with the three kinds of dielectrics, the ZrO_2 MOS-HEMTs are the most influenced by the irradiation. Therefore, the dielectric layer, especially the Al_2O_3 and HfO_2 helped diminish the damage on the 2DEGs of the devices on the AlGaIn/GaN HS.

6.3.2 AlInN/GaN

Previous publications have shown the effects of irradiation on AlInN/GaN based HEMTs. Proton irradiation with $1 \times 10^{14} cm^{-2}$ on AlInN/GaN HEMTs has shown DC properties decrease due to mobility

and sheet carrier density decrease, and the irradiation created new defect levels located between gate and drain contacts[306].

In the following part, we will compare the results among the AlInN/GaN conventional devices and MOS devices using Al_2O_3 , HfO_2 and ZrO_2 before and after irradiation.

a) SD and MOS-D

The IV characteristics of the AlInN/GaN-based Schottky and MOS-Ds are shown in Figure 6-10. I_{rev} decreased in SD and ZrO_2 MOS-Ds. I_{rev} decreased by 10 times decrease in the SDs, I_{rev} decreased by 10^2 times and I_{for} decreased by 10^3 times in the ZrO_2 MOS-Ds. However, in the HfO_2 and Al_2O_3 based MOS-Ds, I_{rev} increased by 10 times and I_{for} increased by 10^2 . This shows that the ZrO_2 could be the most suitable dielectric on AlInN/GaN heterostructure.

Figure 6-10 IV properties of the AlInN/GaN-based diodes (a) before and (b) after irradiation

The capacitance voltage characteristics of the devices are shown in Figure 6-11. Similar to SD and MOS-D in the others heterostructures, positive V_{th} shift was observed in all the devices after irradiation. The V_{th} shift is about +1.2 V for the SD, the smallest shift in the MOS-Ds is about +0.4 V, in the HfO_2 based MOS-Ds, indicating high irradiation robustness off the HfO_2 based MOS-Ds. And the V_{th} shift in Al_2O_3 and ZrO_2 MOS-Ds are 1.1 V and 2.8 V.

Figure 6-11 CV properties of the AlInN/GaN-based diodes (a) before and (b) after irradiation

b) HEMTs and MOS-HEMTs

The IV and transconductance properties of the AlGaIn/GaN-based conventional and MOS-HEMTs are shown in Figure 6-12. The DC IV and transconductance of the conventional HEMTs show that the proton irradiation caused a great decrease of $I_{D,max}$ and $g_{m,max}$, by 15%, and 37.5%, respectively. In addition, a V_{th} shift of around +1.0 V was observed in the conventional HEMTs, in good agreement with the C-V characteristics of the SD.

Figure 6-12 (a) IV and (b) g_m properties of the AlInN/GaN-based (MOS)HEMTs before and after irradiation

The MOS devices showed a lower decrease of the parameters after irradiation, in comparison to the conventional HEMTs. For instance, the MOS-HEMTs with ZrO_2 showed a decrease of $I_{D,max}$ about 1%, and 6%, the decrease of $g_{m,max}$ is about 2% and the V_{th} shift is about +0.1 V. In the HfO_2 and Al_2O_3 MOS-HEMTs, the decrease of $I_{D,max}$ is about 6% and 20%, the increase of R_{ON} is about 15%, and the decrease

of $g_{m,max}$ is about 11% and 6%, the V_{th} shift is about +1.7 V and +0.8 V, this is different from the results observed in the CV curves.

Upton these observations, different from the AlGaIn/GaN HS, the device design with leakage current decrease as well as the smallest output characteristic degradation is the MOS-HEMTs with ZrO_2 . The leakage current decrease of the MOS-Ds is due to the improvement of isolation in the GaN buffer layer and Ni void formation within the interface, similar to those observed in Al_2O_3 /AlInN/GaN MOS HEMTs [307]. On the other hand, different from this article, we have observed very small dc characterization degradation. This makes our design of AlInN/GaN MOS-HEMTs with ZrO_2 a good option for further study under irradiation environments.

During the study, it is proved that AlInN/GaN HS are more stable under irradiation than the AlGaIn/GaN HS. Regarding the MOS structures, ZrO_2 dielectric is the most suitable for the AlInN/GaN heterostructure devices under irradiation.

6.3.3 GaN/AlInN/GaN

In the study of irradiation effects on AlInN/GaN HEMTs, usually two kinds of designs were used, one is lattice matched AlInN/GaN HS, the other has usually 2.5 nm GaN cap, however, they were not compared directly. The HEMTs after proton irradiation of 5-15 MeV and fixed fluence of $5 \times 10^{15} \text{ cm}^{-2}$ has decreased $I_{D,max}$ by 12% and increased I_{rev} by 10^2 [89]. And the Al_2O_3 /GaN/AlInN/GaN MOS-HEMTs after irradiation shows gear degradation in DC properties due to the higher amount of carrier scattering occurring underneath ohmic metal degrading metal contact and defect generation near the 2DEG channel which increased the resistance of the channel [307].

In the following part, the analysis will be focus first on the effects on the electrical characteristics of SD and MOS-D, and then on the effects on DC properties of the HEMTs and MOS-HEMTs

a) SD and MOS-D

The IV characteristics of the GaN/AlInN/GaN-based Schottky and MOS-Ds are shown in Figure 6-13. In contrast to the AlGaIn/GaN heterostructure, a decrease of I_{rev} and I_{for} was observed after the proton irradiation in the SDs and the ZrO_2 MOS-Ds. I_{rev} of the SDs decreased by 10 times and I_{rev} of the ZrO_2 MOS-Ds by 10^2 times after irradiation. In the HfO_2 and Al_2O_3 MOS-Ds, I_{rev} and I_{for} increased by 10^2 . Even though, I_{rev} and I_{for} of the Al_2O_3 and HfO_2 MOS-D are 10 times smaller than the ZrO_2 MOS-D, and 10^5 smaller than the SD.

Figure 6-13 IV properties of the GaN/AlInN/GaN-based diodes (a) before and (b) after irradiation

The capacitance voltage characteristics of the devices before and after irradiation are shown in Figure 6-14. In the case of SD, positive V_{th} shift was observed by +0.3 V. In the case of MOS-D, like in AlGaIn/GaN, a positive V_{th} shift was observed, of +0.5 V, +1.5 V and +2.9 V, for HfO₂, Al₂O₃ and ZrO₂ gate dielectrics, respectively. Therefore, the MOS-D with HfO₂ showed the highest irradiation robustness out of the other MOS devices.

Figure 6-14 CV characteristics of the GaN/AlInN/GaN-based diodes (a) before and (b) after irradiation

b) HEMTs and MOS-HEMTs

The IV and transconductance of the GaN/AlInN/GaN-based conventional and MOS-HEMTs before and after irradiation are shown in Figure 6-15.

The DC IV and transconductance of the conventional HEMTs show that the proton irradiation caused great decrease of $I_{D,max}$ and $g_{m,max}$, by 11% ,and 65 %, respectively. In addition, a +0.2 V V_{th} shift was observed in the conventional HEMTs, in good agreement with the C-V characteristics of the SD.

The MOS devices showed a lower decrease of the parameters after irradiation, in comparison to the conventional HEMTs. For instance, the MOS-HEMTs with Al_2O_3 and HfO_2 showed a decrease of $I_{D,max}$ and increase of R_{ON} about 5%, and the decrease of $g_{m,max}$ is about 5% in the Al_2O_3 MOS-HEMTs. However, the ZrO_2 MOS-HEMTs showed 18% decrease of $I_{d,max}$ and 22% increase of R_{ON} .

Figure 6-15 (a) IV and (b) g_m properties of the GaN/AlInN/GaN-based (MOS)HEMTs before and after irradiation

The V_{th} positive shift is due to the change of carrier density, as shown in Figure 6-14 (b). The highest decrease of carrier density was observed in the Al_2O_3 MOS structure, which is about 25%, followed by ZrO_2 MOS-Ds (about 13%). However, the carrier density of the conventional and HfO_2 HEMTs shows up to 30% increase instead, and the V_{th} shift is the smallest, about +0.4 V to 0 V.

From these observations, the smallest output characteristic degradation in GaN/AlInN/GaN HS corresponded to the MOS-HEMTs with HfO_2 , the I_{rev} and I_{for} values are at least 10 times smaller than MOS-D with ZrO_2 and 10^5 smaller than the SD. At the same time, the DC characteristic changes caused by the irradiation is negligible. Therefore, the design of GaN/AlInN/GaN MOS-HEMTs with HfO_2 is the best option for further investigation for harsh irradiative environments.

6.4 Summary

In this chapter, the effects of H^+ and He^+ irradiation on AlInN/GaN conventional and HfO_2 MOS devices were studied. With the same fluence ($1 \times 10^{13} cm^{-2}$ and $1 \times 10^{15} cm^{-2}$), the He^+ irradiation showed

more damage on the devices than the H^+ irradiation. The DC characteristics degradation caused by the irradiation on MOS devices is smaller than on the conventional devices, which was explained by the protecting effects of the dielectric layer. The most damage was caused by $1 \times 10^{15} \text{ cm}^{-2} \text{ He}^+$ irradiation, the devices showed enormous decrease of over 200% in DC characteristics. However, the difference between conventional HEMTs and MOS-HEMTs are negligible. The most interesting irradiation condition, small but different degradation of DC properties on both conventional and MOS-HEMTs, is the one with $1 \times 10^{15} \text{ cm}^{-2} \text{ H}^+$.

Afterwards, the effects of H^+ irradiation with $1 \times 10^{15} \text{ cm}^{-2}$ fluence on the AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN conventional and MOS devices were discussed. Firstly, we discussed the effects of proton irradiation on AlGaIn/GaN, GaN/AlInN/GaN and AlInN/GaN SDs and MOS-Ds, with Al_2O_3 , HfO_2 and ZrO_2 dielectric layers. Results show that the MOS-Ds are less affected by the proton irradiation than the SDs. However, in the case of AlInN/GaN and GaN/AlInN/GaN HS, the ZrO_2 MOS-Ds showed I_{rev} and I_{for} decrease after irradiation. This was explained by the improvement of isolation in the GaN buffer layer and Ni void formation within the interface. Then the DC characteristics change of the HEMTs and MOS-HEMTs after irradiation were studied. For the AlGaIn/GaN and GaN/AlInN/GaN HS, the MOS-HEMTs with HfO_2 and Al_2O_3 showed very small decrease on the $I_{\text{D,max}}$, $g_{\text{m,max}}$ and V_{th} , especially HfO_2 , the change is negligible. For the AlInN/GaN HS, the DC characteristics degradation of MOS-HEMTs with ZrO_2 is negligible, together with the leakage current decrease in the MOS-Ds, it is the best option for further studies under irradiation environments.

Chapter 7 Stability of GaN-based MOS-HEMTs after electrical stress

Electrical reliability of AlGaIn/GaN-based devices for switching or RF power applications is of great interest, especially off-state voltage stress [156]. There are some explanations for this, such as hot-electron induced trap formation [156], [308], [309] and electric-field induced defect formation in association with inverse piezoelectric effect in AlGaIn/GaN [46], [151], [310]. During applications, sometimes the devices have to be kept at on state for a long time, in order to imitate the situation, electrical stress like we have discussed in section 2.5.2. Based on this idea, the electrical stability of the HEMT and MOS-HEMT with HfO₂ after gate and drain electrical stress.

During the study, two kinds of electrical stress were carried out, one is off-state stress with voltage biased on the drain side, similar to those discussed in the literatures[311] and the other is voltage bias on the gate side, such as [309], [312]–[314].

7.1 The effects of gate stress

Long term off-state step stress was that voltage stress is applied to the gate side of the device, V_{GS} is stepped from -7 to -39 V, in -2 V steps; each stress lasts for 1800 s, and gate and drain were grounded. The gate step stress is similar to those reported in the literatures [148], [315], [316]. DC IV and transconductance measurements were conducted right after each stress step. The bias stress protocol is shown in Figure 7-1.

Figure 7-1 Gate stress protocol

7.1.1 HfO₂/GaN/AlGaIn/GaN MOS-HEMTs

Figure 7-2 shows the change of IV curves of the devices and the $I_{D,max}$ and R_{ON} change with gate stress voltage in the device. The changing trend of $I_{D,max}$ and R_{ON} shows that the decrease of the device property starts at about -25 V, and the increase reaches to 100% at -35 V.

Figure 7-2 (a) Change of IV curves with gate stress and (b) I_{DS} and R_{ON} changes during step-stress experiments

The transconductance curves of the devices are shown in Figure 7-3. The change of $g_{m,max}$ with stress voltage are shown in Figure 7-3 (b). Similar to the change of $I_{D,max}$, The $g_{m,max}$ has decreased by 22% after -35 V stress.

Figure 7-3 (a) Change of transconductance curves with gate stress and (b) $g_{m,max}$ changes during step-stress experiments

This voltage could be considered as a critical voltage, from which the device shows critical degradation [157], with decreased $I_{D,max}$ and $g_{m,max}$, as already reported in previous publications [315].

There are several explanations for the existence of critical voltage, one is due to metal diffusion at the gate drain edge of the devices, which has been observed from TEM pictures in many previous discussions [148], [156], [137], [187], [315]. Other cause is the presence of O-Ga or O-Ni bondings during or after the electrical stress under the gate. Chien-Fong Lo *et al.* showed that Pt based gate shows improved critical voltage than the conventional Ni/Au gate [315]. Another relevant issues to be discussed have to do with the properties of the epilayer: one is that there will be a lot of crystallographic defects caused by inverse piezoelectric effect from high vertical electric field, mostly at the drain edge of the gate [148], [151], [153], [158]; the other is hot-electron-induced trap generation [317], [318].

7.2 The effects of drain stress

Long term off-state step stress was that Voltage stress is applied to the drain side of the device, V_{DS} is stepped from 13 to 39 V in 2 V step, while keeping $V_{GS} = -7$ V, the device is stressed for 1800 s at each voltage step. DC IV and transconductance measurements were conducted right after each stress step. Figure 7-2 shows the change in $I_{D,max}$ (drain current at $V_{GS} = 1$ V and $V_{DS} = 7$ V), R_{ON} , $I_{G,OFF}$ (gate current at $V_{GS} = -6$ V and $V_{DS} = 0.15$ V) and $g_{m,max}$ as the stress proceeds. The drain bias stress protocol is shown in Figure 7-4.

Figure 7-4 Drain stress protocol

7.2.1 GaN/AlGaN/GaN conventional HEMTs

The IV and transconductance of the conventional HEMTs during the drain stress are shown in Figure 7-5. The changing trend of the $I_{D,max}$, R_{ON} and $g_{m,max}$ are shown in Figure 7-6. Results show that there is a decrease of 47% for the $I_{D,max}$, 100% increase of R_{ON} , and 50% decrease of $g_{m,max}$ in the conventional

HEMTs, especially the $g_{m,max}$ decreased suddenly at drain gate voltage of 33 V. This voltage could be considered as a critical voltage, from which on, the leakage current increase dramatically, causing devices degradation [157], similar to those have seen from previous publications [46], [151], [158].

Figure 7-5 (a) Change of IV curves with gate stress and (b) Change of IV curves with gate stress

In the conventional HEMTs of this case, diffusions occur among dislocations, accelerated by hot-electrons. With the increase of electrical stress voltage, inverse piezo-electric strain would occur, to further accelerate the electron diffusion in the device, causing an increase of gate leakage current and a decrease of dc electrical properties, as we have observed.

Regarding the gradual decrease of the DC behaviors of the devices, there are two possible explanations: one is due to the crystallographic defects caused by inverse piezoelectric effect from high vertical electric field at the drain edge of the gate [148], [151], [153], [158]; and the other is hot-electron-induced trap generation [317], [318].

Figure 7-6 (a) Change in normalized $I_{D,max}$ and R_{ON} and (b) $g_{m,max}$ Change during step-stress experiments

7.2.2 HfO₂/GaN/AlGa_N/Ga_N MOS-HEMTs

The IV and transconductance curves of the MOS-HEMTs during stress are shown in Figure 7-7. There is a decrease of 30% for the $I_{D,max}$ MOS-HEMTs with KOH cleaning. And the $I_{D,max}$, R_{ON} and $I_{G,OFF}$ of both MOS-HEMTs and the conventional HEMTs are shown in Figure 7-8. There is gradual degradation for the MOS-HEMTs, despite cleaning procedures, while for conventional HEMTs, there is a sudden degradation up to $V_{DG}=33$ V, similar to those decrease of $g_{m,max}$, as explained in the previous part. This voltage is the critical voltage of the conventional HEMTs, from which on the leakage current increase dramatically, causing severe devices degradation [157], similar to those seen from previous publications [46], [151], [158].

Figure 7-7 (a) Change of IV curves with gate stress and (b) Change of IV curves with gate stress

There is no sudden decrease of $g_{m,max}$ or sudden increase of $I_{G,OFF}$ observed in the MOS-HEMTs despite cleaning procedure. This is because the critical voltage of the MOS-HEMTs is higher than the maximum stress voltage we have applied during the experiments, suggesting the improving of critical voltage of MOS-HEMTs using HfO₂ dielectric layer.

Figure 7-8 (a) Change in normalized $I_{D,max}$ (left) and R_{ON} (right) in step-stress experiments for three different stress conditions, (b) Change in the gate leakage current $I_{G,off}$ (gate current at $V_{DS} = 0.15$ V and $V_{GS} = -6$ V) in the experiment

Another issue to discuss is the behaviours of the three kinds of MOS-HEMTs using different cleaning procedures. From the normalized $I_{D,max}$, R_{ON} and $g_{m,max}$ change shown in Figure 7-8, almost no difference in the R_{ON} change was observed. However, the $I_{D,max}$ of the MOS-HEMTs with only organic cleaning showed more decrease than the ones with KOH cleaning. Therefore, the best case for all the electrical properties was the MOS-HEMTs with KOH cleaning.

Based on the observed behaviours, the HfO_2 dielectric in between drain and source could help inhibit the hot-electron and inverse piezo electric caused degradation in the devices.

7.3 Summary

In general, the effects of electrical stress on AlGaN/GaN conventional and MOS-HEMTs with HfO_2 are discussed in this chapter. First, we have analyzed the gate step stress, experiments were done on the MOS-HEMTs with 0.5 M KOH cleaning. Results show that there is gradual decrease of $I_{D,max}$ and $g_{m,max}$, as well as gradual increase of R_{ON} in the devices. Besides, there is a gap in the $g_{m,max}$ after stress of -27 V, which is the critical voltage of the MOS-HEMTs at the gate side. This can be explained in two aspects, one is the properties of the gate and the other is the properties of the heterostructures. For the first one, there might be gate metal diffusion or O-Ga and O-Ni bondings at the gate drain side. For the other aspect, there might be the crystallographic defects due to inverse piezoelectrical properties or hot electron induced traps.

Then, the effects of drain electrical stress on both conventional HEMTs and MOS-HEMTs were discussed. Firstly, the difference of the stress effects between conventional HEMTs and MOS-HEMTs

are compared. Results show that there is critical point of gate drain voltage at about 33 V in the conventional HEMTs, which is not observed in the MOS-HEMTs. Different from the previous discussion before, this critical voltage mostly probably due to the properties of the heterostructure: the crystallographic defects due to inverse piezoelectrical properties or hot electron induced traps. This is not observed in the MOS-HEMTs, implying the improvements of the MOS-HEMTs with HfO_2 dielectric layers.

A short discussion about the comparison among the MOS-HEMTs with different cleaning procedures is given. The MOS-HEMTs with KOH cleaning have shown the best behavior among the three kinds of HEMTs.

Chapter 8 The improvement of thermal and irradiation stability of Gd_2O_3 dielectric on GaN-based MOS-HEMTs

According to the discussion from the previous chapters, the MOS-HEMTs with HfO_2 in between source and drain shows the best performance compared with conventional HEMTs and MOS-HEMTs with Al_2O_3 and ZrO_2 .

In order to further study the MOS devices with high-k dielectrics, the use a relatively new material, Gd_2O_3 , was investigated. Gd_2O_3 on GaN have been investigated to be able to achieve low leakage current densities and low dispersion [58], hence arising as a promising candidate for gate dielectric on GaN-based MOS-HEMTs. In fact, Gd_2O_3 thin layers, either deposited by molecular beam epitaxy (MBE) [58] or electron-beam evaporation [59] to prevent surface damage on GaN or AlGaIn/GaN heterostructures, were investigated. However, further research is still needed to study the stability of the AlGaIn/GaN MOS-HEMTs using Gd_2O_3 as gate insulator. Moreover, in this case, the Gd_2O_3 gate dielectric was deposited under the gate metal, in order to analyze the single effects of the gate dielectric.

In this chapter, the behaviors of the MOS devices using Gd_2O_3 as gate dielectric just under the gate metal will be discussed at RT and harsh environments, including elevated temperatures and proton irradiation environment. Firstly, the properties of AlGaIn/GaN conventional devices and MOS devices with Gd_2O_3 layer are compared at RT. Then the effects of different thermal stresses are discussed. On one hand, the effects of a short thermal annealing, and on the other hand, the effects of step thermal test, and the effects of a long term storage test. Besides the thermal stability, the irradiation hardness of the conventional and MOS devices with Gd_2O_3 are also compared.

In these studies, both SDs/MOS-Ds and HEMT/MOS-HEMTs have been used. The diodes are squares with length of 100 μm , and the HEMTs geometry is $L_G = 1.2 \mu\text{m}$, $W_G = 50 \mu\text{m}$, and $L_{SD} = 5 \mu\text{m}$, with equal gate-drain and gate-source distances.

8.1 Effects of Gd_2O_3 on AlGaIn/GaN heterostructures

8.1.1 Schottky diodes and MOS-diodes

Firstly, the properties of the diodes with and without the Gd_2O_3 dielectric layer are analyzed at RT. I-V characteristics of the Schottky and MOS-Ds are shown in Figure 8-1. MOS-Ds showed about 10^4 lower reverse leakage current (I_{rev}) than the Schottky diodes. The ideality factor η obtained from the I-V and C-V characterizations was 3.5, and the barrier height was calculated to be 0.85 eV for the Schottky diodes, close to the previous calculated values [324].

Figure 8-1 I-V properties of Schottky Diodes and Gd₂O₃ based MOS-Ds

Afterwards, C-V characteristics of the diodes were done accordingly, shown in Figure 8-2. The relative dielectric constant of the Gd₂O₃ layer was estimated ($\epsilon_r = 11 \sim 13$). This value is similar to those reported in the literature [325]. From the C-V curves, we have observed capacitance decrease, negative threshold voltage (V_{th}) shift of about -2 V compared with Schottky diodes, the hysteresis observed from the curves are about 0.33 V and there is mid-gap to flatband stretch-out. The capacitance decreases and negative shift of V_{th} is due to the introduction of a gate insulator between gate metal and the heterostructure. The hysteresis and mid-gap-to-flatband stretch-out are indications of possible border charges in the dielectric close to Gd₂O₃/AlGaIn interface and interface charges in oxide and oxide-heterostructure interface [59].

Then quantitative analysis of the trap densities can be generated. From hysteresis, we know that there are slow interface traps in the oxide, the value can be estimated to be $4.7 \times 10^{11} \text{ cm}^{-2}$, the maximum interface state density was obtained to be $3.1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

Figure 8-2 C-V properties of GaN/AlGaIn/GaN (a) SDs and (b) Gd₂O₃ based MOS-Ds

8.1.2 HEMTs and MOS-HEMTs

The DC-IV properties of the HMETs and MOS-HEMTs are going to be discussed. The curves were plotted in Figure 8-3. The DC output characteristics of the AlGaIn/GaN conventional and MOS-HEMTs show that there is a 15% increase in maximum drain current ($I_{D,max}$) in MOS-HEMTs. There is no significant difference observed in ON-resistance ($R_{on}= 6.5\pm0.9 \ \Omega\cdot\text{mm}$) between the two kinds of devices.

Figure 8-3 I_D - V_{DS} of AlGaIn/GaN and Gd_2O_3 MOS-HEMTs at room temperature

The transconductance curves are shown in Figure 8-4, where we can observe that there is no big change in maximum transconductance ($g_{m,max}= 155\pm5 \text{ mS/mm}$); however, there is a negative shift of threshold voltage, the shift (ΔV_{th}) is about -2.5 V, in accordance with those observed in the diodes, indicating the positive charges either in the interface or in the bulk.

Figure 8-4 g_m - V_{GS} of AlGaIn/GaN and Gd_2O_3 MOS-HEMTs at room temperature

The transfer properties of the devices are shown in Figure 8-5, the off-state current at $V_{GS} = -8$ V ($I_{D, OFF}$) of MOS-HEMTs was 3 nA/mm at $V_{DS} = 10$ V. It is about 10^3 lower than that of the conventional HEMTs.

Figure 8-5 I_D - V_{GS} of AlGaIn/GaN and Gd_2O_3 MOS-HEMTs at (a) $V_D = 0.1$ V and (b) 9.9 V

In order to analyze the trapping phenomenon of the devices, pulse measurements were carried out on the devices, and the curves are plotted in Figure 8-6. Gate lag ratio and drain lag ratio increased by 30% and 40% in the MOS-HEMTs, respectively, which means there is less trapping effects in the MOS-HEMTs with Gd_2O_3 dielectric. The improved GLR means there is less surface traps, and the increased DLR shows that there are less traps in the AlGaIn/GaN interface or in the channel.

Figure 8-6 Pulsed IV curves of (a) AlGaIn/GaN and (b) Gd_2O_3 AlGaIn/GaN MOS-HEMTs at RT

In general, from DC measurement results of the devices, we can see that the reverse and forward leakage currents of the MOS-Ds with Gd_2O_3 dielectric layer have decreased by 10^4 respect to those of

the Schottky diodes. Also, the Gd_2O_3 MOS-HEMTs have off-state current 10^3 times smaller than the conventional HEMTs. These observations prove that the Gd_2O_3 dielectric layer helped suppressed the OFF-state drain currents, and there is no significant decrease in R_{ON} or $g_{m,\text{max}}$ caused by the Gd_2O_3 dielectric, even though there is a decrease of $I_{D,\text{max}}$. From the pulsed measurement results, we have observed that there are less trapping effects in the MOS devices. This further proves that Gd_2O_3 based MOS-HEMTs are suitable for high frequency applications. Due to the well performance of the devices, thermal tests and irradiation tests were performed on the devices to check the effects of the Gd_2O_3 on the thermal stability and irradiation hardness of the devices.

8.2 The effects of short thermal test

Usually, short thermal annealing could improve the devices properties by reducing the trap density, recovering the damages induced during dielectric deposition, and improve the current density and transconductance [73], [143], [196]. Now we can discuss the properties of the devices after short thermal annealing test. The annealing condition in the test takes place at 500°C , and it takes only 5 minutes.

8.2.1 Schottky diodes and MOS diodes

I-V characteristics of the Schottky and MOS-Ds after the thermal test are shown in Figure 8-7. No significant change was observed in any of the devices, highlighting the thermal robustness of the Gd_2O_3 dielectric. I_{rev} in the reverse biased region (-6 to -2 V) increased by 10 times in the MOS-Ds.

Figure 8-7 I-V properties of SDs and Gd_2O_3 based MOS-Ds before and after STA

In order to get the cause of this increase, we have tried to fit the gate current with different electron transport mechanisms, as shown in Figure 8-8. The parameters extracted from the PFE and SE fitting were close to theoretical values, which made PFE and SE the dominant transport mechanisms. In contrast, the Schottky diodes did not show significant differences before and after the short thermal test. Therefore, the increase of reverse leakage current in the MOS-Ds after the short thermal annealing is due to the change of the dominant leakage current mechanisms in this kind of devices.

Figure 8-8 (a) PFE and (b) TAT fitting plots of the MOS-Ds before and after short thermal test

From the C-V characteristics of the MOS-Ds at room temperature shown in Figure 8-9, we have calculated the dielectric constant of the Gd₂O₃ layer to be $\epsilon_r = 11$ [325], and there is no change after the short thermal test. A positive shift in the C-V curves of the MOS-Ds was observed after short thermal test. This can be attributed to the increase of negative fixed charges in the oxide or the decrease of positive fixed charges in the oxide [59], [100]. A small hysteresis was observed, which shows that the charges in the oxide near the oxide/semiconductor interface are reduced by the thermal annealing.

Figure 8-9 C-V properties of (a) SDs and (b) Gd_2O_3 based MOS-Ds

The midgap-to-flatband stretch out was similar to the situation observed from the CV curves of the as-fabricated devices, and the interface state density calculated using the same method was $1.3 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. It was smaller than the value of the as-fabricated device, showing the effects of thermal annealing on the improvement of the MOS-device's performance.

Figure 8-10 Schematic illustration of D_{it} energy range corresponding to measurement frequency

8.2.2 HEMTs and MOS-HEMTs

The I-V curves of the MOS-HEMTs are shown in Figure 8-11. In the curves we can see that the saturation region at $V_{GS}=1 \text{ V}$ were flatter than those of the conventional HEMTs, suggesting lower self-heating effects in the MOS-HEMTs [140], [326]. $I_{D,max}$ increased 3% in HEMTs and decreased 6% in MOS-HEMTs, R_{on} and $I_{G,leak}$ stay stable in both MOS-HEMTs and HEMTs.

Figure 8-11 DC-IV characteristics comparison between the HEMTs and the MOS-HEMTs

$I_{D,OFF}$ of the two kinds of HEMTs are similar after the short thermal test, both close to 1×10^{-8} A/mm, and $I_{D,OFF}$ of the conventional HEMTs decreased by two orders of magnitude; showing the beneficial effects of short thermal annealing on HEMTs.

Figure 8-12 I_D - V_{GS} at $V_{DS} = 10$ V of HEMTs and MOS-HEMTs before and after STA.

V_{th} was obtained from the intercept of the linear extrapolation of the g_m - V_G characteristics measured at $V_{DS} = 0.1$ V. V_{th} of the MOS-HEMTs shifted positively to -5.5 V, in accordance with the C-V results.

Figure 8-13 Transfer characteristics comparison between the HEMTs and the MOS-HEMTs

After the thermal test, the pulse IV curves of the devices and the DLR and GLR achieved from the curves are shown in Figure 8-14 and Figure 8-15. There is almost no change in the gate lag of the MOS-HEMTs in contrast to HEMTs, which has an increase of 54%. The drain lag increased similarly on both kind of devices and a drop in the pulse current is observed. This effect is likely related to the presence of GaN-buffer interface traps after the thermal test.

Figure 8-14 pulsed current for $(V_{DS,Q}, V_{GS,Q}) = (15 \text{ V}, -8 \text{ V})$ before and after STA.

Figure 8-15 (a) GLR and (b) DLR of HEMTs and MOS-HEMTs from pulse measurements

Therefore, the short thermal annealing process is beneficial for electrical behaviors of both conventional and MOS-HEMTs. Due to this, the properties of the devices after short thermal annealing were taken as the reference in the following discussion.

8.3 The effects of the thermal cycling test

In the thermal stability studies, high-temperature operation of AlGaIn/GaN HEMTs on Si has been evaluated previously by several groups [140], [231], [319]. However, there is very little work on the thermal stability of insulated-gate AlGaIn/GaN structures on Si substrates for high-temperature applications, in particular those using Gd_2O_3 as gate insulator.

8.3.1 Schottky diodes and MOS-Ds

Schottky and MOS-Ds were subjected to a thermal cycle test from RT to 425°C with increment of 100°C . The I-V characteristics of the devices presented in Figure 8-16 showed that the I_{rev} increased gradually with temperature in both kinds of devices. I_{rev} of MOS-Ds at 425°C gave a value at least 10 times lower than that of the Schottky-diodes at RT, demonstrating the effectiveness of the Gd_2O_3 gate dielectric in the suppression of gate leakage current at high temperature. In addition, I_{rev} recovered to the initial values at RT, showing that the increase of I_{rev} caused by high temperature is not permanent on both kinds of diodes.

Figure 8-16 I-V-T characteristics of (a) SDs and (b) MOS-Ds during the thermal cycle test

The C-V characteristics in Figure 8-17 showed that there was no hysteresis in the MOS-Ds during the thermal cycle test; therefore, fewer traps in the oxide near the semiconductor interface are activated by temperature compared with the as fabricated devices. Also, there was no significant change in the midgap-to-flatband stretchout after the thermal cycle in the MOS-didoes, showing that the interface traps density in the MOS-Ds does not increase at high temperature.

Figure 8-17 C-V-T characteristics of (a) SDs and (b) MOS-Ds during the thermal cycle test

However, when the devices were heated up to 225°C, V_{th} in MOS-Ds shifted negatively by ~ 0.5 V. The cause of the negative shift is the thermal activation of charges in the devices. By fitting the current density curve with the theoretical curves of different electron transport mechanisms, one of the dominant electron transport mechanisms in the MOS-Ds was trap assisted tunneling (TAT), and the energy level of the traps is in the range of 0.24 eV and 0.32 eV, which is most probably caused by shallow traps in AlGaIn/GaN interface [327]. When the temperature is higher than 225°C, V_{th} in MOS-Ds shifted positively to -4.6 V at 425°C, which is close to the initial V_{th} value. This positive shift could

be explained by oxygen related complexes such as $2(O_N)$ [154]. The activation energy could be extracted from the fitting curve of the gate current with theoretical TAT curves, and it is calculated to be 0.42 eV. With increasing temperature, the role of TAT at the trap energy of 0.24 eV and 0.32 eV became less significant.

8.3.2 HEMTs and MOS-HEMTs

At RT after the thermal cycle test, V_{th} becomes stable at -4.6 V. Moreover, no major changes were observed in the C-V characteristics of the Schottky diodes during the thermal cycle test. This shows that the thermally activated traps during the thermal cycle have no noteworthy effects on the electrical behavior of the devices.

Figure 8-18 I_D - V_{DS} -T curves of the (a) HEMTs and (b) MOS-HEMTs at thermal cycle

The output characteristics of the devices (I_D - V_{DS} -T) at $V_{GS} = 0$ V (Figure 8-18) show that $I_{D,max}$ decreased with increasing temperature in a rate that was similar between the two kinds of devices. $I_{D,max}$ of MOS-HEMTs at 425°C was ~40% of the value at RT. It is less affected by high temperature compared with the previous studies, where $I_{D,max}$ at 425°C shows ~30% of the value at RT using $Al_2O_3/AlGaIn/GaN$ MOS-HFETs [35], and $I_{D,max}$ decreases by ~40% at 200°C in $SiO_2/AlGaIn/GaN$ grown on sapphire [298].

The transfer characteristics of the devices at $V_{DS} = 10$ V during the thermal cycle test (I_D - V_{GS} -T), displayed in Figure 8-19, show that $I_{D,OFF}$ of the conventional HEMTs increased by 4 orders of magnitude (from 80 nA/mm at RT to 19 μ A/mm at 225°C, and to 0.2 mA/mm at 425°C), and $I_{D,OFF}$ of the MOS-HEMTs gave no significant change.

Figure 8-19 I_D - V_{GS} - T curves of the (a) HEMTs and (b) MOS-HEMTs

In addition, the transconductance-gate voltage curves are shown in Figure 8-20. At 425°C, $g_{m,max}$ decreased by ~53% in HEMTs and ~45% in MOS-HEMTs on average, which is less than the drop observed in previous studies, where $g_{m,max}$ decreases by ~70% at 420°C in $Al_2O_3/AlGaIn/GaN$ MOS-HFETs [35]. These results show that the MOS-HEMTs using Gd_2O_3 dielectric that we have fabricated in this study show better thermal behavior compared with previous studies using Al_2O_3 or SiO_2 gate dielectrics.

Figure 8-20 g_m - V_{GS} - T curves of the (a) HEMTs and (b) MOS-HEMTs

Threshold voltage V_{th} extracted from the g_m - V_G curves are shown in Figure 8-21. V_{th} values shifted from ~-6 V up to ~-4 V with the increasing temperature, and stabilized at ~-5 V after the cycle, in agreement with the C-V characteristics. According to previous discussions, the shift is possibly caused by surface hopping, and the activation energy can be calculated to be 0.21 eV, similar to what we have observed previously [328], [329].

Figure 8-21 V_{th} change with temperatures

The pulsed measurements were taken place at room temperature after the thermal cycle test, the curves are show in Figure 8-22. The GLR of the MOS-HEMTs are about 67% better than those of conventional HEMTs, and the DLR of the MOS-HEMTs is close to 1.

Figure 8-22 Pulsed IV curves of (a) HEMTs and (b) MOS-HEMTs after thermal cycle

In summary, the DC IV performances of the devices decrease with increasing temperature in both conventional HEMTs and MOS-HEMTs. However, with the protection of dielectric layer under the gate, the MOS-HEMTs were less influenced by temperature. The trapping effects on the devices surface or in the channel interface was depressed due to the Gd_2O_3 dielectric layer.

8.4 The effects of long thermal test

The long term thermal test was conducted to check the life time and stability of the heterostructure and dielectrics after a period of high temperature storage.

8.4.1 Schottky diodes and MOS-Ds

The I-V characteristics of the Schottky and MOS-Ds during the long thermal test at 500 °C are shown in Figure 8-23. I_{rev} increased simultaneously in both kinds of devices after six days. I_{rev} of MOS-Ds was three orders of magnitude lower than the Schottky diodes after eight days. The forward leakage current of Schottky diodes increased by 10^3 , from 0.1 A/cm² to 200 A/cm² after one day, and this increase was irreversible during this process. Therefore, a permanent degradation happened to the Schottky diodes during the long thermal test in contrast to the MOS-Ds.

Figure 8-23 I-V characteristics of the (a) SDs and (b) MOS-Ds during long thermal test

C-V characteristics were taken place, and the curves are shown in Figure 8-24. No significant change was observed in the MOS-Ds during the long thermal test. This tells us that V_{th} of the MOS-Ds are stabilized after the previous tests. Schottky diodes' capacitance decreased to the value of the MOS-Ds after about five days' storage at 500 °C. This could be related to the irreversible degradation caused by the long time high temperature storage or the AlGaIn/GaN strain relaxation caused by gate metal diffusion into the AlGaIn layer during the high temperature storage [330], [331].

Figure 8-24 C-V characteristics of the (a) SDs and (b) MOS-Ds during long thermal test

8.4.2 HEMTs and MOS-HEMTs

I_D - V_{GS} characteristics of the HEMTs and MOS-HEMTs at $V_{DS} = 10$ V during the long thermal test are shown in Figure 8-25. $I_{D,OFF}$ of HEMTs increased by four orders of magnitude after one day at 500°C , leading to a permanent degradation, as observed in the Schottky diodes. In contrast, $I_{D,OFF}$ of MOS-HEMTs had less than one order of magnitude increase after the long thermal tests. The ON/OFF current ratio of the MOS-HEMTs was about 10^8 after the long thermal test, indicating an excellent charge modulation effect and good thermal stability. This result is as good as those achieved using MoS_2 transistors using $\text{Pb}(\text{Zr}_{0.52}\text{Ti}_{0.48})\text{O}_3$ as dielectric [332].

Figure 8-25 I_{DS} - V_{GS} characteristics at $V_{GS} = 10$ V of (a) HEMTs and (b) MOS-HEMTs during the long thermal test.

After one day long thermal test, the HEMTs showed a 20% decrease in $I_{D,max}$, a 77% increase in R_{on} , and a 75% decrease in $g_{m,max}$. On the other hand, the MOS-HEMTs had stable $I_{D,max}$ (~ 0.6 A/mm), R_{on}

($\sim 6.5 \Omega \cdot \text{mm}$), $g_{m,\text{max}}$ ($\sim 95 \text{ mS/mm}$) and V_{th} ($\sim -5 \text{ V}$) during the long thermal test. Furthermore, $g_{m,\text{max}}$ in the MOS-HEMTs was about 40% higher than that of the conventional HEMTs. The improved DC behaviors prove that our fabricated Gd_2O_3 MOS-HEMTs are suitable for high temperature applications.

Figure 8-26 g_m - V_{GS} curves of (a) HEMTs and (b) MOS-HEMTs at $V_{\text{DS}} = 0.1 \text{ V}$ during the long thermal test

The gate lag ratio and drain lag ratio changes of HEMTs and MOS-HEMTs are shown in Figure 8-27. The GLR of the HEMTs decreased by 60% after one day during long thermal test respect to the as-fabricated devices, which can be related to the increase of surface states or traps in the area between gate and drain that behave like a virtual gate [282]. A similar behaviour was expected in the MOS-HEMTs because there was no passivation in between gate and drain. However, the reduction of gate lag ratio of MOS-HEMTs was less than 20%, suggesting that the use of the gate dielectric would diminish the virtual gate effects by means of physical separation of electrons between the gate metal contact and the surface states near the gate. The drain lag ratio values did not change significantly with thermal tests, and followed a similar trend in both kinds of devices, because the drain lag are caused by existence of trapping effects in the buffer.

Figure 8-27 (a)GLR and (b)DLR of HEMTs and MOS-HEMTs from pulse measurements during before and after the short, cycle and one-day-long test

In summary, the AlGaIn/GaN MOS-HEMTs with Gd_2O_3 dielectric layer had a low gate leakage current and stable DC behavior during the long thermal test. In contrast, the conventional HEMTs showed permanent degradation after a one-day thermal storage at 500°C : increased gate leakage current and on-resistance, reduced maximum drain current, maximum transconductance and gate lag ratio. In addition, we also concluded that a soft thermal annealing process enhanced the thermal stability of the MOS-HEMTs with Gd_2O_3 dielectric. Therefore, MOS-HEMTs using Gd_2O_3 dielectric with improved time tolerance and stability are well qualified candidates for high temperature applications.

8.5 Comparison of the irradiation effects on conventional and MOS AlGaIn/GaN devices

In the field of irradiation hardness study of the devices, the irradiation effects on AlGaIn/GaN-based HEMTs and MOS-HEMTs (using Al_2O_3 [78], NbAlO [80], SiO_2 [320], MgO or Sc_2O_3 [79]) have been explored using different energies and fluences, experimentally [6, 7] and by simulation [77], [173], [175]. For instance, the Al_2O_3 /AlGaIn/GaN MOS-HEMTs showed over 50% decrease in maximum drain current after $5 \times 10^{15}\text{ cm}^{-2}$ fluence irradiation with 5 MeV protons [78]. NbAlO AlGaIn/GaN Metal Insulator Semiconductor (MIS) HEMTs with Si_3N_4 passivation showed a decrease in DC-IV properties after 3 MeV proton irradiation with $1 \times 10^{15}\text{ cm}^{-2}$ fluence [80]. However, the degradation mechanisms of the devices after irradiation are still unclear in many cases. Therefore, the effects of proton irradiation on the AlGaIn/GaN HEMTs and Gd_2O_3 AlGaIn/GaN MOS-HEMTs were studied and compared.

In this part, we investigated the effects of proton irradiation with $1 \times 10^{13} \text{ cm}^{-2}$ and $1 \times 10^{15} \text{ cm}^{-2}$ on AlGaN/GaN conventional and AlGaN/GaN MOS devices with Gd_2O_3 as the gate dielectric. In these studies, the proton energy was 2 MeV.

8.5.1 Schottky diodes and MOS-Ds

Firstly, we are focusing on the properties of the diodes with and without the Gd_2O_3 dielectric layer. For the diodes, I-V characteristics of the AlGaN/GaN Schottky and Gd_2O_3 based MOS-Ds, before and after proton irradiation, are plotted in Figure 8-28. Results show that after the irradiation, I_{rev} increased in both Schottky diodes and MOS-Ds. However, I_{rev} of the MOS-Ds was 10^3 lower than that of the Schottky diodes after irradiation. Similar increases in I_{rev} have been observed in conventional HEMTs after irradiation with proton of 5 MeV and $2 \times 10^{14} \text{ cm}^{-2}$ [75].

Figure 8-28 I-V properties of SDs and Gd_2O_3 based MOS-Ds before and after irradiation

The capacitance-voltage characteristics of the Schottky and MOS-Ds are shown in Figure 8-29. Both Schottky and MOS-Ds showed a positive V_{th} shift after irradiation: from -4.2 V to -3.7 V in Schottky diodes, and from -5.5 V to -5.0 V in MOS-Ds. This shift could be related to the creation of acceptor type defects in the Gd_2O_3 /heterostructure interface or in the AlGaN/GaN channel. These defects are, most likely, N vacancies [173] and Ga-N divacancies [307], [333], [334] and Ga vacancies [76]. The n_s and μ measured decreased after irradiation for all the devices. However, the decrease of n_s and μ in the MOS-HEMTs is smaller than that of the conventional HEMTs.

Figure 8-29 C-V properties of (a) SDs and (b) Gd_2O_3 based MOS-Ds before and after irradiation

8.5.2 HEMTs and MOS-HEMTs

DC I-V characteristics of the conventional and MOS-HEMTs before and after proton irradiation are shown in Figure 8-30. For the conventional HEMTs, $I_{D,\max}$ and R_{ON} decreased and increased by 30%, respectively, after irradiation. On the contrary, for the MOS-HEMTs, $I_{D,\max}$ decreased only by 15% and R_{ON} did not change significantly by irradiation.

Figure 8-30 DC-IV characteristics comparison between the HEMTs and the MOS-HEMTs

The cause of $I_{D,\max}$ reduction and R_{ON} increase is related to the decrease of sheet carrier density and electron mobility in the channel [25, 31, 32]. During transconductance measurements, the Schottky gate HEMTs showed a 29% decrease of the peak transconductance ($g_{m,\max}$), and the MOS-HEMTs showed only a 10% reduction. Positive V_{th} shift was observed in the conventional and MOS-HEMT, as

those observed in the MOS-Ds, with a similar tendency as MIS-HEMTs using NbAlO after irradiation [80].

Figure 8-31 g_m - V_G of HEMTs and MOS-HEMTs before and after irradiation.

V_{th} was obtained from the intercept of the linear extrapolation of the g_m - V_G characteristics measured at $V_{DS} = 0.1$ V. V_{th} of the MOS-HEMTs shifted positively to -5.5 V, in accordance with the C-V results.

Figure 8-32 I_D - V_{GS} comparison between the (a) conventional HEMTs and (b) MOS-HEMTs

The off state drain current (I_{OFF}) are shown in Figure 8-32, I_{OFF} increased after irradiation in both kinds of HEMTs, but the increase in the MOS gate HEMTs is about two orders of magnitude smaller, than that of the Schottky gate HEMTs. Therefore, the on/off current ratio in the MOS-HEMTs is 10^2 higher than in conventional HEMTs, which makes Gd_2O_3 dielectric layer also very attractive for switching applications under proton irradiation environment.

Figure 8-33 shows that the gate and drain lag ratio decreased over 13% in conventional HEMTs, and about 6% in MOS-HEMTs after irradiation, proving the existence of irradiation caused defects in the devices. However, the MOS-HEMTs showed 28% higher gate lag ratio and 18% higher drain lag ratio than the conventional HEMTs, showing that the Gd_2O_3 dielectric under the gate is able to diminish the effects of irradiation on the heterostructure. It works as an irradiation-hardening mechanism, partially protecting the HEMTs from crushing down during proton irradiation.

Figure 8-33 (a) Gate and (b) Drain lag ratio of HEMTs and MOS-HEMTs from pulse measurements

RF measurements were performed on devices after irradiation. f_T and $f_{\max}$ can be derived from the hybrid parameter (H_{21}) and Unilateral Gain (U), when they equal to 0, as shown in Figure 8-34. Results show that the MOS-HEMTs after irradiation has $f_{\max}$ twice as high as that of conventional HEMTs, and f_T three times, showing regardless of the RF behaviors of the devices before irradiation, MOS-HEMTs have better RF properties than conventional HEMTs after proton irradiation.

Figure 8-34 H_{21} and U curves of the conventional and MOS-HEMTs after irradiation

In order to gain further insight on the degradation mechanisms of the devices after irradiation, STEM measurements in the gate region before and after irradiation were compared between Schottky gate and MOS-HEMTs.

In the case of conventional HEMTs, a tilt of the gate edge and voids under the gate were observed after irradiation, as shown in Figure 8-35(c), in contrast to the device before irradiation in Figure 8-35(a). The origin of these voids is likely the diffusion of Ni into Au in the Ni/Au gate metal via defect migration mechanisms such as vacancy exchange or Frenkel pair formation/recombination. In the MOS-HEMTs, neither the gate edge tilt nor the irradiation induced Ni voids were observed (Figure 8-35(d)), showing that the use of the Gd_2O_3 gate dielectric is effective to mitigate the detrimental damage of the gate stack in the GaN-based HEMTs.

Figure 8-35 STEM cross-section images before and after irradiation of the Ni/Au gates on the (a)(c) conventional HEMTs and (b)(d) Gd_2O_3 -AlGaIn/GaN MOS-HEMTs.

Defects are induced through ion-electron collision to the devices during the proton irradiation. On one hand, the collisions cause electrons generation and recombination in the heterostructure, producing vacancies and defects in the device. These vacancies and defects would lead to sheet carrier

density and carrier mobility decrease, and result in a positive shift in V_{TH} and a decrease in current density [26, 29, 33]. On the other hand, during the collision of protons and electrons, heat would be generated in the heterostructure, which would be partial cause of the diffusion between the metals [322].

8.6 Summary

In this part, we were discussing the effects of Gd_2O_3 on the AlGaIn/GaN-based devices, including diodes and HEMTs. The results show that the I_{rev} and I_{for} has decreased by about 10^4 , and the leakage current of the MOS-HEMTs has decreased by 10^3 times, the on/off ratio of MOS-HEMTs has increased accordingly. There is also slight decrease of $I_{D,max}$, $g_{m,max}$ and increase of R_{ON} , but this is due to the increase of the gate contact and channel distance.

The thermal stability of the devices during a short thermal annealing, step thermal cycle process and long term thermal process, have been studied. The Gd_2O_3 MOS-HEMTs had a low gate leakage current and stable DC behaviour during the long thermal test. In contrast, the conventional HEMTs showed permanent degradation after a one-day thermal storage at $500^\circ C$: increased gate leakage current and on-resistance, reduced maximum drain current, maximum transconductance and gate lag ratio. In addition, we also concluded that a soft thermal annealing process enhanced the thermal stability of the MOS-HEMTs with Gd_2O_3 dielectric. Therefore, MOS-HEMTs using Gd_2O_3 dielectric with improved time tolerance and stability are well qualified candidates for high temperature applications. For all the conventional devices. Also, results during the thermal cycle tests have shown that the MOS-HEMTs were less influenced by temperature due to the protection of dielectric layer under the gate, and the trapping effects on the devices surface or in the channel interface was depressed due to the Gd_2O_3 dielectric layer.

Chapter 9 Conclusions and future work

In this chapter, the main conclusions of the thesis will be shown, highlighting the main contributions of the author. Then, a discussion of the possible future work will be presented.

9.1 Conclusions

Contribution to the fabrication processing improvements of devices isolation

In this work, the devices isolation was improved by optimizing mesa etching process, using ICP-RIE. The plasma composition was adjusted during the process. Results show that the composition of Cl_2/BCl_3 : 10:1 could give the best results with smooth morphology and smallest leakage current.

Contribution to the comparison of dielectrics on GaN HS

Three kinds of gate dielectrics were used in the fabrication of MOS-HEMTs on three kinds of HS: $\text{Al}_2\text{O}_3/\text{HfO}_2/\text{ZrO}_2$ on AlGaIn/GaN, AlInN/GaN and GaN/AlInN/GaN HS. The IV and CV characteristics of the diodes showed that the AlGaIn/GaN had smaller leakage current than AlInN/GaN and GaN/AlInN/GaN HS, and AlInN/GaN HEMTs showed the highest $I_{D,\text{max}}$ and $g_{m,\text{max}}$ values among the three kinds of devices. Using the dielectric layer, the leakage current and the off-state current of the devices were decreased effectively by at least three orders of magnitude. From this study, it is concluded that HfO_2 is the most effective dielectric layer in decreasing leakage current and trapping phenomena on all three kinds of HS.

Optimization of cleaning procedure before dielectric deposition

Based on the results that were achieved, the performance of the MOS-HEMTs was further improved using a pre-cleaning using KOH solution. Results show that C related defects are removed from the surface, which led to less trapping effects and smaller current collapse. Besides, the thermal stability of the MOS-HEMTs was improved with pre deposition cleaning.

Thermal stability tests of the devices

After a step thermal test, it was shown that the AlInN/GaN HEMTs were more sensitive to temperature change than AlGaIn/GaN HEMTs. AlInN/GaN MOS HEMTs with HfO_2 gate dielectric layer were thermally more stable than the AlInN/GaN HEMTs. The trapping centers in the devices were analysed. The most active trapping center in the AlGaIn/GaN and AlInN/GaN HS is O complex (O_N) and O vacancy (V^-).

Device stability tests after irradiation

HfO₂ has proven to be effective in reducing the irradiation damage caused by H⁺ and He⁺ irradiation on the AlInN/GaN HEMTs by performing as a buffering layer on the devices. Then the H⁺ irradiation on MOS HEMTs on AlGaN/GaN, AlInN/GaN and GaN/AlInN/GaN HS was studied. HfO₂ and Al₂O₃ was proven to be effectively in protecting the devices with negligible DC characteristic decrease on AlGaN/GaN and GaN/AlGaN/GaN HS, and ZrO₂ on the AlInN/GaN HS after irradiation can reduce the leakage current without damaging the DC properties of the MOS-HEMTs.

Device stability tests after electrical stress

The AlGaN/GaN MOS-HEMTs with HfO₂ has proven to be effective in improving the critical voltage compared with the HEMTs. The critical gate drain voltage was estimated to be 33 V in the AlGaN/GaN HEMTs, due to the inverse-piezoelectrical effects. However, for the MOS-HETMs with 0.5 M KOH cleaning, the critical voltage was improved to a value beyond measurement range.

Device stability with Gd₂O₃ dielectric

After studying the commonly used high-k dielectrics, we have tried a new kind of dielectric material: Gd₂O₃. In this work, the results of AlGaN/GaN MOS-HETMs with Gd₂O₃ show that the Gd₂O₃ help decreased the leakage current by over 10⁴, and it showed stable DC behavior during a LONG thermal test, compared with the permanent degradation observed in the conventional HEMTs after a one-day thermal storage at 500°C. The irradiation effects on the HEMTs and MOS HEMTs have shown that Gd₂O₃ gate dielectric eases the electrical degradation by proton irradiation. Moreover, Gd₂O₃ layer under the gate metallization helps to avoid the tilt of the gate edge and voids under the gate. These results show that the use of the Gd₂O₃ gate dielectric is effective to mitigate the damage to the gate stack in the GaN based HEMTs, and open the possibility of developing Gd₂O₃ based MOS-HEMT to enhance the device robustness for high radiative environment applications.

9.2 Future work

Some promising experiments could be further studied taking into account the results and problems experienced during the work:

Chemical cleaning optimization before dielectric deposition

During the work, we have studied the effects of chemical cleaning using KOH (0.5 M) on the MOS devices, however, there are several study using BOE, or HCl solution to improve the dielectric properties. The effects of surface cleaning using solutions with different pH values could have different effects on the HS, which might lead to better results.

Optimization of STA temperature

During the study, STA has proven to be helpful in improving device properties, however, we did not optimize the annealing temperature during the study. More work should be done on the optimization of the STA temperature to get the exact temperature which the STA should take place. Also, simulations of devices behaviors with temperature could be done at the same time.

Further study of device stability during long thermal test

During this thesis, we have compared the thermal stability after a long thermal test of the AlGaIn/GaN HEMTs and MOS-HEMTs with Gd_2O_3 , however, the thermal stability of the HfO_2 MOS-HEMTs, especially those on AlGaIn/GaN HS could be studied as well.

Further study on device stability under irradiation

During the study, we have studied the irradiation using H^+ and He^+ . However, there are all kinds of ions in the atmosphere. We could study the effects of irradiation using β particles, ^{60}Co , γ rays and so on.

Another study is the *in situ* characterization while irradiating, which is closer to the real atmosphere, where the devices should be operating in the irradiation environments.

Optimization of gate metal on the MOS-HEMTs

During the work, we have been using the same kind of gate metal for both conventional devices and MOS devices regardless of dielectric layer. However, the effects of dielectric layers with difference kinds of Schottky contact are different. So it would be interesting to improve the Schottky metal contact in the study.

Comparison of the effects of dielectrics under the gate and in between source and drain at RT and after different stress test

During the study, in some cases (Al_2O_3 , HfO_2 and ZrO_2), the dielectrics were deposited in between source and drain; in some cases (Gd_2O_3), the dielectric was deposited under gate only. We studied the devices characteristics at RT and after difference stress conditions, however, there is no direct comparison among the two kinds of devices. However, it is worth comparing the two cases.

Passivation of the devices

During the study, we did not make extra passivation in order to study the effect of dielectric layers on the devices, however, the device performance could be improved using extra passivation. Therefore, it would be interesting for further study.

Surface morphology and trapping study using other techniques

During our work, only electrical study was done, it would be very interesting to study the electron trapping effects using different techniques, such as DLTS. Also, the simulation of the devices could be helpful.

Appendix A : Devices used in the study

Structure	Dielectric	Deposition Technique	Position	Study
5 nm GaN/22 nm Al _{0.32} Ga _{0.68} N/ 0.1 μm GaN/Si	5 nm Gd ₂ O ₃	HPS	Under the gate	RT, Thermal stability, proton irradiation
	5 nm HfO ₂	ALD	Between source and drain	Chemical cleaning, STA, electrical stress
25 nm Al _{0.25} Ga _{0.75} N/ 0.6 μm GaN/Si	5 nm Al ₂ O ₃	ALD	Between source and drain	RT, proton irradiation
	5 nm HfO ₂			
	5 nm ZrO ₂			
10 nm Al _{0.83} In _{0.17} N /0.6 μm GaN/Si	5 nm HfO ₂	ALD	Between source and drain	RT, proton and helium irradiation
	5 nm Al ₂ O ₃			RT, proton irradiation
	5 nm HfO ₂			
	5 nm ZrO ₂			
3 nm GaN/10 nm Al _{0.83} In _{0.17} N/0.6 μm GaN/Si	5 nm Al ₂ O ₃	ALD	Between source and drain	RT, proton irradiation
	5 nm HfO ₂			
	5 nm ZrO ₂			
	5 nm HfO ₂			RT, thermal cycle

Appendix B Fabrication processes

B.1 Sample cleaning

1. Ultrasonic bath in soap for 10 minutes
2. Ultrasonic bath in deionized water for 10 minutes
3. Acetone for 10 minutes
4. rinsed in IPA for 10 minutes at 65°C
5. Rinsed in DIW for 5-10 minutes
6. Blow dry with N₂ gas

B.2 Mesa lithography recipe

1. Coat the sample with poly-methyl-methacrylate (PMMA)
2. Spin for 120 s
3. Bake on hotplate at 160°C for 10 minutes
4. Expose with mask for 1000 s using vacuum contact
5. Develop in PMMA developer (m317) for 3 minutes with slight agitation
6. Rinse in IPA for 30 seconds with agitation
7. Rinsed in DIW for 5-10 minutes
8. Blow dry with N₂ gun
9. Clean with O₂ plasma with 10 w for 1 minute

B.3 Mesa ICP etch recipe

ICP Power	40 W
RIE Power	100 W

Chamber Pressure	5 mTorr
Cl ₂ flow flux	10 sccm
Temperature	20°C

B.4 Ohmic lithography recipe

1. Coat the sample with 1 μm poly-methyl-methacrylate (PMMA)
2. Spin for 120 s
3. Bake on hotplate at 160°C for 10 minutes
4. Expose with mask aligner for 1000 s using vacuum contact
5. Develop in PMMA developer (M517) for 3 minutes with slight agitation
6. Rinse in IPA for 30 seconds with agitation
7. Rinsed in DIW for 5-10 minutes
8. Blow dry with N₂ gun
9. Clean with O₂ plasma with 10 W for 1 minute

B.5 Ohmic metallization recipe

1. De-oxidise in HF:H₂O (1:10) solution for 10 seconds
2. Deposit ohmic contact of 20 nm Ti/ 120 nm Al/ 40 nm Ni/ 50 nm Au using e-beam evaporation
3. Soak in warm acetone (65°C) for at least 30 minutes for lift-off
4. Agitate in isopropyl alcohol (IPA) for at least 10 minutes
5. Rinsed in DIW for 5-10 minutes
6. Blow dry with N₂ gun
7. Anneal at 875°C for 45 s in a two-step ramp using rapid thermal annealer (RTA)

B.6 Gate lithography recipe

1. Coat the sample with 1 μm poly-methyl-methacrylate (PMMA)
2. Spin for 120 s
3. Bake on hotplate at 160°C for 10 minutes
4. Expose with mask aligner for 1000 s using vacuum contact
5. Develop in PMMA developer (M517) for 3 minutes with slight agitation
6. Rinse in IPA for 30 seconds with agitation
7. Rinsed in DIW for 5-10 minutes
8. Blow dry with N₂ gun
9. Clean with O₂ plasma with 10 W for 1 minute

B.7 Gate metallization recipe

1. De-oxidise in HF:H₂O(1:10) solution for 10 seconds
2. Deposit gate metal contact of 50 nm Ni/ 200 nm Ai using e-beam evaporation
3. Soak in warm acetone (65°C) for at least 30 minutes for lift-off
4. Agitate in isopropyl alcohol (IPA) for at least 10 minutes
5. Rinsed in DIW for 5-10 minutes
6. Blow dry with N₂ gun

B.8 Feeds lithography recipe

1. Coat the sample with 1 μm poly-methyl-methacrylate (PMMA)
2. Spin for 120 s
3. Bake on hotplate at 160°C for 10 minutes
4. Expose with mask aligner for 1000 s using vacuum contact
5. Develop in PMMA developer(MK317) for 3 minutes with slight agitation

6. Rinse in IPA for 30 seconds with agitation
7. Rinsed in DIW for 5-10 minutes
8. Blow dry with N₂ gun
9. Clean with O₂ plasma with 10 W for 1 minute

B.9 Feeds metallization recipe

1. De-oxidise in HF:H₂O(1:10) solution for 10 seconds
2. Deposit gate metal contact of 10 nm Ti/ 300 nm Au using e-beam evaporation
3. Soak in warm acetone (65°C) for at least 30 minutes for lift-off
4. Agitate in isopropyl alcohol (IPA) for at least 10 minutes
5. Blow dry with N₂ gun

Appendix C Fabrication and characterization techniques

C.1 Photolithography technique

Optical lithography is a method performed to duplicate a resist image of the mask used onto a wafer using a mask aligner, we have MJB4 mask aligner from SUSS MicroTec for the work, as shown in Figure C-1.

Figure C-1 picture of the MJB4 mask aligner

Photoresist is a radiation-sensitive compound. According to their reaction to UV light or radiation, two kinds of photoresists can be used for optical lithography: positive and negative photoresist. For positive photoresist, the exposed regions become more soluble in developer solutions and can be easily removed through resist development process, resulting in the mask pattern being replicated on the resist coated wafer. While for the negative photoresist, the exposed areas become less soluble in developer solutions and remain unexposed during resist development, which results in patterns opposite to those on the mask being defined on the wafer. In this way, the sample would be patterned with the photoresist which would be resistant to treatments. During the study, we have been using positive photoresist: polymethyl methacrylate (PMMA) all the time.

An illustration of the optical system of a mask aligner which is used to replica a mask pattern during optical lithography is shown in the figure below. Firstly, Ultra violet light from the source

would be collected by the condenser, the light passes through the imaging lens to form a floating image of the mask to selectively expose the resist. Therefore, the substrate can be isotropically or anisotropically etched, lifted-off, plated or metallized according to the plan.

Figure C-2 optical system of a mask linear used to replicate a mask pattern during optical lithography

C.2 ICP etching technique

ICP is chemical and ion-induced etching system, it has high ion density ($>10^{11} \text{ cm}^{-3}$) and high radical density, which could lead to high etch rate; it has RF and ICP generators which could be controlled separately, providing separate control over ion energy and ion density, enabling high process flexibility; it can be operated at low pressure; it has clamping and helium cooling standard, providing excellent temperature control. The structure of the ICP system was shown in the figure below. The standard parameters are summarized in the previous table (Table 3-1).

Figure C-3 Schematic of ICP system [335]

C.3 Metallization

The equipment used during evaporation is shown in the figure below. Metals are heated above its melting point in a vacuum chamber. The evaporated atoms then travel at line trajectories due to a long mean free-path created by the vacuum and deposit on the wafers.

Figure C-4 thermal evaporator for metal deposition

C.4 Rapid thermal annealing

In this work, we have used the two step RTA process, shown in Figure C-5. It consists of a first stage of rapid heating ramp at 15°C/s up to 800°C for 7 s, followed by a second stage of heating at 15°C/s up to 850°C for 30 s. Then, the system was cooled to RT naturally.

Figure C-5 Scheme of the two-step thermal annealing

Figure C-6 RTA oven from AET Technologies

C.5 High pressure sputtering (HPS)

The HPS technique works in the pressure of mbar range, which lies between 2 and 3 orders of magnitude above conventional sputtering. The ion damage on the substrate during growth is

small, and interface oxide caused by the dielectric growth is inhibited from this sputtering technique [225]. This is because the mean free path of the electrons in the HPS system is small: in the order of 1 mm. There will be collision among plasmas before arriving the substrate, from which the plasmas would be heated in a distance of less than 1 cm. Therefore, we could put the sample about 2- 3 cm away from the target, and achieve high quality films with good interface property.

The sputtering process is a two-step procedure developed by colleagues from UCM [190], [225], [226]. Firstly, a thin metallic Gd film is sputtered by HPS using a metallic Gd target and a pure Ar atmosphere; then, without extracting the sample from the system, the Gd₂O₃ films are *in situ* plasma oxidized, by adjusting gas composition and plasma parameters.

The dielectric growth process was optimized for several groups of samples, and the final sputtering conditions with the most suitable layer thickness, the smoothest and most homogeneous surface is shown in Table C-1.

Table C-1 HPS main parameters

Vacuum Pressure (mbar)	1.4×10 ⁻⁶
Power (W)	30
Process Pressure (mbar)	0.5
Gas Fluences	95% Ar+5% O ₂
Temperature	25.2
Gd sputtering time (s)	120
Oxidation time (s)	300

RMS roughness of 5 μm × 5 μm areas of the fabricated samples is about 2.1 nm, and the thickness is about 5 nm, measured by TEM.

C.6 Atomic layer deposition (ALD)

Atomic layer deposition (ALD) is a thin-film deposition technique with atomic scale precision growth. It is a vapor phase technique capable of producing thin films of a variety of materials including aluminum oxide (Al₂O₃), hafnia (HfO₂), Yttrium oxide (Y₂O₃), zirconia (ZrO₂) and so on. ALD technique is a sequential, self-limiting reaction, it has a lot of advantages on growing high-

aspect ratio structures with good thickness control to about 1 nm level. It is a powerful technique for industrial and research applications [336]. The equipment used during the study is shown in Figure C-7.

Figure C-7 A schematic of an atomic layer deposition (ALD) tool [337]

Several precursor gases for a target material will be dosed into a vacuum chamber sequentially under computer control. Firstly, a precursor is introduced into the process chamber producing a monolayer on the substrate, then the chamber is purged with an inert carrier gas to remove unreacted precursor and reaction by-products. Afterwards, a second precursor is pulsed into the chamber reacting with the first precursor to produce a monolayer of the desired film on the substrate. The procedure then continues by cycling this process. A schematic of ALD cycle for Al_2O_3 deposition is shown in Figure C-8.

Figure C-8 ALD cycle for Al_2O_3 deposited using TMA and O_2 plasma (A. TMA chemisorbtion B. TMA purge C. O_2 plasma D. Short post plasma purge) [337]

During the device fabrication processes in the work, the dielectric layer was deposited on the sample after Ohmic metal deposition. Then gate lithography and metal deposition were conducted. Afterwards, feeds lithography were made; in order to improve the contact property between feeds metal and ohmic metals, the samples were rinsed in $\text{HF}:\text{H}_2\text{O}$ (1:10) for 1 minute to remove the dielectrics. Then feed metal were deposited. In this way, we have achieved the dielectric layer in the areas between source and drain contacts.

C.7 Thermal stress

During the thermal stress, the blue furnace used during the study is shown in Figure C-9. Firstly, the sample was put on the sampel holder in the oven, then the oven was filled with N_2 gases; afterwards, the oven was heated with the temperature controlled by a thermalmeter.

Figure C-9 Conventional annealing furnace used during the thermal stress

C.8 Irradiation stress

The protons and heliums were produced with a 5 MV Cockcroft-Walton tandem accelerator at Centro de Micro Análisis de Materiales (CMAM) in the Universidad Autónoma de Madrid (UAM), as shown in Figure C-10. Prior to the irradiation, the homogeneity of the collimated beam was measured with a quartz reference sample.

Figure C-10 5 MV Cockcroft-Walton tandem accelerator at CMAM used for the ion beam irradiation

Appendix D Characterization techniques

D.1 Transmission line method (TLM)

The properties (contact resistance R_c and sheet resistance R_{sheet}) of the ohmic contact can be checked using TLM, which consists of a series of ohmic contacts with a step distance. In order to avoid the influence, the parasitic resistance introduced by the probes, four-point technique was used. The typical arrangement for TLM test pattern is shown in Figure D-1.

Figure D-1 Scheme of ohmic contacts

The total resistance gotten from the measurements consists of three components:

$$R_T = 2R_m + 2R_C + R_{semi} \quad \text{D-1}$$

Where R_m is the resistance caused by the contact, R_C is due to the metal/semiconductor interface, and R_{semi} is the semiconductor resistance.

Figure D-2 typical arrangement for a TLM test pattern [263].

In most cases, the resistivity of the metal in the contact is low compared with the contact resistance ($R_m < R_C$), so it could be ignored.

The semiconductor resistance is:

$$R_{semi} = R_{SH} \frac{L}{W} \quad D-2$$

$$R_T = R_{SH} \frac{L}{W} + 2R_C \quad D-3$$

By constructing a list of contacts with different length, the total resistances of each contacts can be plotted, and the sheet resistance can be found from the slope of the line and the contact resistance can be achieved from the zero-length resistance.

Figure D-3 representation of measured values of resistances

D.2 Hall measurements

Hall measurement using van der Pauw are used to characterized the 2DEG carrier density and mobility. A current is applied between the two parallel contacts (I_{12}) and the resultsing voltage is measured between the other two contacts (V_{34}), in this way, the longitudinal resistance (R_{12}) will be calculated:

$$R_{12} = \frac{V_{12}}{I_{34}} \quad \text{D-4}$$

The resistivity (ρ) can be extracted from the resistance.

Then a current is applied to the two diagonal ohmic contacts (I_{13}), and the voltage can be measured between the other two contacts (V_{24}), the Hall resistance is calculated:

$$R_H = \frac{V_{24}}{I_{13}} \quad \text{D-5}$$

In the end, the 2DEG carrier density (n_s) and the mobility (μ) can be extracted using:

$$n_s = \frac{1}{q \cdot R_H} \quad \text{D-6}$$

$$\mu_H = \frac{R_H}{\rho} \quad \text{D-7}$$

D.3 Electron transportation mechanisms in the diodes

The transport mechanisms in rectifying contacts are thermionic emission, field emission and tunneling, which make electrons travelling over or through the Schottky barriers possible. When metal and a semiconductor are contacted, the alignment of the bands is closely related to the Schottky barrier height (SBH) [338], it can be expressed as :

$$\text{SBH} = \Phi_M - \chi_s, \quad \text{D-D-8}$$

where χ_s is the electron affinity (EA) of the semiconductor. A scheme of band alignments at a semiconductor metal junction is shown below.

For GaN-based semiconductors, metal with high work function (Φ_M) is generally used to fabricate Schottky contacts [13], [28], [339]–[341].

Figure D-4 Schematic of band alignments at a semiconductor/metal junction [229]

According to Chiu [120], conduction mechanisms in a dielectric include two kinds of main electron transport mechanisms in general: electrode limited mechanism and bulk limited mechanism. The electrode limited conduction mechanisms depend on the properties of metal dielectric interface, and some of the most important parameter is the metal-dielectric barrier height and the carrier effective mass of in the dielectric. The electrode limited mechanism includes Schottky emission (SE), Thermionic-field emission (TFE), Fowler-Nordheim tunneling (FNT), and direct tunneling.

Figure D-5 I-V properties of the diodes

The bulk limited conduction mechanisms depend on the properties of the dielectric, and the most important parameter are the traps in the dielectric. By studying the bulk limited conduction mechanisms, trap energy level, trap spacing, trap density and the dielectric relaxation time. The bulk limited mechanism includes Poole-Frenkel emission (PFE), hopping conduction or trap assisted tunneling (TAT), ohmic contact, space charge limited conduction, ionic conduction; grain boundary limited conduction and so on.

Figure D-6. Classification of conduction mechanisms in dielectric films. [120]

1) Schottky emission (SE) mechanism

The working mechanism of Schottky emission, also named Thermionic emission, is that the electrons in the metal could overcome the energy barrier height at the metal-dielectric interface by thermal activation. The schematic energy band diagram of Schottky emission is shown below:

Figure D-7 Schematic energy band diagram of Schottky emission. [120]

The normal expression of SE current density (J_{SE}) is:

$$J_{SE} = A^* T^2 \exp \frac{-q(\phi_b - \sqrt{qE_{OX}/4\pi\epsilon_{OX}})}{kT} \quad D-9$$

$$A^* = \frac{4\pi q k^2 m^*}{h^3} = \frac{120 m^*}{m}, \quad D-10$$

where A^* is the effective Richardson's constant, m^* is the effective electron mass in the oxide, which is $1.03 m_e$ for Gd_2O_3 [342], $0.29 m_e$ for $AlGaN/GaN$ [20], h is Plank's constant, q is the electronic charge, ϕ_b is the barrier height, ϵ_{OX} is the dielectric constant, and k is the Boltzmann's constant, and T is the absolute temperature.

$\ln(J/T^2) \sim \sqrt{E_{OX}}$ can be plotted as a linear curve, and the value of ϕ_b and the dielectric constant ϵ_{OX} can be extracted from the intercept and the slope of the curve, respectively.

2) Fowler-Nordheim tunneling (FNT) based mechanism

When the barrier height is less than 10 nm, quantum mechanism could be effective. Electrons could penetrate through the barrier through tunneling. The schematic energy band diagram of FNT is shown below:

Figure D-8 Schematic energy band diagram of Fowler-Nordheim tunneling. [120]

FNT caused leakage current density (J_{FNT}) could be expressed as

$$J_{FNT} = \frac{q^3}{8\pi\hbar q\phi_b} E_{OX}^2 \exp \left[-\frac{8}{3} \frac{\pi\sqrt{2m_{OX}^*} (q\phi_b)^{3/2}}{qh E_{OX}} \right], \quad D-11$$

Equation (4) could be rearranged as $\ln(J/E_{OX}^2) \sim \frac{1}{E_{OX}}$, and ϕ_b can be estimated from the slope of the linear fit.

Previously publications show that the dominant electron transport mechanism in $\text{SiN}_x/\text{AlGaIn}/\text{GaIn}$ MIS structure is FNT at high electric field [343]. And FNT appeared in the reverse biased region in $\text{AlGaIn}/\text{GaIn}$ [324], [344] and AlInN/GaIn Schottky HEMTs [84], and it is dominant in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaIn}$ MOS structure at low temperatures ($T < 0^\circ\text{C}$) and high electrical filed [115].

3) Direct tunneling (DT)

When the voltage on the dielectric is not large enough, direct tunneling is the dominant electron transport mechanisms. The schematic energy band diagram of DT is shown below. However, this effect is usually observed when the dielectric thickness is smaller than 3.5 nm observed in SiO_2/Si MIS devices.

Figure D-9 Schematic energy band diagram of Direct tunneling. [120]

4) Thermionic field emission (TEM)

Thermionic-field emission happens in between Schottky emission and field emission. The electrons should have the energy between the Fermi level of metal and the conduction band edge of dielectric. The schematic energy band diagram of thermionic-field emission and the difference among thermionic emission, thermionic-field emission, and field emission are shown in the figures below.

TFE caused leakage current density (J_{TFE}) could be expressed as

$$J_{TFE} = \frac{q^2 \sqrt{\pi m_{OX}^*} \sqrt{kT}}{2h^2 q \phi_b} E_{OX} \exp\left(-\frac{q\phi_b}{kT}\right) \exp\left[-\frac{(hqE_{OX})^2}{96\pi^2 m(kT)^3}\right], \quad D-12$$

Equation (4) could be rearranged as $\ln(J/E_{OX}) \sim \frac{1}{E_{OX}^2}$, and ϕ_b can be estimated from the slope of the linear fit.

Figure D-10 Schematic energy band diagram of TFE, and the differences among SE, TFE and FE . [120]

5) Poole-Frenkel emission (PFE)

Those kinds of transport mechanisms are based on traps in the dielectric, such as PFE and TAT as shown below, and the most relevant parameter is the trap energy level.

Poole-Frenkel emission is like the Schottky emission; electrons are thermally excited and emitted from traps into the dielectric. The schematic energy band diagram of Poole-Frenkel emission is shown in the figures below. Because PFE is usually caused by the thermal activation, this electro transport mechanism is mostly observed at high electric field or high temperatures.

Figure D-11 Schematic energy band diagram of Poole-Frenkel emission. [120]

The current density caused by PFE J_{PFE} is given by:

$$J_{PFE} = q\mu N_c E_{OX} \exp \left[-\frac{q}{kT} (\phi_t - \sqrt{qE_{OX}/\pi\epsilon_{OX}}) \right], \quad D-13$$

where ϕ_t is the trap energy level below the conduction band edge of the dielectric. The dielectric constant could be derived from the slope of $\ln(J/E_{OX}) \sim \sqrt{E_{OX}}$ plots.

Previously published literature shows that the dominant electron conduction mechanism in SiN_x/AlGaIn/GaN MIS structure is PFE at low electric field [343]; and the dominant conduction mechanism in Ta₂O₅/GaN MOS-Ds is PFE at high gate bias [81].

6) Trap assisted tunneling (TAT)

Trap assisted tunneling is that the electrons hopping through the dielectric with the help of traps in the dielectric, the differences the schematic energy band diagrams among DT, FNT and TAT are shown below. At relatively low gate bias condition, DT and TAT will work. When gate bias increases, FNT and TAT will work.

Figure D-12 Difference among schematic energy band diagrams of DT, FNT and TAT. [345]

There is another condition that there are steps during tunneling, which mean the electrons need the help of other traps, it is then called hopping, schematic energy band diagrams among DT, FNT and TAT are shown below.

Trap assisted tunneling in ultra-thin dielectric film has been studied [345]; previous publications show that the dominant electron conduction mechanisms in Al₂O₃/AlGaIn/GaN MOS structure is TAT with trap energy level at 1.7-2.3 eV [115], and

Tunneling current density J_{TAT} is given by:

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm_{OX}}}{3hE_{OX}} \phi_t^{3/2}\right) \quad \text{D-14}$$

From the slopes of plots $\ln J_{TAT} \sim \frac{1}{E_{OX}}$, the trap energy level ϕ_t can be derived as a function of the temperature and electric field range.

Figure D-13 Schematic energy band diagrams of Hopping. [120]

7) Other mechanisms

The other electron mechanisms include ohmic contact, space charge limited conduction, ionic conduction, grain boundary limited conduction and so on. Those conduction mechanisms are less studied than the previously listed mechanisms.

Ohmic conduction is the mobility of electrons in the conduction band or the holes in the valence band. Due to the high energy band gap of the dielectric, there is only a small number of electrons can be excited from the valence band or from the traps bands. Schematic energy band diagrams of Ohmic contact is given below, and the current density due to ohmic conduction can be given as

$$J = \sigma E = nq\mu E, n = N_c e^{-\left(\frac{E_C - E_F}{kT}\right)} \quad \text{D-15}$$

Where σ is the electrical conductivity, n is the number of electrons in the conduction band, μ is electron mobility, and N_c is the effective density of the conduction band. Literature shows that the dominant electron conduction mechanism in GaN-based MOS-Ds using Ta₂O₅ dielectric film is Ohmic conduction at low gate bias [81].

Space charge limited conduction is like the electron conduction mechanisms in a vacuum diode. The schematic energy band diagrams of space charge limited conduction is given below.

Figure D-14 Schematic energy band diagrams of ohmic conduction and space charge limited conduction. [120]

The charge distribution follows Poisson's equation:

$$\frac{\partial^2 V}{\partial^2 x} = -\frac{\rho(x)}{\epsilon_0} \quad \text{D-16}$$

$$v(x) = \sqrt{\frac{2qV(x)}{m}} \quad \text{D-17}$$

$$j_x = qn(x)v(x) \quad \text{D-18}$$

$$J = \frac{4\epsilon_0}{9} \left(\frac{2e}{m}\right)^{\frac{1}{2}} \frac{\sqrt[3]{V^2}}{d^2} \quad \text{D-19}$$

In solid materials, continuity equation can be written as:

$$j_x = en(x)v(x) + eD \frac{dn}{dx} \quad \text{D-20}$$

Due to existence of lattice defects in the dielectric, ions may jump from one defect site to another with the help of external electric field. The ionic conduction current can be expressed as:

$$J = J_0 e^{-\left(\frac{q\phi_B}{kT} - \frac{Eqd}{2kT}\right)} \quad \text{D-21}$$

D.4 Capacitance-voltage characteristics

C-V characteristics of the diodes are usually taken place, the sweep usually takes 0.1 s/step, from cut off voltage to 0 V, and then from 0 V to the original cut off voltage. For the MOS-Ds, the

relative dielectric constant of the layer can be estimated. And quantitative analysis of the interface trap densities can be generated from the capacitance voltage shifts of the diodes.

Figure D-15 C-V properties of Schottky Diodes and MOS-Ds

The 2DEG density(n_s) versus depth (z) can be obtained using:

$$n_s = \frac{\int_{V_1}^{V_2} C dV}{q \cdot A} \quad \text{D-22}$$

$$z = \epsilon_r \epsilon_0 \frac{A}{C} \quad \text{D-23}$$

Where C is the measured capacitance, q is the electron charge, A is the area, ϵ_r and ϵ_0 are the relevant and absolute dielectric constant

From hysteresis, we know that there are slow interface traps in the oxide, the value can be estimated, using the following approximation:

$$\Delta N_{oxide} = \left(\frac{C_{ox}}{q}\right) \Delta V_{hyst} \quad \text{D-24}$$

where C_{ox} is oxide capacitance.

The interface state density was estimated roughly using the conductance method [188]:

$$\frac{G_p}{\omega} = \frac{\omega G_m C_{ox}^2}{G_m^2 + \omega^2 (C_{ox} - C_m)^2} \quad \text{D-25}$$

$$D_{it} = \frac{2.5}{q} \left(\frac{G_p}{\omega}\right)_{max} \quad \text{D-26}$$

where G_p is the equivalent parallel conductance, G_m is measured conductance, C_m is measured capacitance, $\omega = 2\pi f$, f is the measurement frequency.

The capacitance and the applied voltage on the diodes can be written as [346]:

$$\frac{1}{C^2} = \frac{2(V_{bi} - \frac{kT}{q} - V)}{A^2 q N_d \epsilon_0 \epsilon} \quad \text{D-27}$$

Where V_{bi} is the built-in voltage, ϵ is the dielectric constant. The built in voltage could be deducted from the slope of the $\frac{1}{C^2} - V$ curve, and the carrier density can be deducted from the intercept of the linear fit [347]. Built-in voltages are shown in the table below:

The carrier density in the hetero-structure can also be studied from the C-V relation [108][346],

$$C = -\frac{dQ}{dV} = qA \frac{d}{dV} \int_0^z N dx = qAN(z) \frac{dz}{dV} \quad \text{D-28}$$

$$N = \frac{C^3}{q\epsilon_0\epsilon} \frac{dV}{dC} = \frac{2}{q\epsilon_0\epsilon d(1/C^2)/dV} \quad \text{D-29}$$

$$z = \frac{\epsilon_0\epsilon}{C} \quad \text{D-30}$$

Where V is the applied gate voltage, ϵ_0 is the dielectric constant, ϵ is the relative dielectric constant. The curves show no significant difference among the diodes after irradiation with different doses.

The capacitance measurements were taken using a HP4284A LCR analyser, as shown in

Figure D-16 HP4284A LCR analyser

D.5 Electrical characterizations of the HEMTs

1) DC IV characterization

The basic operating parameters of HEMT for high-power operations are: the maximum drain current ($I_{D,max}$), the maximum transconductance ($g_{m,max}$), the threshold voltage (V_{th}), and the power density (P_{out}). These parameters can be extracted from the output and the transfer characteristics (Figure D-17).

Figure D-17. DC (a) output and (b) transfer characteristics of a AlGaIn/GaN HEMTs

The maximum drain current ($I_{D,max}$) for long channel HEMTs can be expressed as [100]:

$$I_{D,max} = \frac{\mu\epsilon W}{2Ld} (V_{GS} - V_T)^2 \quad D-31$$

where W and L are the gate width and length, respectively, ϵ is the semiconductor dielectric constant and d is the distance of the gate to the 2DEG.

During the measurements, the $I_{D,max}$ was taken at the saturation region where $V_{GS} = 1$ V.

The on resistance (R_{ON}) can be deduced from the curves at the linear region :

$$R_{ON} = \frac{V_{DS}}{I_D} \quad D-32$$

During the work, the R_{ON} is usually calculated at the linear region of the IV curves at $V_G = 1$ V, usually $V_{DS} = 2$ V.

Transconductance (g_m) is a measure of the variation of the drain current with the gate voltage and it is related to the gain of the device. It can be expressed as

$$g_m = \frac{\partial I_D}{\partial V_G} \bigg|_{V_D=Constant} = \frac{\mu\epsilon W}{Ld} (V_g - V_{th}) \quad D-33$$

During the work, the $g_{m,amx}$ is compared among all devices, it is usually taken as the maximum g_m at $V_{DS} = 4.9$ V.

Threshold voltage is defined as the value of the V_{GS} for which the channel conductivity is null, therefore it determines when the channel starts to conduct. It also can be expressed as:

$$V_{th} = \phi_B - \Delta E_C - \frac{qN_D}{2\epsilon} d^2 \quad D-34$$

where ϕ_B is the gate Schottky-barrier height, and ΔE_C is the conduction band difference between the two sides of heterojunctions, and N_D is the background doping of the GaN layer.

During the work, the V_{th} of the HEMTs is defined as the intercept of the transconductance linear fit with the V_{GS} -axis at $V_{DS} = 0.1$ V.

Power density is an evaluation of the output power of the devices. It can be defined as:

$$dP_{out} = \frac{I_{D,max} \cdot (V_{BD} - V_K)}{8} \quad D-35$$

where V_{BD} is breakdown voltage and V_K is knee voltage.

The IV characterization were carried out using a Agilent 4156C semiconductor parameter analyser on a Karl Suss DC probe station or DC/RF probe station with Wenesco hot plate.

Figure D-18 (a) Agilent 4156C semiconductor parameter analyser and (b) Karl Suss DC probe station

2) Pulsed IV characterizations

Pulsed characterization was used to evaluate the self-heating and trapping effects in the HEMTs, which are partially responsible of the failure mechanisms and limit the devices reliability. Square voltage signals are pulsed from a static quiescent bias point (Q) to activate current at the end of the pulsed duration, then the devices will be kept at Q point until the next voltage pulse is applied. The thermal and trapping effects depends on Q point. During the pulse measurements, the other two important parameters are the pulse duration (τ_{ON}) and the pulse period (τ), and τ_{ON} should be short enough compared with τ .

The set-up of the pulsed measurements system was designed by Dra Dara Martin-Horcajo using an Agilent 81150A pulse function arbitrary noise generator and a Yokogawa DLM2000 digital oscilloscope remotely controlled by a PC using LabView.

Figure D-19 Illustration of the pulsed characterization system used during the study

Pulsed I-V measurements at different bias conditions are usually conducted to identify the origin of the traps. Figure D-20 shows the pulsed output characteristics at different quiescent points ($V_{ds,Q}$, $V_{gs,Q}$):

- (a) at $V_{ds,Q} = 0$ V and $V_{gs,Q} = 0$ V, where no trapping effects are detected and it is used as reference,
- (b) at $V_{ds} = 0$ V and $V_{gs} = -8$ V, the drain current is reduced due to gate lag,
- (c) at $V_{ds} = 15$ V and $V_{gs} = -8$ V.

Figure D-20 Double pulsed I-V characterization of AlGaIn/GaN HEMTs

GLR and DLR is calculated from the drain current ration at the linear region.

$$GLR = \frac{I_{D,pulse-8,0}(V_D=4.5 V)}{I_{D,pulse-0,0}(V_D=4.5 V)} \quad D-36$$

$$DLR = \frac{I_{D,pulse-8,15}(V_D=4.5 V)}{I_{D,pulse-8,0}(V_D=4.5 V)} \quad D-37$$

3) RF characterizations

The RF parameters of interest for power transistors are the unity current gain frequency (f_T), the maximum oscillation frequency (f_{max}), the output power (P_{out}), maximum available gain (MAG) and power added efficiency (PAE). f_T and f_{max} can be extracted from the small signal RF behavior of the HEMT, tested by means of S-parameters measurements [124], as shown in Appendix III. The parameters are calculated from large signal RF characteristics as follows:

The stability factor (k):

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{12}S_{21}|} \quad D-38$$

Maximum stable gain(MSG) if $k < 1$ and maximum available gain (MAG) if $k \geq 1$:

$$MSG = (k - \sqrt{k^2 - 1}) \left| \frac{S_{21}}{S_{12}} \right| \quad D-39$$

$$MAG = \left| \frac{S_{21}}{S_{12}} \right| \quad D-40$$

Figure D-21 MSG/MAG typical behaviour for a HEMT

The Unilateral Gain (U):

$$U = \frac{1}{2} \frac{\left| \frac{S_{21}}{S_{12}} - 1 \right|^2}{k \left| \frac{S_{21}}{S_{12}} \right| - \text{Re} \left(\frac{S_{21}}{S_{12}} \right)} \quad \text{D-41}$$

Transmission Hybrid parameters:

$$H_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}} \quad \text{D-42}$$

f_{MAX} is the frequency at which $U=0$ dB or $\text{MSG/MAG} = 0$ dB

Figure D-22 H_{21} and U of the device

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- Peer review articles

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