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*Analysis and Comparison of Topologies of
Three-Phase Active Rectifiers for Aircraft
Applications*

TESIS DOCTORAL

Autor: **Sisi Zhao**

Máster en Electrónica Industrial, Universidad Politécnica de Madrid

Directores: **Pedro Alou Cervera, Jesús Ángel Oliver Ramírez**

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献给我亲爱的父亲母亲，
谢谢你们给予我全部的爱，陪伴，与支持。

—爱你们的思思

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Sisi Zhao
in Madrid, December 2017.

Abstract

The constantly boosting air traffic in aircraft industry, has demanded future aircraft to evolve towards higher efficiency, lower take-off weight, and thus less air pollution. Conventional aircraft are composed of four different power subsystems after the engine: mechanical, hydraulic, pneumatic and electrical. However there has been an emerging trend to replace the first three parts by electrical equipment which are more efficient, light-weighted, and accordingly less CO₂ emissions. Thus aiming at the MEA concept, more electrical power conversion is required which calls for converter topologies that can provide high efficiency and high power density. Nowadays the rectifiers on the aircraft mainly employ passive solutions involving uncontrolled diode bridges and mains-frequency transformers, since they are extremely reliable. Thus more enhanced rectifier topologies are demanded, with better performance and controllability, meanwhile complying the corresponding standards.

In Chapter 2 an overview of the state of the art is provided. Both two-stage structure and single-stage with isolation structure, as candidates for aircraft applications are reviewed and briefly compared.

In this dissertation, the standards that the rectifier systems have to comply are MIL-STD-704F regarding input three-phase power quality, and MIL-STD-461F regarding EMI issues. Besides, galvanic isolation is also a basic requirement for safety concerns. As a contribution, a single-stage isolated three-phase buck-type rectifier topology is proposed. Its operating principle and modulation method in SVM are both thoroughly discussed in Chapter 3. Due to the bridge-leg structure, together with sufficient leakage inductance from the transformer, ZVS can be achieved in every switching instant of this rectifier using the presented asymmetrical modulation sequence. Thus ZVS is an outstanding feature of this topology, which improves the overall efficiency of the rectifier, as well as EMI performance. Detailed analysis on ZVS conditions are presented.

Throughout the literature, VIENNA Rectifier III is a topology variation close to the proposed one. However the difference in both phase-leg implementation and modulation sequence makes the proposed rectifier feature less conduction losses, and

capability of realizing ZVS which VIENNA Rectifier III does not have. A detailed comparison is also carried out.

In Chapter 4, the design of the proposed rectifier is carried out following the presented design guidelines. Transformer is the key component in the topology, since volt-second balance has to be maintained during operation meanwhile presenting sufficient leakage inductance for the ZVS feature. Upon finishing the transformer leakage inductance and winding resistance are measured, and the results show good accordance to the design. Since the proposed rectifier features buck-type topology, the input currents present a pulsating waveform. In order to filter this pulsating current to a smooth sinusoidal-shaped current and comply with the MIL-STD-461F standard, a two-stage EMI filter is designed. Simulation results show that at nominal power, the rectifier together with the designed EMI filter can comply with the standard and meanwhile maintaining a very low THD and nearly-unity power factor. Next, the voltage and current stresses of all the semiconductor devices in the topology are derived. Output filter $L_o - C_o$ is also designed.

With the diode rectifier on the secondary, ringing effect occurs due to the leakage inductance in the transformer and the parasitic capacitance of the diodes on the secondary. This ringing introduces high voltage peak and high-frequency noises that can cause EMI issues. A passive snubber solution and an active snubber solution are both presented and designed for the rectifier. Simulation results are shown to prove the functionality of both solutions. Finally a breakdown of total losses estimation is provided at the end of this chapter.

In Chapter 5, a hardware demonstrator is designed and constructed to validate the theoretical analysis presented in the dissertation. First, the prototype test working as phase-shifted full-bridge DC-DC converter is performed with each snubber solution installed. Waveforms and measurement results are presented and compared. Next, prototype test working as the proposed rectifier (AC-DC test) is performed and measurement results show very good accordance to the simulation in terms of THD and PF.

In the last chapter, a summary with highlighted contributions and conclusions from this work is addressed and a vision of future work is given.

Resumen

El constante impulso del tráfico aéreo en la industria aeronáutica, ha exigido que los futuros aviones evolucionen hacia una mayor eficiencia, menor peso de despegue y, por tanto, menos contaminación atmosférica. Los aviones convencionales se componen de cuatro subsistemas de energía diferentes después de la turbina: mecánico, hidráulico, neumático y eléctrico. Sin embargo, hay una tendencia emergente para reemplazar los tres primeros subsistemas por equipos eléctricos, los cuales son más eficientes, de peso ligero, y por consiguiente, con menos emisiones de CO₂. Por lo tanto, dentro del concepto del avión más eléctrico (MEA), se requiere una mayor conversión de energía eléctrica que requiere de topologías de convertidor de alta eficiencia y alta densidad de potencia. Hoy en día los rectificadores de aviónica emplean principalmente soluciones pasivas, que implican puentes de diodos no controlados y transformadores a frecuencia de red, mientras son extremadamente fiables. Así pues las topologías de rectificador más avanzadas tienen un mejor rendimiento y controlabilidad, mientras que se exige que cumplan con los requisitos correspondientes.

En el capítulo 2 se proporciona la visión general del estado del arte. Los candidatos son: la estructura de dos etapas y la de una sola con aislamiento, y se repasan y se comparan brevemente. En esta disertación, los estándares que los sistemas de rectificador tienen que cumplir son principalmente MIL-STD-704F con respecto a voltaje trifásico de la entrada, y MIL-STD-461F con respecto a problemas de EMI. Además, el aislamiento galvánico es también un requisito básico por preocupaciones de seguridad. Como contribución, se propone una topología de rectificador de tipo reductor trifásico aislada de una sola etapa. Su principio de funcionamiento y el método de la modulación vectorial se discuten a fondo. Debido a la estructura de la pierna del puente, junto con la suficiente inductancia de fuga del transformador, ZVS se puede alcanzar en cada instante de la conmutación de este rectificador usando la secuencia asimétrica presentada de la modulación. Así, el ZVS es una característica excepcional de esta topología, que aumenta el rendimiento del rectificador. Se presenta el análisis detallados, sobre las condiciones de ZVS.

A lo largo de la bibliografía, el rectificador III de VIENNA es una variación topológica cercana a la propuesta. Sin embargo, la diferencia en la ejecución de la fase-pierna y la secuencia de la modulación, hace que la característica propuesta del rectificador tenga menos pérdidas de conducción, y capacidad de realizar ZVS, que el rectificador III de VIENNA no tiene. También se realiza una comparación detallada.

En el capítulo 4, el diseño del rectificador propuesto se lleva a cabo siguiendo las pautas de diseño presentadas. El transformador es el componente clave en la topología, ya que se debe mantener el equilibrio de voltios-segundo mientras se alcanza la suficiente inductancia de fuga para la característica de ZVS. Al acabar la manufactura del transformador, la inductancia de fuga y la resistencia del devanado se miden. Los resultados se concuerdan bien al diseño. Puesto que el rectificador propuesto ofrece la topología del tipo reductor, las corrientes de entrada presentan una forma de onda pulsante. Con el fin de filtrar esta corriente pulsante una forma de corriente sinusoidal suave y cumplir con el estándar MIL-STD-461F, un filtro EMI de dos etapas se ha diseñado. Los resultados de la simulación demuestran que en la potencia nominal, el rectificador junto con su filtro EMI pueden cumplir con el estándar y mientras tanto mantener un THD muy bajo y un factor de potencia cercano a la unidad. A continuación, se derivan las especificaciones de tensión y corriente de los semiconductores de la topología. El filtro de salida $L_o - C_o$ también se ha diseñado.

Con el rectificador del diodo en el secundario, las oscilaciones ocurren debido a la inductancia de fuga del transformador y a la capacidad parásita de los diodos en el secundario. Estas oscilaciones introducen picos de alta tensión y ruidos de alta frecuencia que pueden causar problemas de EMI. Soluciones de atenuador pasivo y activo se presentan y se diseñan para el rectificador. Los resultados de la simulación demuestran la funcionalidad de ambas soluciones. Al final de este capítulo, se proporciona un desglose de la estimación de las pérdidas totales.

En el capítulo 5, se diseña y construye un prototipo para validar el análisis teórico presentado en la disertación. Con el prototipo que trabaja primero como convertidor puente completo de fase desplazada se realiza con cada solución de atenuador instalado. Las formas de onda y las medidas se presentan y comparan. A continuación, se realiza una prueba del prototipo trabajando como el rectificador

propuesto y las medidas concuerdan muy bien con la simulación en términos de THD y de factor de potencia.

En el último capítulo, se aborda un resumen de las contribuciones y conclusiones de este trabajo y se da una visión de las líneas futuras.

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Introduction

1.1 Motivation

During the recent decades, notable technological advances in the aircraft industry have improved aircraft efficiency and reduced the costs of air transportation. It is reflected in an average yearly growth rate of 9% since 1960 in worldwide air passenger traffic [1]. Today air transport produces 2% of total man-made CO₂ emissions, and this is probable to increase to 3% by 2050. In this contest, there are not only harsh environmental but also commercial pressures on aircraft manufacturers to improve the performance of future aircraft in terms of efficiency, take-off weight, safety, and air pollution [2].

Today the conventional civil aircraft are composed of four different power distribution subsystems: mechanical, hydraulic, pneumatic and electrical [3]. The mechanical power from the turbine is used to supply fuel and oil pumps. The hydraulically powered actuators are able to generate large forces, so it is used to move the flight control, landing gears, braking, doors and so on. Some bleed air of the turbine as pneumatic power is used for cabin pressure, air conditioning, and icing protection of the wings. An electrical generator is connected to a shaft of the gas turbine and generates electrical power for lighting, avionics, galley, flight entertainment and other electrical loads on board [3].

Thus there has been this emerging trend of increasing efficiency and reducing the weight of the aircraft as well as CO₂ emissions by replacing heavy mechanical, pneumatic or hydraulic driven elements by electronic equipment. This is commonly known as More Electric Aircraft (MEA) concept [4]. Technology studies for military aircraft carried out in the 90s expect a reduction of the take-off weight of 6.5% and an increase of mean flying hours between failures of 5.4% by application of MEA concept [5].

Figure 1.1: Conventional electrical power generation using a mechanical gearbox to transfer the variable speed of the engine shaft to a shaft with constant speed.

Thus for the increasing demand for the electrical power conversion systems on board, new converter topologies with higher efficiency, higher power density and good controllability are of top interest in the field of power electronics.

1.2 Three-phase rectifiers in nowadays aircraft

In a conventional aircraft the electrical generators are connected with the turbine via a mechanical gear box which transfers the variable speed of the engine shaft to a constant speed shaft to generate a three-phase power source with a constant mains frequency of 400 Hz and a voltage of 115 Vrms. This is depicted in Figure 1.1 [6].

The conventional rectifiers employed in nowadays aircraft are relying on the passive solutions. These passive systems consisting of a three-phase diode bridge usually exhibit very poor input current quality and power factor. The conduction interval can, however, be enlarged if either three inductors are inserted on the AC-side or a single inductor is inserted on the DC-side of the rectifier bridge. This considerably improves system performance but still a THD_I above 30% and a power factor below 0.952 exists [7]. The input current quality can be enhanced considerably if two or more phase-shifted rectifier bridges are connected in parallel which results in passive multi-pulse rectifier systems. Transformers are used for phase-shifting and isolation and such systems are called Transformer Rectifier Units (TRU). Figure 1.2 [8] depicts this kind of rectifier topology of passive 12-pulse with inter-phase transformer on the AC-side [8].

The presented rectifier provides high reliability due to the line commutating diode bridges and high reliability due to the fact that no high-frequency switching is employed. However, apart from line filtering inductors, the interphase transformers are key part of the rectifier which increments significantly the total weight [9].

1.3. Organization of the dissertation

Figure 1.2: Passive 12-pulse rectifier system with inter-phase transformer located on the AC-side.

Furthermore, this type of rectifier systems offer no dedicated control of the DC output voltage, unless adding another active stage at the output [10].

Therefore, enhanced rectifier topologies are required to overcome these drawbacks. Active rectifiers show a controlled output voltage and also controlled sinusoidally shaped mains currents, and thus will become the focus of interest in this dissertation.

1.3 Organization of the dissertation

The objective of this dissertation is to propose a three-phase single-stage isolated active rectifier topology under the demanding More Electric Aircraft initiative.

After this Introduction chapter, the work of this dissertation is developed by the following 5 chapters:

Chapter 2 introduces the active PFC rectifiers with galvanic isolation for the intended aircraft application. Suitable state-of-the-art topologies, respectively under conventional two-stage structure and isolated single-stage structure, are provided and briefly compared.

In **Chapter 3** the proposed rectifier topology is introduced. Its operating principle and modulation method are analyzed in details. ZVS feature is an outstanding advantage of the proposed topology and is described thoroughly. In the end, similarity and difference between the proposed rectifier and the VIENNA

Rectifier III from literature are provided. This chapter is the essential contribution of the dissertation.

Chapter 4 addresses the design guideline for the proposed rectifier, complying certain military standards. This is a contribution of the dissertation also. In the end, component choice to realize the design of the rectifier prototype is listed.

In **Chapter 5** the construction of the hardware demonstrator for the proposed rectifier is described. First, experimental results of the rectifier prototype working as a phase-shifted DC-DC full-bridge are presented. Next, the prototype test working as the proposed three-phase AC-DC is performed. Measurements and waveforms are presented which validate the functionality and performance of the proposed rectifier topology.

In the end, **Chapter 6** summarizes the work done in this dissertation and highlights the main contributions. Furthermore, a vision of the future work is given.

Study of the state of the art

As previously mentioned, nowadays the three-phase rectifiers in the aircraft are mainly relying on passive solutions. They present high volume and weight due to the line-side transformer structure, and provide no control over the output voltage. Thus in order to accelerate the emerging trend of MEA, this chapter will present an overview of the state-of-the-art unidirectional rectifier topologies with galvanic isolation. The focus is given on rectifier systems with low weight and high power density as those are the main requirements for MEA applications.

2.1 Conventional two-stage rectifier with isolation

Three-phase AC-DC power supplies with features such galvanic isolation, low input current THD_I and high power factor conventionally consist of two cascaded converter stages, shown in Figure 2.1. The first AC-DC stage serves as an active-front-end which is in charge of realizing PFC and low THD_I, meanwhile meeting EMI standards. And the second stage is an isolated DC-DC converter which provides tight regulation of the output, and dynamic requirements. In between these two stages, usually there is a DC-link capacitor (or in some cases a DC-link inductor), which in general is relatively large. Its function is to buffer energy and thus decouples the dynamics of the AC-DC stage and the DC-DC stage. In addition, this allows to separate the design and optimization issues for each stage. Moreover, the closed-loop control scheme can be designed for each stage individually.

Thus in applications where the input and output voltage range is wide and energy storage is allowed, two-stage topologies are of interest due to their flexibility provided by the voltage in the DC-link capacitor [11, 12]. Several state-of-the-art topology candidates for each stage are listed below.

Figure 2.1: Block diagram of the two-stage rectifier system with galvanic isolation.

2.1.1 Topologies for three-phase active PFC rectifiers

In [7, 13, 14] a very thorough classification and analysis of three-phase rectifier topologies is addressed. It concludes the unidirectional three-phase rectifier systems into the following three categories:

- Passive systems, which comprise only mains-frequency commutated devices and no high-frequency switching devices, mains-frequency passive components for input current shaping and/or output voltage soothing, with no output voltage regulation.
- Hybrid systems, which have mains-frequency commutated diode bridges with forced commutated circuit sections, mains-frequency and/or switching-frequency passive components, the majority with regulated output voltage.
- Active PFC systems, which exhibit forced commutation, exclusively switching-frequency passive components, and fully regulated output voltage.

Whereas, in the application field considered in this dissertation, the controllability of the rectifier output voltage is an essential improvement since it can facilitate individual design and control on each stage, meanwhile ease the voltage regulation effort on the DC-DC stage. Moreover, the PFC capability is also a requirement for the application. Thus, the rectifier topologies under review for this section are those which can shape sinusoidal input currents with PFC capability, and regulate the output voltage at the same time. The suitable rectifier topologies are categorized into boost-type PFC rectifiers and buck-type PFC rectifiers. Below

2.1. Conventional two-stage rectifier with isolation

Figure 2.2: Circuit topology of three-phase six-switch boost-type PFC rectifier.

several most popular topologies in industrial applications [13] are depicted and commented.

Boost-type PFC rectifiers are developed based on the idea of DC-DC boost converter. Thus they feature three-phase input line inductors and output DC capacitor. Figure 2.2 [13] depicts the three-phase six-switch boost-type PFC rectifier. The phase legs are all paralleled to the output DC capacitor which is considered as a voltage source, and each switching node is connected to a line-side inductor. Each phase leg is modulated in a pattern that a switching-period averaged sinusoidal voltage (regarding virtual output midpoint) is presented in the switching node of each leg. Accordingly, sinusoidal currents are impressed through the input inductors. Moreover since the sinusoidal voltages can be formed independent of the current flow, sinusoidal currents of any phase displacement regarding the mains voltages can be impressed. Particularly currents can even flow in counter-phase against the mains voltages, which suggests power flowing back from the DC side to the mains. The bidirectionality is an intrinsic advantage of this six-switch boost-type rectifier topology since no extra components are needed, unlike other unidirectional topologies. On the other hand, since this topology is boost derived, the output voltage needs to stay higher than a limit in order to make sure of the controlled functionality, to be exact:

$$U_{pn} > \sqrt{3}\hat{U}_N \quad (2.1)$$

This suggests the necessity of higher voltage-rating semiconductor devices, compared to the buck-derived rectifier topologies under the same mains voltages. Besides,

Figure 2.3: Circuit topology of three-phase VIENNA Rectifier (boost-type).

since the three-phase inductors are mains-frequency inductors, volume and weight are considerable compared to the DC side inductor in those buck-derived rectifier topologies.

Besides, since the output capacitor of boost-type rectifier needs to reach a certain DC level before the rectifier can perform its normal function and this output DC capacitor is usually large, issues like soft-start and limiting inrush current have to be incorporated into the development phase of the rectifier.

The above mentioned three-phase six-switch boost-type PFC rectifier is a two-level rectifier since voltage at switching nodes exhibits two levels only. Next, a three-level rectifier was proposed and thoroughly analyzed in [15, 16, 17, 18, 19, 20], known as VIENNA Rectifier, whose circuit topology is depicted in Figure 2.3 [13]. By splitting the output capacitor into two, the midpoint M is created. Thus three voltage levels can be formed in the switching node of each phase leg. This essentially reduces the inductance value needed to achieve the same peak ripple value compared to the aforementioned two-level six-switch boost-type rectifier. Naturally with the existence of midpoint M, the capacitor voltage balance has to be included into modulation algorithm. Besides, the power transistors in this three-level topology withstand only half of the peak value of the maximum line-to-line voltage, thus lower voltage-rating devices can be used compared to the six-switch boost rectifier case. Equation 2.1 still holds true for VIENNA rectifier, but the achievable phase displacement is only $\Phi \in (-30^\circ, +30^\circ)$ according to [13].

More detailed comparison between two-level boost-type rectifiers and the three-level ones can be found in [2, 21, 22, 23].

2.1. Conventional two-stage rectifier with isolation

Figure 2.4: Circuit topology of three-phase six-switch buck-type rectifier.

In the category of buck-type PFC rectifiers, [24, 25, 26] proposed and thoroughly discussed the modulation method for the six-switch buck-type rectifier, drawn in Figure 2.4 [13]. It features DC side output inductor as a constant current source and AC side Δ - or Y-connected filtering capacitors to provide the high-frequency pulsating currents. Due to its unidirectionality, diodes are placed in series with each MOSFET to define the unique current direction through upper and lower MOSFET of each phase leg. Thus in order to achieve ohmic behavior of each phase, the upper MOSFET of each phase only switches when that phase has positive voltage, and vice versa. Thus the pulsating current demanded in each phase from the input filtering capacitors are changing between two levels inside a switching period: zero and the DC inductor current when its phase has positive voltage; zero and negative DC inductor current when its phase shows negative voltage. Modulation is done in a way that the switching-period-averaged phase current exhibits a sinusoidal manner proportional and in phase with its phase voltage. However due to this heavily pulsating PWM phase currents, usually bigger AC side filtering effort is needed compared to the boost-type rectifier. Freewheeling of the output DC inductor current can be done in principle turning on the whole leg, however placing an extra freewheeling diode can save control complexity and meanwhile decrease conduction losses.

Due to its buck-type nature, the output voltage cannot surpass a certain value, to be exact:

Figure 2.5: Circuit topology of three-phase three-switch buck-type rectifier.

$$U_{pn} < \frac{3}{2} \hat{U}_N \quad (2.2)$$

and the phase displacement can be:

$$\Phi \in (-30^\circ, +30^\circ) \quad (2.3)$$

It can be seen that, with the topology depicted as it is in Figure 2.4, the power flow from DC side back to the mains are not possible. However only under the condition that output voltage reverses its sign, power can be fed back to the AC mains.

A topology derivation has been made in [27, 28], aiming at combing the two MOSFETs in each phase-leg into only one MOSFET but adding two extra diodes to separate currents of different directions. Figure 2.5 [13] depicts the topology of this three-switch buck-type rectifier. The modulation signals of each MOSFET is the OR logic of the two MOSFETs in each phase-leg of the previously mentioned six-switch rectifier. Due to the reduction in the number of MOSFETs, the driving effort is relaxed, however the controllability of this three-switch buck-type rectifier is limited, i.e. no possibility for reverse power flow back to the mains. Equation 2.2 and 2.3 are still applicable for this three-switch topology.

Another buck-type topology derivation was proposed in [29, 30], denoted as SWISS Rectifier, and its circuit topology is drawn in Figure 2.6 [13]. Unlike the

2.1. Conventional two-stage rectifier with isolation

Figure 2.6: Circuit topology of three-phase SWISS Rectifier (buck-type).

aforementioned six-switch or three-switch buck-type rectifiers which have direct control at the phase-leg, SWISS Rectifier features an uncontrolled three-phase diode bridge, in combination with a third-harmonic injection circuit. By the functionality of the diode bridge, the upper rail always presents the maximum voltage of all three phases, and lower rail with the minimum of all three phases. Since the output DC side inductor suppresses a dc current, switches S_+ and S_- are modulated in a manner that a current (i_{S_+} or i_{S_-}) proportional to the rail voltage is conducted through each rail respectively. The difference between i_{S_+} and i_{S_-} is injected by the active third-harmonic injection network. The current injection circuit comprises of three four-quadrant switching pairs which are gated at twice the mains frequency. They provide current path for the phase that cannot naturally conduct current by the diode bridge, i.e. the phase with minimum absolute value. Following the same modulation law as the six-switch and the three-switch buck-type rectifiers, equations 2.2 and 2.3 still hold true.

2.1.2 Topologies for DC-DC converters with galvanic isolation

Galvanic isolation makes the DC-DC converter topology more complicated and bulky due to the existence of the isolation transformer. Also the parasitics of the transformer (e.g. leakage inductance, magnetizing inductance, and winding capacitance) brings more design considerations on the operation of the circuit. Since this thesis is focused on three-phase rectifier systems from hundreds of Watts to several Kilowatts, some topology candidates appeared in the literature are reviewed below.

Figure 2.7: Circuit topology of phase-shifted full-bridge (PSFB) DC-DC converter with ZVS.

First, a full-bridge ZVS PWM DC-DC converter is proposed in [31], and its circuit topology is depicted in Figure 2.7 [31]. This phase-shift full-bridge (PSFB) topology is widely used in medium to high power applications. This topology can achieve ZVS by integrating the leakage inductance into the transformer, therefore is favorable for high voltage applications where the switching losses are significant due to the energy stored in the parasitic capacitance of the switches [31]. On the other hand, leakage inductance is commonly achieved by doing worse interleaving between the primary and secondary windings, which compromises winding losses. Another option could be to include an extra inductor in series, to achieve the needed leakage inductance value for ZVS, meanwhile having good interleaving in the transformer. However this solution compromised volume and weight.

Another DC-DC with isolation topology candidate can be found in the literature, known as dual active bridge (DAB), and its circuit topology is depicted in Figure 2.8 [32]. This topology features active full-bridge on both sides, and thus exhibits bidirectionality. Furthermore, it can operate over wide input and output voltage range, which makes it more favorable for applications such as battery charger.

Another similar bidirectional DC-DC with isolation topology is known as series resonant converter (SRC), and its circuit topology is depicted in Figure 2.9 [32].

2.1. Conventional two-stage rectifier with isolation

Figure 2.8: Circuit topology of dual active bridge (DAB).

Figure 2.9: Circuit topology of series resonant converter (SRC).

Adding a capacitor in series to the inductance L in dual active bridge (DAB) leads to this series resonant converter (SRC). The SRC can also operate with bidirectional power flow within a wide range of input and output voltages. In [32], a detailed comparison of modulation methods and design perspectives between two converter topologies is provided and it is suggested to add a second stage in order to keep high efficiency and being able to regulate the output voltage. However in the aircraft application considered in this dissertation, bidirectionality is not a requirement. Moreover, compared to the PSFB topology, DAB and SRC incorporate more switching devices which increase the control complexity and driving effort.

2.1.3 Two-stage topologies for active AC-DC + isolated DC-DC

In [33] a two-stage topology was proposed, aiming at integrating a three-phase buck-type rectifier with a current fed full-bridge, by sharing the intermediate inductor which serves as both the output inductor of the buck-type rectifier and

Figure 2.10: Circuit topology of three-phase buck-type rectifier integrated with Current-Fed Full-Bridge.

the input inductor of the current fed full-bridge. The circuit topology is drawn in Figure 2.10 [33]. The modulation of the buck-type rectifier and duty cycle of the full-bridge are synchronized in a manner that always the current ripple through the link inductor is minimized thus the size of these two inductors can be reduced. Besides, for the full-bridge MOSFETs, all of them can realize ZVS, and only the lower two MOSFETs can also realize ZCS.

2.2 Single-stage rectifier with isolation

The above mentioned AC-DC rectifier in cascaded with an isolated DC-DC converter normally exhibits reduction in overall efficiency, bulky DC-link capacitors, large total component count and thus increased control complexity. Besides, although ZVS feature can be realized in certain DC-DC converter topologies, the rectifier topologies barely show ZVS capabilities. Thus, three-phase rectifier topologies featuring single-stage with isolation, aiming at higher efficiency and power density, have emerged since early 90s, depicted as block diagram in Figure 2.11.

Throughout [34, 35, 36, 37], a novel ZVS three-phase isolated PWM buck-type rectifier was proposed. Its circuit diagram is shown in Figure 2.12 [34]. Notably, each switching position is composed of a bidirectional switching pair, featuring a four-quadrant switch. The modulation algorithm of the topology performs two ZVS phase-shifted full-bridge subtopologies in one complete switching cycle, in order to form sinusoidal phase currents, shown as Figure 2.13 [34]. The main waveforms such

2.2. Single-stage rectifier with isolation

Figure 2.11: Block diagram of the single-stage rectifier system with galvanic isolation.

Figure 2.12: Circuit topology of the ZVS three-phase isolated PWM buck-type rectifier.

as transformer primary voltage and current, secondary voltage, and phase 1 current are depicted in Figure 2.14 [34].

Apart from the standard features such as forming low-distortion sinusoidal phase currents with unity power factor, the significant advantage of this topology is that, soft switching conditions are provided for all switches due to the merit of the leakage inductance in the transformer together with its full-bridge structure. Thus switching losses are eliminated, which greatly reduces the EMI problems, even potential system failure due to noise interference.

The number of controlled semiconductor devices in this topology is 12 for MOSFETs, together with 4 high-frequency diodes at the secondary. Regarding conduction losses, there are only 4 MOSFETs always conducting on the current path. Being a buck-type converter, this ZVS isolated PWM rectifier becomes a good candidate for medium-power, high input voltage applications.

Figure 2.13: Subtopologies of the ZVS three-phase isolated PWM buck-type rectifier, composed of Bridge X and Y.

Figure 2.14: Main waveforms of the ZVS isolated PWM buck-type rectifier in one switching period.

2.2. Single-stage rectifier with isolation

Figure 2.15: Circuit topology of VIENNA Rectifier III.

Following this theory of direct matrix-type rectifier with galvanic isolation, VIENNA Rectifier III was proposed in [38, 39, 40] and its circuit topology is depicted in Figure 2.15 [38].

This rectifier can shape sinusoidal mains currents in phase with the corresponding phase voltages. Notably this rectifier topology only has 5 controlled semiconductor devices, which greatly reduces the control complexity. However due to its highly integrated phase-leg implementation, soft-switching can not be achieved and it exhibits big conduction losses since there are 6 devices conducting in the current path. To conclude, VIENNA Rectifier III is ideally suited for, e.g. the realization of welding current sources with low effects on the mains, or for telecom power supply modules with moderately high efficiency and high power density.

Since VIENNA Rectifier III is a close variation to the proposed topology in this dissertation, its operational waveforms and modulation algorithms will be further discussed in section 3.4.

It can be seen that VIENNA Rectifier III is a buck-type topology which features compressed DC output current and pulsating input phase currents. Meanwhile, the boost-type counterpart of VIENNA Rectifier III, as the other derivation of VIENNA topology, called VIENNA Rectifier II, was proposed in [41, 42]. The circuit topology of VIENNA Rectifier II is drawn in Figure 2.16 [41].

Figure 2.16: Circuit topology of VIENNA Rectifier II.

Being in the field of three-phase boost-type active rectifiers, TAIPEI rectifier was first proposed in [43], featuring a ZVS PFC Discontinuous-Conduction Mode (DCM) rectifier with only two switches. It can achieve less than 5% THD_I over the entire input range and above 20% load, also it features ZVS of all the switches without any additional soft-switching circuitry. It also maintains high efficiency ($>97.5\%$) even at half load.

Based on the TAIPEI rectifier architecture, the isolated single-stage TAIPEI rectifier was proposed in [44] and depicted in Figure 2.17 [44]. It integrates the TAIPEI rectifier with a phase-shifted ZVS full-bridge converter, having in common a bridge-leg $S_1 - S_2$, which serves as the switches of the boost front end and meanwhile the leading-leg switches of the ZVS full-bridge. The energy required to achieve ZVS of switches S_1 and S_2 is stored both in boost inductors $L_1 - L_3$ and the leakage inductance of the transformer. However since the inductance of these boost inductors is relatively large, ZVS can be achieved for S_1 and S_2 even at low power levels. Consequently the leakage inductance of the transformer can be minimized in order to reduce the losses in the transformer. On the other hand, the energy required to achieve ZVS for S_3 and S_4 is stored in output inductor L_o which is also large. Thus the ZVS range is extended compared to a conventional phase-shifted DC-DC full-bridge.

2.2. Single-stage rectifier with isolation

Figure 2.17: Circuit topology of the isolated single-stage TAIPEI rectifier.

As a result, this single-stage TAIPEI rectifier can shape sinusoidal phase currents with THD_I below 5% from full load down to 20% load, and efficiency between 94% and 95.5% from full load down to 40%.

Being a boost-type rectifier, the input phase inductors present DCM currents, thus an EMI filter is still needed, which potentially increases the system volume and weight compared to a conventional CCM boost-type rectifier (e.g. VIENNA Rectifier II).

Next, an Isolated Integrated Active Filter Matrix-type ($I^2\text{AFM}$) PFC rectifier was proposed in [45], and its circuit topology is drawn in Figure 2.18 [45]. This $I^2\text{AFM}$ rectifier consists of an uncontrolled hybrid rectifier with integrated active filter, and a ZVS phase-shifted DC-DC full-bridge converter. Since the AC-DC stage is uncontrolled, the v_{dc} after rectifier stage presents a six-fold voltage shape, thus for the DC-DC stage its duty cycle (i.e. phase-shift) is controlled in a reciprocal fashion so that DC voltage at the output is achieved.

Figure 2.18: Circuit topology of the Isolated Integrated Active Filter Matrix-type (I²AFM) PFC rectifier.

Here again the leakage inductance of the transformer is utilized to achieve ZVS for the DC-DC, which almost eliminates all switching losses and results in high overall efficiency. As a result, with a single DC-DC converter the system can reach 97% of efficiency at nominal load, while with two parallel interleaved DC-DC converters the overall efficiency can be improved up to 97.6%.

Under the ideology of matrix-type rectifier, a phase-modular isolated single-stage rectifier was proposed in [46, 47], denoted as IMY/ Δ -Rectifier with circuit diagram, shown in Figure 2.19 [46]. It features a phase-modular structure which greatly simplifies the control and reduces the cost and development time of the hardware. Besides, the MOSFETs in phase module only need to withstand phase voltage instead of line-to-line voltage, which opt for lower-voltage devices and consequently lower on-state resistance. With the merit of its full-bridge structure in each phase module, ZVS can be achieved with sufficient leakage inductance in the transformer. In terms of component counts, there are 12 controlled MOSFETs and always 6 semiconductor devices being conducting in the current path.

The calculated efficiency of this IMY/ Δ -Rectifier stays above 96% from full load down to 20% of load with different input voltages.

SWISS Rectifier was proposed in [48, 49], based on the existence of the three-phase 6-switch buck-type PFC rectifier. Later a single-stage with isolation Swiss-Forward topology was proposed in [50, 51], and its circuit diagram is depicted in Figure 2.20 [51]. The Swiss-Forward rectifier combines two Forward converters with resonant reset after the Swiss rectifier, one for the upper rail, one for the lower

2.2. Single-stage rectifier with isolation

Figure 2.19: Circuit topology of the three-phase phase-modular isolated matrix-type PFC Y/Δ-Rectifier (IMY/Δ-Rectifier).

Figure 2.20: Circuit topology of the SWISS-forward rectifier with resonant reset.

rail. The choice of forward converter as the high-frequency isolation, minimizes the use of switching devices since the forward switch on the primary is performed simultaneously by the upper/lower rail switch of the SWISS rectifier topology.

The measured efficiency of the Swiss-Forward rectifier prototype peaks 93.6% and it is obtained at maximum power. From one third up to the nominal power, the experimental results show a THD_I always below 4% and a close to unity power factor after PFC. This proposed topology is more suitable for applications with a tight input/output voltage range.

Proposed Rectifier Topology

In the previous chapter, conventional two-stage topologies and isolated single-stage topologies are listed and commented according to the state of the art. Since the single-stage solution tends to show relatively higher power density due to less component counts, and higher overall efficiency due to single-stage process of power, it is becoming more and more interesting on the industrial stage.

In this chapter, the proposed single-stage rectifier topology is introduced with its operating principle analyzed in section 3.1. Next, modulation method for the proposed rectifier and its representation in Space Vector Modulation (SVM) is discussed in section 3.2. One of the main advantageous features of the proposed rectifier is its Zero Voltage Switching (ZVS) capability, due to its unique bridge-leg structure. The detailed analysis of this feature is developed in section 3.3. Lastly, the difference between the proposed rectifier and its close variation VIENNA Rectifier III is thoroughly explained in section 3.4, being different in both phase-leg implementation and modulation sequence.

3.1 Operating principle

Figure 3.1 presents the proposed circuit topology of the three-phase single-stage isolated buck-type rectifier. The concept of this circuit combines the demanding of PWM sinusoidal input currents with a high-frequency transformer for single-stage isolation purpose. Since the circuit is a buck-derived topology, discontinuous PWM currents are presented at the input of the rectifier (i.e. $i_{rec,a}$, $i_{rec,b}$ and $i_{rec,c}$ in Figure 3.1). Hence an EMI filter is necessary to filter out the high frequency current components, being able comply with EMI standard meanwhile demanding a sinusoidal-shaped current at line frequency in phase with the three-phase source. Note that the first stage capacitors of the EMI filter C are not only essential for

Figure 3.1: Topology of the proposed three-phase single-stage isolated buck-type rectifier.

Figure 3.2: Sectors 1-12 of the mains phase voltage.

reaching certain EMI attenuation, but also fundamental to the rectifier functionality since they have to be placed very close to the switching stage, in order to provide high-frequency discontinuous currents with minimum paths.

The diode bridge $D_{N\pm}$ are low frequency diodes instead of high frequency ones, since they only conduct for the 120° -wide interval, where its phase voltage is at the maximum (for D_{N+}) or the minimum (for D_{N-}). To demonstrate the operating principle of the proposed rectifier, 12 sectors of the mains phase voltage are divided and shown in Figure 3.2. Thus by the functionality of $D_{N\pm}$, upper rail point P always presents the most positive voltage among the three phases, and likewise the most negative voltage at lower rail point N. Correspondingly the voltage u_{PN} exhibits a six-fold waveform in one line cycle, marked as the black solid curve in Figure 3.2.

3.1. Operating principle

Next, in Figure 3.1 if MOSFET S_{x1} , S_{x2} , S_{y1} and S_{y2} perform conventional phase-shifted full-bridge logic with u_{PN} supplied on the bridge legs, only the most positive and the most negative phase will have path to demand current from the source. However, the phase in the middle will not have path to conduct current, which accordingly cannot fulfill the ohmic behavior for each phase. Thus a bidirectional switching path is introduced by switching pairs S_{ya} S_{yb} , and S_{yc} . In Figure 3.1, the left one of the switching pair is denoted as S_{yN+} , and the right one as S_{yN-} . Thus, the functionality of the bidirectional switches S_{ya} S_{yb} S_{yc} have to be integrated into the functionality of the full-bridge switches, noting that the below listed two requirements have to be accomplished at the same time:

- Transformer volt-second balance,
- Ohmic behavior for each phase (under the condition of no reactive power handling).

Figure 3.3: Operating principle (shown in sector 1) of the proposed rectifier topology.

To demonstrate the operating principle of the proposed rectifier, sector 1 in Figure 3.2 (where $u_a > 0 > u_b > u_c$) is used for illustration. The main operating waveforms inside one switching cycle is depicted in Figure 3.3. u_{prim} depicts the voltage applied across the primary of the transformer. In each switching cycle, there are five operation states: three active states (marked as time intervals t_1 , t_2 and t_3) and two freewheeling states (each with time interval of $t_4/2$). States 1, 3 and 5 are active states where each phase current, averaged over one switching period, is proportional to its corresponding phase voltage, shown as $i_{rec,a}$, $i_{rec,b}$ and $i_{rec,c}$ in Figure 3.3. Also the driven signals for the switches S_{x1} , S_{x2} , S_{y1} , S_{y2} and the bidirectional switch S_{yb} are shown in Figure 3.3. Driven signals for S_{ya} and S_{yc} are not shown in Figure 3.3 because they are totally off in sector 1.

Furthermore, for explicit illustration, the current paths for above mentioned five operation states are depicted in Figure 3.4 a)-e) respectively. D_{a+} and D_{c-} are always forward biased in sector 1, which means that u_a is applied at point P and u_c at point N. Figure 3.4 a) is correspondent to the active state t_1 . Here S_{x1} and S_{yb} are on, thus the voltage $u_a - u_b$ is applied on the primary of the transformer. $i_{rec,a}$ shows a discrete positive current with dc level of $I_{dc} \frac{N_2}{N_1}$ (I_{dc} is the output dc inductor current which is assumed constant in one switching period). Meanwhile the current circulates back through the bidirectional switch to phase B as $i_{rec,b}$. Next in Figure 3.4 b) for the freewheeling time $t_4/2$, S_{yb} is off and S_{y1} is on, resulting to a zero voltage on the primary of the transformer. Thus no current is demanded from the mains and, meanwhile the transformer leakage current is freewheeling in the primary and output inductor current is freewheeling through the diode bridge on the secondary. In time interval t_2 , S_{x2} is on after S_{x1} is turned off, thus a negative voltage is applied on the primary of the transformer with the value of $-(u_a - u_c)$. Consequently, $i_{rec,a}$ presents again a positive current of $I_{dc} \frac{N_2}{N_1}$ while $i_{rec,c}$ shows a negative $-I_{dc} \frac{N_2}{N_1}$ correspondingly (see Figure 3.4 c)). At the beginning of the freewheeling time $t_4/2$, S_{y1} is turned off and then S_{y2} is turned on. Same like before, zero voltage applied on the primary of the transformer thus there is no direct power transfer between primary and secondary (see Figure 3.4 d)). Time interval t_3 is the last state in a switching period, where a reverse voltage of the one in interval t_2 is applied on the transformer, aiming at balancing the flux in the transformer over one switching period (see Figure 3.4 e)). Namely in the waveform of u_{prim} , the

3.2. Modulation method

integral area over time intervals t_1 and t_3 has to be equal to the area of t_2 . After time interval t_3 , starts again the active state t_1 of the next period.

3.2 Modulation method

The modulation method is the essence of the performance for the proposed rectifier topology. Following the operating principle shown in Figure 3.3, the key is to calculate the timing of each state, which accordingly defines the duty cycle and switching sequence of all the MOSFETs.

Since this topology is also a buck-type rectifier topology, the definition of modulation index M in [47] is still valid here. Thus, there is:

$$M = \frac{2}{3} \cdot \frac{N_1}{N_2} \cdot \frac{u_{out}}{\hat{U}_N} \quad (3.1)$$

where u_{out} represents the dc output voltage and $\hat{U}_N$ represents the amplitude of the input phase voltages.

First, to ensure the transformer volt-second balance, the magnetizing flux increment and decrement have to be equalized over one switching period. This implies that (e.g. in sector 1),

$$(u_a - u_b) \cdot t_1 + (u_a - u_c) \cdot t_3 = (u_a - u_c) \cdot t_2 \quad (3.2)$$

which derives

$$t_2 - t_3 = \frac{u_a - u_b}{u_a - u_c} \cdot t_1 \quad (3.3)$$

Besides, for the most negative phase C in this sector 1, according to the desired phase ohmic behavior, there is

$$t_2 + t_3 = \frac{M}{\hat{U}_N} \cdot |u_c| \cdot T_{sw} \quad (3.4)$$

Meanwhile to maintain ohmic behavior for phase in the middle (i.e. phase B in sector 1), there exists

Figure 3.4: Current paths of different operation states of the proposed rectifier.

3.2. Modulation method

$$t_1 = \frac{M}{\hat{U}_N} \cdot |u_b| \cdot T_{sw} \quad (3.5)$$

Combining equation 3.3 and 3.4, we can obtain

$$t_2 = \frac{1}{2} \left(\frac{M}{\hat{U}_N} \cdot |u_c| + \frac{u_a - u_b}{u_a - u_c} \cdot \frac{M}{\hat{U}_N} \cdot |u_b| \right) \cdot T_{sw} \quad (3.6)$$

and

$$t_3 = \frac{1}{2} \left(\frac{M}{\hat{U}_N} \cdot |u_c| - \frac{u_a - u_b}{u_a - u_c} \cdot \frac{M}{\hat{U}_N} \cdot |u_b| \right) \cdot T_{sw} \quad (3.7)$$

In the end, the total freewheeling time can be calculated as

$$t_4 = T_{sw} - t_1 - t_2 - t_3 \quad (3.8)$$

and each $t_4/2$ will be placed according to Figure 3.3.

Again, according to Figure 3.3, duty cycle for all the switches in sector 1 can be obtained:

$$d_{S_{yb}} = t_1/T_{sw} \quad (3.9)$$

$$d_{S_{y1}} = (t_2 + \frac{1}{2}t_4)/T_{sw} \quad (3.10)$$

$$d_{S_{y2}} = (t_3 + \frac{1}{2}t_4)/T_{sw} \quad (3.11)$$

$$d_{S_{x1}} = (t_1 + t_3 + \frac{1}{2}t_4)/T_{sw} \quad (3.12)$$

$$d_{S_{x2}} = (t_2 + \frac{1}{2}t_4)/T_{sw} \quad (3.13)$$

The above mentioned modulation method can also be represented in the form of Space Vector Modulation (SVM), modulating the current vector by the composition of different switching states. The three-phase sinusoidal mains voltage can be represented as

$$u_a = \hat{U}_N \cos \theta \quad (3.14)$$

$$u_b = \hat{U}_N \cos(\theta - \frac{2\pi}{3}) \quad (3.15)$$

$$u_c = \hat{U}_N \cos(\theta + \frac{2\pi}{3}) \quad (3.16)$$

where $\theta = \omega t$. According to the definition, the rectifier input voltage space vector

$$\vec{u}_r = \frac{3}{2}(u_a + u_b e^{j\frac{2\pi}{3}} + u_c e^{-j\frac{2\pi}{3}}) \quad (3.17)$$

Thus in the same manner, the rectifier input current space vector can be described as

$$\vec{i}_r = \frac{3}{2}(i_{rec,a} + i_{rec,b} e^{j\frac{2\pi}{3}} + i_{rec,c} e^{-j\frac{2\pi}{3}}) \quad (3.18)$$

In order to avoid the short circuit of input line-to-line voltages,

- out of bridge leg S_{y1} S_{y2} S_{yn} only one switch can be turned on in every instant,
- bridge leg S_{x1} and S_{x2} cannot be turned on at the same time.

Noting that the bidirectional switch S_{yn} represents the one of whose phase voltage in the middle of all three, i.e. here S_{yb} for sector 1.

Following the above mentioned rule, we name variable S_y to represent the states of bridge leg S_{y1} S_{y2} S_{yN} . When S_y is “1” it means S_{y1} is on; “0” means S_{yN} is on; “-1” means S_{y2} is on. Similarly for variable S_x , “1” means S_{x1} is on and “-1” means S_{x2} is on. Thus Table 3.1 concludes these available switching states and its corresponding current value in each phase, as well as the rectifier current space vector and voltage applied on the transformer primary side, under sector 1 and 2.

With the above mentioned available vectors of switching states, any rectifier current vector reference in sector 1 can be formed with the sequence illustrated earlier in Figure 3.3. Thus Figure 3.5 shows this vector composition forming a rectifier current vector $\vec{i}_{r,ref}$ in sector 1, with the three most nearby current vectors. It can be noticed that, even though vector (“1,-1”, $+u_{ac}$) and (“-1,1”, $-u_{ac}$) both

3.2. Modulation method

S_x	S_y	$i_{rec,a}$	$i_{rec,b}$	$i_{rec,c}$	$\vec{i}_r$	u_{prim}
1	0	$\frac{N_2}{N_1} I_{dc}$	$-\frac{N_2}{N_1} I_{dc}$	0	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{dc} e^{-j\frac{\pi}{6}}$	$+u_{ab}$
-1	1	$\frac{N_2}{N_1} I_{dc}$	0	$-\frac{N_2}{N_1} I_{dc}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{dc} e^{j\frac{\pi}{6}}$	$-u_{ac}$
1	-1	$\frac{N_2}{N_1} I_{dc}$	0	$-\frac{N_2}{N_1} I_{dc}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{dc} e^{j\frac{\pi}{6}}$	$+u_{ac}$
-1	0	0	$\frac{N_2}{N_1} I_{dc}$	$-\frac{N_2}{N_1} I_{dc}$	$\frac{2}{\sqrt{3}} \frac{N_2}{N_1} I_{dc} e^{j\frac{\pi}{2}}$	$-u_{bc}$
1	1	0	0	0	0 (Freewheeling)	0
-1	-1	0	0	0	0 (Freewheeling)	0

Table 3.1: Available switching states of bridge leg S_x S_y , as well as the rectifier input phase currents $i_{rec,a}$ $i_{rec,b}$ $i_{rec,c}$, rectifier input current space vector $\vec{i}_r$ and transformer primary voltage u_{prim} , for sectors 1 and 2.

show the same vector in space, they play opposite roles in balancing the transformer volt-second according to equation 3.2.

Figure 3.5: Space vectors of $\vec{i}_r$ corresponding to the switching states listed in Table 3.1 under sector 1 and 2, and the composed rectifier input current space vector $\vec{i}_{r,ref}$ while in sector 1.

3.3 Zero Voltage Switching (ZVS) feature

By the merit of the full-bridge architecture, the presence of leakage inductance in the transformer enables soft-switching for each switching transition, this almost eliminates all switching losses above certain load level [31]. However in this proposed topology, the functionality of bidirectional path is integrated into the full-bridge operation inside every switching period, thus all the bidirectional switching pairs (S_{ya} , S_{yb} and S_{yc}) can also realize ZVS.

Similar to a conventional phase-shifted full-bridge, for leading leg switches S_{y1} , S_{y2} and S_y , at the moment before each of their turn-on, the rectifier is always in an active state where the energy used to charge or discharge the output capacitance of the switches is the energy stored in the $L_{lk,1}$ plus the energy stored in the output filter inductor L_o . Since the energy in L_o is quite large compared to the energy needed to charge the output capacitance, it can be considered to charge as a constant current on MOSFET C_{oss} . And the charging current $I_{p,max}$ corresponds to the peak value of output inductor current ripple reflected to the primary, i.e:

$$I_{p,max} = I_{L,max} \cdot \frac{N_2}{N_1} \quad (3.19)$$

and the most strict moment to achieve ZVS regarding MOSFET u_{DS} is the moment when the maximum line-to-line voltage reaches its peak:

$$U_{DS,max} = \sqrt{3}\hat{U}_N \quad (3.20)$$

For a more precise analysis, the non-linear behavior of MOSFET C_{oss} should be considered. Thus the minimum deadtime applied on leading leg switches (t_{δ_1}) can be obtained by

$$2 \int_0^{U_{DS,max}} C_{oss}(u_{DS}) \cdot d(u_{DS}) = I_{p,max} \cdot t_{\delta_1} \quad (3.21)$$

The left part can be easily achieved by integrating the area below the provided C_{oss} - u_{DS} curve in MOSFET device datasheet.

On the other hand, the turn-on of the lagging leg switches S_{x1} , S_{x2} happens after a freewheeling state, which means that only the energy stored in the $L_{lk,1}$ is available for charging or discharging its C_{oss} . Then the energy stored in $L_{lk,1}$ has to comply

3.3. Zero Voltage Switching (ZVS) feature

$$E = \frac{1}{2} L_{lk,1} I_{p2}^2 = \int_0^{U_{DS,max}} C_{oss}(u_{DS}) \cdot d(u_{DS}^2) \quad (3.22)$$

where I_{p2} is the primary current at turn-on moment of the lagging leg switch which has

$$I_{p2} = (I_{L,max} - \frac{u_{out}}{L_o} \frac{t_4}{2}) \cdot \frac{N_2}{N_1} \quad (3.23)$$

Figure 3.6: ZVS details of one switching period in sector 1.

Thus, the resonance between $L_{lk,1}$ and C_{oss} provides a sinusoidal voltage rise across the switch to be turned on. Thus the deadtime for the lagging leg switches (t_{δ_2}) should be at one fourth of the resonant period

$$t_{\delta_2} = \frac{T_{res}}{4} = \frac{\pi}{2} \sqrt{L_{lk,1} C_{oss}} \quad (3.24)$$

However in practice, the deadtime needs to be adjusted experimentally [37] due to wide variation of the parasitics in the prototype, and the approximation of equation 3.21 and 3.24 gives only a fairly good initial estimation.

The simulation result using GeckoCIRCUITS [52], showing this ZVS behavior of one switching period in sector 1, is captured in Figure 3.6. Proper deadtime has been applied among the driven signals S_{y1} , S_{y2} , S_{x1} , S_{x2} , S_{yb+} and S_{yb-} . All the marked five switching instants (ZVS instant 1-5) can realize zero-voltage turn-on. Below is the analysis in details. Note that the $C_{oss} - u_{DS}$ characteristic of Infineon 650V CoolMOS Power Transistor IPW65R045C7 is utilized.

- ZVS instant 1

Right before ZVS instant 1, the rectifier is in active state where only S_{x1} and S_{y2} are on, a positive transformer primary current i_{prim} is flowing through both switches positively (see i_{Sx1} and i_{Sy2}). In this scenario, S_{yb+} is the one that is blocking the voltage between phase B and C. Thus S_{yb-} can be turn on a little bit before or even at the same time when S_{y2} is turned off. It can be seen in the shaded area indicating this instant, that S_{yb-} is turned on with zero-voltage. Once after S_{y2} is off, the this active state current which carries the energy of not only the leakage inductance but also the output dc inductor, will start to charge the C_{oss} of S_{y2} , thus the potential in node Y from Figure 3.1 will start to rise from the most negative phase (phase C in sector 1) and since S_{yb-} is on, which gives the current path and once this voltage at node Y reaches phase B voltage, the antiparallel diode of S_{yb+} will conduct and clamp the voltage. This is shown as u_{Syb+} dropping to zero in the shaded area. With a proper deadtime ensured, S_{yb+} is turned on with zero voltage.

- ZVS instant 2

For ZVS instants 2-5, the functionality is very similar to the ZVS behavior of Phase-Shifted Full-Bridge converter analyzed in [31]. When S_{yb+} and S_{yb-}

3.4. Derivation of the proposed topology: comparison with VIENNA Rectifier III

are turned off at the same time, the primary current continues to charge the C_{oss} of S_{y2} and discharge that of S_{y1} till node Y reaches voltage on point P (phase A voltage in sector 1), thus the antiparallel diode of S_{y1} will conduct and clamp the voltage. With a proper deadtime, S_{y1} can be turned on with zero-voltage. This is verified as $u_{S_{y1}}$ reaching zero before S_{y1} is turned on in the shaded area. From this instant on, the rectifier enters freewheeling mode through S_{y1} and S_{x1} .

- ZVS instant 3

For ZVS instant 3, S_{x1} turns off, and this freewheeling current (carrying only the energy of transformer leakage inductance) starts to charge the C_{oss} of S_{x1} and discharges that of S_{x2} . This makes voltage potential at node X drop till it reaches voltage at point N. Thus the antiparallel diode of S_{x2} will conduct and clamp the voltage. After a sufficient deadtime, S_{x2} can be turned on with zero-voltage. This is shown as $u_{S_{x2}}$ reaching zero before S_{x2} driven signal is on, highlighted in the shaded area of ZVS instant 3.

- ZVS instant 4

ZVS instant 4 is very close to the ZVS instant 2, only being different that the active current in this instant is the negative of instant 2, and charging and discharging of the C_{oss} of S_{y1} and S_{y2} swing the whole range of u_{PN} . The ZVS turn-on can be observed by curve $u_{S_{y2}}$ reaching zero before the driven signal of S_{y2} jumps high, highlighted in the shaded area of this instant.

- ZVS instant 5

This ZVS instant shows great resemblance to instant 3, only being different that the freewheeling current is negative. The zero-voltage turn-on is verified by the curve $u_{S_{x1}}$ being zero at the moment when S_{x1} turns on, highlighted in the shaded area.

3.4 Derivation of the proposed topology: comparison with VIENNA Rectifier III

The proposed topology has a close variation, which was mentioned before in section 2.2, and shown in previous Figure 2.15, known as VIENNA Rectifier III. It is

Chapter 3. Proposed Rectifier Topology

S_R	S_S	S_T	S_+	S_-	$i_{U,R}$	$i_{U,S}$	$i_{U,T}$	$\vec{i}_{U,j}$	$u_{T,1}$	$\text{sign}(u_{T,1})$
0	0	0	x	x	0	0	0	0	0	0
0	1	0	0	1	0	$+\frac{N_2}{N_1}I_o$	$-\frac{N_2}{N_1}I_o$	$\frac{2}{\sqrt{3}}\frac{N_2}{N_1}I_o e^{+j\frac{\pi}{2}}$	$+u_{N,ST}$	+
0	0	1	1	0	$+\frac{N_2}{N_1}I_o$	0	$-\frac{N_2}{N_1}I_o$	$\frac{2}{\sqrt{3}}\frac{N_2}{N_1}I_o e^{+j\frac{\pi}{6}}$	$-u_{N,RT}$	-
0	1	0	1	0	$+\frac{N_2}{N_1}I_o$	$-\frac{N_2}{N_1}I_o$	0	$\frac{2}{\sqrt{3}}\frac{N_2}{N_1}I_o e^{-j\frac{\pi}{6}}$	$-u_{N,RS}$	-
1	0	0	0	1	$+\frac{N_2}{N_1}I_o$	0	$-\frac{N_2}{N_1}I_o$	$\frac{2}{\sqrt{3}}\frac{N_2}{N_1}I_o e^{+j\frac{\pi}{6}}$	$+u_{N,RT}$	+

Table 3.2: Admissible switching states S_R , S_S and S_T of VIENNA Rectifier III and related switching states S_+ and S_- as well as the rectifier input phase currents $i_{U,i}$ $i_{rec,b}$ $i_{rec,c}$, rectifier input current space vectors $\vec{i}_{U,j}$, transformer primary voltage $u_{T,1}$, and $\text{sign}(u_{T,1})$ for sectors 1 and 2.

also a three-phase buck-type rectifier integrated with a high-frequency transformer to realize a single-stage AC-DC conversion. Besides, sinusoidal input currents are formed also using current SVM algorithm; symmetric transformer magnetization is guaranteed by pre-control signals. The comparison will be done in the following aspects:

1. Switching states and SVM

The available switching states of the two rectifiers are the same. Table 3.2 shows the available switching states of VIENNA Rectifier III, together with its input phase currents, input current space vector, and the transformer primary voltage. It can be seen that, in comparison with the proposed rectifier (see Table 3.1), the switching states and formed rectifier current vectors are the same. Explicitly, both rectifiers have four active switching states, out of which, two of them provide the same current vector but with opposite transformer polarization. Consequently, the space vector representation of VIENNA Rectifier III is depicted in Figure 3.7.

2. Transformer volt-second balance

Since both rectifiers can generate the same available current space vectors and the corresponding voltage applied on the transformer is the same under each switching state, the transformer volt-second balance follows the same rule. The only difference is that, as shown in Figure 3.3, there are only three active states in the proposed topology, while in VIENNA Rectifier III (see Figure 3.8) the two active states $+u_{RT}$ and $-u_{RS}$ are divided into half and placed symmetrically around the active state $-u_{RT}$. The advantage of the

3.4. Derivation of the proposed topology: comparison with VIENNA Rectifier III

Figure 3.7: Current space vectors of VIENNA rectifier III under sector 1 and 2 while formed rectifier input current in sector 1.

sequence for the proposed rectifier is that, it facilitates the ZVS feature in every switching transition for the merit of its integrated full-bridge structure (stated in section 3.3), while VIENNA Rectifier III cannot realize ZVS and has one more switching transition than the proposed one.

3. Number of semiconductor devices

VIENNA Rectifier III has only five MOSFETs which shows great simplicity in driving issues, while the proposed has 10 MOSFETs to drive. Nevertheless, from the conduction losses perspective, VIENNA Rectifier III has 6 semiconductor devices conducting in series on the current path in each active state, while the proposed one has only 4. This is further demonstrated in [53], that different realizations of phase-leg implementation, leads to different losses performance. Figure 3.9 in [53] provides four phase-leg implementation alternatives for VIENNA-type rectifier, where (c) represents the VIENNA Rectifier III implementation and (d) stands for the proposed rectifier. Moreover, in Figure 3.10, the losses distribution chart provided in [53], (d) clearly shows significant reduction in the diode conduction losses, and slightly less MOSFET switching losses.

Figure 3.8: Operating waveforms of VIENNA rectifier III for one switching period under sector 1.

Figure 3.9: Alternative phase-leg implementations of VIENNA-type rectifier.

Since phase-leg implementation (d) shows overall less losses compared to (c) which is the case utilized in VIENNA Rectifier III, a variation in the topology can be made while still following the symmetrical modulation method proposed in VIENNA

3.4. Derivation of the proposed topology: comparison with VIENNA Rectifier III

Figure 3.10: Loss distribution and comparison between three-phase active rectifier topologies.

Rectifier III. Figure 3.11 depicts the current path of all six operation states. It can be seen that ZVS cannot be achieved in all switching transitions.

Thus an asymmetrical modulation method can be implemented by rearranging the given states, in order to reach ZVS in all transitions. The current paths of different operation state of this proposed asymmetrical modulation sequence is depicted in Figure 3.12. In the beginning of a switching period, first the same two half states c) and e) in Figure 3.11 are combined together, then the freewheeling state f), next the active state a), followed by free-wheeling state b), in the end of the period the active state d). After this rearrangement of sequence, not only the freewheeling current is enabled to circulate in the primary side of the rectifier, but also the current direction prior to the MOSFET turn-on is favorable for achieving ZVS. This ZVS feature greatly improves the switching losses of the rectifier. Furthermore, only one switch will be turned on or off at each switching instant, instead of two turned on or off at the same time in the original VIENNA III Rectifier (see Figure 3.8 S_R S_S S_T S_+ S_- signals). This also simplifies the control logic complexity, which accordingly decreases the chance of system failure.

It is further worth noticing that, an auxiliary bridge leg can be connected between point P, N and Y, shown as shaded MOSFETs S_{y1} and S_{y2} in Figure 3.12 a) and b). This auxiliary leg can shorten the freewheeling path in Figure 3.12 b), making freewheeling current only circulate between S_{y1} and S_{x1} , in stead of going

Figure 3.11: Current paths of different operation states of VIENNA III Rectifier with improved phase-leg implementation, working under its original symmetrical modulation sequence.

3.4. Derivation of the proposed topology: comparison with VIENNA Rectifier III

Figure 3.12: Current paths of different operation states of VIENNA III Rectifier with improved phase-leg implementation, working under the proposed asymmetrical modulation sequence.

through S_{ya} , D_{a+} and S_{x1} . The same applied for Figure 3.12 d) that freewheeling current is flowing between S_{y2} and S_{x2} , in stead of through S_{yc} , D_{c-} and S_{x2} . This further decreases the conduction losses of the rectifier. Moreover, the existence of S_{y1} in active state c) of Figure 3.12 can connect phase A voltage to point B only turning on S_{y1} , taking advantage of the forward biased D_{a+} , in stead of driving two MOSFET pair S_{ya} . The same works for existence S_{y2} in active state e) of Figure 3.12. Thus, with the benefit of added leg S_{y1} and S_{y2} and the proposed asymmetrical modulation sequence, the rectifier is proposed in this thesis, having the topology shown in Figure 3.1), and current paths of different operation state inside one switching period shown as Figure 3.4.

Rectifier design

The previous chapter discussed the operating principle, modulation method and the important ZVS feature of the proposed rectifier topology. In this chapter, a design guideline of the proposed rectifier is provided, including the transformer design, EMI filter design, semiconductor device selection, output filter $L_o - C_o$ design, and the secondary side snubber circuit design. In the end of this chapter, a losses estimation is presented and simulation results are provided to validate the functionality of the proposed rectifier topology.

The application of the proposed rectifier topology is rooted in avionic utilities, and military standards MIL-STD-461F [54] and MIL-STD-704F [55] have to be complied. Thus in order to build a hardware demonstrator, the design specification and requirements are shown in Table 4.1 below.

Table 4.1: Design specifications and requirements for the hardware demonstrator of the proposed isolated single-stage three-phase rectifier

Parameter	Value
Galvanic Isolation	Yes
Input three-phase voltage	115 V _{rms} nominal (108-118 V _{rms})
Mains frequency	400 Hz nominal (393-407 Hz)
Power Factor	>0.85 (50% load-nominal load)
THD _I	≤ 5%
Switching frequency	100 kHz
Output voltage	270 V nominal
Output power rated	3.3 kW
Semiconductor voltage derating	65%
Electrolytic capacitors	Not allowed
Temperature derating	70%

4.1 Transformer design

The transformer is one of the most important components in the proposed topology. It offers galvanic isolation, and also the modulation of the rectifier is tightly connected to the presence of the transformer, as discussed in sections 3.1 and 3.2. Besides, based on the desired ZVS feature, the leakage inductance L_{lk} of the transformer has to be decided and integrated into the design of the transformer.

The waveforms of the transformer primary voltage and primary current inside one switching cycle of sector 1 can be found as u_{prim} and i_{prim} respectively in Figure 3.6. Even though in active state t_1 voltage stress on transformer is smaller compared to active states t_3 and t_5 , the maximum flux density $\hat{B}$ is defined when the primary voltage reaches peak value of the maximum line-to-line voltage, i.e. $\theta = \frac{n\pi}{6}$ ($n=1, 3, 5\dots$). This can be seen in Figure 4.24 which will be mentioned in future section 4.7 and its zoom-in in Figure 4.25. Also at these moments, active state time interval t_1 (see Figure 3.3) equals to zero since the average current demanded by the phase in the middle will be 0. Therefore, active state time interval t_3 and t_5 (also see Figure 3.3) will be equal. Thus the rectifier will work like a classical phase-shifted full-bridge DC-DC [31] which gives the maximum flux density:

$$\hat{B} = \frac{\sqrt{3}\hat{U}_N \cdot T_{sw}/2}{N_1 \cdot A_{core}} \quad (4.1)$$

where A_{core} represents the cross-sectional area of the chosen core.

Also based on equation 3.1, the turns ratio of the transformer can be represented as:

$$N_1/N_2 = \frac{3}{2} \cdot M \cdot \frac{\hat{U}_N}{u_{out}} \quad (4.2)$$

Usually the nominal modulation index for nominal output power is set no bigger than 0.9 to leave enough margin for the transient behavior [46] and also take into consideration of the duty cycle loss from applied duty cycle on the primary to the effective duty cycle on the secondary for full-bridge topology [31]. Finally the turns ratio is fixed at $N_1 : N_2 = 1:1.5$, with the modulation index for nominal condition $M_{nom}=0.8$.

4.1. Transformer design

Figure 4.1: Photo of the chosen transformer core PM87/70 with material N27 from EPCOS.

The transformer core selection is mainly influenced by the allowed space between the primary PCB assemble and the secondary PCB assemble. According to the 3D CAD design of the rectifier which will be shown later in Figure 5.2, as well as the easy availability in the laboratory, the space opts for an EPCOS PM87/70 core with material N27 (picture shown in Figure 4.1).

Next to achieve ZVS, sufficient leakage inductance $L_{lk,1}$ as discussed in section 3.3 can be achieved by adding layers of insulator (e.g. kapton tape) between primary and secondary windings. However this worsens the coupling between the primary and secondary, and thus increases the winding AC losses. Another option could be to build a transformer with good interleaving between primary and secondary, which helps decreasing winding AC losses in the transformer, but meanwhile inserting an external inductor in series with the transformer to realize ZVS. This external inductor in series with the transformer has to be designed apart and presents a high AC flux and a high AC RMS current that would penalize a lot the total losses.

Below a comparison of two different winding strategies is presented to see the effect on leakage inductance and AC winding resistance. The focus here is only on the transformer itself, that is to say, the external inductor for good interleaving case is not discussed here. To be accurate, separation of primary and secondary to

Figure 4.2: PEmag winding strategy design of the transformer with EPCOS PM87 N27 core, separation between primary and secondary windings to achieve desired leakage inductance.

achieve leakage inductance, is compared with good interleaving between primary and secondary. The winding strategies are both designed in PEmag from ANSYS [56], and the 2D FEA modeling in Maxwell (also from ANSYS) is provoked to calculate the leakage inductance and winding losses of each design. For both winding positioning strategies, the primary winding consists of 10 turns with solid wire of AWG 19 (ϕ 0.91 mm), 10 in parallel; and the secondary composes 15 turns with solid wire of AWG 19 also, 8 in parallel. Figure 4.2 presents the separated winding strategy, where yellow color stands for primary winding and red for the secondary. The blue color represents insulator layer of 6.5 mm horizontal width. Next, Figure 4.3 exhibits the winding strategy of good interleaving. After running 2D modeling, the obtained results regarding leakage inductance and AC winding resistance, both reflected on primary side, are concluded in Table 4.2.

It can be seen from Table 4.2 that, by separating primary and secondary windings, the desired leakage inductance can be easily integrated into the transformer at the cost of a bit worse AC winding resistance (132 m Ω vs 40 m Ω).

4.1. Transformer design

Figure 4.3: PEmag winding strategy design of the transformer with EPCOS PM87 N27 core, good interleaving between primary and secondary windings.

Meanwhile DC resistance for both winding strategies are similar since the number of turns and paralleled windings are exactly the same in both cases.

Thus, the selected option to construct the transformer for the proposed rectifier is to integrate the series inductance in the transformer since the required leakage inductance is small (around $3 \mu\text{H}$) having a sensible impact on the transformer performance.

Table 4.2: Comparison of the results obtained from 2D FEA modeling of the two different winding strategies in PEmag.

	Separated windings (Figure 4.2)	Interleaved windings (Figure 4.3)
$L_{lk,1}$ @ 100 kHz	$3.6 \mu\text{H}$	280 nH
$R_{AC,1}$ @ 100 kHz	132 m Ω	40 m Ω

Figure 4.4: Impedance analyzer measurement of the finished transformer primary side with secondary winding short-circuited, equivalent circuit $L_s - R_s$.

Besides, since this is a high-frequency transformer which the current through windings exhibits mainly switching-frequency harmonic content, Litz wire is preferred instead of solid wire for the sake of minimizing the winding losses from skin effect. The constructed transformer winding strategy is thus similar to Figure 4.2, having a 6.5mm isolation distance between primary and secondary. The primary winding consists of 10 turns of Litz wire (200 strands $\times \phi$ 0.07 mm), 10 in parallel. Afterwards a 6.5 mm thick layer of kapton isolation tape is wrapped to fix the primary winding in position but also provide separation from secondary. The secondary winding consists of 15 turns of Litz wire (200 strands $\times \phi$ 0.07 mm), 4 in parallel. It is worth noticing that there is no air gap needed since the transformer provides direct energy transfer in active states and no energy transfer in freewheeling states.

Upon finishing, the transformer is measured by Agilent 4294A precision impedance analyzer [57]. Figure 4.4 shows the impedance measurement of the transformer primary side with the secondary winding short-circuited. In this equivalent circuit model $L_s - R_s$, L_s at 100 kHz represents the leakage inductance value reflected on the primary $L_{lk,1}$, which shows 2.8 μ H. And R_s at 100 kHz suggests the AC winding resistance reflected on the primary $R_{AC,1}$, which equals to 49.7 m Ω . Figure 4.5 measures the impedance of the primary side while the secondary is open, in this equivalent circuit model $L_s - R_s$. L_s at 100 kHz represents

4.1. Transformer design

Figure 4.5: Impedance analyzer measurement of the finished transformer primary side with secondary winding open, equivalent circuit $L_s - R_s$.

Figure 4.6: Impedance analyzer measurement of the finished transformer primary side with secondary winding open, measuring $|Z| - \theta$.

Table 4.3: Losses estimation of the finished transformer

Core losses	3.7 W
AC winding losses	14.3 W
Total	18 W

the magnetizing inductance at the primary side $L_{mag,1}$, which equals to 1.2 mH. Furthermore, Figure 4.6 measures the same thing, shown in impedance and phase mode. The resonance at 225 kHz is due to the winding capacitance $C_{trafo,1}$, which is calculated as 510 pF.

It is worth noticing that $L_{lk,1}$ value is essential to the ZVS behavior analyzed in section 3.3. While on the other hand, the value of leakage inductance and winding capacitance reflected on the secondary, i.e. $L_{lk,2}$ and $C_{trafo,2}$, are of importance to the ringing effect on the secondary diode bridge, which will be discussed in details in section 4.5.

Since the proposed topology features the positive-negative balanced flux in the transformer, the current in the primary of the transformer has a trapezoidal waveform (see Figure 3.6). It can be seen that, the primary and secondary currents have very small DC bias values, which makes its DC winding losses negligible. Thus its switching-frequency (100 kHz) harmonic component contributes most to the AC winding losses. In the end, the losses calculation of the finished transformer is provided in Table 4.3, mainly considering core losses and AC winding losses at 100 kHz.

4.2 EMI filter design

As presented in Figure 3.3, the input phase currents of the proposed rectifier present pulsating waveforms, thus an adequate EMI filter is necessary to filter this pulsating currents into sinusoidal currents demanded from the three-phase source. Since this rectifier is based on aircraft application, the EMC standard to comply is the military standard MIL-STD-461F. This imposes more difficulty in input filter design compared to CISPR Class A and B [58] in industrial application. In CISPR Class A and B, the EMI spectrum has limit in the range of 150 kHz-30 MHz, thus the

4.2. EMI filter design

Figure 4.7: CE102 limit of the EMC standard MIL-STD-461F for the rectifier to comply.

switching frequency can be chosen below 150 kHz with the grid frequency being 50/60 Hz so that the current spectral component at switching frequency (or even the first several harmonics of switching frequency) does not have to be considered for the input filter design [46]. However, in MIL-STD-461F, the limit starts from 10 kHz (see Figure 4.8) which is much smaller compared to the starting frequency of CISPR Class A and B, meanwhile being closer to the mains frequency (400 Hz). Therefore, the switching frequency has to be placed inside the MIL-STD-461F frequency range and moreover, the EMI filter has to be designed to attenuate the very first harmonic of switching frequency.

Furthermore, in general buck-type rectifiers feature pulsating input current. Meanwhile boost-type rectifiers due to their necessary input line inductors, present input current waveforms at mains-frequency with small high-frequency ripples. Thus, the proposed rectifier topology, being in the category of buck-type rectifiers, requires higher EMI filtering effort. This is intrinsically a disadvantage of the proposed rectifier. Shown in Figure 4.9, a two-stage filter with $R-L_d$ series damping [59] is employed, noting that the first stage filter capacitors C_1 have to be placed close to the rectifier switching stage in order to maintain a low commutation inductance

Figure 4.8: Simulation result of input phase current spectrum with LISN (complying with the MIL-STD-461F standard).

Figure 4.9: Circuit diagram of the two-stage input EMI filter for the proposed rectifier topology.

[46]. The designed EMI filter has components values as following: $L_1=L_2=270 \mu\text{H}$, $C_1=1.5 \mu\text{F}$, $C_2=1 \mu\text{F}$, $L_{d1}=L_{d2}=50 \mu\text{H}$, $R_{d1}=R_{d2}=5 \Omega$.

The attenuation Bode diagram of the designed EMI filter is simulated in PSIM [60], and the result is shown in Figure 4.10. It is clear that the rectifier current harmonic at switching frequency is attenuated 103 dB, while the mains fundamental harmonic is not amplified. It is also worth noticing that there are two damped resonant peaks at the range of 2 kHz-8 kHz, which can amplify the low frequency harmonics (i.e. mainly 5th-10th harmonics). However this is inevitable since for this aircraft application the mains frequency is fixed at 400 Hz while the 100 kHz switching frequency harmonic has to be sufficiently attenuated to comply with

4.2. EMI filter design

Figure 4.10: Simulation result of the attenuation Bode diagram of the designed EMI filter.

Figure 4.11: Simulation result of the mains Power Factor of the rectifier with designed EMI filter, under different load conditions.

the MIL-STD-461F standard. Thus the resonance of the two-stage EMI filter has to stay inside this range, i.e. beyond 400 Hz but adequately damped, and sufficiently below 100 kHz so that enough attenuation can be assured. Furthermore, optimal damping can be applied to minimize the influence of this unwanted low-frequency amplifications, compromising the losses in the damping network [59]. Meanwhile, from the point of view of the rectifier operation, factors such as unbalance between positive and negative half mains cycle, cross-sector distortion, should also be minimized so that finally the mains side will not see big harmonic contents on these frequencies before the EMI filtering.

Since the rectifier is emulating a resistive behavior, the power factor at the mains side can be obtained by sweeping different load conditions (i.e. different emulated resistor values) from 330 W (10% of nominal load) to 3.3 kW (nominal load), also in PSIM. Figure 4.11 presents the curve of the PF regarding different load conditions. At full load, the PF shows a desirable value of 0.999. Besides, from 30% load up to full load, the PF stays always above 0.95. According to the standard MIL-STD-704F, the power factor of AC equipment greater than 500 VA shall be between 0.85 lagging and unity when operating at 50% or more of its rated load current in steady state condition [55]. It can be seen that the power factor performance of the designed rectifier complies MIL-STD-704F totally.

4.3 Semiconductor device selection

The transistors in this topology can be classified into two groups: those switching at high frequency (i.e. switching frequency), and those switching at an equivalently intermediate frequency between mains frequency and switching frequency. The full-bridge switches (S_{y1} , S_{y2} , S_{x1} and S_{x2}) are always switching at switching frequency, and the bidirectional switching pairs (S_{ya} , S_{yb} and S_{yc}) are only switching during the sectors where its corresponding phase voltage has the minimum absolute value.

4.3.1 MOSFETs S_{y1} , S_{y2} , S_{x1} and S_{x2}

The voltage stress on the full-bridge switches has an envelope of maximal line to line voltage, which gives peak voltage stress:

4.3. Semiconductor device selection

$$\hat{u}_{S_{y1/y2/x1/x2}} = \sqrt{3} \cdot \hat{U}_N \quad (4.3)$$

Regarding the current stress, the behavior of the two legs (leg S_{y1} - S_{y2} , leg S_{x1} - S_{x2}) are not exactly the same because: S_{x1} and S_{x2} are always conducting current in a complementary manner inside each switching cycle; while S_{y1} and S_{y2} are not, since S_{y1} S_{y2} together with one of the bidirectional switching pairs S_{yN} , all three of them are conducting current alternatively inside every switching cycle. Moreover, this current stress on the semiconductors depends on modulation index M , output inductor current I_{dc} and the turns-ratio of the transformer N_2/N_1 .

Thus, the RMS current through the switches S_{y1} and S_{y2} are derived:

$$I_{S_{y1/y2},RMS} = \sqrt{\frac{3}{\pi}(0.5236 - 0.134M)} \cdot \frac{N_2}{N_1} I_{dc} \quad (4.4)$$

Since S_{x1} and S_{x2} are alternatively sharing the current $\frac{N_2}{N_1} I_{dc}$ inside every switching cycle, also its on-time is symmetrical during every 30°-sector, which yields to the RMS currents of S_{x1} and S_{x2} :

$$I_{S_{x1/x2},RMS} = \frac{\sqrt{2}}{2} \cdot \frac{N_2}{N_1} I_{dc} \quad (4.5)$$

According to the values at nominal load, there are $I_{S_{y1/y2},RMS} = 11.54$ A and $I_{S_{x1/x2},RMS} = 12.94$ A. Infineon IPW65R045C7 MOSFET (650 V CoolMOS C7 series) is employed for switches $S_{x1/x2/y1/y2}$, and according to its datasheet, a typical $R_{DS,on} = 0.06 \Omega$ (at junction temperature of 125°C) can be expected. Thus total conduction losses on MOSFETs $S_{y1/y2}$ can be estimated as $P_{TotalLosses,S_{y1/y2}} = I_{S_{y1/y2},RMS}^2 \cdot R_{DS,on} \cdot 2 = 16$ W. And likewise for $S_{x1/x2}$, there is $P_{TotalLosses,S_{x1/x2}} = I_{S_{x1/x2},RMS}^2 \cdot R_{DS,on} \cdot 2 = 20.1$ W.

4.3.2 MOSFETs S_{ya} , S_{yb} and S_{yc}

The highest voltage stress on the bidirectional switching pairs occurs at the moment when one phase voltage reaches its maximum amplitude and the other two are equal to negative half of the maximum amplitude, resulting in:

$$\hat{u}_{S_{yN}} = \sqrt{3} \cdot \hat{U}_N \quad (4.6)$$

Regarding the current stress, as discussed in 4.3.1, S_{yN} together with S_{y1} S_{y2} are conducting current alternatively inside every switching cycle. Thus the RMS current through the bidirectional switching pairs over one mains period are derived respectively:

$$I_{S_{yN},RMS} = \sqrt{\frac{(2 - \sqrt{3})M}{2\pi}} \cdot \frac{N_2}{N_1} I_{dc} \quad (4.7)$$

According to the values at nominal load, there exists $I_{S_{yN},RMS} = 3.38$ A. Infineon IPW65R037C6 MOSFET (650 V CoolMOS C6 series) is employed for all six switches of S_{yN} , and according to its datasheet, a typical $R_{DS,on} = 0.05 \, \Omega$ (at junction temperature of 125°C) can be assumed. Thus total conduction losses on MOSFETs S_{ya} , S_{yb} and S_{yc} can be estimated as $P_{TotalLosses,S_{yN}} = I_{S_{yN},RMS}^2 \cdot R_{DS,on} \cdot 6 = 3.4$ W.

4.3.3 Input diode bridge $D_{N\pm}$

The three-phase diode bridge D_{N+} and D_{N-} are low frequency devices which switch at three times of the mains frequency. The voltage stress on the three-phase diode rectifier is equal to the maximal line-to-line input voltage, which leads to the highest voltage stress:

$$\hat{u}_{D_{N\pm}} = \sqrt{3} \cdot \hat{U}_N \quad (4.8)$$

Regarding the current stress, the average and RMS currents through the three-phase diode bridge are respectively given by:

$$I_{D_{N\pm},avg} = \frac{\sqrt{3}M}{2\pi} \cdot \frac{N_2}{N_1} I_{dc} \quad (4.9)$$

$$I_{D_{N\pm},RMS} = \sqrt{\frac{\sqrt{3}M}{2\pi}} \cdot \frac{N_2}{N_1} I_{dc} \quad (4.10)$$

According to the values at nominal load, there are $I_{D_{N\pm},avg} = 4.03$ A and $I_{D_{N\pm},RMS} = 8.6$ A. The device chosen for the input diode bridge is STTH30R04 ultrafast recovery diode from ST Microelectronics (will be listed in future Table 4.6). According to its datasheet, a typical value for evaluating the diode conduction losses

4.3. Semiconductor device selection

can be $V_F = 0.8$ V and $R_D = 0.00625$ Ω . Thus conduction losses in each diode can be derived as

$$P_{Losses, D_{N\pm}} = I_{D_{N\pm}, avg} \cdot V_F + I_{D_{N\pm}, RMS}^2 \cdot R_D \quad (4.11)$$

Since they are ultrafast recovery diodes, the reverse recovery losses can be ignored. Thus for all the six diodes in the three-phase bridge, a total losses of $P_{TotalLosses, D_{N\pm}} = 3.69$ W x 6 = 22.1 W can be expected.

4.3.4 Output diodes D_{1-4}

The output diode rectifier is working at switching frequency, and its voltage stress corresponds to the voltage stress in the low frequency input diodes multiplied by the turns-ratio of the transformer, which is,

$$\hat{u}_{D_{1-4}} = \frac{N_2}{N_1} \cdot \sqrt{3} \cdot \hat{U}_N \quad (4.12)$$

However in reality, voltage ringing on the output diode rectifier will be observed due to the interaction of the presented leakage inductance of the transformer together with the parasitic capacitance of these diodes in the output rectifier. This will cause the blocking voltage of the diodes to be higher than this ideal level. This part will be further discussed in the following section 4.5. In conclusion, certain voltage margin has to be given to this ideal voltage level while choosing devices, depends on whether with snubber or not and furthermore which type of snubber will be implemented.

The rectifier diode chosen in this design is CREE 1200 V/43 A C4D30120D SiC Schottky diode. This 1200 V voltage rating is adequate for the ringing case without snubber. However two snubber solutions will also be designed and implemented in the prototype test.

The current stress through the output diode rectifier is derived as below:

$$I_{D_{1-4}, avg} = \frac{1}{2} \cdot I_{dc} \quad (4.13)$$

$$I_{D_{1-4}, RMS} = \frac{\sqrt{2}}{2} \cdot I_{dc} \quad (4.14)$$

According to the values at nominal load, there are $I_{D1-4,avg} = 6.1$ A and $I_{D1-4,RMS} = 8.63$ A. C4D30120D SiC Schottky Diode from CREE (will be listed in future Table 4.6) is chosen as output diode on the secondary. According to its datasheet, a typical value for evaluating the diode conduction losses can be $V_F = 1$ V and $R_D = 0.025 \Omega$. Thus conduction losses in each output diode can be derived as

$$P_{Losses,D1-4} = I_{D1-4,avg} \cdot V_F + I_{D1-4,RMS}^2 \cdot R_D \quad (4.15)$$

Since it is SiC Schottky diode, the reverse recovery losses can be ignored. Thus for all the six diodes in the three-phase bridge, a total losses of $P_{TotalLosses,D1-4} = 7.96$ W x 4 = 31.8 W can be expected.

4.4 Output inductor L_o design

Since the proposed topology is derived from buck-type rectifier, which is also known as Current-Source rectifier, an output dc inductor is necessary to suppress and maintain the dc output current. Meanwhile this output inductor current also defines the dc level of the pulsating current that each phase is demanding from the closest stage of EMI capacitors (see $i_{rec,a/b/c}$ from Figure 3.3).

Output filter $L_o - C_o$ can be designed based on dc inductor current ripple and output voltage ripple values. The inductor current waveform at nominal load can be seen from former mentioned Figure 4.24. Assuming that the output voltage (u_{out}) ripple is negligible across C_o , the maximum inductor current ripple happens at moments $\theta = \frac{n\pi}{6}$ (n=1, 3, 5...). where the phase in the middle is crossing zero thus no current is demanded from the bidirectional path, which gives the maximum inductor current ripple value:

$$\Delta i_{L,pp,max} = \frac{u_{out} \cdot (1 - \frac{\sqrt{3}}{2}M)}{2 \cdot f_{sw} \cdot L_o} = \frac{3M\hat{U}_N}{4L_o f_{sw}} \frac{N_2}{N_1} (1 - \frac{\sqrt{3}}{2}M) \quad (4.16)$$

According to empirical data, the dc inductor ripple is usually fixed to be 20% of the average current value I_L . Here

$$I_{L,nom} = I_{o,nom} = \frac{P_{o,nom}}{U_{o,nom}} = 12.2A \quad (4.17)$$

4.4. Output inductor L_o design

Figure 4.12: PExprt calculation result of the output 100 μ H inductor on EPCOS ETD54 N97 core.

and we have $f_{sw} = 100$ kHz, modulation index for nominal condition $M_{nom} = 0.8$, and also $N_2 : N_1 = 1.5:1$ fixed from transformer design in section 4.1. Thus we can derive the needed value of L_o in order to suppress the maximum inductor current ripple into 20% of its dc value:

$$L_o = 200\mu H \quad (4.18)$$

For the sake of providing even impedance for the common mode noise coming from the secondary switching stage to the dc output, this L_o is better to be split evenly into two inductors and placed on the upper output rail and lower output rail respectively.

The inductor core selection is primarily influenced by the allowed space in the prototype and easy availability from the distributor, since a box-shaped prototype is intended to maximize the power density. Consequently, according to the 3D CAD design of the rectifier later will be shown in Figure 5.2, the space below the secondary

Figure 4.13: PEXprt constructive result of the chosen $100\ \mu\text{H}$ inductor on EPCOS ETD54 N97 core.

heatsink and output capacitors of the secondary stage can be utilized to place these two inductors. As a result, EPCOS ETD54/28/19 ferrite core is deployed in the design for each $100\ \mu\text{H}$ inductor. As for the material, N27, N87 and N97 are all available, however N97 exhibits the least core losses and most proper for $100\ \text{kHz}$ operation range according to the datasheet of ETD54/28/19 core. As a result, the design of the inductor is mainly focused on the winding design on EPCOS ETD54 core with N97 material.

ANSYS PEXprt is used to calculate the optimal combination of different wire diameter, number of turns and paralleled windings. Figure 4.12 lists the best 10 calculation results considering solid copper wire diameter AWG17-20, maximum 10 windings in parallel.

4.4. Output inductor L_o design

Figure 4.14: PExprt losses calculation of the chosen 100 μ H inductor on EPCOS ETD54 N97 core.

It can be seen that first two options both show least and very similar losses, as well as a durable window filling factor, only being different that one is 8 of AWG18 ($\phi=1$ mm) in parallel, while the other is 10 of AWG19 ($\phi=0.9$ mm) in parallel. The number of turns is 19, and the air gap is 1.52 mm. Based on the easy availability of the solid copper wire in the laboratory, the winding strategy of 10 paralleled ϕ 0.9 mm copper wire is utilized. Figure 4.13 shows the construction details of each 100 μ H inductor, and the image depicts the vertical cross-sectional view of a symmetrically mirrored half of the inductor, with gap in the central leg.

The losses calculation of the selected inductor is obtained by calling Finite Elements Analysis (FEA) run in PEmag (also from ANSYS). The losses distribution is presented in Figure 4.14. It is clear that the losses are mainly winding losses (2.5 W), taking up 95.7% of the total losses. Besides, the core losses are only 112.5 mW.

Due to the selected winding strategy, the window area is fully occupied, thus the current density in the winding shows a favorable value of 1.88 A/mm².

In the classical approach, the coil former coming in a set with the ungapped core is usually used, and sheets of paper are put in between the two half cores in order to reach the desired gap length. However with the increasing popularity of affordable 3D printers, the bobbin for this inductor is printed by BQ Witbox 3D printer [61] with plastic filament. The height of the printed bobbin includes the desired air gap length in order to fully utilize the window area for winding.

4.5 Secondary ringing effect and snubber circuit

The ringing across the diode rectifier on the secondary side is caused by the leakage inductance of the transformer, winding parasitic capacitance and the parasitic capacitance of the diode.

This ringing occurs when the secondary voltage rises and diode rectifier is getting into one diagonal pair reverse biased while the other diagonal pair keeps forward biased, after a freewheeling state. The leakage inductance rings together with the winding parasitic capacitance and the diode parasitic capacitance, which gives the ringing frequency:

$$f_{ring} = \frac{1}{2\pi\sqrt{L_{lk,2} \cdot (C_{trafo,2} + C_d)}} \quad (4.19)$$

where $L_{lk,2}$ is the leakage inductance of the transformer reflected at the secondary, $C_{trafo,2}$ is the winding parasitic capacitance on the secondary, and C_d is the parasitic capacitance of the rectifier diode.

Since sufficient $L_{lk,2}$ is needed to achieve ZVS behavior, in order to minimize the ringing losses, fast-recovery Schottky diode is preferable due to its smaller parasitic capacitance value.

Figure 4.15 shows the simulation of this phenomenon. It is worth noticing that normally this ringing can produce 2-3 times higher voltage peak than the voltage applied to the secondary, which accordingly requires a higher voltage rating diode. Besides, the excessive ringing can also cause EMI problems and even control failures.

Thus, the ringing is better to be snubbed, the simplest option is to parallel an RC snubber closely to each rectifier diode, but this would introduce large losses

4.5. Secondary ringing effect and snubber circuit

Figure 4.15: Simulation result of the ringing effect on the secondary side of a phase-shifted full-bridge DC-DC without snubber, at nominal power.

since the ringing energy is dissipated on R and the same in all four positions of the rectifier diode. Furthermore, because of the necessity of a sufficiently large leakage inductance integrated in the transformer for reaching ZVS on the primary side, the ringing frequency is lower which makes the use of RC snubber bulky and impractical. In this case, a less lossy snubber that can return part the ringing energy back to the output would be preferable.

Figure 4.16: Passive snubber circuit applied on the secondary.

Figure 4.17: Active snubber circuit applied on the secondary.

In [31], a passive snubber was presented, shown in Figure 4.16 [31], to clamp the maximum peak voltage (i.e. the first ringing peak), and return part of the energy to the output. While the ringing occurs, the ringing energy is transferred through diode D_c to capacitor C_c , thus the first ringing peak is snubbed and clamped to the DC voltage value on C_c . Afterwards, C_c is discharged slowly through R_c to the output.

Another solution proposed in [62], features an active snubber, shown in Figure 4.17 [62]. It is composed of a high-voltage low-power MOSFET Q_s in series with a relatively big high-voltage capacitor C_s , which is paralleled to the secondary rectifier. When the secondary voltage starts to build up, i.e. the ringing is about to occur, Q_s is turned on so that C_s is paralleled to fix the secondary voltage. Afterwards, when the secondary side gets into freewheeling state from active power

4.5. Secondary ringing effect and snubber circuit

transfer state, Q_s is turned off so that C_s is disconnected. This solution not only limits the overshoot of the rectifier voltage, but also eliminates the ringing in a non-dissipative manner. This increases the overall efficiency of the converter, which makes this snubber more suitable in high-voltage high-power applications.

In the following sections 4.5.1 and 4.5.2, the design guideline of these two snubbers together with simulation results are presented.

4.5.1 Passive snubber design

The idea of the clamping circuit is to balance the charge in the clamping capacitor C_c . In Figure 4.16 there is only one output inductor on the upper rail, while in our proposed converter, for the purpose of providing symmetrical impedances for rejecting common mode noise [30], the output inductor is split evenly into both upper and lower rail. Thus, this passive snubber structure needs to be duplicated for the lower rail also. This makes the final passive snubber circuit as Figure 4.18.

Noticing that the intermediate point between two snubber capacitors needs to have a fixed middle potential to ensure charge balance in two capacitors, thus this middle point is connected to a split capacitor pairs, whose middle point potential is ensured by same resistance R5 and R6 as shown in Figure 4.18.

Simulation results of DC-DC operation at nominal power is depicted in Figure 4.19. One can see that the first ringing peak is snubbed to 460 V (u_{sec}) instead of the unsnubbed ringing peak of 800 V in Figure 4.15. Besides, after the

Figure 4.18: Improved passive snubber circuit applied on secondary side.

Figure 4.19: Simulation result of the improved passive snubber circuit applied on the secondary side, working as phase-shifted full-bridge DC-DC at nominal power.

Table 4.4: List of components employed in the passive snubber implementation

Component	Description
Snubber diodes $D_c \times 2$	Multicomp ES3J 600 V/30 A ultrafast diode
Snubber capacitors $C_c \times 2$	KEMET 1000 V 47 nF multilayer capacitor (C2220C473KDRACTUC2220C473)
Snubber resistors $R_c \times 2$	Caddock TO220 30 W 1 k Ω power resistor (MP930-1k-1%)
Snubber split resistors $R_{split} \times 2$	Multicomp 300 k Ω 500 V SM2512 thick film resistor (MCPWR12FTEA3003)
Snubber split capacitors $C_{split} \times 2$	WIMA 250 V 1 μ F film capacitor (MKS4F041004F00JSSD)

first peak, the rest of the ringing is also more damped compared to the case without snubber in Figure 4.15.

4.5. Secondary ringing effect and snubber circuit

Figure 4.20: Active snubber circuit applied on the secondary side.

To conclude this part, Table 4.4 lists the components employed for this passive snubber installation.

4.5.2 Active snubber design

The active snubber is applied on the rectifier secondary as shown in Figure 4.20. Note that MOSFET Q_s source is connected to the capacitor C_s , to take advantage of the anti-parasitic diode. When the secondary voltage finishes building up, C_s is being charged thus firstly the anti-parasitic diode will naturally conduct. Within a short delay, Q_s is turned on to ensure less conduction losses, meanwhile benefiting from ZVS. Simulation results of DC-DC operation at nominal power is depicted in Figure 4.21.

The duty cycle difference between primary voltage and secondary voltage, D_{diff} , is the time between the turn-on of lagging-leg switch (MOSFET S_{x1} or S_{x2}) and the moment when secondary voltage builds up to $V_{in} \frac{N_2}{N_1}$. This D_{diff} time is the minimum delay that Q_s needs regarding the turn-on of S_{x1} or S_{x2} . The slope of the primary current rising during this time is $\frac{V_{in}}{L_{lk}}$.

In the end, Table 4.5 lists the components employed for this active snubber installation.

Figure 4.21: Simulation result of the active snubber circuit applied on the secondary side, working as phase-shifted full-bridge DC-DC at nominal power.

Table 4.5: List of components employed in the active snubber implementation

Component	Description
Snubber capacitor C_s	WIMA 600 V 20 μ F Film Capacitors (DCP4I052006JD2KSSD)
Snubber MOSFET Q_s	ST Microelectronics 600 V 10 A TO220 MOSFET (STP11NM60ND)

4.6 Losses estimation

In order to validate the concept of proposed rectifier topology, the design guideline of a 3.3 kW rectifier including EMI filter has been thoroughly discussed in this chapter. A list of the main components is provided in Table 4.6. And the corresponding distribution of losses estimation, at 3.3 kW nominal power, is listed in Figure 4.22. In this losses estimation, the losses considered are:

- EMI Filter
Inductor losses of differential inductors L_1 and L_2 , damping inductors L_{d1} and L_{d2} , damping resistor losses of R_{d1} and R_{d2} , for all three phases. Capacitor losses are neglected.
- Input Diodes
 $D_{N\pm}$ conduction losses only. Since the chosen devices are ultra fast recovery diodes, the reverse recovery losses are neglected.
- MOSFETs
Conduction losses of S_{ya} S_{yb} S_{yc} , S_{y1} and S_{y2} , S_{x1} and S_{x2} respectively. Since all the switches can achieve ZVS, switching losses are not considered.
- Transformer
Core losses and AC winding losses.
- Output Diodes
 D_{1-4} conduction losses only. Since the output diodes are all SiC Schottky diodes, reverse recovery losses neglected.
- Output Inductors
Two dc output inductors core losses and winding losses.

In the end, this estimation shows an overall efficiency of 95.7%, which is moderate compared to the state-of-the-art rectifier topologies with isolation [39, 45, 46, 51]. This is due to the stricter military EMI standard and also the harsh semiconductor voltage and temperature derating applied according to Table 4.1.

Table 4.6: List of the main components employed in the prototype of the proposed isolated single-stage three-phase buck-type rectifier.

Component	Description
$L_1=L_2=270 \mu\text{H}$	MAGNETICS toroid powder core 58083, N=60, solid copper wire of 1.5 mm diameter
$C_1=3 \times 0.47 \mu\text{F}$	EPCOS $0.47\mu\text{F}$ B32923 (305 Vac) EMI suppression film capacitor
$C_2=3 \times 0.33 \mu\text{F}$	EPCOS $0.33\mu\text{F}$ B32923 (305 Vac) EMI suppression film capacitor
$L_{d1}=L_{d2}=55 \mu\text{H}$	MAGNETICS toroid powder core 58548, N=20, solid copper wire of 1.5 mm diameter
$R_{d1}=R_{d2}=5 \Omega$	OHMITE 45F5R0E (5W) silicone-ceramic conformal axial terminal wirewound resistor
Input diodes $D_{N\pm}$	ST Microelectronics 400 V/30 A STTH30R04 ultra fast recovery diode
Bidirectional switches $S_{ya/b/c}$	Infineon 650 V CoolMOS C6 series (IPW65R037C6)
Full-bridge switches $S_{x1/x2/y1/y2}$	Infineon 650 V CoolMOS C7 series (IPW65R045C7)
Primary heatsink	Fischer Elektronik LA-6 Cooling aggregates with axial fan
Transformer	EPCOS ferrite core PM87 material N27, $N_1/N_2=10/15$, primary Litz wire 200 strands $\times \phi$ 0.07 mm, 10 in parallel, insulator material kapton of horizontal width 6.5 mm, secondary Litz wire 200 strands $\times \phi$ 0.07 mm, 4 in parallel
Output diodes D_{1-4}	CREE 1200 V/43 A C4D30120D SiC Schottky diode
Output inductor $L_o=2 \times 100 \mu\text{H}$	EPCOS ferrite core ETD54 material N97, airgap 1.5 mm, 19 turns, solid wire of 0.9 mm diameter 10 in parallel
Output capacitor $C_o=4 \times 50 \mu\text{F}$	WIMA $50 \mu\text{F}$ DCP4I055007JD2KYSD (600 Vdc) film capacitor

4.7. Simulation validation

Figure 4.22: Distribution of losses estimation for the prototype design at $P_{o,nom}=3.3$ kW.

4.7 Simulation validation

Based on the previous mentioned modulation method, the steady-state operation of the proposed rectifier including EMI filter working under nominal input and nominal load is simulated in GeckoCIRCUITS [52]. The values of transformer turns ratio, EMI filter, and output filter used in this simulation are designed in the previous sections respectively. Again, the proposed rectifier topology is depicted in Figure 4.23, for the convenience of better understanding the waveforms.

Figure 4.24 depicts the main waveforms in the simulation. The rectifier pulsating input currents are shown as $i_{rec,a}$, $i_{rec,b}$ and $i_{rec,c}$, which can be seen in phase with the three-phase source voltages u_a , u_b and u_c . The phase currents after filtering by EMI filter are depicted as i_a , i_b and i_c , which show a desirable $THD_I=1.5\%$. The time intervals t_1 , t_2 , t_3 , and t_4 derived in section 3.2 are depicted as duty cycle values. It is worth noticing that, the active state interval t_1 is the interval when the phase with minimum absolute value out of the three is allowed to conduct current through the bidirectional switch pair, thus it has exactly the triangular shape of the third harmonic of the three-phase voltages. S_{ya} , S_{yb} and S_{yc} are the driven signals for the bidirectional switching pairs. It can be seen that, each switching pair only switches when its corresponding phase voltage is in the middle of all three. As discussed in

Figure 4.23: Topology of the proposed three-phase single-stage isolated buck-type rectifier.

section 4.1, the transformer primary voltage u_{prim} is switching but shows positive and negative envelopes of a six-fold waveform. The output DC inductor current i_L is also presented, and exhibits a ripple value of 2.4 A (20% of $I_{L,nom}$). Furthermore, the shaded area (around $\theta = \frac{\pi}{6}$) in Figure 4.24 is zoomed in and shown in Figure 4.25.

4.7. Simulation validation

Figure 4.24: Simulation result of the rectifier with EMI filter under nominal input and nominal load, showing main waveforms.

Figure 4.25: Zoom-in of Figure 4.24 at $\theta = \frac{\pi}{6}$ area, showing the same main waveforms.

Experimental validation

In the previous chapter, the detailed design guideline is presented and also waveforms of simulation results are provided. Here in this chapter, a hardware demonstrator is constructed and tested in order to validate experimentally the concept and design of the proposed rectifier topology. Experimental results are performed at nominal power, which validates the expected efficiency, THD, and PF according to the simulation results.

5.1 Construction of hardware demonstrator

The constructed rectifier system has a block diagram shown as Figure 5.1. The 3D CAD model using Autodesk Inventor [63] was designed prior to the routing of each PCB, aiming at maximizing the power density, facilitating component selection and spatial distribution process as 3D design iterations evolve. Besides, once all the PCBs are routed and fabricated, this 3D CAD model can serve as the manual to mount the components, assemble the parts and double check the mechanical structure. In the end, the 3D CAD model of the designed rectifier power stage with EMI filter included is captured in Figure 5.2, and the main components are marked.

The final version of rectifier hardware demonstrator is shown in Figure 5.3, which includes the primary PCB and secondary PCB of the rectifier, transformer, driver boards for the primary side MOSFETs, three-phase voltages sensor board, and on top of all lies the EMI filter board.

Besides, in order to receive measurements and send modulation signals to the power stage, a control PCB is designed, loaded with a Texas Instruments F28377D controlCARD [64], together with other signal conditioning and protection circuitry. A picture of this control PCB is provided in Figure 5.4.

Figure 5.1: Block diagram of the hardware demonstrator of the proposed rectifier, including power stage and digital control stage.

Figure 5.2: 3D CAD model of the designed rectifier power stage including the EMI filter.

5.1. Construction of hardware demonstrator

Figure 5.3: Picture of the assembled rectifier (dimension: length 414mm x width 100mm x height 140mm).

Figure 5.4: Picture of the Control PCB loaded with a TI F28377D controlCARD (dimension: length 250mm x width 250mm).

Figure 5.5: Schematics for the preliminary tests, working as phase-shifted full-bridge DC-DC converter.

5.2 Preliminary tests

In order to start testing the prototype, first it is tested as phase-shifted full-bridge DC-DC converter at equivalently nominal DC input and nominal load. Figure 5.5 provides the schematic of this test condition, and the components drawn in gray color are not conducting. Figure 5.6 depicts the hardware demonstrator setup for phase-shifted full-bridge DC-DC test. The EMI board on top is removed, leaving the last stage filter capacitor as the input capacitor for this DC-DC converter. For the DC input, phase A is fed with the positive point of DC input, while phase B and C are tied together and fed with the negative point of DC input. Subsequently diode D_{a+} , D_{b-} , and D_{c-} are forward biased, and the rest of the diodes are reverse blocked. Bidirectional switch pair S_{ya} , S_{yb} , and S_{yc} are all disabled by placing a jumper at their gate-source pins. MOSFETS S_{y1} , S_{y2} , S_{x1} , and S_{x2} are driven with phase-shifted full-bridge logic, in order to test the losses and thermal condition of the converter under nominal power.

In section 5.2.1 the experimental results of phase-shifted full-bridge at nominal working condition is presented. In section 5.2.2 and 5.2.3 the experimental results are provided employing the aforementioned passive snubber (section 4.5.1) and active snubber (section 4.5.2) solution respectively.

5.2.1 Phase-shifted full-bridge (DC-DC)

Figure 5.7 depicts the waveforms on the primary side of the DC-DC, without snubber circuit, under 1.6 kW load, 210 VDC input and 200 VDC output. This test without

5.2. Preliminary tests

Figure 5.6: Prototype picture of the test setup as phase-shifted full-bridge DC-DC converter.

snubber didn't push up to nominal input voltage out of the concern of breaking the diode rectifier. Ch1 and Ch2 measure the gate-source signals of the MOSFET S_{y1} and S_{y2} respectively. Ch3 shows the drain-source signal of MOSFET S_{y2} . It can be seen that ZVS is present on the switching of leg S_{y1} - S_{y2} , since the instant when S_{y2} turns off (Ch2 goes low), the drain-source voltage of S_{y2} starts to rise till it reaches DC input (Ch3 goes high), which means drain-source of S_{y1} reaches zero, then soon later S_{y1} is turned on (Ch1 goes high) with no spiky ringing. The same is observed for the other instant When S_{y1} turns off and S_{y2} turns on.

Transformer primary current i_{prim} (Ch4) is positive-negative balanced with the merit of the DC flux blocking capacitor (C_{dc}). High frequency ringing is observed, it is the ringing reflected to the primary side, based on the discussion in section 4.5.

Another issue that can be observed is that ZVS is also present in the other leg S_{x1} and S_{x2} even though they are not measured. It can be seen from the instant

Figure 5.7: Experimental result of the converter without snubber, working at 1.6 kW as phase-shifted full-bridge DC-DC, showing waveforms of MOSFET S_{y1} gate-source (Ch1 in yellow, 5V/div), MOSFET S_{y2} gate-source (Ch2 in blue, 5 V/div), MOSFET S_{y2} drain-source (Ch3 in pink, 100 V/div), and transformer primary current i_{prim} (Ch4 in green, 5 A/div).

when the primary side goes from freewheeling to active state, there is just little ringing noise reflected on the gate-source signals of S_{y1} and S_{y2} .

The upper oscilloscope in Figure 5.8 shows more measured waveforms. Ch2 depicts the primary voltage of the transformer u_{prim} and Ch3 shows the secondary u_{sec} . Ringing on the secondary is observed the same as simulated in Figure 4.15, which causes 2-3 times higher peak than the original DC value applied on the secondary. Moreover, converter efficiency is compromised since ringing energy is wasted. Ch4 shows the output inductor current i_L .

Figure 5.9 shows the power quality measurements, where Element 1 indicates the characteristics at the converter DC input, and Element 4 provides the values at the DC output. Efficiency measurement η_1 is configured as P_{out}/P_{in} to get the converter efficiency, which in this case equals to 95.12%.

5.2. Preliminary tests

Figure 5.8: Experimental result of the converter without snubber, working at 1.6 kW as phase-shifted full-bridge DC-DC, upper oscilloscope showing waveforms of primary voltage u_{prim} (Ch2 in blue, 250 V/div), secondary voltage u_{sec} (Ch3 in pink, 250 V/div).

5.2.2 Phase-shifted full-bridge (DC-DC) with passive snubber

As discussed in section 4.5.1, the passive snubber solution is applied on the prototype secondary side. Figure 5.10 and Figure 5.11 show the picture of the prototype (only secondary side, top view and front view) with passive snubber installed, indicated as the schematic in Figure 4.18 and the components listed in Table 4.4. The nominal power working condition is tested, i.e. 270 V input voltage, 290 V output voltage, 3.3 kW load.

Figure 5.12 shows the waveforms from the primary side measured by Rhode&Schwarz RTE1104 oscilloscope [65]. Ch1 and Ch2 measure the gate-source signals of the MOSFET S_{y1} and S_{y2} respectively. Ch3 shows the drain-source signal

Figure 5.9: Experimental result of the converter without snubber, working at 1.6 kW as phase-shifted full-bridge DC-DC, showing power quality measurements.

Figure 5.10: Prototype picture of the secondary side with passive snubber installed (top view).

5.2. Preliminary tests

Figure 5.11: Prototype picture of the secondary side with passive snubber installed (front view).

of MOSFET S_{y2} . Transformer primary current i_{prim} is measured in Ch4. It can be seen that apart from the ZVS behavior in four MOSFETs, i_{prim} resembles the simulation result presented in Figure 4.19. The transformer current has an inrush peak where the ringing should have occurred, this is when the current flows into the clamping capacitor C_c of the passive snubber and later becomes more damped compared to the ringing case measured in Figure 5.7.

Figure 5.13 presents more waveforms measured with Tektronix MSO 4104 oscilloscope [66]. Ch1 shows the transformer primary voltage u_{prim} and Ch2 for the secondary voltage u_{sec} . Ch3 measures the output inductor current i_L . The secondary voltage shows resemblance to the one from simulation in Figure 4.19, which the first ringing peak is snubbed and the rest of ringing is more damped compared to the unsnubbed ringing behavior shown in Figure 5.8.

The power quality (e.g. efficiency) is measured by Yokogawa WT1800 precision power analyzer [67]. Figure 5.14 shows the DC input and DC output power quality

Figure 5.12: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with passive snubber applied, showing waveforms of MOSFET S_{y1} gate-source (Ch1 in yellow, 5 V/div), MOSFET S_{y2} gate-source (Ch2 in blue, 5 V/div), MOSFET S_{y2} drain-source (Ch3 in pink, 100 V/div), transformer i_{prim} (Ch4 in green, 5 A/div), at time scale of 4 $\mu\text{s}/\text{div}$.

Figure 5.13: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with passive snubber applied, showing waveforms of primary voltage u_{prim} (Ch1 in yellow, 250 V/div), secondary voltage u_{sec} (Ch2 in blue, 250 V/div), output inductor current i_L (Ch3 in pink, 2 A/div), at time scale of 4 $\mu\text{s}/\text{div}$.

5.2. Preliminary tests

Figure 5.14: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with passive snubber applied, showing power quality measurements.

Figure 5.15: Thermal camera capture of the secondary stage of the prototype working at 3.3 kW, with passive snubber applied (top view).

Figure 5.16: Thermal camera capture of the secondary stage of the prototype working at 3.3 kW, with passive snubber applied (front view).

measurements as Element 1 and Element 4. The efficiency shows 95.63% which is improved by 0.5% (i.e. 16.5 W) compared to the case without snubber.

In order to monitor the operating temperature of the prototype, especially for the hot spot on the installed passive snubber, Fluke Ti400 Infrared Camera [68] is utilized. Figure 5.15 and Figure 5.16 are the thermal camera snapshots (top view and front view respectively) on the secondary stage while the converter is working at 3.3 kW. It can be seen from the brightest point, there is approximately 57°C on the diodes in the charging path of the snubber circuit, and 70°C on the resistor in the discharging path.

5.2.3 Phase-shifted full-bridge (DC-DC) with active snubber

Based on the discussion in section 4.5.2, the active snubber is installed on the prototype secondary side. Figure 5.17 depicts the prototype (secondary side, left view) with active snubber installed, whose schematic is according to Figure 4.20 and components listed as Table 4.5. The driven signal timing issue, discussed in section 4.5.2, is implemented on the prototype and experimental results are provided as below.

Figure 5.17: Prototype picture of the secondary side with active snubber installed (left view).

5.2. Preliminary tests

Figure 5.18: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with active snubber applied, showing waveforms of MOSFET S_{y1} gate-source (Ch1 in yellow, 5 V/div), MOSFET S_{y2} gate-source (Ch2 in blue, 5 V/div), MOSFET S_{y2} drain-source (Ch3 in pink, 100 V/div), transformer i_{prim} (Ch4 in green, 10 A/div), at time scale of 4 μs /div.

Figure 5.19: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with active snubber applied, showing waveforms of MOSFET S_{x1} gate-source (Ch1 in yellow, 5 V/div), MOSFET S_{snub} gate-source (Ch2 in blue, 5V/div), MOSFET S_{y2} gate-source (Ch3 in pink, 5 V/div), transformer i_{prim} (Ch4 in green, 10 A/div), at time scale of 4 μs /div.

Figure 5.20: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with active snubber applied, showing waveforms of primary voltage u_{prim} (Ch1 in yellow, 250 V/div), secondary voltage u_{sec} (Ch2 in blue, 250 V/div), output inductor current i_L (Ch3 in pink, 2 A/div), at time scale of 2 μ s/div.

Figure 5.21: Experimental result of phase-shifted full-bridge DC-DC at 3.3 kW with active snubber applied, showing power quality measurements.

5.2. Preliminary tests

Figure 5.18 shows the measurements taken from the primary side of the converter, Ch1 represents the gate-source signal of MOSFET S_{y1} , Ch2 for MOSFET S_{y2} , Ch3 for the drain-source of S_{y2} , and Ch4 shows the current i_{prim} through the primary side of the transformer. It can be seen that ZVS is achieved in the transitions. Furthermore, i_{prim} shows resemblance to the simulated one in Figure 4.21. In order to illustrate the timing of snubber switch gating signal regarding other signals, capture in Figure 5.19 shows: Ch1 for the gate-source signal of MOSFET S_{x1} , Ch2 for the gate-source signal of snubber switch S_{snub} , Ch3 for the gate-source signal of MOSFET S_{y2} , and Ch4 still for i_{prim} .

Figure 5.20 depicts more waveforms measured from the secondary side of the converter with active snubber implemented. Ch1 shows the transformer primary voltage u_{prim} , Ch2 shows that of the secondary side u_{sec} , and Ch3 measures the output inductor current i_L . The secondary voltage exhibits great resemblance to the one from simulation in Figure 4.21. It is clear that the ringing is completely eliminated. This lowers the voltage stress of the diode rectifiers and meanwhile the non-dissipative snubber circuit increases the system efficiency.

Figure 5.21 captures the DC input and DC output power quality measurements as Element 1 and 4 respectively. The efficiency is 96.04% which is improved by 0.4% (i.e. 13.2 W) than the passive snubber case (95.63% from Figure 5.14), and 0.9% (i.e. 29.7 W) compared to the case without snubber.

5.2.4 Comparison of snubber solutions

In order to compare the two snubber solutions, efficiency measurements are done with each snubber implemented under a wide power range. The result is shown in Figure 5.22. It can be seen that, over the power range from 10% load to full load, active snubber always shows better efficiency than the passive one. This is because the active one in principle is non-dissipative, however in reality the MOSFET S_{snub} incorporates small conduction losses, since the current charging and discharging the C_{snub} is small. On the other hand, the passive snubber still has dissipative losses on the discharging resistor even though part of the energy is returned to the output.

Figure 5.22: Comparison of efficiency measurement under different load power between the passive snubber and the active snubber implementation.

5.3 Rectifier tests (AC-DC)

The rectifier tests on the prototype started with debugging and pretests of several essential functional parts. Which are:

Calibration of sensor board for measuring u_{ab} and u_{bc} , and the signal conditioning part in cascade on control PCB, right before entering the ADC channels of the TI MCU F28377D controlCARD.

Calibration of current sensors at the input of EMI filter for measuring phase currents, and the signal conditioning part in cascade on control PCB, before entering ADC channels of the MCU, besides, validation of the over-current protection circuitry.

Programming of the rectifier modulation algorithm inside MCU, according to different sectors. Besides, the SPI (Serial Peripheral Interface) of the MCU is utilized with a DAC (Digital-Analog Converter) circuitry in order to demonstrate key digital signals on the oscilloscope (e.g. PLL sector information.)

Figure 5.23 shows the generated PWM signals based on different PLL sectors. Ch1 is the signal coming out of the DAC circuitry, which shows the sector value from 1 to 12. Digital channels D0-D6 demonstrate driven signals for MOSFETs

5.3. Rectifier tests (AC-DC)

Figure 5.23: Experimental result of the MCU generated PWM signals according to different PLL sectors.

S_{y1} , S_{y2} , S_{x1} , S_{x2} and S_{ya} , S_{yb} , S_{ye} respectively. The zoom-in shows around the area of sector 1 changing into sector 2.

5.3.1 Rectifier open-loop test with passive snubber

The experimental results of the proposed three-phase rectifier at nominal input (115 Vrms line-to-neutral), operating under nominal load (3.3 kW, 270 V) with the passive snubber installed, are shown below. At the input, after the three-phase source and before the EMI filter of the rectifier, Yokogawa WT1800 precision power analyzer is used to measure the waveforms and characteristics of the three-phase voltages and currents. Figure 5.24 demonstrates these three-phase voltages U_1 U_2 U_3 and currents I_1 I_2 I_3 . One can see that, three-phase voltage has a line frequency of 400Hz and the three-phase currents have a very sinusoidal-like shape.

The characteristic numbers of these waveforms are calculated also by Yokogawa WT1800, a capture is shown in Figure 5.25. Element 1, 2 and 3 correspond to input phase A, B and C respectively, while Element 4 represents the DC output. Notably, the constructed rectifier prototype exhibits a very good THD_I of 1.9%, and the standard is defined for a THD_I below 5%. Regarding Power Factor, in the capture

Figure 5.24: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing waveforms of three-phase input voltages (U1 U2 U3) and currents (I1 I2 I3).

it shows an excellent PF of 0.9996 while the standard is above 0.85. η_1 in the last row stands for the efficiency of the rectifier including the EMI filter, which is 93.7%.

The axial fan in the primary-side heatsink is supplied with 12 V DC and can offer a maximum free-air flow 56 m³/h. The measured temperature of the primary heatsink is 55°C. The transformer winding temperature is measured by a pre-placed K-type thermocouple (connected to a multimeter) inside the windings, and the transformer windings show a temperature of 45°C.

Figure 5.26 represents detailed waveform measurements of the rectifier. Ch1 measures the transformer primary side voltage u_{prim} ; Ch2 presents the transformer secondary voltage u_{sec} , which can be seen clearly the passive snubber clamping the first ringing peak; Ch3 is the PLL sector value coming after DAC, the zoom-in shows the area in the middle of sector 1; Ch4 measures the dc output inductor current i_L .

In Figure 5.27 more waveforms are presented. The zoom-in shows also the area in the middle of sector 1. Ch1 presents the PLL sector information; Ch2 measures the gate-source of MOSFET S_{y2} ; Ch3 measures the gate-source of MOSFET S_{x2} ; Ch4 shows the current through the primary of the transformer i_{prim} . It demonstrates that the turn-on instant of S_{y2} (Ch2) marks the change from an active state to a

5.3. Rectifier tests (AC-DC)

Figure 5.25: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing power quality measurements of the three-phase input (Elements 1-3) and DC output (Element 4).

Figure 5.26: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing waveforms of u_{prim} (Ch1 in yellow, 200 V/div), u_{sec} (Ch2 in blue, 200 V/div), sector signal after DAC (Ch3 in pink, 1 V/div), dc output inductor current i_L (Ch4 in green, 2 A/div), at time scale of 4 μ s/div.

Figure 5.27: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{y2} (Ch2 in blue, 5 V/div), gate-source signal of S_{x2} (Ch3 in pink, 5 V/div), transformer primary current i_{prim} (Ch4 in green, 5 A/div), at time scale of 4 μ s/div.

Figure 5.28: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Figure 5.27, showing waveforms of sector signal after DAC (Ch1 in yellow, 400 mV/div), gate-source signal of S_{y2} (Ch2 in blue, 5 V/div), gate-source signal of S_{x2} (Ch3 in pink, 5 V/div), transformer primary current i_{prim} (Ch4 in green, 5 A/div), at time scale of 2 μ s/div.

5.3. Rectifier tests (AC-DC)

freewheeling state, while the turn-on and turn-off of S_{x2} (Ch3) shows the change from a freewheeling state to an active state. Notably the i_{prim} waveform presents great resemblance to the one in DC-DC test scenario with passive snubber (see Figure 5.12). When the secondary diode bridge first enters the active state, the first current peak flows into the secondary snubber capacitor and the snubber clamps its voltage so that the ringing is mitigated.

A zoom-in of Figure 5.27 is also presented, as Figure 5.28, to further demonstrate the details inside one switching period. Active state time intervals t_1 t_2 and t_3 , as well as freewheeling state time interval t_4 , are marked in this capture, corresponding to the illustration in Figure 3.3.

In order to show the ZVS details, the drain-source voltage of both switches S_{y2} and S_{x2} are measured individually together with its gate-source signal. Figure 5.29 captures the waveforms of Ch1 for PLL sector information, Ch2 for gate-source of MOSFET S_{y2} , Ch3 for drain-source voltage of S_{y2} and Ch4 for transformer primary current i_{prim} . It is worth noticing that Ch2 in this Figure 5.29 measures the same signal as Ch2 in Figure 5.28, which are both gate-source of S_{y2} . Besides, Ch3 as drain-source voltage of S_{y2} shows three levels: when it is turned off but one of the bidirectional switch S_{yn} is on, it blocks an intermediate voltage level; next, when S_{y1} is on, it blocks the maximum line-to-line voltage; in the end, when it is turned on, it shows zero. This measured waveforms exhibits great accordance to the simulated ones (S_{y2} and $U_{S_{y2}}$) in Figure 3.6.

Furthermore in order to see the detailed ZVS behaviors, based on Figure 5.29, zoom-in captures focused on the turn-on and turn-off instants are presented respectively in Figure 5.30 and Figure 5.31. It can be seen from Figure 5.30, the drain-source of S_{y2} (Ch3) drops to zero before gate-source of S_{y2} (Ch2) is turned on. And in Figure 5.31, gate-source of S_{y2} (Ch2) is turned off and then its drain-source voltage starts to rise to an intermediate value and facilitates the ZVS turn-on of S_{yn} . These measured ZVS instants also coincide with the simulated ones in Figure 3.6.

As to the ZVS behavior of S_{x2} , Figure 5.32 is captured, with Ch1 for PLL sector information, Ch2 for gate-source signal of MOSFET S_{x2} , Ch3 for drain-source voltage of S_{x2} , and Ch4 for transformer primary current i_{prim} . It can be easily seen that, the drain-source voltage of S_{x2} (Ch3) maintains zero when its gate-source (Ch2) is on (+12 V); and when its gate-source (Ch2) is off (-5V), the drain-source

Figure 5.29: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, ZVS details on MOSFET S_{y2} , showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{y2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{y2} (Ch3 in pink, 100 V/div), transformer primary current i_{prim} (Ch4 in green, 5 A/div), at time scale of 2 μ s/div.

Figure 5.30: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Figure 5.29 at MOSFET S_{y2} turn-on instant, showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{y2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{y2} (Ch3 in pink, 100 V/div), and transformer primary current i_{prim} (Ch4 in green, 5 A/div).

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Figure 5.31: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Figure 5.29 at MOSFET S_{y2} turn-off instant, showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{y2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{y2} (Ch3 in pink, 100 V/div), and transformer primary current i_{prim} (Ch4 in green, 5 A/div).

of S_{x2} (Ch3) blocks maximum line-to-line voltage. These measured waveforms of S_{x2} also shows good agreement to the simulated ones (S_{x2} and U_{Sx2}) in Figure 3.6.

In order to see the detailed switching instants of S_{x2} , based on Figure 5.32, zoom-in captures focused on the turn-on and turn-off instants are presented individually in Figure 5.33 and Figure 5.34. It is clearly seen from Figure 5.33 that, the drain-source voltage of S_{x2} (Ch3) falls to zero before gate-source of S_{x2} (Ch2) turns on. Also in Figure 5.34, after gate-source of S_{x2} (Ch2) turns off, its drain-source voltage starts to rises till the maximum line-to-line voltage and finally facilitates the ZVS turn-on of its upper-side switch S_{x1} . This also corresponds to the simulated instants in Figure 3.6.

Figure 5.32: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, ZVS details on MOSFET S_{x2} , showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{x2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{x2} (Ch3 in pink, 100 V/div), transformer primary current i_{prim} (Ch4 in green, 5 A/div), at time scale of 2 μ s/div.

Figure 5.33: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Figure 5.32 at MOSFET S_{x2} turn-on instant, showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{x2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{x2} (Ch3 in pink, 100 V/div), and transformer primary current i_{prim} (Ch4 in green, 5 A/div).

5.3. Rectifier tests (AC-DC)

Figure 5.34: Experimental result of the three-phase rectifier working at 3.3 kW with passive snubber installed, zoom-in of Figure 5.32 at MOSFET S_{x2} turn-off instant, showing waveforms of sector signal after DAC (Ch1 in yellow, 1 V/div), gate-source signal of S_{x2} (Ch2 in blue, 5 V/div), drain-source voltage of S_{x2} (Ch3 in pink, 100 V/div), and transformer primary current i_{prim} (Ch4 in green, 5 A/div).

Conclusion and future work

6.1 Conclusion and contribution

In this dissertation, first a survey is done on the state-of-the-art rectifier topologies, both the conventional two-stage ones and the single-stage with isolation ones. Next, an isolated single-stage three-phase buck-type rectifier topology together with its modulation method is proposed for the intended More Electric Aircraft application. The proposed topology features not only a single-stage structure with galvanic isolation, but also ZVS features in each switching transition, which greatly increases the rectifier efficiency.

The first and main contribution of this thesis is the proposed rectifier topology and the corresponding theoretical analysis on the operating principle. The calculation of timing for each active state and freewheeling state is the essence of the modulation for the rectifier. Apart from the transformer turns ratio N_1/N_2 , the other control variable is modulation index M (according to equation 3.1) which controls the amount of power to be transferred from AC-side to the DC-side, like any other three-phase buck-type rectifiers. Current SVM method to compose the input rectifier current is discussed in details, also as a heritage of three-phase buck-type rectifiers. Furthermore, given the existence of the high-frequency transformer, volt-second balance of the transformer has to be considered and integrated into the calculation of modulation timing in each switching period.

The second contribution of this dissertation is the analysis of the zero-voltage-switching characteristic for every switching transition (see section 3.3). The full-bridge-like structure together with the proper modulation sequence provides ZVS easily with just adequate leakage inductance and sufficient deadtime. Necessary requirements for reaching ZVS above certain load level are derived, verification in simulation results are provided in Figure 3.6.

The third contribution of this work is the comparison with VIENNA Rectifier III from the literature. In section 3.4, the topological derivation from VIENNA Rectifier III (with its symmetrical modulation sequence) to the proposed rectifier topology (with its asymmetrical modulation sequence) is discussed, proving that the proposed rectifier not only presents less conduction losses, but also shows ZVS feature that VIENNA Rectifier III cannot provide.

Next contribution in the dissertation, is the complete rectifier design guideline given in Chapter 4. It shows that the key point in the transformer design is to achieve the desired leakage inductance by separating the primary winding and the secondary winding, although this increases the winding AC losses compared to a well interleaved case. However this leakage inductance is essential for achieving ZVS, which can reduce the EMI filtering effort, as well as potential control failure due to noise interference among switches. Another option could be to build a transformer with good interleaving between primary and secondary windings, which helps decreasing winding AC losses in the transformer, but meanwhile inserting an external inductor in series with the transformer to realize ZVS. This external inductor in series with the transformer presents a high AC flux and a high AC RMS current that would penalize a lot the losses. The selected option for the prototype developed in this thesis is to integrate the series inductance in the transformer since the required leakage inductance was small having a sensible impact on the transformer performance. The finished transformer presents a leakage inductance of $2.8 \mu\text{H}$ and the magnetizing inductance of 1.2 mH reflected on the primary side. And in experimental results later presented in section 5.3.1, the transformer winding shows a temperature of only 45°C at nominal 3.3 kW load. Next, the EMI filter design presents a two-stage with $R - L_d$ series damping. In GeckoCIRCUITS this EMI filter is proven to comply with the EMC standard MIL-STD-461F. The average and RMS currents of all semiconductor devices are derived analytically. The output filter design guideline is also extracted.

Another contribution of the dissertation is that a passive and an active snubber from the literature are both analyzed and incorporated into the design of the proposed rectifier. From the comparison of the experimental results of the two snubber solutions, as shown in section 5.2.4, the passive snubber can only clamp the first ringing peak, while the active snubber can totally get rid

6.2. Future work

of all the ringing on the secondary side maintaining a fixed DC value. In terms of efficiency, the active snubber solution always presents 0.4%-2% higher efficiency than the passive one, throughout the whole power range.

In the end, theoretical analysis for the proposed rectifier topology is validated by testing a hardware demonstrator. At nominal power, this three-phase single-stage isolated rectifier including EMI filter, shows an excellent THD_I of 1.9% and a near-unity PF of 0.9996. The efficiency at nominal power is 93.7% which can be greatly improved if other low on-resistance devices (e.g. SiC or GaN devices) will be employed in the prototype, since right now all the MOSFETs are Si MOSFETs from Infineon CoolMOS series.

6.2 Future work

There are several tasks that can be done for future research in order to complete the scope of the proposed rectifier topology, and to further improve the performance of the hardware demonstrator.

- **Modeling and control loop design** is the immediate future work that can be done to further complete the analysis of the proposed rectifier. The small-signal modeling of the rectifier control plant can be verified by measuring the rectifier working under steady state, injecting a small disturbance signal sweeping from low frequency to high frequency, employing Bode 100 analyzer [69] from OMICRON Lab).
- **Parallel capability of the proposed topology** could also be a promising topic for future research, since for higher power applications, paralleled converter structure may outrun one converter rated for full power in terms of efficiency and weight.
- **The detailed analysis of η - ρ -Pareto Front** including EMI filter can be useful for future rectifier design and easy comparison with other topologies.
- **Thorough and standardized comparison between the proposed rectifier topology and other single-stage with isolation topologies** can certainly be very interesting as future research line. Furthermore, comparing

the conventional 2-stage approach with single-stage approach in terms of efficiency and power density could also be very interesting for industry.

- **Employing cutting-edge wide bandgap semiconductor devices** such as SiC MOSFETs or GaN FETs, which usually exhibit lower on-state resistance and parasitic capacitance over Si MOSFETs. Thus less conduction losses should be obtained, besides, ZVS can be achieved either for wider range or with less leakage inductance from transformer. Higher overall efficiency should be expected for the rectifier prototype.
- **Integrating the control board into the assembly of the rectifier prototype** can provide shorter path and potentially less noise interference for the high frequency driven signals and measurements, besides the power density of the rectifier prototype can be further maximized.

6.3 Diffusion of the results

The following papers have been published during the work on this thesis:

Referred journal papers

1. **S. Zhao**, J. M. Molina, M. Silva, J. A. Oliver, P. Alou, J. Torres, F. Arévalo, O. García, J. A. Cobos, “Design of Energy Control Method for Three-Phase Buck-Type Rectifier with Very Demanding Load Steps to Achieve Smooth Input Currents” IEEE Transactions on Power Electronics, vol. 31, no. 4, pp. 3217-3226, April 2016.

Referred conference papers

1. **S. Zhao**, M. Silva, J. A. Oliver, P. Alou, O. García and J. A. Cobos, “Analysis and Design of an Isolated Single-Stage Three-Phase Full-Bridge with Current Injection Path PFC Rectifier for Aircraft Application” IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2015.
2. **S. Zhao**, J. M. Molina, M. Silva, J. A. Oliver, P. Alou, J. Torres, F. Arévalo, O. García, J. A. Cobos, “Design of Energy Control Method for Three-Phase

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- Buck-Type Rectifier with Very Demanding Load Steps” IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2014.
3. U. Borović, **S. Zhao**, M. Silva, Y. E. Bouvier, M. Vasić, J. A. Oliver, P. Alou, J. A. Cobos, F. Arevalo, J. GarciaTembleque, J. Carmena, C. Garcia and P. Pejovic “Comparison of Three-phase Active Rectifier Solutions for Avionic Applications: Impact of the Avionic Standard DO-160 F and Failure Modes” IEEE Energy Conversion Congress and Exposition (ECCE), Sep. 2016.
 4. U. Borović, **S. Zhao**, M. Silva, Y. E. Bouvier, M. Vasić, J. A. Oliver, P. Alou, J. A. Cobos, P. Pejović, “Comparison of three-phase active rectifiers for aircraft application” Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), Jul. 2015.
 5. M. R. Ramos, **S. Zhao**, J. M. Molina, P. Alou, J. A. Oliver, J. A. Cobos, “3-Phase rectifier system with very demanding dynamic load” Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), Jul. 2015.
 6. J. M. Molina, **S. Zhao**, M. Silva, J. A. Oliver, P. Alou, J. Torres, F. Arévalo, O. García, J. A. Cobos, “Power Distribution in a 13 kW Three-Phase Rectifier System: Impact on Weight, Volume and Efficiency” IEEE Applied Power Electronics Conference and Exposition (APEC), Mar. 2014.
 7. J. M. Molina, **S. Zhao**, M. Silva, J. A. Oliver, P. Alou, J. Torres, F. Arévalo, O. García, J. A. Cobos, “3-Phase Rectifier System with very demanding dynamic load: Architecture analysis and control strategy” Seminario Anual de Automática, Electrónica Industrial e Instrumentación (SAAEI), Jul. 2013.

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