Power estimation technique for DSP architectures

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ABSTRACT

The main goal of power estimation is to optimize the power consumption of a electronic design. Power is a strongly pattern dependent function. Input statistics greatly influence on average power. We solve the pattern dependence problem for intellectual property (IP) designs. In this paper, we present a power macro-modeling technique for digital signal processing (DSP) architectures in terms of the statistical knowledge of their primary inputs. During the power estimation procedure, the sequence of an input stream is generated by a genetic algorithm using input metrics. Then, a Monte Carlo zero delay simulation is performed and a power dissipation macro-model function is built from power dissipation results. From then on, this macro-model function can be used to estimate power dissipation of the system just by using the statistics of the macro-block's primary inputs. In experiments with the DSP system, the average error is 26%.

1. Introduction

During the years of inception in the digital age, the use of integrated circuits (IC) was confined to traditional digital electronic systems such as wearable computers, wireless communication systems. Nowadays not only those devices play an increasingly important role but also the use of integrated systems is much more widespread, from controllers used in home appliances to the automobile industry. The digital electronic circuits are becoming more application specific. The shrinking of devices due to the development of new fabrication technology has increased dramatically the number of transistors available for use in a single chip. The larger capacity of the chips is also being used to extend the functionality of the systems. However, the importance of low power dissipative digital circuits is being increased rapidly. In order to handle the ever increasingly complexity, CAD tools have been developed. Those tools also help minimizing power dissipation of digital devices and accurate power estimation tools are needed at high abstraction levels.

Power estimation for a digital circuit involves in two factors: how to model the circuit itself and how to model input signals. There are different techniques for both of them. Input signals can be generated as test vectors or they can be modeled probabilistically or statistically. Circuit macro-modeling techniques can also further classified into two categories: Those that use power coefficients measured on sample circuits, and those that analyze current and voltage from an equivalent circuit model. Given an input signal models, the macro-model estimates maximum power dissipation, or average power dissipation, or total energy consumed during certain cycle. Therefore, accurate and efficient power estimation tools characterized by the techniques it takes for circuit modeling, signal modeling and by the types of power estimation it supports.

In this paper, we present a power estimation methodology at register transfer level (RTL) based on macro-modeling techniques applied on FIR filter. The main challenge in establishing RTL power estimation methodology is the construction of efficient and accurate macro-models of the power dissipation. Such macro-models should be automatically built, and

should produce reliable average power estimates. RTL power estimation is a key feature for synthesis-based design flow. RTL allows an early design space exploration which in turn reduces design time. At this level designs are usually described hierarchically. The main challenge in estimating the power dissipation of a hierarchical design is the construction of accurate black-box power models for the leaves of the hierarchy, which only functional descriptions are available at the RTL. We restrict our scope to structural RTL representations whose leaf components are combinational logic blocks and state-holding elements such as registers. Moreover, complex sequential logic blocks are directly described as RTL primitives.

In response to this need, the power macro-modeling technique is a promising solution to face the problem of high-level power estimation. The macro-model construction consists of generating a mapping between the power dissipation of a circuit and certain statistics of the input signals. The application of power macro-modeling on the macro-blocks of an entire system requires knowledge of the signal statistics among the different blocks. To obtain this information, the architect must perform different functional simulations.

Recently, a number of techniques for power estimation of DSP architectures have been proposed. We will focus on digital finite impulse response (FIR) filter that is typically used in many DSP systems to perform signal preconditioning, anti-aliasing, band selection, decimation/interpolation, low-pass filtering, and video convolution functions. A digital filter is simply a discrete-time, discrete-amplitude convolver. Basic Fourier transform theory states that the linear convolution of two sequences in the time domain is the same as multiplication of two corresponding spectral sequences in the frequency domain. Filtering is in essence the multiplication of the signal spectrum by the frequency domain impulse response of the filter.

Various power estimation techniques have been introduced previously. They can be divided into two categories: *probabilistic* and *statistical*. Probabilistic techniques [1–3] use the probabilities of the input stream and their propagation into the circuit to estimate the internal switching activities of the circuit. These techniques are very efficient, but they cannot capture accurately factors like glitch generation, propagation, etc. On the other hand, in statistical techniques [4–6] the circuit is simulated under randomly generated input patterns and the power dissipation is monitored using a power estimator. Therefore, the power values obtained are used to estimate the power consumption for every input stream. For accurate power estimation, we need to produce a required number of simulated vectors, which is usually high and causes run time problem. To handle this problem, a Monte Carlo simulation technique was presented in [7] that uses input vectors randomly generated to obtain the power values. Several samples combined with previous ones are required to determine whether the entire process needs to be repeated in order to satisfy a given criteria.

Most existing approaches of statistical power estimation consider the input signal probabilities and their average switching activities of the input signal and use signal probabilities propagation methods to estimate the internal switching activities [8]. In those approaches, there is no guarantee that the estimated power keeps any relation with the real dissipation of the circuit. To solve this problem, a look-up table (LUT) based macro-model was presented in [9] and further improved in [10] that stores the equi-spaced discrete measured power values of the input signal statistics. The interpolation method was introduced in the case of the input statistics do not correspond to any value stored on the LUT. In [11,12] the interpolation scheme was improved by using the power sensitivity concept. For better accuracy, numerous power macro-modeling techniques [13,14] have been introduced.

Recently, we presented power macro-models for intellectual property (IP) macro-blocks and the IP-based digital system in [15–17]. In this paper, we continue our research developing a power macro-modeling technique for DSP architectures such as FIR filter. Our model is LUT based. The input metrics of our macro-model are the average input signal probability P_{in}, the average input transition density D_{in}, the input spatial correlation S_{in}, and the input temporal correlation T_{in}. Our technique achieves relatively good accuracy.

The rest of this paper is organized as follows. In Section 2 we give the background for the input parameters of our power macro-model. In Section 3, we discuss problem formulation and in Section 4 is about our proposed power estimation methodology. This macro-model is evaluated in Section 5. Section 6 summarizes our work.

2. Power macro-modeling background

Our macro-model is LUT based approach and it estimates the average power dissipation $P_{\text{block\_avg}}$ of FIR filter macro-block using

$$P_{\text{block\_avg}} = f(P_{\text{in}}, D_{\text{in}}, S_{\text{in}}, T_{\text{in}}). \tag{1}$$

The macro-model function $f(.)$ is obtained for a given DSP macro-block simulating different input sample streams with several values of the input metrics: P_{in}, D_{in}, S_{in}, and T_{in}. For a given macro-block with a number of primary inputs r and an input binary stream q of length s is: $q = \{(q_{11}, q_{12}, \ldots, q_{1r}), (q_{21}, q_{22}, \ldots, q_{2r}), \ldots, (q_{s1}, q_{s2}, \ldots, q_{sr})\}$ and the input metrics are defined as follows [10,13,18,19] using

$$P_{\text{in}} = \frac{\sum_{i=1}^{r} \sum_{j=1}^{s} q_{ij}}{r \times s}, \tag{2}$$

$$D_{\text{in}} = \frac{\sum_{j=1}^{r} \sum_{i=1}^{s-1} q_{ij} \oplus q_{i+1j}}{r \times (s-1)}, \tag{3}$$

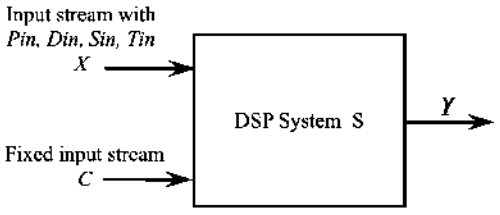

Fig. 1. Block diagram of DSP system S.

$$S_{\text{in}} = \frac{\sum_{j=1}^{r}\sum_{k=1}^{r}\sum_{i=1}^{s} q_{ij} \oplus q_{ik}}{s \times r \times (r-1)}, \tag{4}$$

$$T_{\text{in}} = \frac{\sum_{j=1}^{r}\sum_{t-1}^{s-t+1}(y_j \otimes q_j)}{r \times s}. \tag{5}$$

Once the input metrics are selected, the input sequences are computed by our genetic algorithm (GA) in [20,21]. Monte Carlo zero-delay simulation technique [7] is performed and for the macro-blocks, the power dissipation is obtained by our macro-model function.

3. Problem formulation

For the DSP system S of its macro-blocks, the given statistical signals X and C at the two different input nodes, the algorithm generates an input stream according to X. At the primary input node, X signal gives the metrics, P_{in}, D_{in}, S_{in}, T_{in}, while for the secondary input node, C signal is *fixed-coefficients* (constant) stream as shown in Fig. 1. The power estimation problem for S, under the zero-delay model can be stated as:

Give the RTL description of FIR filter with N inputs and M outputs and the zero-delays of its gates, and assuming that the period of the applied input vectors is greater or equal to the settling time of the circuit, estimate the average power consumption of the circuit for an input vector stream through the calculation of the circuit average switching activity.

The accuracy of the switching activity evaluation is strongly depended on the data correlation of the circuit signals and the assumed zero gate delay model. Concerning data correlation, it includes the temporal and spatial correlation. In case of zero-delay model, a gate performs at most one transition in a clock cycle, which is called functional or useful transition.

4. Proposed macro-modeling methodology

In this section, we present an application of power macro-model in the context of high-level DSP system. Several approaches [12–14] have been proposed to construct power macro-models on ISCAS-85 benchmark circuits. We have observed that the same methodology works as well for the DSP macro-blocks such as delay elements (shift registers), multipliers, adders (that part of the FIR filter) in terms of the statistical knowledge of their primary inputs.

Recently we have presented a macro-model for different IP blocks and the IP-based digital system in [15–17]. The proposed methodology was described as follows: in our static power macro-modeling procedure, the sequence of an input stream was generated for a desired input metrics: P_{in}, D_{in}, S_{in}, and T_{in}. Then using functional simulations and a power estimator, the output stream sequence and the average power dissipation $P_{\text{block\_avg}}$ was extracted by the output waveforms of the IP macro-block. At this moment, the power function (1) can be defined. All this process is divided in two steps. In the first one, the metrics of the inputs/outputs (I/O) sequences were computed by our GA [20,21] and the power function was obtained using $P_{\text{block\_avg}}$ in (1). The interpolation scheme [11,12] can be applied (to improve power sensitivity concept), if the input metrics do not match based on their characteristics. In the second one, Monte Carlo zero delay simulation [7] was performed with different sequences of their signal statistics to evaluated the quality of the power function $P_{\text{block\_avg}}$. At the end we get the power results.

In this section, we continue our previous work and present the application of the statistical power estimation method for DSP architectures such as digital FIR filter. In our preliminary work, the approach intends to reduce the intensive amount of simulations at a higher abstraction level. We use same macro-model information presented in [15–17]. Now, instead of simulating every macro-block, we applied the Monte Carlo zero delay simulation to the entire system. The block diagram of the digital FIR filter is shown in Fig. 2.

The application of the power macro-modeling on each macro-block requires knowledge of the input signal statistics among these blocks. To obtain this information, different functional simulations need to be performed with different input statistical values of each macro-block. For example in Fig. 2, the inputs of the delay element (shift registers) and the multiplier blocks are the inputs of FIR filter, while the outputs of shift registers are the inputs of the multipliers and the multiplier's outputs are the inputs of the adders and so on. The output signal statistical information for each macro-block

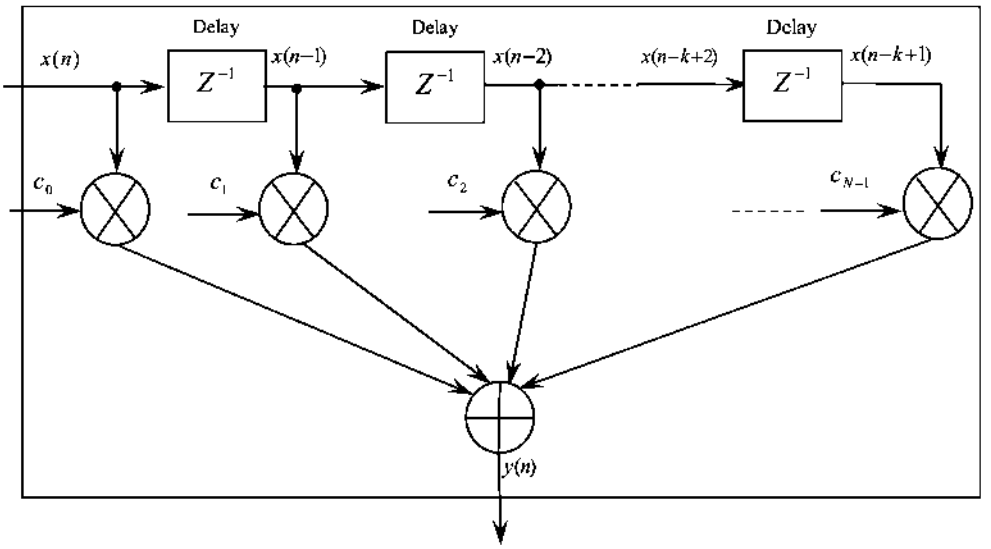

Fig. 2. An N-tap digital FIR filter.

can be used as an input signal statistics of the reference connected block. During the nth input signal sampling period, the sequence $[x(n), x(n-1), x(n-2), \ldots, x(n-k+1)]$ for the delay element block, we generate random input vector stream of 25 different values using input metrics P_{in}, D_{in}, S_{in}, T_{in}, while for the multiplier blocks of input c_n is fixed vector stream because of *fixed-coefficients* values. Then to construct the LUT, the filter is simulated 25 times and for each macro-block, 25 different values of input metrics are measured using functional simulations. The average power dissipation $P_{\text{FIR-filter}}$ is extracted using (6). We compare the estimated power $P_{\text{FIR-filter}}$ in (6) with the simulated power estimation to evaluate the accuracy of the power macro-model function in (1)

$$P_{\text{FIR-filter}} = \sum_{i=1}^{n} P_{\text{block}_{\text{i\_avg}}}. \tag{6}$$

For the delay element, the macro-model is constructed for one-bit, as there is no interaction between different bit slices, and the internal capacitances associated with each bit is approximately same for all the bits. The clock power is not considered, while making the power macro-model for one-bit delay element, as it is a constant number.

5. Experimental results

In this section, we show the results of our LUT based power macro-modeling approach. We have implemented this approach and built the power macro-model at the RTL. The accuracy of the proposed model is evaluated for our low-pass FIR filter. To do this, we generate random input vectors for different values of P_{in}, D_{in}, S_{in}, T_{in}, just to the delay element (shift registers) in Fig. 2. The power is estimated using Monte Carlo zero delay simulation technique. The power values extracted by LUT are compared to those obtained from simulations, and the average and maximum errors are computed. In [16,17] the macro-models gives very good results, but it does not give good accuracy for the case when one of input has constant values. This however, is a very common case in DSP systems, where adders and multipliers used to implement digital filters have one constant input; we refer to these as being *fixed-coefficient* multipliers.

The characteristics of the filter are shown in Table 1. We have considered unsigned Array multipliers of fixed-coefficient values of 8, 16-bit width and ripple carry adders of 8, 16–32 bit width respectively. The magnitude and the phase response is shown in Fig. 3. We have generated various randomly input values of P_{in}, D_{in}, S_{in}, T_{in} of range between $[0, 1]$. In Table 2, we illustrate the set number of the input vectors and the average relative errors of the estimate values obtained with our macro-model. Reference values for the circuit's power dissipation are obtained using time delays from the Synopsys PowerCompiler. It is evident from this table that the function is more accurate estimating the average power in some cases than others. The given input metrics values are more accurate for the specify range between $[0.2, 0.8]$ and less accurate between $[0, 0.2]$ and $[0.8, 1]$. One important source of error comes from do not consider on the macro-model, the power consumption of interconnects among different macro-blocks, and also other factors like glitch activities. For an individual block, we measured just 1–2% error. But for the entire filter with interconnects the error is 20–40%. In our experiments, the average error is 26.34%.

The results demonstrate that the transition density D_{in} is very effective to estimate power dissipation and relatively linear to the power measures. The correlation metrics S_{in} and T_{in} do not affect significantly the power dissipation and are less sensitive than the transition density. Regression analysis is performed to fit the model's coefficients. Fig. 4 illustrates

Table 1
Low-pass filter specifications.

Characteristics	Fixed point equiripple low-pass filter
Sampling frequency	102,550 Hz
End of the passband	70
Beginning of the stopband	14,900
Passband ripple	0.1
Stopband attenuation	11

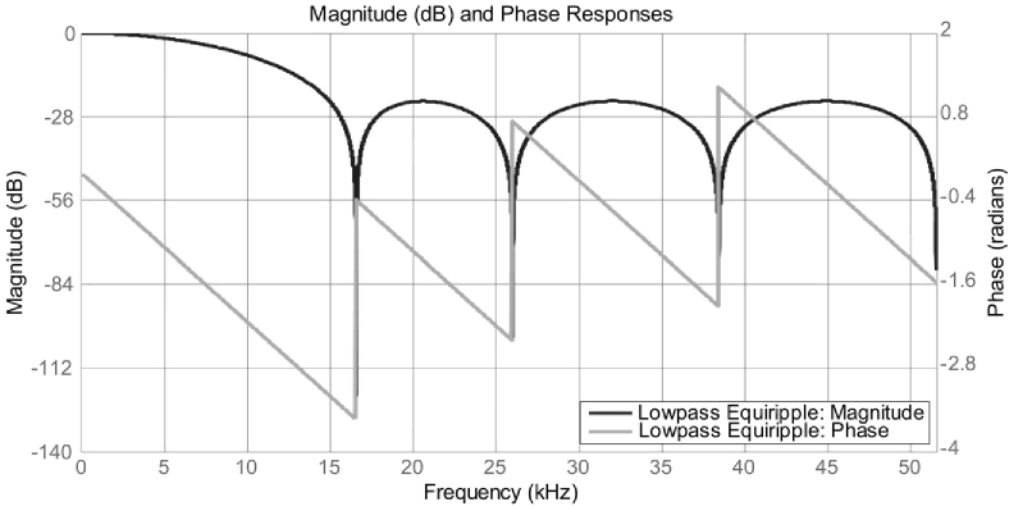

Fig. 3. Magnitude and the phase response of the FIR filter.

Table 2
Accuracy of power estimation.

FIR filter sets	Average error
Set-1	3.82%
Set-2	20.15%
Set-3	27.41%
Set-4	32.78%
Set-5	30.91%
Set-6	36.74%
Set-7	3.47%
Set-8	8.24%
Set-9	28.47%
Set-10	24.49%
Set-11	30.66
Set-12	54.82%
Set-13	39.13%
Set-14	38.06%
Set-15	47.03%
Set-16	28.52%
Set-17	50.96%
Set-18	20.25%
Set-19	18.81%
Set-20	21.95%
Set-21	9.27%
Set-22	11.57%
Set-23	18.23%

the correlation between the simulated power estimation and the estimated power values. For the FIR filter, we measured good correlation coefficient that is around 74%. Dotted circles in Fig. 4 indicate those spots where the error is much larger and the convergence coefficient decreases, especially when the given input metrics value is between [0, 0.2] or [0.8, 1]. The minimum simulations length can be determined through convergence analysis. Converging on the average power figure help us to identify the minimum length necessary for each simulation, by considering when the power consumption gets close to a steady value. We found the interval length is 4000 for the FIR filter. The warm-up length was about 800 while the steady state value at 2000.

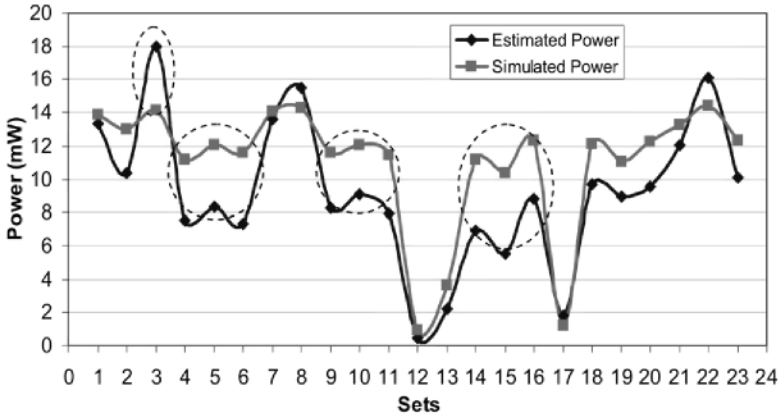

Fig. 4. Power comparison between macro-model and reference simulated power. Larger error spots for metric values between [0, 0.2] or [0.8, 1].

6. Conclusions

Power is a strongly pattern dependent function. Input statistics greatly influence on average power. We solve the pattern dependence problem for IP designs. We analyzed the application of linear and non parametric regression for the automatic construction of RTL power macro-models. In this way we generate macro-models that approximately take into account not only the transition activity at the I/Os, but also the input arrival times and the spatio-temporal correlation of the data.

We have presented a new power macro-modeling technique for high-level power estimation applied on FIR filter using different DSP macro-blocks. In our preliminary work, for individual blocks, we measured just 1–2% error. But now for an entire filter with interconnects between those blocks, the error is 20–32%. This is because the macro-model should consider the power consumption of the interconnects among different macro-blocks and other factors like glitches. We demonstrated relatively better accuracy in some cases than in others. Our model showed an average error of 26.34% and a correlation coefficient of 74%. Currently, we are evaluating our macro-model on other digital systems and improving its accuracy.

References

[1] A.A. Ghose, S. Devdas, K. Keutzer, J. White, Estimation of average switching activity in combinational and sequential circuits, in: Proc. 29th Design Automation Conference, June 1992, pp. 253–259.
[2] F.N. Najm, R. Burch, P. Yang, I.N. Hajj, Probabilistic simulation for reliability analysis of CMOS circuits, IEEE Trans. Comput.-Aided Design Integrated Circuits Syst. 9 (4) (1990) 439–450.
[3] R. Marculescu, D. Marculescu, M. Pedram, Logic level power estimation considering spatiotemporal correlations, in: Proc. IEEE International Conference on Computer Aided Design, November 1994, pp. 224–228.
[4] G.Y. Yacoub, W.H. Ku, An accurate simulation technique for short-circuit power dissipation, in: Proc. International Symposium on Circuits and Systems, 1989, pp. 1157–1161.
[5] C.M. Huizer, Power dissipation analysis of CMOS VLSI circuits by means of switch-level simulation, in: IEEE European Solid State Circuits Conf., 1990, pp. 61–64.
[6] C. Deng, Power analysis for CMOS/BiCMOS circuits, in: Proc. 1994 International Workshop on Low Power Design, April 1994, pp. 3–8.
[7] R. Burch, F.N. Najm, P. Yang, T. Trick, A Monte Carlo approach for power estimation, IEEE Trans. VLSI Syst. 1 (1) (1993) 63–71.
[8] A.A. Ismaeel, M.A. Breuer, The probability of error detection in sequential circuits using random test vectors, J. Electron. Test. 1 (1991) 245–256.
[9] S. Gupta, F.N. Najm, Power macromodeling for high level power estimation, in: Proc. 34th Design Automation Conference, June 1997.
[10] S. Gupta, F.N. Najm, Analytical model for high level power modeling of combinational and sequential circuits, in: Proc. IEEE Alessandro Volta Workshop on Low Power Design, March 1999.
[11] Z. Chen, K. Roy, T.L. Chou, Power sensitivity—A new method to estimate power dissipation considering uncertain specifications of primary inputs, in: Proc. IEEE International Conference on Computer Aided Design, November 1997.
[12] Z. Chen, K. Roy, A power macromodeling technique based on power sensitivity, in: Proc. 35th Design Automation Conference, June 1998.
[13] S. Gupta, F.N. Najm, Power macromodeling for high level power estimation, in: Proc. IEEE Transactions on VLSI, 1999.
[14] X. Liu, M.C. Papaefthymiou, Incorporation of input glitches into power macromodeling, in: Proc. IEEE Int. Symp. on Circuits and Systems, May 2002.
[15] Y.A. Durrani, T. Riesgo, Statistical power estimation for IP-based design, in: Proc. IEEE Conference on Industrial Electronics Society, November 2006, pp. 4935–4939.
[16] Y.A. Durrani, T. Riesgo, Power macromodeling for IP modules, in: Proc. IEEE International Conference on Electronics, Circuits and Systems, December 2006, pp. 1172–1175.
[17] Y.A. Durrani, A. Abril, T. Riesgo, Efficient power macromodeling technique for IP-based digital system, in: Proc. IEEE International Symposium on Circuits & Systems, May 2007.
[18] X. Liu, M. Papaefthymiou, A static power estimation methodology for IP-based design, in: Proc. IEEE Conference on Design, Automation, & Test in Europe, 2001.
[19] X. Liu, M.C. Papaefthymiou, HyPE: Hybrid power estimation for IP-based systems-on-chip, Proc. IEEE Trans. CAD Integrated Circuits Syst. 24 (7) (2005) 1089–1103.
[20] Y.A. Durrani, T. Riesgo, F. Machado, Power estimation for register transfer level by genetic algorithm, in: Proc. International Conference on Informatics in Control Automation and Robotics, August 2006, pp. 527–530.
[21] Y.A. Durrani, T. Riesgo, F. Machado, Statistical power estimation for register transfer level, in: Proc. International Conference for Mixed Design of Integrated Circuits and Systems, June 2006, pp. 522–527.

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