Highly Efficient Linear Power Amplifier for Driving Fast Slew Rate Capacitive Loads

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I. INTRODUCTION

The role of modern inkjet printing is becoming more and more important in applications such as marking of food, beverage and medical packaging as well as in large format applications such as the reproduction of billboards and banners. It is here that power operational amplifiers are fulfilling a crucial role in the design of inkjet printers. The piezoelectric technique of inkjet printing employs a crystal that flexes whenever a voltage pulse is applied to the piezo transducer, thereby forcing a droplet of ink out of the nozzle. Each time a voltage pulse is applied to the piezoelectric material, it deforms, forcing a tiny droplet 50 to 60 microns in diameter onto the surface to be printed. When the voltage returns to zero, the material is restored to its original shape, drawing ink into the reservoir and thus preparing it for the application of the next drop. This cycle repeats many times per second, each time the print head makes a pass across the printing area. A representative printing head configuration might employ a single power amplifier to drive up to 1024 nozzles with an equivalent load of approximately 100nF. The power amplifier may be connected to any number of nozzles at any one instant—from 0 to 1024. At any instant, the print head with 1024 nozzles is emitting anywhere from 0 to 1024 ink droplets as governed by the printing program instructions. Various waveforms have been devised for printing various kinds of inks and media. These waveforms are developed empirically and are then stored in a computer so that the optimal waveform for each ink and its specific application can be retrieved at a later time. The simplest is a trapezoidal waveform, which has a controlled ramp on the up slope and a ramp with a possible slightly different slope on the down side. These slopes are well controlled but not necessarily symmetric. The rise on

the up slope is likely to be faster, whereas on the down slope a longer fall time is necessary. This ensures sufficient ink will flow from the ink magazine to the nozzle chamber to supply ink for the next droplet to be dispensed. The power amplifier must be designed to deal with any arbitrary wave shape that may be required for a given printing solution.

The most common solution for the power amplifier that has to reproduce these trapezoidal waveforms is a linear one (Class B or AB). However, the main problem with this approach is the high power losses due to the charging and discharging of the capacitive load [1-3]. Fig.1 and Fig.2 show the output stage of a linear amplifier (implemented with MOSFETs) and currents that are conducted by each transistor in the case of a piezo-electric load (capacitive load) and trapezoidal output voltage. It can be easily seen that the transistors have to dissipate power during the charging and discharging as well. If we assume an ideal class B amplifier driving a typical industrial inkjet print head, with specifications given in Table 1, worst-case power consumption is as follows:

$$P_{loss \text{ positive edge}} = I_{load} t_{rise} f_{pulse_max} (V_{supply} - V_{average \text{ out}}) \quad (1)$$

$$I_{load} = C_{load} \frac{dV_{out}}{dt} = 4.5A \quad (2)$$

$$P_{loss \text{ positive edge}} = P_{loss \text{ negative edge}} = 93W \quad P_{total} = 186W \quad (3)$$

Having in mind that the supply voltage needs 10V to 15V of headroom so that the output signal is not distorted the power dissipation is higher than 200W and Such considerable power dissipation is undesirable because of the size of the required heat sinking and the negative impact on operational costs of the inkjet printing machine. In this paper we present a linear PA that employs Envelope Tracking in order to significantly decrease the power consumption. Firstly, an analysis regarding the possible architectures is presented and later the experimental

results that clearly show huge power savings that can be obtained.

TABLE I. SPECIFICATIONS OF THE INKJET PIEZO-ELECTRIC LOAD

Load	Capacitive (150pF – 150nF)
Output voltage range	0V – 135V
Slew rate of the output voltage	45 V/ μ s
Pulse frequency	Up to 110kHz
Positive voltage supply	140V
Negative voltage supply	-10V

Fig. 1. Output stage of a class B amplifier with capacitive load

Fig. 2. Voltage and current waveforms in the case of a capacitive load and trapezoidal output voltage

II. POSSIBLE SOLUTIONS FOR THE INKJET PRINTER HEAD DRIVER

Having in mind that the piezoelectric load is practically a capacitor, application where the real output power hardly exists, the most promising solution for the driver of the ink jet printer head would be a bidirectional dc-dc converter, which could be implemented with relatively high efficiency, small size as well as low weight. Some of the most common solutions are based on a bidirectional buck converter [4-6], full bridge [7, 8], flyback [1] and even an LLC converter [9]. Depending on the voltage needed to correctly drive the piezo load, the driver could be implemented in a single stage [10] or in a two stages [11,12]. Although this approach might be very efficient, there are two important drawbacks from the point of view of the analyzed application:

- Voltage/current ripple
- Pulse dynamic, i.e. driver bandwidth

The inkjet printer head requires the driving voltage to be as smooth as possible in order to avoid excessive power losses on the parasitic resistances of the piezo load. It implicitly has an important impact on the design of the converter's output filter and on the selection of its switching frequency. Nevertheless, due to the very fast voltage slew rates that have to be reproduced, the output filter has to be relatively light, which consequently leads to a solution with a very high switching frequency. Some simplified simulations that were conducted showed that the needed bandwidth for the driver is close to 1MHz, therefore the switching frequency is at least 7MHz–10MHz. This high switching frequency in combination with relatively high voltages and currents may lead to very high switching losses, unless GaN transistors are employed. Additionally, in order to guarantee a high quality of the output waveform (very low ripple) at least a second order filter would be required which complicates the design. This could be seen as a drawback from the point of view of potential customers as GaN technology is not as mature as Si.

On the other hand, linear power amplifiers were the most employed during the early development period of drive amplifiers. Class A, class B or class AB linear amplifiers suffer from very high power losses, but have distinct advantages, such as low signal distortion, good static performance, high integration level, simple structure and low electromagnetic interference.

Combining these two approaches it is possible to exploit good sides of each technique. The stage that will drive the piezo load will be implemented with a class AB amplifier, providing a good linearity and wide bandwidth, while a highly efficient dc-dc converter will supply it with a dynamic voltage, following as close as possible the output voltage.

The considered approach was to apply an envelope tracking technique in which the linear PA is supplied with a variable voltage following the output voltage in order to decrease the voltage drop of the pass element (MOSFET). The reasons to use this technique were that there is already a linear amplifier that is capable of driving the desired loads and its design includes all the necessary protections and any variation of the supply voltage would be filtered thanks to the amplifier's Power Supply

Rejection ability, and, in that way, the high quality of the output signals is maintained. In order to implement it correctly, the variable voltage supply should follow the output as close as possible, but in this way it would be necessary to switch at very high switching frequencies, just like in the case of a piezo driver based on a dc-dc converter. The design of the output filter would be easier due to the class AB amplifier's Power Supply Rejection Ratio, but the high switching frequency would be needed once again in order to have an output filter with "low inertia" which would enable fast tracking of the output voltage. Therefore, in order to avoid an envelope tracker that employs high switching frequency (and suffers from the associated power losses), a solution based on a multilevel converter was applied [13]. The main idea can be seen in Fig.3. The PA's voltage supply roughly follows the output voltage producing multilevel voltages. In this way, the voltage drop on the conducting MOSFET is decreased significantly, in comparison with the constant voltage supply case, and the switching frequency is one order of magnitude lower than in the case of the solution based on a PWM dc-dc converter. It is important to notice that the load is strictly capacitive and as a consequence of that it is easy to determine which MOSFET of the PA's output stage conducts at any time. For example, the rising edge of the output voltage means positive current to the load, i.e. the n-channel MOSFET conducts, and it is necessary to vary only the positive supply voltage, while the negative can be maintained at a constant level. A similar conclusion can be drawn for the falling edge of the output voltage. In another words, although the linear PA has two voltage supply rails, it is necessary to modulate only one at a time.

Using this information, it is possible to use a single multilevel converter to modulate both (positive and negative) voltage rails as presented in Fig.4. The main idea is to multiplex the single multilevel converter output to the positive and to the negative supply rail by a set of switches together with two fixed voltages. The switches are controlled like it is presented in Table II.

Power savings will be obviously made during the rising edge because of the relatively low voltage drop across the nMOS transistor. In the case of the falling edge energy savings are due to the fact that the load capacitance energy is returned to the input source (pMOS transistor drain has positive voltage) and once again due to the low voltage drop across the employed pMOS transistor.

III. ANALYSIS, OPTIMIZATION AND PROPOSED ARCHITECTURE

The multilevel converter can be implemented using switching cells that are placed in series, like it is explained in [13] or by generating all the necessary voltage levels and then employing a voltage level selector (analog multiplexer) [14, 15]. In the case of the implementation with switching cells, each switching cell needs an independent voltage supply and having in mind that there is only one main voltage input, all cell voltage supplies have to be generated by a single-input-multiple output converter, Fig. 5. In order to avoid the complexity of this converter, the multilevel cells can be implemented as three-level (full bridge) cells that are capable of adding and subtracting voltages. In the case of the implementation with an analog

multiplexer, it is necessary to generate all the voltage levels using a single-input-multiple output converter, as well, but the outputs do not have to be mutually isolated. Nevertheless, the voltage selector has to be implemented with two MOSFETs in series, Fig.5. Another drawback of this approach is that each voltage level is formed by an independent voltage source.

TABLE II. STATE OF THE MULTIPLEXER SWITCHES DEPENDING ON THE OUTPUT VOLTAGE

Time instant	Closed switches
Rising edge	SW_B and SW_D
Falling edge	SW_A and SW_C
Maximum voltage	SW_A and SW_C
Minimum voltage	SW_B and SW_D

Fig. 3. Simplified representation of the load voltage and multilevel voltages supplied to the rails of the linear PA

Fig. 4. Simplified schematic of the proposed solution for the envelope tracker based on a single multilevel converter

In order to decrease the complexity of the single-input-multiple output converter that is needed in both implementations of the multilevel converter, it was decided to employ only three level cells. Next step was to select the number of voltage levels that should be implemented and their distribution. The power loss calculation was performed under the following assumptions:

- the load is a 50nF capacitor
- the pulse pattern is composed of three pulses (100%, 75% and 50% of maximum amplitude) with repetition rate of 110kHz

The optimization of the number of the applied voltage levels and their distribution showed that the voltage levels should be equidistantly distributed. Fig. 6 shows the total calculated power losses depending on the number of applied voltage levels. The presented power losses do not include power losses in the stage that has to generate the needed cell voltage supplies and auxiliary supplies or switching and conduction losses of the employed switching cells. Nevertheless, these results point to two very important conclusions:

- Power losses in the linear amplifier quickly decrease with just a few voltage levels applied
- Increasing the number of levels beyond four does not bring a huge advantage from the point of view of power saving. However, it makes the overall system significantly more complex because each voltage level needs additional electronics (MOSFET driver and level shifters for the logic signals) and auxiliary supply.

These conclusions led to the decision to use four levels and the multilevel converter was implemented as it is shown in Fig. 7, using a main power supply of 140V (V_{in}), one three-level cell supplied by 35V and one highly efficient buck converter that produces 70V. The cell voltage supply was implemented with a flyback converter due to its robustness and simplicity. In a standard approach it would be necessary to use two envelope trackers to supply the linear amplifier (one for the positive and one for the negative rail).

Fig. 5. Multilevel implementation with switching cells (left) and voltage level selector (right)

Fig. 6. Power losses in the linear amplifier depending on the number of applied voltage levels

However, by analyzing Fig. 3, it can easily be seen that there is only one supply rail that is modulated at a time. Thanks to this, only one envelope tracker can be used to modulate both supply rails and it is implemented by combining the multilevel converter with an analog multiplexer (MOSFETs Q5-Q7) that is shown in Fig. 7, as well.

Additionally, the flyback converter that supplies the three level switching cell, produces the negative voltage that has to be applied to the negative supply rail ($-V_s = -10V$) and two auxiliary voltage supplies for the transistor drivers in the analog multiplexer. The flyback converter processes a very low share of the total power budget because the three-level cell alternates its output and during the period of one voltage pulse it practically does not provide energy to the piezo load. It supplies only the energy lost due to the switching and conduction losses. The bulk power comes directly from the main input voltage and the buck converter.

Fig. 7. Simplified schematic of the proposed multilevel converter

Fig.8. shows a pie chart that represents the power processed by each voltage source in the case of the load of 110nF and 110 kHz repetition rate for the multilevel converter from Fig.7 during the rising edge of the pulse. It can be seen that the 35V voltage source contributes with less than 5% of the output power just like previously explained, while the 70V and 140V sources provide almost the complete output power. This conclusion is important because the average power of the 35V source will determine the size of the flyback transformer, while the average power of the 70V source will determine the size of the buck inductor. The power demanded from the 140V source is supplied in an extremely efficient way via one MOSFET and this helps a lot to avoid unnecessary power conversion and power losses.

To obtain better and more precise estimation of the overall losses, switching and conduction losses of the three level cell and the multiplexer should be added to the results shown in Fig. 6. Additionally, there will be some static power consumption due to the auxiliary voltages that are necessary to supply MOSFET drivers and level shifters for the gate signals. A rough estimation of these losses and complete MOSFET switching and gate losses is around 8W-10W, while the static power consumption will be between 2W and 5W. Therefore, additional power consumption due to the switching cell and multiplexer is between 10W and 15W.

It is interesting and important to notice that as a consequence of this additional power consumption there is a minimal load for which it is useful to apply this technique. For example, in the case of a pulse of the maximum amplitude (135V) the minimum load for which this technique could be applied is around 10nF. Naturally, depending on the pulse repetition rate and the probability of each pulse, this minimum load will differ.

Employing the multilevel converter with the analog multiplexer in the aforementioned way will supply the positive voltage rail of the linear PA with: 35V, 70V, 105V and 140V, while the negative rail is supplied by 105V, 70V, 35V and -10V (additional output of the flyback converter).

IV. EXPERIMENTAL VERIFICATION

A prototype of the proposed envelope tracker was constructed and a simplified schematic of the system can be seen in Fig.9. Rather than using an external input signal, an FPGA was used to store and generated a pulse pattern, as well as the control signals for the multilevel converter and the analog multiplexer switches. The system was tested with relatively high capacitive loads (47nF, 94nF and 140nF) because the power losses are the most critical in these cases.

Two pulse patterns were used:

- a single pulse with maximum amplitude and frequency
- three subsequent pulses with 100%, 75% and 50% of the maximum amplitude (to emulate more realistic inkjet pulses)

Fig.10 and Fig.11 show the PA output and supply voltages for single- and multi-pulse operation, driving different loads (95nF vs. 47nF), at maximum pulse repetition rate (110kHz). Table III presents an overview of the measured power consumptions and measured power savings. It can be seen that the power savings vary between 30% and almost 50%, depending on the pulse characteristics.

Fig. 8. Net power demanded from each voltage source in the proposed multilevel converter during the rising edge of the output pulse ($C_{load}=110nF$ and $f_{pulse}=110kHz$)

Fig. 9. Simplified schematic of the implemented system

TABLE III. AN OVERVIEW OF THE OBTAINED POWER SAVINGS FOR DIFFERENT PULSE PATTERNS AND CAPACITIVE LOADS

Output waveform	Repetition rate	Capacitive load	Measured Power dissipation Multilevel supply	Measured Power dissipation Constant voltage	Power Savings
Single pulse, maximal amplitude	110 kHz	47 nF	71W	106W	33%
Single pulse, maximal amplitude	110 kHz	95 nF	120W	222W	46%
Single pulse, maximal amplitude	30 kHz	140 nF	54W	87W	38%
Three pulses, 100%, 75% and 50% amplitudes	30 kHz	47 nF	51W	89W	43%

For the last test case, three pulses of different amplitude Fig. 11), an estimation of the power loss and power loss breakdown is shown in Fig. 12. It can be seen that the linear PA contributes most to the power loss, two thirds, approximately. The rest is a combination of the MOSFET switching losses, conduction losses and converter static losses. The static losses are practically one third of the losses of the proposed multilevel converter and in order to decrease this the design of the auxiliary supplies should be optimized.

Fig. 10. Load voltage (magenta trace, 110kHz, amplitude of 130V, 95nF load) and Multilevel voltages at supply rails (green and red traces) (20V/div, 1µs/div)

Fig. 11. Load voltage (magenta trace, 110kHz) and Multilevel voltages at supply rails (red and green traces) in the case of 47nF load and three different pulses

Fig. 12. Estimated power loss breakdown in the case of the pulse pattern with three different pulses ($C_{load}=47nF$, pulse pattern repetition rate 30kHz)

V. CONCLUSIONS

The paper describes a way to mitigate power dissipation of linear amplifiers driving capacitive loads (inkjet printer heads) by means of an envelope tracking (ET) power supply. Due to the very fast voltage slew rate that has to be reproduced (45V/µs) in combination with high voltages and currents (135V and 5A), power amplifiers or envelope tracker based on a switching dc-dc converter might suffer from high switching losses. Due to this, it was decided to employ a multilevel converter that approximately tracks the output voltage. In this way the switching frequency of the multilevel is comparable to the frequency of the reproduced voltage pulse.

Having in mind that the load is purely capacitive, in every time instant it is known which transistors conduct in the output stage of the linear PA. This information is used to modulate only one power supply rail and, in that way, use only one multilevel converter that is intelligently multiplexed with constant voltage supplies.

A prototype was built to prove the concept and the results clearly show that it is possible to obtain power savings between 30% and 50% (depending on the load, frequency, pulse pattern etc.) in comparison to the PA being supplied with constant voltages. By analyzing the obtained results it was seen that approximately one third of the power losses are due to the employed multilevel converter and analog multiplexer. Further improvements can be realized by improving the design of the auxiliary supplies and by employment of GaN transistors.

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