Development of the lattice matched GaInP/GaInAs/Ge triple junction solar cell with an efficiency over 40%

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Abstract—This paper summarizes the state-of-the-art of the lattice matched GaInP/Ga(In)As/Ge triple-junction solar cell developed at the Solar Energy Institute of UPM (IES-UPM). Different research topics tackled over the last years about this structure are described. As result of this work, an efficiency of $\sim 40\%$ at $\sim 415\times$ is presented.

Keywords—multijunction solar cell, MOVPE, III-V semiconductors, Ge wafers.

I. INTRODUCTION

Concentrator Photovoltaic (CPV) technology is based on III-V Multijunction Solar Cells (MJSC) which are especially suitable for harvesting solar energy since they possess the highest conversion efficiency among PV technologies.

The monolithic two-terminal lattice matched GaInP/Ga(In)As/Ge triple-junction solar cell (3JSC) is an established architecture that has been widely used in the CPV industry. This kind of solar cell has reached a record efficiency of 41.6% at 364 suns [1] and the state-of-the-art efficiencies in industrial products are in the range of 39-40%. Despite new architectures are being developed (i.e., UMM, IMM, wafer bonded, dilute nitrides...) with champion efficiencies of $\sim 44-46\%$ [2, 3], the aforementioned lattice matched 3JSC is still the workhorse of the CPV market due to its robustness, technological maturity and lower production costs. This is why one of the main efforts over the last years at the Solar Energy Institute of UPM (IES-UPM) has been to improve the lattice matched $\text{Ga}_{0.51}\text{In}_{0.49}\text{P}/\text{Ga}_{0.99}\text{In}_{0.01}\text{As}/\text{Ge}$ triple-junction solar cell whose efficiency has reached values close to the state-of-the-art. An important added value of this research has been the deep comprehension of the interaction between layers and materials during the MOVPE process that will be of great help in the development of MJSCs with more than three junctions that the III-V Semiconductor Group at IES-UPM is also pursuing.

II. EXPERIMENTAL

3JSCs were grown on a horizontal, low pressure Aixtron MOVPE reactor AIX 200/4. AsH_3 , PH_3 , TMGa , TMAI , TMIIn , DETe , DMZn , DTBSi_2 and CBr_4 are used as constituent and dopant precursors. P-type gallium doped Ge (100) wafers with 6° misorientation to [111] were used.

Reflectance Anisotropy Spectroscopy (RAS) was used as a highly surface-sensitive spectroscopic in-situ tool during the epitaxial growth of the semiconductor layers. 3JSC epiwafers were processed following conventional photolithographic techniques. The front grid geometry used was the inverted square configuration with an active area of 1 mm^2 [4]. AuGe/Ni/Au is used for the front contact on n-GaAs, while pure gold is used for the back contact on Ge. Antireflective coatings (ARC) were deposited to minimize optical losses. Typical ARC layers used at IES-UPM are a ZnS/MgF_2 stack with thicknesses of $\sim 40-50\text{ nm}$ for the ZnS and $\sim 80-100\text{ nm}$ for MgF_2 .

Material and solar cell characterization is of paramount importance in these developments. As an example, X-ray diffraction, Atomic Force Microscopy or Electro-Capacitance-Voltage have been widely used during each epitaxial batch to get information about semiconductor layers quality. Additionally, in this work Secondary Ion Mass Spectroscopy (SIMS) with Cs^+ primary ions detection and negative ions detection was used for the quantification of Ge in the first two semiconductor layers (GaInP nucleation and Ga(In)As buffer layer) and also for doping profiles in the tunnel junctions. A custom-built External Quantum Efficiency (EQE) setup based on a Xe-lamp source and a monochromator is used. Short-circuit current density (J_{sc}) was calculated from the convolution of the EQE with the reference spectrum (AM1.5d ASTM G173-03 normalized to 1000 W/m^2). Measurements under concentration were performed with a flash simulator. For a detailed explanation of the concentration set-up, the reader is referred to [5].

III. RESULTS AND DISCUSSION

A 3JSC is a complex structure that consists of more than 20 layers of III-V ternaries and quaternaries of the arsenide and phosphide relatives. In order to accomplish a good performance of the solar cell it is mandatory that each layer achieves specific characteristics in terms of thickness, lattice-matching, doping level, band lineup at the heterostructure interfaces, etc. Thus, a close interaction between epitaxy, material and device characterization together with simulation is a must. A schematic of the standard version of the lattice matched GaInP/GaInAs/Ge 3JSC structures developed at IES-UPM is shown in Fig. 1. In the following, the research

topics tackled in the last years about this structure at IES-UPM are described.

TC	CAP	400nm n+ GaAs[Si,Te] $> 2 \cdot 10^{18} cm^{-3}$
	Window	25nm n AlInP[Te] $> 5 \cdot 10^{18} cm^{-3}$
	Emitter	24nm n GaInP[Te] $\sim 3 \cdot 10^{18} cm^{-3}$
		70nm n GaInP[Te] $> 7 \cdot 10^{17} cm^{-3}$
		45nm n GaInP[Si] $\sim 7 \cdot 10^{17} cm^{-3}$
TJ	Base	1300nm p GaInP[Zn] $\sim 9 \cdot 10^{16} cm^{-3}$
	BSF	100nm p AlGaInP[Zn] $\sim 4 \cdot 10^{18} cm^{-3}$
	Anode	25nm p++ AlGaAs[C] $\sim 6 \cdot 10^{19} cm^{-3}$
	Cathode	20nm n++ GaInP [Te] $\sim 1 \cdot 10^{19} cm^{-3}$
	Window	20nm n GaInP [Si] $> 1 \cdot 10^{18} cm^{-3}$
MC	Emitter	140nm n GaInAs [Si] $\sim 1 \cdot 10^{17} cm^{-3}$
	Base	3320nm p GaInAs [Zn] $\sim 1 \cdot 10^{17} cm^{-3}$
	BSF	150nm p AlGaAs [C] $\sim 1 \cdot 10^{18} cm^{-3}$
	p-barrier	30nm p+ AlGaAs [C] $\sim 5 \cdot 10^{19} cm^{-3}$
	Anode	20nm p++ AlGaAs [C] $\sim 5 \cdot 10^{19} cm^{-3}$
TJ	Cathode	20nm n GaAs [Te] $\sim 2 \cdot 10^{19} cm^{-3}$
	n-barrier	50nm n AlGaAs [Te] $\sim 4 \cdot 10^{18} cm^{-3}$
	Buffer	500nm n GaInAs [Si] $\sim 1 \cdot 10^{18} cm^{-3}$
	Nucleation	50nm n GaInP [Si] $\sim 1 \cdot 10^{18} cm^{-3}$
	Emitter	
BC	Substrate p ⁺⁺ Ge	

Fig. 1. Semiconductor structure of the GaInP/GaInAs/Ge solar cell developed at IES-UPM. Ge bottom cell (BC), Ga(In)As middle cell (MC) and GaInP top cell (TC) are series-connected by tunnel junctions (TJs).

A. MOVPE growth of III/V materials on Ge substrates

Germanium wafers are typically used as the substrate of choice for the epitaxial growth by MOVPE of semiconductor structures of 3JSCs for space and terrestrial concentrator applications [6]. However, Ge wafers add extra challenges on the epitaxial growth, in comparison to MJSC grown on GaAs or InP substrates. First, since Ge presents a non-polar structure, a heteroepitaxial routine is required to grow defect-free polar III-V layers on a Ge substrate. This can be accomplished by the use of a misoriented Ge substrate [7], together with a dedicated surface preparation prior to growth [8-11]. For this particular case, RAS has been used as an in-situ characterization technique in order to have a careful control of the growing surface. As an example, with this technique, the heteronucleation of GaInP layers on Ge was carefully controlled in terms of Ge wafer preparation, PH_3 annealing conditions and GaInP growth parameters [12].

Secondly, the cross-diffusion that takes place during the epitaxial growth must be controlled. On the one hand, group III and V elements are dopants in Ge. This is of key relevance when the Ge wafer has to act as a solar cell (as is the case of GaInP/Ga(In)As/Ge triple junction solar cells) since the diffusion of these elements determines the configuration of the resulting Ge p/n junction and thus rules the solar cell performance [13, 14]. With the aim of designing shallower emitters and due to the lower diffusion coefficient of P in Ge, in comparison to As, a GaInP nucleation layer is used instead of a GaAs one.

On the other hand, Ge is in turn a dopant in III-V semiconductors as reported in several studies [15-17], that can diffuse into the first III-V epilayers during the epitaxial growth. We refer to this process as Ge solid-phase diffusion. Secondary Ion Mass Spectroscopy (SIMS) has been used to assess the impact of the Ge solid-phase diffusion in the first III-V layers deposited on Ge substrates. Ge penetrates not only the GaInP nucleation layer but also reaches the subsequent GaInAs buffer layer, which is made thick enough

(~500 nm) to avoid Ge to reach active layers grown afterwards such as the first tunnel junction (see Fig. 2).

Fig. 2. SIMS measurement of the Ge concentration in the first two layers grown on a complete 3JSC (~50nm GaInP and ~500nm Ga(In)As). Ge in-diffusion penetrates the thin GaInP nucleation layer and reaches the Ga(In)As buffer layer with a diffusion profile up to 215nm. The flat region on the left corresponds to the region where Ge autodoping dominates over Ge in-diffusion.

In addition to solid-phase diffusion, Ge autodoping is another phenomenon causing an additional source of Ge contamination into III-V materials, associated with Ge atoms evaporated or etched from the Ge substrate that reach the front growth surface and thus can be incorporated into III-V epilayers as an unintended background dopant. A deep analysis was performed on GaInP and GaInAs layers grown lattice matched to Ge substrates. The role of V/III ratio and temperature together with reactor pre-conditions have been found to be key aspects to be considered when growing on Ge substrates [18]. In the particular case of the 3JSC developed at IES-UPM, Ge contamination was more intense in GaInP layers (such as the GaInP TC) than in GaInAs layers due to the growth parameters used in each case. Additionally, Ge contamination was found to be minimized with a reactor preconditioning based on a GaInAs/GaInP/GaInAs coating [18].

B. Improvement of the Ge BC

In the design of the lattice matched 3JSC (see Fig. 1), the Ge wafer has also a photovoltaic role acting as the Ge bottom cell (BC). Therefore, the characteristics of the Ge BC are the result of the direct processes designed for its formation (i.e. the so called nucleation) and the indirect processes that the subcell withstands during the growth of the rest of the structure (in particular the thermal load associated with the growth of the upper subcells). A deep analysis has been performed in our group to understand the impact of the aforementioned thermal load. This study has confirmed that the V_{OC} obtained in Ge cells grown as single junction devices is significantly higher than that of a Ge BC in a 3JSC. This V_{OC} loss can be as high as 55 mV [19, 20] together with a drop in short-circuit current density in the BC of ~2.3 mA/cm² (due to thicker emitters as a result of a deeper III-V elements diffusion during the thermal load). Simulations confirm that all these losses can be explained by the degradation in the minority carrier properties at the emitter region, especially close to the GaInP/Ge interface [19]. With the aim of alleviating such thermal load, an emphasis was put on the design of new nucleation routines

(modifying the two first semiconductor layers) with lower thermal load. A significant improvement was achieved especially with a thinner GaInP nucleation layer (down to 50 nm) and a thinner GaInAs buffer (around 500nm) layer this last one together with a temperature reduction from 675°C to 600°C. This new design resulted in a better BC performance. After its integration in a complete 3JSC, a gain of 50 mV was achieved in comparison to the previous design developed in our group [21].

C. Development of a highly conductive, highly transparent tunnel junction

Monolithic series connection of the 3JSC subcells is achieved by using tunnel junctions, which are designed to have minimum optical absorption and low electrical losses. A highly transparent, high band gap tunnel junction (TJ) made from $p^{++}\text{AlGaAs:C}/n^{++}\text{GaInP:Te}$ has been developed in our group. This TJ was intended to be placed between the GaInP TC and the Ga(In)As MC to increase transparency from previous AlGaAs/GaAs designs [22]. Moreover, I-V curves of this new TJ design resulted in a device performance with a J_{peak} of 235 A/cm² which enables its operation with a negligible power loss up to concentrations of ~15.000 suns [23]. Despite the high bandgap of the materials used, which typically give rise to low tunneling, this high performance was achieved by inserting a quantum well at the junction, which modifies the band lineup and boost the tunneling current. As an example of the importance of a careful design of the heterostructures in the 3JSC design, with this new TJ, the middle cell window was changed from n-AlGaAs to n-GaInP window layer. This brought about a non-negligible series resistance (between the GaInP cathode and its neighboring n-GaInAs emitter) which was found to be mitigated with doping levels higher than $1 \cdot 10^{18}\text{cm}^{-3}$ [21, 24].

D. Improvement of the GaInP TC

An intensive work was done in our group [24, 25] to develop the GaInP TC in the quest for the optimum growth window to maximize its morphological quality (smoothness, lack of hillocks,...). This was carried out by optimizing epitaxial growth parameters such as growth temperature growth rate, V/III ratio... In order to increase the conversion efficiency of a 3JSC, the bandgap energy of the GaInP TC should be increased as much as possible [26]. This can be achieved by minimizing the degree of ordering of the alloy. A detailed work was done to reduce the ordering in both GaInP base [24] and GaInP emitter regions [21] using Sb as surfactant. Since Sb is introduced during the epitaxial growth of the GaInP layers, its role is to affect the growth surface by reducing the amount of P dimers present, which is the driving force for ordering. This was carefully controlled by in situ monitoring the growth with RAS [27]. The satisfactory reduction of CuPt ordering was confirmed by PL measurements [28] and also by EQE measurements which reveal an energy shift towards higher bandgaps in the cut-off wavelength without affecting the minority carrier lifetime [29]. Additionally TEM measurements confirmed both the modulation of the GaInP ordering and the persistence of the type of ordering (CuPtB) with the use of Sb [30].

Moreover, since the goal of the 3JSC devices developed is to work under high concentration (>1000 suns), the

conductivity of the front side of the solar cell has to be maximized. In addition to the well-known effect of lowering the emitter sheet resistance, we have found that when doping densities higher than 10^{19}cm^{-3} are achieved in the AlInP window, the current is able to spread through it, thus helping the emitter in the lateral current transport [31]. This can be achieved with the use of Se and Te as dopants [32]. For this, DTBSi precursor used in the AlInP window was substituted by DETe. Furthermore, the doping level at the GaInP emitter region was also slightly modified. A higher doping level ($7 \cdot 10^{17}$ - $3 \cdot 10^{18}\text{cm}^{-3}$ again with DETe) was achieved at the region close to the AlInP window interface and a lower doping level ($\sim 7 \cdot 10^{17}\text{cm}^{-3}$ with DTBSi) at the region close to the GaInP base. This way we could achieve a high conductivity while minimizing the impact of high doping levels on the carrier collection efficiency of the emitter [21].

E. 3JSC performance

3JSC batches were developed integrating the different improvements achieved during this study. The electrical performance of final 3JSC structures was analyzed. Fig. 3 shows an example of the external quantum efficiency of one structure without ARC. The EQE of each subcell with its corresponding short-circuit current J_{SC} is plotted. As it can be appreciated, a perfect current matching has been obtained between top and middle subcells.

Fig. 3 External Quantum Efficiency of the 3JSC developed in this work. Measurements carried out on devices without ARC layers.

As a final step of this work, ARC layers were deposited and the triple 3JSCs were measured under concentrated light. Fig. 4 shows the I-V curve of the best structure developed with an efficiency of ~40.04 % at ~415 suns.

Fig. 4. I-V curves at ~415X of the 3JSC developed at IES-UPM.

This result confirms the satisfactory development of the lattice matched 3JSC at IES-UPM. Additionally, most of the outcomes analyzed during this work are being implemented in other architectures in our group with more than 3 junctions with the goal of achieving even higher efficiencies > 45% (i.e; IMM or dilute nitrides).

IV. SUMMARY AND CONCLUSIONS

The lattice matched GaInP/GaInAs/Ge triple junction solar cell presented in this work is the result of an intensive work carried out over the last years at IES-UPM. Many challenges concerning this complex structure have been addressed in order to enhance its efficiency. Special consideration has been put on the epitaxial growth of III-V materials on Ge substrates, including Ge solid-phase diffusion and autodoping, etc. A new nucleation routine was developed to mitigate the effect of thermal load and to enhance its electrical performance with a gain of 50 mV. Additionally, a new tunnel junction was designed with a J_{peak} of 235 A/cm². Moreover, an increase of the energy band gap of the GaInP TC with the use of Sb as surfactant during its growth was achieved. Furthermore, the doping level of both GaInP TC and AlInP window layer were slightly increased with the use of DETe. As a result of all this work, a satisfactory efficiency of 40.04 % at 415 suns has been presented. Additionally, most of the aspects tackled in this work can be implemented in several architectures with more than 3 junctions where even higher efficiencies are expected (>45%).

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