DEPARTAMENTO DE AUTOMÁTICA, INGENIERÍA
ELECTRÓNICA E INFORMÁTICA INDUSTRIAL

ESCUELA TÉCNICA SUPERIOR DE INGENIEROS
INDUSTRIALES

CENTRO DE ELECTRÓNICA INDUSTRIAL

*Contributions to The Design Methodology of
Three-phase Active Rectifiers to Comply with
Avionic Standards: Input Voltage Distortion
and Phase Loss*

TESIS DOCTORAL

Autor: **Uroš Borović**

Máster en Electrónica Industrial, Universidad Politécnica de Madrid

Directores: **Pedro Alou Cervera, Jesús Ángel Oliver Ramírez**

Doctores Ingenieros Industrial por la Universidad Politécnica de Madrid

2019

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Посвећено мом оцу Јовану
Dedicated to my father Jovan

Acknowledgements

In the first place, I would like to express gratitude to my tutors: Professor Pedro Alou and Professor Jesús A. Oliver for giving me the opportunity to do my PhD thesis at the Centro de Electrónica Industrial, Universidad Politécnica de Madrid (CEI-UPM). The knowledge that I acquired in the field of power electronics during my five year long stay with CEI is already benefiting me in the industry. Beyond any doubt fundamentals that I learned and people that I met at CEI are going to be the basis for my further professional development, weather it may be in industry, academia or someplace else.

Secondly, it would have been impossible without the cooperation and strong support from my now ex CEI colleagues in the three-phase rectifier team that have already passed the threshold of obtaining their PhD titles: Dr. Sisi Zhao and Dr. Marcelo Silva. Thanks to you I learned a lot of details about power electronics design and control development.

Thirdly, I must express my sincerest gratitude to my BSc degree tutor, Professor Predrag Pejović from School of Electrical Engineering, University of Belgrade. Even though our collaboration was officially over back in July 2013, he continued to substantially offer me support whenever I needed it. When my motivation for this work was almost exhausted, he was there to encourage me and to give me small impulse of positive energy that returned me on the right track. For all those reasons, I am forever wholeheartedly thankful.

Besides, I'm also grateful to Prof. Pat Wheeler from University of Nottingham for offering me a chance to conduct a quality research in the field of power electronics applied in the aerospace for three months during 2017. I collaborated with highly motivated people and broadened my knowledge of aircraft electrical systems. I am especially grateful to Mohamed Rashed and to Serhiy Bozhko for being my technical leaders during those times. It was an enlightening experience to learn from top-level laboratory in power electronics field.

I also thank all the professors and technicians in our center: Javier Uceda, José A. Cobos, Oscar García, Miroslav Vasić, Teresa Riesgo, Eduardo de la Torre, Jorge Portilla, Felix Moreno, Rafael Asensi, Roberto Prieto. Also, many thanks to Justo

and Fernando for their support in the lab work. Moreover, I am very grateful to Yolanda Rodrigo for her invaluable administrative help and support in general.

To all my colleagues, Vladan, Nico, Iñigo, Guillermo, David Aledo, Diego, Hesam, Lixin, Licheng, and all those former colleagues in CEI, thank you for quality time that we spent both at CEI as well as during social activities.

Last but not the least, I would like to thank my sister Senka for her love and support along this journey. I am also very indebted to my beloved uncle Vojin and aunt Vesna for making my childhood days happier and care-free. Their support certainly had a very positive influence on my character development. Moreover, I must express my eternal gratitude for the blessing of all unconditional love, support and understanding that my mother Jovanka gave me. Without her I would not be the person that I am nor would I be where I am now in life. Finally, I dedicate this thesis to my late father Jovan who would be undoubtedly very proud to witness the successful closure of my academic studies.

Uroš Borović
in Berlin, September 2019.

Abstract

In the ever-growing market of the civil aerospace industry, there has been a constant need for improvement in many fields. Due to rapid advancements in the field of electrical engineering the trend called More Electric Aircraft (MEA) has emerged as a response. Its goal is to reduce CO₂ emissions by implementing new technologies in the aircraft. The natural way of minimizing the emissions is by decrementing the total weight of the airplane which will in turn reduce operating costs and total fuel consumption. The MEA trend is predominantly reflected in replacing heavy and maintenance costly hydraulic, pneumatic and mechanical parts of the aircraft system with electrical equivalents.

This work is focused on providing contributions in the field of three-phase active rectifiers that could be employed in the future airliners, while complying with requirements from avionic standards such as DO-160G. The AC/DC conversion is mainly done by passive three-phase multi-pulse rectifiers that are extremely reliable, but present significant drawbacks in the weight, volume, efficiency and lack of controllability. The active rectifiers can overcome all these challenges, keeping in mind that reliability must not be significantly impaired.

In this thesis a review of the state-of-the-art three-phase AC/DC converters is done in Chapter 2, followed by first main contribution regarding low-frequency current emissions under 10 % three-phase voltage Total Harmonic Distortion (THD) from DO-160G in Chapter 3. The design methodology is proposed that translates the individual harmonic requirements to an admittance profile that the connected three-phase load must consider in order to be fully compliant with this requirement. The design methodology is chosen to be carried out in synchronous reference frame or dq frame. The proposed admittance limits are then applied to the three-phase buck-type rectifier. It is shown that in this case, the bandwidth of the current controller used for input admittance shaping is not a very demanding parameter. On the other hand, design of input Electromagnetic Interference (EMI) differential filter is demonstrated to be critical due to its rather low characteristic impedance. The design is afterwards extensively analyzed and verified by simulation results.

The same design methodology is then applied on the three-phase boost-type rectifier, namely the VIENNA rectifier. It is shown that in this case there exists a trade-off between input inductor size and current controller bandwidth, and that, for the approximately same size of magnetic components, the boost-type rectifier requires higher current controller bandwidth than its buck-type counterpart. It is also demonstrated that boost-type topologies are rather insensitive to the EMI filter design due to rather small values of the input capacitors compared to the buck-type case. Finally, the results are verified by simulation and conducted on a 10 kW SiC prototype.

In Chapter 4, the second main contribution of this work is reflected and it aims to provide a robust control strategy for a three-phase three-wire six-switch boost-type rectifier against arbitrary input phase failure scenario, in order to cope with the single-phase loss requirement of DO-160G. The fundamental idea lies in control of positive and negative sequence components of the three-phase system after the failure occurrence. Therefore, the applied rectifier closed-loop current control consists of four identical PI controllers, two for each sequence d and q components. Since each grid fault case generates unique values of positive and negative sequence voltage vectors, a mathematical derivation of d and q components of each rotating sequence is presented. The precise mathematical extraction of necessary positive and negative sequence voltage and current components needed to cope with any grid fault scenario is proposed. The total number of analyzed failure cases is nine, where three are related to phase-to-phase short-circuit, three to open-phase case, and three to phase-to-neutral fault. Moreover, a mathematical link between instantaneous amplitudes of each individual phase and positive and negative sequence component values is also provided. The derived link utilized on input three-phase voltages and currents provides a simple way of detecting the nine grid failure cases so that adequate current controller references can be provided which guarantee optimal power flow. Finally, the proposed analysis is backed up by simulation and experimental results, conducted on a full SiC 3.45 kW prototype.

In the last Chapter, a summary with highlighted contributions and conclusions from this work is addressed and a vision of possible future work is provided.

Resumen

En el mercado de la aviación civil, en constante crecimiento, siempre ha habido una continua necesidad de mejora en muchos campos. Como respuesta a los rápidos avances en la ingeniería eléctrica, ha emergido la tendencia llamada “avión más eléctrico” (“More Electric Aircraft” o MEA). El objetivo es reducir las emisiones de CO₂, implementando nuevas tecnologías en el avión. El modo natural de hacer más pequeñas las emisiones es reducir el peso total del avión, que a fin de cuentas reducirá los costes operativos y el consumo total de combustible. La tendencia MEA se refleja principalmente en sustituir piezas mecánicas, neumáticas e hidráulicas, pesadas y de alto coste de mantenimiento, por equivalentes eléctricos.

Este trabajo se centra en proporcionar contribuciones en el campo de los rectificadores trifásicos activos que podrían ser empleadas en el avión del futuro, cumpliendo a la vez con los requisitos de las normas de aviónica, como por ejemplo la DO-160G. la conversión CA/CC se realiza normalmente rectificadores multipulso pasivos que, aunque son tremendamente fiables, presentan inconvenientes, tales como el peso, el volumen, el rendimiento y la falta de controlabilidad. Los rectificadores activos pueden superar todos estos retos, teniendo en cuenta que la fiabilidad no debe verse afectada significativamente.

En esta tesis se proporciona en el capítulo 2 un resumen del estado del arte de los convertidores CA/CC trifásicos, seguido de mi primera contribución en el capítulo 3, en relación con las emisiones de corriente por debajo del 10 % de distorsión armónica total trifásica (THD) según la norma DO-160G. Se ha propuesto una metodología de diseño que traduce los requisitos individuales de armónicos a un perfil de admitancia que debe considerar la carga trifásica conectada para cumplir totalmente con este requisito. La metodología de diseño se ha implementado en el sistema de referencia síncrono dq . Los límites de admitancia propuestos se aplican al rectificador trifásico de topología “buck” (reductora). En este caso se muestra que el ancho de banda del controlador de corriente usado en el modelado de la admitancia no es un parámetro muy exigente. Por otro lado, se demuestra que el filtro diferencial para la Interferencia electromagnética (EMI) es crítico, debido a

su bastante baja impedancia característica. Con posterioridad el diseño se analiza exhaustivamente y se verifican los resultados de simulación.

La misma metodología se ha aplicado al rectificador trifásico de topología “boost” o elevadora, específicamente el rectificador VIENNA. Se muestra que en este caso existe un compromiso entre el tamaño de la bobina y el ancho de banda del controlador de corriente y que, para el mismo tamaño de componentes magnéticos, el rectificador de tipo “boost” requiere un ancho de banda del controlador de corriente mayor que su equivalente de tipo “buck”. Asimismo, se demuestra que las topologías de tipo “boost” son más insensibles al diseño del filtro EMI, debido sus sensiblemente más pequeños condensadores de entrada, en relación con los de tipo “buck”. Finalmente, los resultados se verifican por medio de simulación y de un prototipo de 10 kW basado en tecnología SiC.

En el capítulo 4 se muestra la segunda contribución principal de este trabajo y se pretende proporcionar una estrategia de control robusta para un rectificador trifásico de tres hilos, basado en topología “boost” con seis interruptores, que soporte un caso de fallo de fase, con el fin de cumplir el requerimiento de fallo de fase de la norma DO-160G. La idea fundamental reside en el control de las componentes de secuencia positiva y negativa del sistema trifásico tras producirse el fallo. Por tanto, el control de corriente en lazo cerrado implementado en el rectificador consiste en cuatro controladores PI idénticos, dos para las componentes d y q de cada secuencia. Debido a que cada caso de fallo de la red genera valores únicos de los vectores de tensión de secuencia positiva y negativa, se presenta una derivación matemática de las componentes d y q de cada secuencia rotativa. La extracción matemática precisa de las componentes de tensión y corriente de secuencia positiva y negativa, tienen que soportar cualquier escenario de fallo de red. El número total de casos analizados es nueve, de los cuales tres están relacionados con cortocircuitos fase-fase, tres con fases abiertas y tres con fallos fase-neutro. Adicionalmente se proporciona una relación matemática entre las amplitudes instantáneas de cada fase y las componentes de secuencia positiva y negativa. Esta relación aplicada en las corrientes y tensiones trifásicas de entrada proporciona una manera simple de detectar los nueve casos de red, de forma que se pueden suministrar las adecuadas referencias del controlador de corriente que garanticen el flujo óptimo de potencia. Finalmente, el análisis

propuesto está respaldado por resultados de simulación y experimentales, estos últimos obtenidos de un prototipo de 3.45 kW basado en semiconductores “full-SiC”.

En el último capítulo, se presenta un resumen de las contribuciones y conclusiones principales de este trabajo y una visión de posibles trabajos futuros.

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Introduction

1.1 More Electric Aircraft

Global air transport demand exhibits a steady increase, with the world revenue passenger kilometers (RPK) increasing with the yearly rate of 4%, while the number of passenger is rising with an average yearly rate of 10.6% [1]. The main driving force for this rapid growth is a constant improvement in the aircraft design which increased power conversion efficiency which in turn reduced the cost of air transport. The advances in aircraft engines thrust generation, as well as reduction of take-off weight, enabled for better fuel economy which is a key parameter in aircraft industry. Another important goal is reduction of maintenance costs which is driven by use of more reliable technologies.

In an aircraft system, the four main power systems are electrical, mechanical, hydraulic and pneumatic. The rapid advancements in the electronic equipment enabled for the trend of gradually substituting the latter three power systems with electrical equivalents. That trend is called More Electric Aircraft [2]. The main reason for this trend lies in potential large savings in weight if electrical substitutes of other three power systems are used. In the case of military aircraft, the application of MEA concepts is expected to reduce the take-off weight by 6.5 %, increase mean time between failures by 5.4 %, while reducing life cycle costs up to 3.2 % [3].

Over the course of the MEA programme the hydraulic, pneumatic and mechanical systems will be replaced by their electrical equivalents [4]. That yields a considerable increase in electrical power demand on-board. As a comparison, the Airbus A330 has an installed electrical power rating of 300 kVA, while Airbus A380 is at 600 kVA [5]. The most electric aircraft to date is the Boeing's flagship Dreamliner 787 with an installed electrical power capacity at 1 MVA [6].

Figure 1.1: (a) Generator connected via mechanical gearbox to the constant speed shaft resulting a fixed grid frequency of 400 Hz (b) generator directly connected to the variable speed shaft omitting the gearbox which results in variable grid frequency of 360-800 Hz.

The conventional approach in the aircraft electrical power generation lies in connection of the three-phase generator to the constant speed shaft which results in constant grid frequency of 400 Hz and three-phase voltage of 115 V, as shown in Fig. 1.1a. The engine variable speed shaft is connected via mechanical gearbox in order to provide a constant speed shaft. A three-stage permanent magnet excited would field synchronous machine is typically used in civil aircraft applications [7]. The engine startup is usually realized by the on-board pneumatic system. In MEA, however, the bulky and expensive mechanical gearbox is eliminated, thus generator is directly connected to the engine variable speed shaft, as in Fig. 1.1b. As a result, the three-phase voltage grid frequency now becomes variable in the range of 360 Hz to 800 Hz. Moreover, the generator is also used as a starter motor which in turn yields reduction of the aircraft weight [8, 9]. The generators that could be used in future aircraft are either Permanent Magnet Synchronous Machines (PMSM) or Switched Reluctance Machines (SRM) since they exhibit high power density, robustness and tolerance to temperatures [10, 11]. Due to increased electrical power

1.1. More Electric Aircraft

Figure 1.2: Electrical system of a Boeing Dreamliner 787.

on-board, the three-phase voltage level is also increased from 115 V to 230 V in order to reduce conduction losses and save weight in interconnecting cables [7]. On the other hand, the drawback of increasing the three-phase voltage by a factor of two, and by potentially increasing the grid frequency from 400 Hz to 800 Hz, the reactive currents that rectifier EMI filter capacitors draw may become an issue. Namely, the reactive power consumption of these capacitors is proportional to the grid frequency and to the square of the voltage, which gives an increase of unwanted reactive currents by a factor of eight, assuming the same capacitance value.

The one half of electrical system structure of a Boeing Dreamliner 787 [12] is shown in Fig. 1.2, where possible applications of active rectifiers are highlighted in

yellow. The gas turbines are mechanically coupled to two starter/generators that are responsible for main AC bus generation of 230 V/400 V with variable frequency in the range 360-800 Hz. An Auxiliary Power Unit (APU) is also connected to the same bus through another starter/generator and is to be used in the case of emergency. This unit is also used to supply power while the aircraft is on the ground with engines turned off.

Due to variable frequency nature of the grid the impact on the legacy constant frequency AC loads is rather considerable, which yields need of power electronics as a interface if they are required to be connected to this bus [13]. Applying active rectifiers a 540 V DC bus is generated. For the purpose of direct connection of the legacy 115 V loads, the Auto Transformer Unit (ATU) is utilized to generate variable frequency 115 V bus from the 230 V grid. Again, depending on the load type, additional power electronics interface could be required in order to supply the loads that are very sensitive to the variable frequency. Moreover, external power connector when aircraft is on the ground can be connected to this bus. Lastly, the rapid increase of electrical system can, however, lead to grid stability concerns that must be dealt with accordingly [14].

1.2 Aircraft Systems Relevant Regulations

The MEA concept revolves around reducing total weight of the aircraft, CO₂ emissions and cost, while improving reliability, energy conversion efficiency and mean time between failures. All these goals must be always realized in accordance with avionic regulations. The most widely used and the most extensive standard that tries to encircle as many test conditions as possible is the Environmental Conditions and Test Procedures for Airborne Equipment DO-160 published by Radio Technical Commission for Aeronautics with the current issue G [15]. It provides standard procedures and environmental test conditions for testing airborne equipment for the wide spectrum of aircraft from light general aviation airplanes and helicopters through the jumbo-jets and supersonic transport categories of aircraft. The document itself has 26 sections and three appendices. Some examples of tests covered include vibration, power input, radio frequency susceptibility, lightning and electrostatic discharge etc. For the research field of power electronics, the

1.2. Aircraft Systems Relevant Regulations

Section 16 of DO-160G regarding power input is probably the most relevant, along with the Section 21 regarding radio frequency susceptibility. Another two common regulations relevant to aircraft electrical equipment are military standards Aircraft Electric Power Characteristics, MIL-STD-704F [16] and Requirements for the Control of Electromagnetic Interference Characteristics of Subsystems and Equipment, MIL-STD-461G [17]. The aircraft companies often apply their own standards derived from DO-160G and military regulations that are sometimes more stringent [18]. The most relevant aspects of the before-mentioned DO-160G standard are discussed briefly below.

Since the energy storage on the AC bus is not present, the rectifiers are not allowed to regenerate energy back into the grid. Therefore, unidirectional topologies are preferred since their structure inherently prohibits regeneration. For the equipment connected to the AC mains, DO-160G Section 16 defines three different equipment categories that are A(CF) whose primary power source is from constant frequency 400 Hz grid, A(NF) whose primary power source comes from narrow frequency range of 360 to 650 Hz and A(WF) whose primary power source comes from wide frequency range grid of 360 to 800 Hz. The focus in this thesis is going to be on the A(WF) requirements defined in DO-160G.

For the variable frequency grid with 230 V AC voltage, the regulation tolerances that may appear are in the range of ± 1 %. The absolute minimum average voltage of all three phases is 203 V, while the maximum value is at 241 V, which translates into an operating range for the A(WF) equipment of 230 V, $+5/-12$ %. The tolerances for the relative phase displacement are ± 6 electrical degrees. The maximum Total Harmonic Distortion (THD) of the three-phase source is at 10 %.

The requirement regarding voltage unbalance states that it must be conducted at grid frequencies of 360 Hz and 800 Hz. Moreover, the test is conducted at the maximum grid voltages of 244 V in two phases and 228 V in the phase with an unbalance. The test is also conducted at the minimum grid voltages of 200 V in two phases and 216 V in the phase that is subjected to the unbalance.

The equipment is also expected to not cause an unsafe condition or be damaged when subjected to momentary power interruptions that can last anywhere from 0 to 200 ms.

As a response to the load switching and in general regulation of the AC bus, the equipment is expected to handle surge AC voltages. All rise and fall times are required to be less than 1.5 ms. The test is performed at 360 and 800 Hz. Both overvoltage and undervoltage transients are done in the same test. The equipment is set to operate for 5 minutes at 230 V. First, three-phase voltage is increased to 340 V for 30 ms, then returned to 230 V for 5 seconds, then reduced to 140 V for 30 ms and finally returned to 230 V for five seconds. This cycle is performed three times. The equipment is expected to operate normally during and after the transient sequence. This test can have significant impact in the choice nominal active rectifier DC link voltage, as well to the necessary semiconductor voltage ratings.

The normal frequency transients are expected to occur as an AC grid reaction to the engine speed changes, most notably during aircraft take-off and engine shutdown procedures. The variations are expected not to exceed 200 Hz/s. The test is performed starting at 230 V three-phase voltage and 360 Hz for 5 seconds, then the grid frequency is increased to 800 Hz with a rate of change of 100 Hz/s and maintained for 5 seconds, and finally returned to 360 Hz with a rate of change of 200 Hz/s. This cycle is repeated three times. This test may have implications in the rectifier Phase-Locked Loop (PLL) design as well in the general rectifier control.

Another common test that is performed is regarding input phase loss. The test is realized in order to verify that equipment does not suffer damage or an unsafe condition. The test procedure verifies loss of one phase during normal operation, startup of the converter without one phase, loss of two phases during normal operation and finally startup of the converter without two phases. Even if it is not a requirement of this test, it is highly desirable that equipment can continue operating during a phase loss at least at reduced power level. Depending on the level of power required to be provided after a phase loss, this test has high impact on the topology selection, reactive elements design and semiconductor ratings selection.

The low-frequency harmonic content is also required by DO-160G. The test is done at two voltage distortion levels (THDv): one at THDv below 4 % and one at THDv at 10 %. The individual harmonic limits are given in Fig. 1.3 assuming THDv of 0 %. Depending on the harmonic content in the voltage, the individual current limits are increased 1.25 times for every percent of distortion in the corresponding harmonic. The 0 % THDv current limits are designed in a way that passive 12-pulse

1.2. Aircraft Systems Relevant Regulations

Figure 1.3: Individual current limits relative to the fundamental assuming undistorted three-phase voltage waveforms.

rectifiers can be directly applied. However, Boeing has defined more restrictive limits for 11th and 13th harmonic thus forcing the use of 18-pulse rectifiers.

The steady-state full load power factor (PF) is expected to be larger than 0.8 inductive and larger than 0.968 capacitive. No information is given regarding PF requirements at lighter loads. If the rectifier is supposed to maintain high PF at lighter loads, then bidirectional converters must be used due to their ability to compensate large amounts of reactive power. Compared to bidirectional rectifiers, the unidirectional converters have reduced number of applicable switching states, which is directly translated into limited PF compensation capability, especially at lighter loads.

Lastly, the Section 21 of DO-160G defines limits for high-frequency conducted EMI emissions. The limits are important since they have direct impact on the volume and weight of the input EMI suppression filter. The conducted emissions limits are given in Fig. 1.4. The standard covers the usual industrial range of conducted emissions starting at 150 kHz and ending at 30 MHz. Moreover, different categories are defined depending on the separation of the equipment from aircraft radio antennas. Category L equipment is normally located far from apertures of the aircraft and far from antennas. Category M is located in the areas where apertures are EM significant but not in the direct view of the antennas. Category H is defined for equipment that is directly exposed to the radio receiver's antenna. Lastly, the

Figure 1.4: Limits for conducted input current emissions for the power lines of an equipment connected to AC grid according to DO-160G.

category B is defined for equipment that should control its emissions to tolerable levels.

1.3 Objectives and Contributions of this Thesis

This PhD thesis aims to contribute in two specific tests from DO-160G avionics standard.

The first main contribution is to provide a systematic design methodology for the three-phase active rectifiers in order to comply with the previously mentioned current distortion test under 10 % THD_v from DO-160G. An analysis of systematic design methodology for three-phase buck-type and boost-type rectifiers in order to meet with the voltage distortion test requirement is performed. The 10 % THD_v test requirement is translated into equivalent per-harmonic admittance limit in abc domain and a profile of maximum rectifier input admittance versus frequency is obtained. Since the control of the rectifiers is performed in the synchronous reference frame (dq domain), translation of the admittance limits into dq domain is proposed. The newly defined dq admittance profile, due to normalization, is applicable to arbitrary power level with simple shifting by the base admittance governed by the converter nominal power. The derived admittance limits are then applied to three-phase buck-type rectifier and it is shown that main limitation lies in the input LC filter design used for differential EMI filtering. Afterwards, on the case of

1.3. Objectives and Contributions of this Thesis

three-phase boost-type rectifier, namely VIENNA rectifier, it is demonstrated that there exists a trade-off between current controller bandwidth and input inductor size in order to comply with this requirement. Finally, the experimental results conducted on a SiC three-phase 10 kW VIENNA rectifier are shown to tightly back up the proposed theoretical analysis.

The second main contribution is to provide a robust control strategy for a three-phase three-wire six-switch boost-type rectifier against arbitrary input phase failure scenario, in order to cope with the single-phase loss requirement of DO-160G. The fundamental idea lies in control of positive and negative sequence components of the three-phase system after the failure occurrence. Therefore, the applied rectifier closed-loop current control consists of four identical PI controllers, two for each sequence d and q components. Since each grid fault case generates unique values of positive and negative sequence voltage vectors, a mathematical derivation of d and q components of each rotating sequence is calculated. The precise mathematical extraction of necessary positive and negative sequence voltage and current components needed to cope with any grid fault scenario is proposed. The total number of analyzed failure cases is nine, where three are related to phase-to-phase short-circuit, three to open-phase case, and three to phase-to-neutral fault. Moreover, a mathematical link between instantaneous amplitudes of each individual phase and positive and negative sequence component values is also provided. The derived link utilized on input three-phase voltages and currents provides a simple way of detecting the nine grid failure cases so that adequate current controller references can be provided which guarantee optimal power flow. Finally, the proposed analysis is backed up by simulation and experimental results, conducted on a full SiC 3.45 kW prototype.

The following papers have been published during the work on this thesis:

Journal Papers

1. Uroš Borović, Sisi Zhao, Jesus A. Oliver, Pedro Alou, Jose A. Cobos, Predrag Pejović “Design Methodology for Three-phase Buck-Type and Boost-Type Rectifiers to Comply With the DO-160G Current Distortion Test,” *IEEE Transactions on Power Electronics*, accepted for publication, available

on early access, ISSN: 0885-8993 (Print), ISSN: 1941-0107 (Electronic), DOI:10.1109/TPEL.2019.2923404, June 2019.

Conference Papers

1. **U. Borović**; S. Zhao; J. A. Oliver; P. Alou; J. A. Cobos, “Control of a Three-phase Boost Rectifier for Operation Under Single Failure of the AC Line For Avionic Applications,” *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018.
2. Y. E. Bouvier; **U. Borović**; M. Vasić; J. A. Oliver; P. Alou; J. A. Cobos; F. Árevalo; J. C. García-Tembleque; J. Carmena, “DC/DC Fixed Frequency Resonant LLC Full-Bridge Converter With Series-Parallel Transformers for 10kW High Efficiency Aircraft Application,” *IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017.
3. **U. Borović**; S. Zhao; M. Silva; Y. E. Bouvier; M. Vasić; J. A. Oliver; P. Alou; J. A. Cobos; F. Árevalo; J. C. García-Tembleque; J. Carmena; C. García; P. Pejović, “Comparison of Three-Phase Active Rectifier Solutions for Avionic Applications: Impact of the Avionic Standard DO-160 F and Failure Modes,” *IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2016.

1.4 Outline of the Thesis

In Chapter 2 a survey of the state-of-the-art three-phase rectifiers predominantly intended for use in aerospace applications is carried out. The rectifiers reviewed consist of passive and active/hybrid solutions. Literature regarding phase loss from other fields of application is also discussed, since it forms a basis for the main contributions in Chapter 4.

In Chapter 3 a systematic design methodology is proposed in order to comply with the DO-160G current distortion test. The methodology consists of obtaining a profile of maximum converter input admittance as a function of frequency. The derived limits that guarantee compliance with DO-160G, are then applied on the three-phase buck-type rectifier. It is shown that special care must be taken

1.4. Outline of the Thesis

when designing input differential EMI filter. Lastly, the limits are applied on the three-phase boost-type rectifier, namely the VIENNA rectifier. It is demonstrated that in this case there exists a trade-off between current controller bandwidth and input inductor size. Finally, a set of experimental results is obtained on a 10 kW SiC demonstrator prototype.

Chapter 4 analyses three-phase three-wire six-switch boost-type rectifier under event of various phase failure scenarios. Utilizing positive and negative sequence voltages and currents, the control strategy is developed that only requires modifications of current references in order to cope with all nine possible grid fault cases. The cases analyzed are phase-to-phase short-circuit, open-phase fault and short-circuit between phase and source neutral (ground). The analysis is backed up by extensive simulations and experimental setup that employs full-SiC design with a power rating of 3.45 kW.

Analysis of the State-of-the-Art

In this Chapter a survey of state-of-the-art passive and active/hybrid solutions intended for avionic applications is presented. The amount of research conducted in the last decades clearly indicates the trend of constant improvement in the aircraft mainly driven by MEA concepts. Situated on this survey, a strong basis is provided upon which the contributions proposed in Chapters 3 and 4 are made that would make the three-phase active rectifiers one step closer to their extensive application in the aircraft electrical systems.

2.1 Passive Systems

The simplest three-phase rectifier consists of six diodes. It normally exhibits peaks in current which results in very high input current distortion THD_I and very low PF. The interval that diodes conduct current can be enlarged by introducing an inductor on the DC side or in a three-phase configuration on the AC side. This improves the rectifier power quality, but it is still not sufficient to comply with aircraft grid requirements. A further improvement is possible utilizing passive third harmonic injection according to [19] where it is shown that THD_I of 5 % at full load can be achieved.

The input power quality can be considerably improved if two or more phase-shifted full bridge rectifiers are used in parallel resulting in passive multi-pulse rectifiers. If isolation is a requirement, then transformer must be used that is also providing the necessary phase shift between the diode bridges, resulting in systems called Transformer Rectifier Units (TRU) [20]. When the application does not require isolation, then auto transformers may be used which results in Auto Transformer Rectifier Units (ATRU). An example of the TRU is given in Fig. 2.1, while possible ATRU structures are given in Fig. 2.2.

Figure 2.1: Passive current loaded twelve-pulse Transformer Rectifier Unit (TRU).

The use of auto transformer topologies can reduce the size and weight of the unit. The ATRU shown in Fig. 2.2a has auto transformer located on the AC side for the purpose of generating $\pm 15^\circ$ phase shift between the bridges [21]. Due to presence of the inductance at the output in this topology, two interphase reactors are required at the output of the diode bridges in order to ensure current sharing and to decouple their output voltages impressed by the autotransformer on the AC side.

If inductor at the output is omitted and substituted by a three-phase inductance on the AC side, a modification in the AC side interphase auto transformer is necessary as shown in Fig. 2.2b. In this case the AC side auto transformer, apart from generating phase shifts of $\pm 15^\circ$, also ensures the current sharing between the bridges [22]. As shown in [23], the design of the AC interphase auto transformer must be done on three separate cores due to inherent zero-sequence magnetic flux present in the three-phase configuration.

2.1. Passive Systems

Figure 2.2: Examples of passive twelve-pulse Auto Transformer Rectifier Units (ATRUs) (a) current loaded (b) voltage loaded.

Figure 2.3: Three-phase buck-type rectifier.

Nowadays in the aircraft passive transformer based multi-pulse rectifiers are very common in MEA, predominantly 18-pulse rectifiers [24, 25, 26, 27, 28]. The main advantage that they present is extremely high reliability due to line-frequency commutating diodes, good short-term overload capability and low component count. Their significant drawbacks are, however, lack of any control over output DC link voltage or the input currents, modest input current quality reflected in THD_I around 7 % and high weight due to low-frequency magnetic components. These drawbacks offer large design space for active rectifiers and their use in future MEA applications.

2.2 Active Systems

Direct active AC/DC conversion has as a consequence reduced stress on the output DC link capacitor due to constant instantaneous power supplied by a three-phase source assuming symmetrical and balanced source and balanced load. The basic classification of these converters can be made into boost-type and buck-type rectifiers.

In order to have full controllability over the rectifier switches, the three-phase buck-type rectifier [29, 30] must have output voltage below $3/2V_m$, where V_m is peak

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line-to-neutral input source voltage. Due to discontinuous input currents, the size of the input EMI filter is relatively large, particularly input decoupling capacitors. These large input capacitors may impair input PF due to high grid frequencies of 360-800 Hz. As shown in [31], reactive current compensation is possible up to $\pm 30^\circ$ relative to input voltage space vector. The amount of compensation achievable is, however, strongly dependent on the DC link voltage value and the rectifier load. Nonetheless, the three-phase buck-type rectifier presents advantages in terms of standalone startup capability and provides inherent protection against a short-circuit event at the output which can be very interesting for aerospace applications. The basic rectifier structure is given in Fig. 2.3.

In aircraft applications this type of rectifier is referenced rather often. In [32] a novel single-stage AC/DC converter with isolation is proposed following military specifications for conducted EMI, MIL-STD-461G [17]. It is designed for $3 \times 115 \text{ V}_{\text{AC}}$ input, with $270 \text{ V}_{\text{DC}}$ output. Use of single-stage topologies can provide volume savings since the intermediate DC link capacitance is removed. However, the control of this type of systems is rather complex and the rectifier can be very sensitive to grid unbalances. A novel energy control method is proposed in [33] aimed to improve aircraft generator lifetime when supplying constant power loads. The analysis provides an insight into trade-off between DC link capacitor volume and generator lifetime expectancy. In [34] a differential EMI filter design considerations are presented in order to comply with MIL-STD-461G. The optimization process is presented for single and multistage EMI filters aiming to provide near-unity power factor down to 50 % of the load. A novel single-stage buck-type rectifier with isolation is proposed in [35] for $3 \times 115 \text{ V}_{\text{AC}}$ input, $270 \text{ V}_{\text{DC}}$ output voltage levels. It is based on the well-known Swiss rectifier [36]. Detailed power stage design guidelines are provided, as well as Current Space Vector Modulation (CSVM) for reactive power compensation. Furthermore, the low-frequency current harmonic spectrum profile from DO-160G, previously given in Fig. 1.3, was successfully complied by buck-boost rectifier in [37]. Overall, the three-phase buck-type rectifier and its derivations are showing to be an attractive solution for aircraft application.

The simplest and probably fundamental three-phase converter is the three-phase six-switch boost-type rectifier, shown in Fig. 2.4. Dual to the buck-type case, the output DC link voltage must be at least higher than maximum line-to-line

Figure 2.4: Three-phase six-switch boost-type rectifier.

three-phase voltage at $\sqrt{3}V_m$, if Space Vector Modulation (SVM) is used. The output voltage must be even higher if basic Sinusoidal Pulse-Width Modulation (SPWM) is used and it is at $2V_m$. Due to its bidirectional nature, it does not have limitations in reactive power handling and can compensate reactive currents independent of the applied load. Also, being low component and simple topology, it is an interesting solution for aerospace applications. The main drawbacks are its vulnerability to shoot-through failures and the need for extra startup circuitry.

Regarding aircraft applications, this rectifier topology has been often addressed. In [38, 39] this rectifier was designed bearing in mind the Section 21 of DO-160G regarding the emission of radio frequency energy. The Section 21 is fundamentally split into radiated and conducted RF emissions. The work presented in [38] is focused on the conducted RF emissions. In it, on the case of a 6 kW three-phase six-switch boost-type rectifier, a mathematical model is proposed to successfully design and experimentally verify differential (DM) and common-mode (CM) EMI filter in order to be compliant with DO-160G Section 21. As a continuation of that work, in [39], an optimization process for the DM filter is proposed in order to minimize its weight and volume, while maintaining compliance with DO-160G Section 21 and near unity PF. As mentioned before, weight reduction is one of the key parameters of MEA applications. In [40] different SVM strategies are analyzed in order to optimize the switching patterns for the three-phase six-switch boost-type rectifier. A trade-off between current THD and switching losses is also addressed. The optimization

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Figure 2.5: Three-phase VIENNA rectifier.

of input boost inductance and output DC link capacitor size concerning pulsating power loads is analyzed in [41]. Further stability concerns that constant power loads such as Electric Actuator Load present, are extensively analyzed in [42, 43, 44].

The three-phase active rectifiers can further be divided into two-level and three-level (or even more) topologies. The three-level converter systems utilize three voltage or current levels in PWM voltage or current formations. The advantage of the three-level converters is that they present smaller ripple at the input inductors or capacitors, enabling the reduction of passive components, most notably inductors. Moreover, some or all semiconductors are stressed with half of the voltage and/or current which translates into reduced switching and/or conduction losses, as well as reduction of EMI effort. The main drawback of three-level topologies is increased number of devices, complexity in the PWM pattern generation and the need of output voltage capacitors balancing logic.

The typical representative of three-phase three-level voltage source rectifier is VIENNA rectifier originally presented in [45, 46]. There are many ways of implementing the VIENNA rectifier in function of the implementation of the bidirectional switches S_A , S_B and S_C , shown in Fig. 2.5. Depending on the switch configuration, optimization towards MOSFET/IGBT count, conduction or switching loss can be realized [47]. Irrespective to the switch configuration, all semiconductors are stressed with half of the output voltage which enables use of the semiconductors with lower voltage rating. Moreover, due to three-level nature of this topology, the input inductor L_r exhibits around 40 % lower volume for the same peak-to-peak

current ripple compared to the three-phase six-switch boost-type rectifier case, assuming same switching frequency and output voltage. This feature is highly desirable in aircraft applications since it enables considerable weight savings.

A thorough multi-variable optimization process for the three-phase VIENNA rectifier intended for MEA applications and power level of 10 kW is analyzed in [47]. Many experimental prototypes were built with switching frequencies ranging from 72 kHz up to 1 MHz. It was shown that VIENNA rectifier systems can achieve outstanding power density of 14.1 kW/dm³ (including water cooling) with power-to-weight ratio of 9.44 kW/kg. Due to switching frequency of 1 MHz, the time available for cycle-by-cycle regulation is only 1 μ s including ADC conversion time. Thus, in [48] a fully digital controller was implemented in FPGA with total execution time of only 640 ns. The high switching frequencies pose a series of new design challenges. The finite MOSFET turn-off time causes PWM voltage pulse distortions that had little influence at low switching frequencies (below 500 kHz), but starts to be a major contributor to the THD_I at high switching frequencies as analyzed in [49]. An extension of that work is done in [50] employing GaN devices and the result is compared against 0 % THD_v DO-160G limits given in Fig. 1.3. In order to reduce switching loss in [51] a modulation strategy is proposed that enables reduction of the DC link voltage, aiming to improve reliability and maintain high PF. Finally, in [52] a comparison is made between hybrid rectifier consisting of a cascade connection of passive twelve-pulse voltage loaded rectifier from Fig. 2.2b and two interleaved boost converters [53], a three-phase six-switch boost-type rectifier and a VIENNA rectifier for variable input frequency of 400-800 Hz and AC voltage level of 115 V. The twelve-pulse system showed advantages in terms of volume, complexity and efficiency, but exhibited higher system weight. It was concluded that three-phase VIENNA rectifier is the most advantageous solution overall.

In aircraft applications the ability to continue providing power with minimum impact on the quality without one phase is an important advantage for the active rectifiers since the in-use passive multi-pulse rectifiers cannot operate properly under these conditions and must be disconnected, as mentioned in Section 1.2. The phase-loss performance of a 5 kW three-phase delta-switch rectifier is analyzed thoroughly in [54], as well as variable amplitude of the input three-phase voltage, variable 360-800 Hz line frequency and conducted emissions from DO-160G from

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Fig. 1.4. In general, boost-type topologies are used when outage of one phase is required. The three-phase buck-type rectifier from Fig. 2.3 in presented form cannot handle phase-loss due to inherent pulsating voltage present immediately after the rectifier bridge. In the time intervals that mentioned voltage becomes lower than output capacitor voltage, all diodes are reverse polarized, and the rectifier cannot supply energy to the output until next pulse of voltage appears, incurring drastic current distortions. Therefore, for the purpose of handling a phase loss, a modification of the rectifier to three-phase buck-boost topology is proposed in [55]. By removing the output capacitor and placing a boost DC/DC converter, a robust topology is derived that can handle outage of one phase with appropriate control strategy. Lastly, in the case of the grid connected rectifiers/inverters there are many publications regarding the robust control under grid disturbances utilizing the Double Decoupled Synchronous Reference Frame (DDSRF) as in [56, 57, 58, 59, 60]. These important results form the base upon which contributions in Chapter 4 are realized.

Conclusively, in the last several decades, there has been intensive research activity in the field of three-phase active rectifier intended for the applications in the future More Electric Aircraft. In the following two Sections, further contributions are proposed in order to bring these type of rectifier systems a step closer to their final application in aerospace industry.

Design Methodology to Comply With the THD_v Test for Buck and Boost-Type Rectifiers

The main purpose of this Chapter is to provide a systematic design methodology for the three-phase active rectifiers in order to comply with the previously mentioned current distortion test under 10 % Total Harmonic Distortion in Voltage (10 % THD_v test) from DO-160G. First, test setup and the test pass criteria are defined. Then, an analysis of systematic design methodology for three-phase buck-type and boost-type rectifiers in order to meet with the 10 % THD_v test requirement is performed. For a given voltage harmonic profile, the current harmonic limits that have to be satisfied are translated into equivalent per-harmonic admittances in *abc* domain and a profile of maximum rectifier input admittance versus frequency is obtained. Since the control of the rectifiers is performed in the Synchronous Reference Frame (*dq* domain), translation of the admittance limits from *abc* into *dq* domain is proposed, accompanied with development of the corresponding *dq* models of the active rectifiers. The newly defined *dq* admittance profile, due to normalization, is applicable to arbitrary power level with simple shifting by the base admittance governed by the converter nominal power. It is shown that for the buck-type rectifier main limitation lies in the input *LC* filter design used for differential EMI filtering, while for the boost-type rectifiers there exists a trade-off between current controller bandwidth and input inductor size. At the end, the experimental results conducted on a SiC three-phase 10 kW VIENNA rectifier are shown to tightly back up the proposed theoretical analysis.

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Table 3.1: Current harmonic limits for distortion-free input three-phase voltage.

Harmonic order	Limits
3 rd , 5 th , 7 th	$I_3 = I_5 = I_7 = 0.02I_1$
Odd triplen harmonics ($h = 9, 15, 21, \dots, 39$)	$I_h = 0.1I_1/h$
11 th	$I_{11} = 0.1I_1$
13 th	$I_{13} = 0.08I_1$
Odd non-triplen harmonics ($h = 17, 19$)	$I_{17} = I_{19} = 0.04I_1$
Odd non-triplen harmonics ($h = 23, 25$)	$I_{23} = I_{25} = 0.03I_1$
Odd non-triplen harmonics ($h = 29, 31, 35, 37$)	$I_h = 0.3I_1/h$
Even harmonics ($h = 2, 4$)	$I_h = 0.01I_1/h$
Even harmonics ($h > 4$)	$I_h = 0.0025I_1$

3.1 Introduction of the THD_v Test

The 10 % THD_v test is presented in the section 16 related to Power input of the DO-160G [15], specifically 16.7.1. The test requires that, following the distortion of the input three-phase voltages, the currents drawn by the load must have harmonic components below certain predefined limit.

The test itself is done at two voltage distortion levels, one below 4 % THD_v and one at 10 %. Both test conditions are carried out at 360, 400, 500, 600, 650, 700 and 800 Hz grid frequencies. Moreover, two ways of distorting the three-phase voltage are provided. One way of distorting the voltages at the point of common coupling (PCC), shown in Fig. 3.20 and Fig. 3.47, is by simply clipping the three-phase voltages as in Fig. 3.1 until the desired voltage distortion level is met. The second way of distorting the voltages at PCC is by connection of a voltage loaded three-phase 6-pulse full bridge rectifier. In that scenario, distortion level can be produced by varying the load on the full bridge rectifier and/or by increasing the source impedance L_g illustrated in Fig. 3.20 and Fig. 3.47. The standard leaves to the designer to choose which distortion method to apply. It would be beneficial to select the first distortion method since it allows to have a systematic design approach as it is proposed in this Chapter. Namely, in the first option the spectrum of the voltage distortion is generated and controlled by the three-phase source with ideally zero output impedance and therefore independent on the connected load. On the other hand, due to interaction between output impedance of the source and the input impedance of the connected three-phase 6-pulse full bridge rectifier, the

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Figure 3.1: Three-phase voltage waveforms with 10 % distortion.

second distortion method makes the profile of generated voltage harmonics heavily dependent on the connected load, especially around the resonances of the load input EMI filter. Therefore, in order to drastically simplify the design methodology discussed in this Chapter, it is recommended to select first distortion option.

In the section of 16.7.1 of DO-160G the definition of the permissible per-harmonic content is given for the three-phase loads assuming perfect distortion-free voltage ($\text{THD}_v = 0\%$) as in Table 3.1. The defined current harmonics are relaxed by 1.25 % for each 1 % of the harmonic present in the voltage. An example of three-phase voltage with 10 % distortion is given in Fig. 3.1 and the harmonic components relative to the fundamental are given in Fig. 3.2. These voltage harmonics will effectively increase the limits of the input current spectrum defined by Table 3.1. A comparison between current spectrum limits assuming distortion-free input three-phase voltage and the limits with 10 % voltage distortion are given in Fig. 3.3. The harmonics of interest in this test case are up to 40th.

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The two harmonic limits from Fig. 3.3 have to be satisfied for the 0 % THD_v test and 10 % THD_v test conditions respectively. Even though tests will be performed on both distortion levels, the main focus of this Section from this point onward will be on the 10 % THD_v test.

If a division of each spectral component of the defined high THD_v current spectrum with corresponding voltage spectrum is done, then a profile of

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Figure 3.2: Spectrum of the voltage waveform with 10 % distortion.

Figure 3.3: DO-160G current harmonic limits I_n for $\text{THD}_v = 0\%$ (cyan) and for $\text{THD}_v = 10\%$ (magenta).

Figure 3.4: Permissible normalized maximum per-harmonic input converter admittance for the case of single frequency, 4-wire connection.

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Figure 3.5: Permissible normalized maximum per-harmonic input converter admittance for the case of variable frequency $f = 360 - 800$ Hz, 4-wire connection.

per-harmonic admittances is obtained as in (3.1):

$$Y_{\text{in,max},2n-1} = \frac{I_{2n-1}}{V_{2n-1}}, \quad n \in N, \quad (3.1)$$

where $Y_{\text{in,max},2n-1}$ is normalized admittance limit, V_{2n-1} normalized voltage harmonic from Fig. 3.2 and I_{2n-1} normalized current harmonic limit $I_{0,2n-1}$, depicted with cyan bar plot in Fig. 3.3, increased by 1.25 times with respect to normalized spectral components of V_{2n-1} at odd harmonics $2n - 1$ as:

$$I_{2n-1} = I_{0,2n-1} + 1.25V_{2n-1}. \quad (3.2)$$

$Y_{\text{in,max},2n-1}$ is an important parameter since it defines a profile of maximum admittances as a function of frequency. Under the assumption that converters connected to this kind of highly distorted grid do not generate their own voltage or current harmonics, at least in a non-negligible manner, the attached circuitry must have admittances as a function of frequency below these established limits. The mentioned assumption is nowadays mostly a valid approximation for active three-phase rectifiers employing devices with low parasitics. Due to wider bandgap of the SiC material compared to Si, for the same breakdown voltage, SiC devices dies are smaller in size compared to their Si counterparts [61]. That yields lower output capacitance C_{oss} while maintaining the same MOSFET turn on resistance $R_{\text{DS,on}}$. The need for low parasitic output capacitance C_{oss} is very desirable, since it is one

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of the main contributors to low frequency distortion due to its finite charging and discharging time [49, 62]. Therefore, for the latter prototype design, SiC MOSFETs will be used. Effectively, the hypothesis is that the converter input admittance is only given by the theoretical closed-loop average model. The simulation results from the latter Sections will confirm that this assumption is reasonable as long as harmonics in voltage from Fig. 3.2 are above 1 % of the fundamental. For lower percentages the actual distortion coming from the rectifier itself, even though rather small, impacts the result and yields in lower maximum admittance limits than predicted. Nonetheless, by keeping a safe 3 dB margin from the limit on harmonics that have lower than 1 % distortion in voltage, the presented analysis predicts the critical harmonics in a very close manner. The normalized per-harmonic maximum input admittance in dB is shown in Fig. 3.4. If a frequency sweep is done from 360 to 800 Hz a profile of the normalized input admittances is obtained as shown in Fig. 3.5. Taking the minimum of the normalized maximum admittances, we can define the limit depicted by the black line in Fig. 3.5. This limit actually applies when a general converter is connected to the grid with four wires (phases A, B, C and the neutral). Since many of the converters are connected by three-wire connection, due to, for example, reduced cost and simplicity, a relaxation of the defined limit is possible. Observing again Fig. 3.4 and focusing to the lower values, since they are the ones that define the global limit, an interesting conclusion can be made. Namely, there exists a significant impact of harmonics 3, 9, 15, 21, 27 and 33. What all these harmonics have in common is that they are multiples of three, which means that they can be disregarded in the case of a balanced three-wire connection as shown in Fig. 3.6. To illustrate that, we can define a set of balanced three-phase voltages with triplen harmonics as:

$$\begin{aligned} v_{A,3n} &= V_{m,3n} \cos(3n\omega t) \\ v_{B,3n} &= V_{m,3n} \cos\left(3n\left(\omega t - \frac{2\pi}{3}\right)\right) = V_{m,3n} \cos(3n\omega t) \\ v_{C,3n} &= V_{m,3n} \cos\left(3n\left(\omega t + \frac{2\pi}{3}\right)\right) = V_{m,3n} \cos(3n\omega t), \end{aligned} \quad (3.3)$$

where $V_{m,3n}$ is the voltage amplitude of the harmonic $3n$. Since for a three-wired connection sum of currents of all three phases must add up to zero eg. $i_{Ar} + i_{Br} + i_{Cr} = 0$, then it follows that no triplen current harmonics can exist, which translates into infinite impedance of the symmetrical load at these harmonics under symmetrical

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Figure 3.6: A three-wire connection of a three-phase balanced load Z_r .

three-phase voltages. Therefore, for the three-wire case, the admittance limits at triplen harmonics tend to infinity, meaning they are not anymore a constraint in the design process and can be disregarded. By disregarding the admittance limits at triples of the fundamental frequency, a new relaxed 3-wire connection normalized input admittance profile is obtained as shown in Fig. 3.7 on the case of one frequency. The full frequency range converter normalized input admittance for the case of 3-wire connection is shown in Fig. 3.8. The limit depicted by the black line in Fig. 3.8 is the main maximum admittance profile used in this Section, shifted by the appropriate base admittance Y_0 , since both examples analyzed in the latter Sections are indeed 3-wire connected three-phase rectifiers. The normalized limit derived here applies to general power level case. When a design is to be made for a specific power level, the limits just need to be shifted by a base admittance Y_0 as:

$$20 \log Y_0 = 20 \log \frac{I_{A,\text{RMS}}}{V_{A,\text{RMS,L-N}}} = 20 \log \frac{P_{\text{OUT}}}{3V_{A,\text{RMS,L-N}}^2}. \quad (3.4)$$

In this work the selected power level is 10 kW and the defined input line-to-neutral voltage RMS value is 230 V, which gives Y_0 of -24 dB.

The two most popular ways to model and control a three-phase converter are in stationary ($\alpha\beta$ domain) and in Synchronous Reference Frame (dq domain). There are many publications in the field employing one type of modeling [63, 64, 65, 66, 67] or the other [68, 59, 58, 69]. The focus of this thesis will be on the control in dq frame, and therefore the previously derived admittance limits have to be converted into dq domain admittances.

It is well known from three-phase phasor theory that in a balanced system harmonics of the fundamental rotate in the manner given in Table 3.2. Observing

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Figure 3.7: Permissible normalized maximum per-harmonic input converter admittance for the case of single frequency, 3-wire connection.

Figure 3.8: Permissible normalized maximum per-harmonic input converter admittance for the case of variable frequency $f = 360 - 800$ Hz, 3-wire and 4-wire connection.

Table 3.2: Dependence of harmonic and phasor sequence rotation.

Sequence	Harmonic order				
Negative	2nd	5th	8th	11th	...
Zero	3rd	6th	9th	12th	...
Positive	4th	7th	10th	13th	...

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the pattern in Table 3.2, it can be deduced that harmonics of $3n - 1$ always correspond to the negative sequence, the harmonics $3n + 1$ are repeatedly related to the positive sequence and harmonics at $3n$ are zero-sequence. An amplitude invariant dq transformation can be applied for the negative sequence harmonics as:

$$\frac{2}{3}\mathbf{T} \begin{bmatrix} V_{m,3n-1} \cos((3n-1)\omega t + \phi_{0,3n-1}) \\ V_{m,3n-1} \cos((3n-1)(\omega t + \frac{2\pi}{3}) + \phi_{0,3n-1}) \\ V_{m,3n-1} \cos((3n-1)(\omega t - \frac{2\pi}{3}) + \phi_{0,3n-1}) \end{bmatrix}, \quad (3.5)$$

where $\mathbf{T}$ is $abc - dq$ transformation matrix:

$$\mathbf{T} = \begin{bmatrix} \cos(\omega t) & \cos(\omega t - \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \\ -\sin(\omega t) & -\sin(\omega t - \frac{2\pi}{3}) & -\sin(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \quad (3.6)$$

Simplifying (3.5), the following is obtained:

$$\begin{bmatrix} v_{d,3n-1} \\ v_{q,3n-1} \end{bmatrix} = V_{m,3n-1} \begin{bmatrix} \cos(3n\omega t + \phi_{0,3n-1}) \\ -\sin(3n\omega t + \phi_{0,3n-1}) \end{bmatrix}, \quad (3.7)$$

where $v_{d,3n-1}$ and $v_{q,3n-1}$ are d and q component of the negative sequence $3n - 1$ harmonic, $V_{m,3n-1}$ and $\phi_{0,3n-1}$ are its amplitude and initial phase. Similarly for the positive sequence:

$$\begin{bmatrix} v_{d,3n+1} \\ v_{q,3n+1} \end{bmatrix} = V_{m,3n+1} \begin{bmatrix} \cos(3n\omega t + \phi_{0,3n+1}) \\ \sin(3n\omega t + \phi_{0,3n+1}) \end{bmatrix}, \quad (3.8)$$

and for the zero-sequence:

$$\begin{bmatrix} v_{d,3n} \\ v_{q,3n} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix}. \quad (3.9)$$

Moreover, as it will be shown by the simulations and experimental results, due to the symmetry both in the three-phase source waveform and in the connected rectifier, even harmonics $3(2n - 1) \pm 1$ and $6n$ can be disregarded leaving only the ones of interest around even triplens $6n \pm 1$ as:

$$\begin{bmatrix} v_{d,6n\pm 1} \\ v_{q,6n\pm 1} \end{bmatrix} = V_{m,6n\pm 1} \begin{bmatrix} \cos(6n\omega t + \phi_{0,6n\pm 1}) \\ \pm \sin(6n\omega t + \phi_{0,6n\pm 1}) \end{bmatrix} \quad (3.10)$$

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where $v_{d,6n\pm1}$ and $v_{q,6n\pm1}$ are d and q component of the positive and negative sequence $6n \pm 1$ harmonic, $V_{m,6n\pm1}$ and $\phi_{0,6n\pm1}$ are their amplitudes and initial phases. Equation (3.10) is demonstrating that harmonics 5 and 7 from abc domain map to 6th in dq domain, 11th and 13th to 12th, or in general $6n \pm 1$ to $6n$. Observing now the spectrum of input voltage in Fig. 3.2 it can be concluded that the harmonics of interest have initial phases as $\phi_{0,6n\pm1} \in \{0, \pi\}$. According to (3.10) and taking into account initial phases from Fig. 3.2 the amplitudes of voltages and currents in dq domain at $6n\omega$ are:

$$\begin{bmatrix} V_{d,6n} \\ V_{q,6n} \end{bmatrix} = \begin{bmatrix} |V_{m,6n+1} \pm V_{m,6n-1}| \\ |V_{m,6n+1} \mp V_{m,6n-1}| \end{bmatrix} \quad (3.11)$$

$$\begin{bmatrix} I_{d,6n} \\ I_{q,6n} \end{bmatrix} = \begin{bmatrix} |I_{m,6n+1} \pm I_{m,6n-1}| \\ |I_{m,6n+1} \mp I_{m,6n-1}| \end{bmatrix}. \quad (3.12)$$

In abc domain the following holds:

$$i_{abc,6n\pm1} = Y_{abc,6n\pm1} v_{abc,6n\pm1}. \quad (3.13)$$

Combining (3.13), (3.11) and (3.12):

$$\begin{bmatrix} I_{d,6n} \\ I_{q,6n} \end{bmatrix} = \begin{bmatrix} |Y_{abc,6n+1} V_{m,6n+1} \pm Y_{abc,6n-1} V_{m,6n-1}| \\ |Y_{abc,6n+1} V_{m,6n+1} \mp Y_{abc,6n-1} V_{m,6n-1}| \end{bmatrix}. \quad (3.14)$$

The general relationship of currents and voltages in dq domain is:

$$\begin{aligned} i_d &= Y_{dd} v_d + Y_{dq} v_q \\ i_q &= Y_{qd} v_d + Y_{qq} v_q \end{aligned}, \quad (3.15)$$

and as it will be later verified by simulation in Fig. 3.24 and Fig. 3.40, cross-coupled admittances Y_{dq} and Y_{qd} can be disregarded. Neglecting Y_{dq} , Y_{qd} and by plugging in (3.14), (3.11) and (3.12) into (3.15), following is obtained:

$$\begin{bmatrix} Y_{dd,6n} \\ Y_{qq,6n} \end{bmatrix} \approx \begin{bmatrix} \left| \frac{Y_{abc,6n+1} V_{m,6n+1} \pm Y_{abc,6n-1} V_{m,6n-1}}{V_{m,6n+1} \pm V_{m,6n-1}} \right| \\ \left| \frac{Y_{abc,6n+1} V_{m,6n+1} \mp Y_{abc,6n-1} V_{m,6n-1}}{V_{m,6n+1} \mp V_{m,6n-1}} \right| \end{bmatrix}. \quad (3.16)$$

3.3. Design Guidelines for a Three-Phase Buck-Type Rectifier

Assuming that the admittance of the load cannot change by a significant value between harmonics $6n - 1$ and $6n + 1$ in the frequency range of interest, (3.16) can be further simplified as:

$$\begin{bmatrix} Y_{dd,6n} \\ Y_{qq,6n} \end{bmatrix} \approx \begin{bmatrix} Y_{abc,6n\pm1} \\ Y_{abc,6n\pm1} \end{bmatrix}, \quad (3.17)$$

where $Y_{abc,6n\pm1}$ is chosen to be the limit of the more restrictive two nearby harmonics $6n - 1$ and $6n + 1$ from abc domain. It will be shown in the later Sections that, due to very high degree of symmetry in the dq admittances, it is sufficient to satisfy the Y_{dd} limit in order to comply with the 10 % THDv test. As the final conclusion, the admittance limits already derived in Fig. 3.5 and Fig. 3.8 for three and four-wire connection are still valid in the dq domain and will be used as a benchmark in the rest of this Chapter. The proposed design methodology greatly simplifies the requirements of the 10 % THDv test by defining the maximum admittance as a function of frequency that the connected load has to meet in order to be compliant. In the following Sections, by means of current control, closed-loop input admittance of the converters is shaped in order to demonstrate the proposed hypothesis.

3.3 Design Guidelines for a Three-Phase Buck-Type Rectifier

The admittance limits derived in the previous Section are now applied to two fundamental topologies that can be found at the input of a three-phase AC/DC conversion: the three-phase buck-type and three-phase boost-type rectifiers.

The focus of this Section will be on the three-phase buck-type rectifier. First, derivation of the average dq model valid up to half of the switching frequency of the rectifier is done. Then, output inductor current controller is designed in order to shape closed-loop input admittance as per Section 3.2. Afterwards, simple mapping of the reactive components is made between abc and dq domains in order to model the impact of the EMI filtering components. It is shown that special care has to be taken in the design of the EMI filter since it's resonance has to be properly damped in order to meet with the 10 % THDv test. Lastly, it is concluded that the

Figure 3.9: The ideal three-phase buck-type rectifier.

bandwidth of the current controller is not a very critical design parameter, provided that it is at least higher than three times the output LC filter resonance frequency.

3.3.1 Three-Phase Buck-Type Rectifier dq Model Derivation

In order to derive a valid model for the three-phase buck-type rectifier, a focus is given to the ideal simplified rectifier circuit depicted in Fig. 3.9. Since it is a current-source topology, the DC link is modeled as a constant current source with the value i_L while on the AC link an ideal symmetrical, balanced three-phase voltage source is connected. The fundamental idea of this topology is to modulate the current of the DC link in such a way so that the input currents drawn from the three-phase source are also sinusoidal, symmetrical and balanced when a moving average is applied on the switching period. The basic buck-type rectifier from Fig. 3.9 employs six switches that are unidirectional in current conduction, but bidirectional in voltage blocking capability.

Analyzing the circuit, it can be concluded that there must always be a closed path for the current of the DC link to continue flowing from the negative rail back

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to the positive one. Therefore, main restriction is that at any point of time one (and only one) of the positive rail switches must be closed, as well as one of the negative rail. When one switch S_{i+} , $i \in \{A, B, C\}$ of the positive rail is connected and one from the negative rail which is in the different phase leg S_{j-} , $j \in \{A, B, C\}$, $i \neq j$, an energy transfer between AC and DC link is allowed to take place. These switching states are also called active states. When, on the other hand, one switch of the positive rail S_{i+} , $i \in \{A, B, C\}$ and the one that is in the same leg on the negative rail S_{j-} , $j \in \{A, B, C\}$, $i = j$ is closed, output current source is in short-circuit or free-wheeling state, while input voltage AC source does not have a closed path in order to circulate the DC link current. In these states, called inactive states, there is no energy transfer between AC and DC links. Utilizing active and inactive states in a determined sequence, indeed a balanced, symmetrical set of input currents can be achieved.

Mathematically, previous discussion can be described with following switching functions:

$$S_{Ak} + S_{Bk} + S_{Ck} = 1, k \in \{+, -\}, \quad (3.18)$$

where 1 denotes switch S_{ik} , $i \in \{A, B, C\}$ being closed and 0 being open. Instead of the defined switching functions, in the further analysis, it is convenient to use the following:

$$S_A = S_{A+} - S_{A-}, S_B = S_{B+} - S_{B-}, S_C = S_{C+} - S_{C-},$$

where now S_i equal to 1 means that the positive rail switch in the phase i is on, -1 means that the negative rail switch is on, and 0 either that no switch in phase i is on or that the phase is used for employing an inactive state. Moreover, due to (3.18) the following holds:

$$S_A + S_B + S_C = S_{A+} + S_{B+} + S_{C+} - (S_{A-} + S_{B-} + S_{C-}) = 1 - 1 = 0.$$

In order to develop the switching model of the basic buck-type rectifier, it is necessary to find the relationships of input phase currents i_{Ar} , i_{Br} and i_{Cr} as function of S_A , S_B , S_C and i_L and the relationship of the output voltage v_{OUTr} as function of S_A , S_B , S_C , v_{Ag} , v_{Bg} and v_{Cg} . For that purpose a combination of all allowed switching states is made and the dependency of corresponding input currents and voltages

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Table 3.3: Values of input currents, rail voltages and output voltage as a function of allowed switching states.

S_A	S_B	S_C	i_{Ar}	i_{Br}	i_{Cr}	v_+	v_-	v_{OUTr}
0	0	0	0	0	0	v_{Ag}	v_{Ag}	0
1	-1	0	i_L	$-i_L$	0	v_{Ag}	v_{Bg}	$v_{Ag} - v_{Bg}$
1	0	-1	i_L	0	$-i_L$	v_{Ag}	v_{Cg}	$v_{Ag} - v_{Cg}$
0	0	0	0	0	0	v_{Bg}	v_{Bg}	0
-1	1	0	$-i_L$	i_L	0	v_{Bg}	v_{Ag}	$-v_{Ag} + v_{Bg}$
0	1	-1	0	i_L	$-i_L$	v_{Bg}	v_{Cg}	$v_{Bg} - v_{Cg}$
0	0	0	0	0	0	v_{Cg}	v_{Cg}	0
-1	0	1	$-i_L$	0	i_L	v_{Cg}	v_{Ag}	$-v_{Ag} + v_{Cg}$
0	-1	1	0	$-i_L$	i_L	v_{Cg}	v_{Bg}	$-v_{Bg} + v_{Cg}$

is given in Table 3.3. Analyzing the results presented in Table 3.3 the following switching model of the three-phase buck-type rectifier can be obtained:

$$i_{Ar} = S_A i_L, \quad i_{Br} = S_B i_L, \quad i_{Cr} = S_C i_L, \quad (3.19)$$

$$v_{OUTr} = S_A v_{Ag} + S_B v_{Bg} + S_C v_{Cg}. \quad (3.20)$$

If a vector of input rectifier currents, voltages and switching functions is defined as:

$$\mathbf{i}_r = \begin{bmatrix} i_{Ar} \\ i_{Br} \\ i_{Cr} \end{bmatrix}, \quad \mathbf{v}_g = \begin{bmatrix} v_{Ag} \\ v_{Bg} \\ v_{Cg} \end{bmatrix}, \quad \mathbf{s} = \begin{bmatrix} s_A \\ s_B \\ s_C \end{bmatrix}, \quad (3.21)$$

then system of equations that describe the non-linear switching model of the three-phase buck-type rectifier from Fig. 3.9 can be written in compact vector form as:

$$\mathbf{i}_r = \mathbf{s} \mathbf{i}_L, \quad (3.22)$$

$$v_{OUTr} = \mathbf{s}^T \mathbf{v}_g. \quad (3.23)$$

A moving average operator on a switching period T_s is defined as:

$$\bar{x}(t) = \frac{1}{T_s} \int_{t-T_s}^t x(\tau) d\tau, \quad (3.24)$$

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Figure 3.10: The ideal three-phase buck-type rectifier with output LC filter.

where $x(t)$ can be any of the variables previously used in (3.22) and (3.23) and $\bar{x}(t)$ its moving averaged value. Applying averaging operator to the three-phase buck-type rectifier switching model the following set of equations is obtained:

$$\bar{\mathbf{i}}_{\mathbf{r}} = \mathbf{d} \bar{\mathbf{i}}_{\mathbf{L}}, \quad (3.25)$$

$$\bar{v}_{\text{OUTr}} = \mathbf{d}^T \bar{\mathbf{v}}_{\mathbf{g}}, \quad (3.26)$$

where, after averaging on the switching period T_s , the vector of switching functions $\mathbf{s}$ is converted into the vector of duty cycles $\mathbf{d}$. When a current space vector modulation is correctly implemented as per Table 3.3, the vector of duty cycles $\mathbf{d}$ forms a balanced, symmetrical three-phase signal as:

$$\mathbf{d} = \begin{bmatrix} D_m \cos(\omega t + \theta_0) \\ D_m \cos(\omega t - \frac{2\pi}{3} + \theta_0) \\ D_m \cos(\omega t + \frac{2\pi}{3} + \theta_0) \end{bmatrix}, \quad (3.27)$$

where D_m is modulation index that takes the values $D_m \in [0, 1]$, ω grid angular frequency and θ_0 its initial phase that can be used to modulate the rectifier as a resistive, inductive or capacitive three-phase load at the AC input.

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The ideal three-phase buck-type rectifier from Fig. 3.9 used for development of the switched and average model given by (3.22), (3.23) and (3.25), (3.26) respectively, is now going to be extended by inclusion of the LC filter on the output DC link, assuming resistive load R_{OUT} , as shown in Fig. 3.10. That effectively imposes steady-state unidirectional behaviour of the buck-type rectifier since, due to passive DC load, average value of the voltage v_{OUT} cannot be negative anymore. The average model of the buck-type rectifier with output LC filter is now given by following state-space equations:

$$2L_{\text{OUT}} \frac{d\bar{i}_L}{dt} = \mathbf{d}^T \bar{\mathbf{v}}_{\mathbf{g}} - \bar{v}_{\text{OUT}}, \quad (3.28)$$

$$C_{\text{OUT}} \frac{d\bar{v}_{\text{OUT}}}{dt} = \bar{i}_L - \frac{\bar{v}_{\text{OUT}}}{R_{\text{OUT}}}, \quad (3.29)$$

and by (3.25). In order to develop transfer functions and finally control the rectifier, newly obtained non-linear average model of the three-phase buck-type rectifier with output LC filter must be linearized around steady-state operating point. However, vectors $\mathbf{d}$, $\bar{\mathbf{v}}_{\mathbf{g}}$ and $\bar{\mathbf{i}}_{\mathbf{r}}$ all have sinusoidal steady-state. Therefore, definition of a operating point is not a straightforward task. In order to cope with that issue, an introduction of a Synchronous Reference Frame (SRF) or dq frame is done. Normally, SRF rotates at the same angular velocity as the resulting input voltage space vector and it is aligned to it by means of a Phase-Locked Loop (PLL). Therefore, from the point of view of SRF, all space vectors are now seen as stationary in the steady-state.

A general three-phase vector $\mathbf{x}_{\text{abc}}$ is transformed from abc to dq domain by the following mathematical expression:

$$\mathbf{x}_{\text{dq}} = \begin{bmatrix} x_d \\ x_q \end{bmatrix} = \frac{2}{3} \mathbf{T} \mathbf{x}_{\text{abc}}, \quad (3.30)$$

where $\mathbf{T}$ was previously defined in (3.6). Due to factor $2/3$ this transformation is amplitude invariant eg. amplitudes of three-phase values are equal in abc and in dq

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domain. Consequently, inverse dq transformation is done by:

$$\mathbf{x}_{abc} = \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = \mathbf{T}^T \mathbf{x}_{dq}. \quad (3.31)$$

As a result, multiplication of $\frac{2}{3}\mathbf{T}$ with $\mathbf{T}^T$ gives identity matrix of size two:

$$\frac{2}{3}\mathbf{T}\mathbf{T}^T = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}. \quad (3.32)$$

In order to obtain the average dq model of the three-phase buck-type rectifier with output LC filter [31, 70], (3.31) is plugged in (3.28) and (3.25) as:

$$\begin{aligned} 2L_{OUT} \frac{di_L}{dt} &= (\mathbf{T}^T \mathbf{d}_{dq})^T \mathbf{T}^T \mathbf{v}_{g,dq} - v_{OUT} \\ &= \mathbf{d}_{dq}^T \mathbf{T} \mathbf{T}^T \mathbf{v}_{g,dq} - v_{OUT} \\ &= \frac{3}{2} \mathbf{d}_{dq}^T \mathbf{v}_{g,dq} - v_{OUT}, \end{aligned} \quad (3.33)$$

$$\begin{aligned} \mathbf{T}^T \mathbf{i}_{r,dq} &= \mathbf{T}^T \mathbf{d}_{dq} i_L \\ \implies \mathbf{i}_{r,dq} &= \mathbf{d}_{dq} i_L, \end{aligned} \quad (3.34)$$

where the averaging operator has been removed and is always assumed from this point onward. The circuit diagram that represents dq model described with (3.33), (3.34) and (3.29) is given in Fig. 3.11. The newly obtained non-linear model is time invariant and as such can readily be linearized around steady-state DC operating point. Solving the circuit, assuming that the rectifier is emulating pure resistive three-phase load at the input port, the following is obtained:

$$D_D = \frac{2}{3} \frac{V_{OUT}}{V_{GD}}, D_Q = 0, \quad (3.35)$$

$$I_{RD} = D_D I_L, I_{RQ} = 0, \quad (3.36)$$

$$I_L = \frac{V_{OUT}}{R_{OUT}}, \quad (3.37)$$

which represents DC operating point. The linearized dq model is shown in Fig. 3.12, where $\hat{x}$ denotes averaged, small-signal value of a variable x . A set of equations that

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Figure 3.11: dq model of a three-phase buck-type rectifier with output LC filter.

Figure 3.12: Small-signal dq model of a three-phase buck-type rectifier with output LC filter.

describes the linearized circuit is as follows:

$$\hat{i}_{rd} = D_D \hat{i}_l + I_L \hat{d}_d, \quad (3.38)$$

$$\hat{i}_{rq} = D_Q \hat{i}_l + I_L \hat{d}_q, \quad (3.39)$$

$$2sL_{OUT}\hat{i}_l = \frac{3}{2} \left(D_D \hat{v}_{gd} + V_{GD} \hat{d}_d + D_Q \hat{v}_{gq} + V_{GQ} \hat{d}_q \right) - \hat{v}_{out}, \quad (3.40)$$

$$sC_{OUT}\hat{v}_{out} = \hat{i}_l - \frac{\hat{v}_{out}}{R_{OUT}}. \quad (3.41)$$

The system itself consists of four independent inputs $\hat{d}_d$, $\hat{d}_q$, $\hat{v}_{gd}$ and $\hat{v}_{gq}$. The open-loop transfer function on which PI regulator is applied is from duty cycle in d -axis to output inductors current, $G_{ld}(s)$. Another transfer function of interest is

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Figure 3.13: Block diagram of closed current loop three-phase buck-type rectifier in d -axis without EMI filter.

from $\hat{d}_d$ to input rectifier d -axis current $\hat{i}_{rd}$, $G_{dd}(s)$. Moreover, transfer function from $\hat{v}_{gd}$ to output inductors current $\hat{i}_l$, $Y_{ld}(s)$, also modifies the closed-loop input admittance value. Finally, the main transfer function that defines pass/fail criteria of the 10 % THD_v test is the open-loop input admittance in d -axis, $Y_{dd}(s)$, measured from $\hat{v}_{gd}$ to $\hat{i}_{rd}$. All of these mentioned transfer functions are given below:

$$G_{ld}(s) = \frac{\hat{i}_l(s)}{\hat{d}_d(s)} = V_{GD}Y(s) \quad (3.42)$$

$$G_{dd}(s) = \frac{\hat{i}_d(s)}{\hat{d}_d(s)} = D_D V_{GD}Y(s) + I_L \quad (3.43)$$

$$Y_{ld}(s) = \frac{\hat{i}_l(s)}{\hat{v}_{gd}(s)} = D_D Y(s) \quad (3.44)$$

$$Y_{dd}(s) = \frac{\hat{i}_{rd}(s)}{\hat{v}_{gd}(s)} = D_D^2 Y(s), \quad (3.45)$$

where:

$$Y(s) = \frac{3}{2} \frac{1}{R_{OUT}} \frac{R_{OUT}C_{OUT}s + 1}{2L_{OUT}C_{OUT}s^2 + 2L_{OUT}/R_{OUT}s + 1}. \quad (3.46)$$

In order to shape the input admittance $Y_d(s)$, a closed-loop control is imposed on the output inductors current $\hat{i}_l$. The block diagram of the system with current controller $K(s)$ in the form of PI regulator is shown in Fig. 3.13. Applying Mason's

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gain rule to the given block diagram, the closed-loop input admittance is:

$$Y_{d,CL}(s) = Y_{dd}(s) - Y_{ld}(s) \frac{K(s)G_{dd}(s)}{1 + K(s)G_{ld}(s)}. \quad (3.47)$$

The example of this design methodology is conducted on a 10 kW three-phase buck-type rectifier. With input line-to-neutral RMS voltage $V_{Ag,RMS}$ of 230 V and output voltage of 400 V, the steady-state duty cycle in d -axis can be calculated by (3.35) and is $D_D = 0.82$. Moreover, values of output capacitance C_{OUT} , output inductance L_{OUT} and switching frequency f_s have to be provided as a starting point. In [29], a comprehensive design methodology was done which includes calculations of the mentioned reactive components. Assuming f_s of 100 kHz, the value of total output inductance can be calculated as:

$$L_{OUT,tot} = 2L_{OUT} \geq \frac{V_{OUT}}{\Delta i_{Lout,pp,max}} \frac{1 - D_D}{f_s}, \quad (3.48)$$

where $\Delta i_{Lout,pp,max}$ equals to maximum peak-to-peak ripple of the output inductors current. Since total power at the output is equal to 10 kW, it follows that the average value of the inductors current I_L is equal to 25 A. In order for the rectifier to remain in continuous conduction mode (CCM) down to 10 % of the load, $\Delta i_{Lout,pp,max}$ is selected to be 7.5 % of the I_L which gives value of L_{OUT} at 200 μ H. Finally, the value of C_{OUT} is calculated as

$$C_{OUT} \geq \frac{I_L}{\Delta V_{OUT}} \Delta t_h, \quad (3.49)$$

where Δt_h is hold-up time at which the output capacitor voltage drops by ΔV_{OUT} during a three-phase input power loss, assuming constant discharge current of I_L . Here, hold-up time is selected to be one period of 800 Hz and the allowed voltage drop of 20 % which gives output capacitance C_{OUT} of approximately 400 μ F.

With values selected, the open-loop transfer function $G_{ld}(s)$ and loop-gain $K(s)G_{ld}(s)$ with cross-over frequency of 4.2 kHz Bode plots are given in Fig. 3.14. In them, a transport delay T_d of $0.75T_s$ is assumed which corresponds to double update of duty cycle at the switching frequency f_s . The corresponding parameters K_P and K_I of the regulator $K(s)$ are 0.024879 A^{-1} and 39.3088 C^{-1} respectively. A comparison of open-loop input admittance $Y_{dd}(s)$ and closed-loop input admittance

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Figure 3.14: Bode plot of open-loop transfer function $G_{id}(s)$ and loop-gain $L_{id}(s) = K(s)G_{id}(s)$ assuming transport delay $T_d = 0.75T_s$.

Figure 3.15: Bode plot of open-loop input admittance $Y_{dd}(s)$ and closed-loop input admittance $Y_{d,CL}(s)$ for various current control loop bandwidths.

with different current controller bandwidths against 3-wire 10 % THD_v limits is given in Fig. 3.15. As it can be seen, the faster the current controller, the lower the closed-loop input admittance. However, it can also be noted that even 2.2 kHz cross-over frequency of current loop is enough to force the $Y_{d,CL}$ below the derived limits for the 10 % THD_v test. Therefore, it can be concluded that it is sufficient for the rectifier to operate in closed current loop with relatively low controller bandwidth in order to comply with the 10 % THD_v test. From this point onward, the cross-over frequency of the current loop is assumed at 4.2 kHz.

Even though example of the closed-loop input admittance gives good insight into the rectifier ability to reject harmonics, it is of little practical use. Namely, due to high frequency PWM shape of input currents, differential EMI filter must

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be included. Therefore, special attention is now given to the conversion of resistors, capacitors and inductors from abc to dq domain when they are located on the AC side of the rectifier.

A general set of equations of a balanced three-phase star connected capacitor C is given by:

$$\begin{aligned} i_A &= C \frac{dv_A}{dt} \\ i_B &= C \frac{dv_B}{dt}, \\ i_C &= C \frac{dv_C}{dt} \end{aligned} \quad (3.50)$$

or rewritten in vector form similar to (3.21):

$$\mathbf{i} = C \frac{d\mathbf{v}}{dt}. \quad (3.51)$$

Applying (3.31):

$$\mathbf{T}^T \mathbf{i}_{dq} = C \frac{d(\mathbf{T}^T \mathbf{v}_{dq})}{dt}, \quad (3.52)$$

and expanding further:

$$\mathbf{T}^T \mathbf{i}_{dq} = C \frac{d\mathbf{T}^T}{dt} \mathbf{v}_{dq} + C \mathbf{T}^T \frac{d\mathbf{v}_{dq}}{dt}. \quad (3.53)$$

Multiplying from the left with $2/3 \mathbf{T}$:

$$\frac{2}{3} \mathbf{T} \mathbf{T}^T \mathbf{i}_{dq} = C \frac{2}{3} \mathbf{T} \frac{d\mathbf{T}^T}{dt} \mathbf{v}_{dq} + C \frac{2}{3} \mathbf{T} \mathbf{T}^T \frac{d\mathbf{v}_{dq}}{dt}. \quad (3.54)$$

According to (3.32), $2/3 \mathbf{T} \mathbf{T}^T$ is equal to identity matrix of size two. Therefore, it is of interest to develop $(d\mathbf{T}^T)/(dt)$ further as:

$$\frac{d\mathbf{T}^T}{dt} = -\omega \begin{bmatrix} \sin(\omega t) & \cos(\omega t) \\ \sin(\omega t - \frac{2\pi}{3}) & \cos(\omega t - \frac{2\pi}{3}) \\ \sin(\omega t + \frac{2\pi}{3}) & \cos(\omega t + \frac{2\pi}{3}) \end{bmatrix}. \quad (3.55)$$

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Multiplying (3.6) and (3.55) it is obtained:

$$\frac{2}{3}\mathbf{T}\frac{d\mathbf{T}^T}{dt} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix}. \quad (3.56)$$

Plugging in (3.56) to (3.54) finally yields:

$$\mathbf{i}_{dq} = \begin{bmatrix} 0 & -\omega C \\ \omega C & 0 \end{bmatrix} \mathbf{v}_{dq} + C \frac{d\mathbf{v}_{dq}}{dt}, \quad (3.57)$$

or rewritten in the form of system of two equations:

$$i_d = -\omega C v_q + C \frac{dv_d}{dt} \quad (3.58)$$

$$i_q = \omega C v_d + C \frac{dv_q}{dt}. \quad (3.59)$$

A similar pattern of mathematical manipulations can be done in order to map a balanced three-phase inductor L from abc to dq domain. In abc domain balanced three-phase inductance L it is described by following equations:

$$\begin{aligned} v_A &= L \frac{di_A}{dt} \\ v_B &= L \frac{di_B}{dt}, \\ v_C &= L \frac{di_C}{dt} \end{aligned} \quad (3.60)$$

or in more compact vector form:

$$\mathbf{v} = L \frac{d\mathbf{i}}{dt}. \quad (3.61)$$

It is easily observable that just by interchanging current and voltage vectors, with respect to the capacitor case given by (3.51), the dq mapped three-phase inductance L is represented by:

$$\mathbf{v}_{dq} = \begin{bmatrix} 0 & -\omega L \\ \omega L & 0 \end{bmatrix} \mathbf{i}_{dq} + L \frac{d\mathbf{i}_{dq}}{dt}, \quad (3.62)$$

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Figure 3.16: Mapping of a three-phase inductance L and a three-phase capacitance C from abc to dq domain.

or rewritten in the form of system of two equations:

$$v_d = -\omega L i_q + L \frac{di_d}{dt} \quad (3.63)$$

$$v_q = \omega L i_d + L \frac{di_q}{dt}. \quad (3.64)$$

The graphical illustration of mapping of the three-phase capacitance C and three-phase inductance L is given in Fig. 3.16. It can be seen that the values of inductance or capacitance are preserved, with an addition of cross-coupling terms in the form of current-controlled voltage sources in the inductor case and voltage-controlled current sources in the capacitor case. They represent the influence of d sub-circuit on q and vice-versa.

On the other hand, a balanced three-phase resistance R is mapped from abc to dq domain unchanged since voltage to current relationship is frequency independent.

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Figure 3.17: dq model of a three-phase buck-type rectifier with output LC filter and input C_e EMI capacitor.

Using the developed mapping scheme of the passive components, an EMI filter can be successfully modeled and its influence to the 10 % THD_v test addressed in detail.

Due to discontinuous input currents, a decoupling capacitor C_e must be included on the rectifier input port. In [29] the following equation for capacitor selection is proposed:

$$C_e \geq \frac{I_L D_D (1 - D_D)}{\Delta v_{C_e, pp, max} f_s}, \quad (3.65)$$

where $\Delta v_{ce, pp, max}$ is maximum allowed peak-to-peak voltage ripple occurring on the capacitor C_e . The large value of capacitance C_e although helps minimize the ripple and high frequency EMI filtering effort, it is penalizing rectifier PF since it is connected in parallel to the three-phase source. On the other hand, too low value would yield large ripple voltage and difficulties for the measurement subsystem. As a good compromise value, maximum peak-to-peak ripple voltage is chosen to be 10 % of V_{GD} , which gives capacitance C_e of 1.15 μF . Adding C_e to the dq model of the rectifier, as shown in Fig. 3.17, modifies the input admittance. The effect on the input admittance is, due to superposition, very simple to assess and is given by:

$$Y_{d, CL, C_e}(s) = Y_{d, CL}(s) + sC_e, \quad (3.66)$$

where $Y_{d, CL}(s)$ is previously calculated in (3.47). In Fig. 3.18, a comparison of closed-loop input admittance $Y_{d, CL}$ without C_e and closed-loop input admittance Y_{d, CL, C_e} for different C_e values with respect to the value that provides 10 % ripple

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Figure 3.18: Bode plot of closed-loop input admittance $Y_{d,CL}(s)$ without C_e and closed-loop input admittance $Y_{d,CL,Ce}(s)$ for different C_e values.

Figure 3.19: Single resistor damping options for LC differential EMI filter: (a) parallel $R_d - C_d$, (b) parallel $R_d - L_d$, (c) series $R_d - L_d$.

according to (3.65) is shown. It can be concluded that there is a maximum capacitance C_e that will draw reactive currents high enough to impose failure of the 10 % THD_v test. In the case at hand, the value is approximately 4 times higher than the value that is used for the remainder of this analysis.

Although this analysis imposed a maximum value of capacitance C_e , it represents best case scenario. Namely, in real applications, there exists an impedance between the three-phase source and rectifier input capacitance. It is manifested as source output impedance and/or impedance of interconnecting cabling. Normally, impedance of that kind is inductive in nature, especially in avionic applications where three-phase generators are commonly electrical machines. In order for the proposed modeling to be complete, an inductive series impedance L_g is included from this point onward, and its effect analyzed in detail.

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Addition of L_g along with C_e adds a resonance into all transfer functions that is undamped. As a consequence, filter output impedance becomes infinite at resonant frequency and will cause instability of the converter. In order to cope this issue, in [71] an optimal single resistor damping of LC filters is proposed. In it, three ways of designing an optimally damped LC filter has been given as shown in Fig. 3.19. The term "optimal" refers to minimum peak of LC filter impedance for a given reactive damping element value. A brief discussion is provided below regarding advantages and disadvantages of these three damping methods.

The parallel $R_d - C_d$ option given in Fig. 3.19a has the advantage that no extra inductive element is used, thus total system weight increment is marginal. In order for this damping method to be effective, in the vicinity of $L_g - C_e$ resonant frequency, R_d must have a value that is at least comparable to the impedance of C_d . Moreover, at high frequencies, LC filter attenuation is not affected by the parallel damping branch. However, since this work is focused on the three-phase rectifiers, both C_e and C_d present an undesired reactive load. Therefore, if this damping method is chosen, the combined value of C_e and C_d must be kept to a minimal practical value in order not to impair PF at 800 Hz and to avoid unnecessary increment in total system volume. Apart from handling harmonics around resonant frequency, R_d also sees component at grid frequency which means that it cannot take too high values since it will compromise total system efficiency.

The second provided damping option is parallel $R_d - L_d$ given in Fig. 3.19b. In order for this damping method to be effective, in the vicinity of $L_g - C_e$ resonant frequency, R_d must have a value that is at least comparable to the impedance of L_d . The main advantage is that the damping inductor L_d does not carry full line current, therefore expected weight increment is not high. Moreover, it does not reactively load the three-phase source in a relevant manner. The downside of this case is that high frequency attenuation is degraded since equivalent inductor after resonance seen by the source is reduced to $L_g || L_d$. The trade-off is reflected in damping peak reduction against high frequency attenuation degradation.

The last provided damping method is series $R_d - L_d$ given in Fig. 3.19c. Similar to the previous case, in order for this damping method to be effective, in the vicinity of $L_g - C_e$ resonant frequency, R_d must have a value that is at least comparable to the impedance of L_d . The advantage of this method is that high frequency attenuation is

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not compromised. Also, impact on the rectifier PF remains insignificant. However, main drawback of this option is that L_d carries full line current thus system weight increment is significant. The main trade-off in this case lies in the damping efficiency versus damping inductor size.

Based on the previously proposed damping methods and aircraft application specifics, more appropriate solution is now selected. Since in aircraft systems weight is the most important parameter, both methods that utilize inductive damping are presenting an issue. The series $R_d - L_d$ given in Fig. 3.19c does not offer significant benefits at the price of large increment of weight. The parallel $R_d - L_d$ given in Fig. 3.19b could be an interesting solution, since high frequency attenuation may be compromised for the sake of damping efficiency. Moreover, PF would remain unchanged. However, in order to reduce the weight of the system, in this work L_g is assumed that it is source output impedance incremented by the parasitic inductances of the interconnecting cabling, making it inaccessible for the designer. That assumption is mostly justified since in aircraft systems three-phase voltage generation is done by electrical machines which do have inductive output impedance due to windings in stator. Therefore, this work is always going to assume parallel $R_d - C_d$ option given in Fig. 3.19a and its design criteria is addressed next.

Work presented in [71] also provides a simple equation for calculation of R_d :

$$R_d = \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)} \frac{L_g}{C_e}} \quad (3.67)$$

where $n = C_d/C_e$. For a given set of L_g , C_e and C_d , (3.67) gives a value of R_d that guarantees minimum peak in the filter impedance. As a good compromise value between rectifier PF at 800 Hz and minimization of damping peak, a value of n is chosen to be 0.52 which yields C_d of 0.6 μ F. That value is always assumed for the remainder of this Section. Apart from the negative effect on the PF of this damping method, the damping resistance is dissipating extra unnecessary energy at line frequency. Assuming that impedance of C_d at line frequency is much larger than the resistance R_d , the following holds:

$$P_{Rd} = R_d I_d^2 = \frac{1}{2} R_d (\omega C_d V_{GD})^2. \quad (3.68)$$

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Therefore, for a fixed C_d , the higher the line inductance L_g , the higher the value of R_d and the dissipation P_{Rd} as per (3.67) and (3.68) respectively. Taking for example L_g of 135 μH , it follows R_d of 26 Ω and P_{Rd} of 12.5 W at 800 Hz grid frequency, which translates into 0.4 % efficiency loss at full load of 10 kW. Moreover, P_{Rd} is load independent, thus it would be beneficial to reduce it in order to improve efficiency over whole output power range. In order to minimize this effect, idea from series $R_d - L_d$ from Fig. 3.19c can be used. Since in this case current flowing through R_d is very low, the size of L_d is going to be very small and its impact on the overall system weight marginal. Placing of L_d in parallel with R_d from Fig. 3.19a has some constraints. Namely, since power loss at highest line frequency is desired to be minimized, it follows that the smaller its value, the lower the power loss P_{Rd} . On the other side, if L_d is chosen to be too low, then it would short-circuit R_d around $L_g - C_e$ resonant frequency which would defeat its purpose. Therefore, there exists an optimum range of L_d in which it would considerably reduce power dissipation P_{Rd} , while presenting sufficiently large impedance around filter resonance in order not to impair damping resistor effectiveness.

If at maximum grid frequency $f_{\max}$, the impedance of L_d must be k times the R_d , then limit for the maximum $L_{d,\max}$ is obtained as:

$$L_{d,\max} = \frac{kR_d}{2\pi f_{\max}} = \frac{k}{2\pi f_{\max}} \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)} \frac{L_g}{C_e}}. \quad (3.69)$$

On the other hand, if at $L_g - C_e$ resonant angular frequency ω_0 , the impedance of L_d must be p times the R_d , then limit for the minimum $L_{d,\min}$ is obtained as:

$$L_{d,\min} = \frac{pR_d}{\omega_0} = p \sqrt{\frac{(2+n)(4+3n)}{2n^2(4+n)}} L_g. \quad (3.70)$$

Since minimum value of $L_{d,\min}$ is proportional to L_g while the maximum value $L_{d,\max}$ is proportional to $\sqrt{L_g}$, then it follows that the set of equations (3.69)-(3.70) can result in no solution if k and p are selected to be too strict. Experiments show that $p = 3$ and $k = 10$ provide a good compromise between damping effectiveness reduction and damping resistance power dissipation reduction. Since all parameters of the damping branch, except L_g are defined, the final three-phase buck-type

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Figure 3.20: The three-phase buck-type rectifier with output LC filter and input differential EMI stage.

Figure 3.21: dq model of a three-phase buck-type rectifier with output LC filter and input differential EMI stage.

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rectifier circuit is given in Fig. 3.20, while its equivalent dq model is provided in Fig. 3.21. The final buck-type rectifier circuit has included output free-wheeling diode D_{FW} which helps reduce conduction losses during an inactive state. It also increments reliability since it eliminates the forbidden state in which all switches are open by always providing a path for current i_L . Its addition does not modify the previously presented dq modeling approach in any way.

In order to analyze the effect of L_g on the 10 % THD_v test, a range of possible L_g values is addressed next. Normally, the maximum line impedance $L_{g,max}$ is governed by the generator output power in the sense that it is reverse proportional to the machine nominal power and it is a very important parameter since it imposes a limit in the current controller bandwidth. Namely, for a desired current controller bandwidth f_{BW} , the maximum value of $L_{g,max}$ value can be estimated. As a first approximation, the $L_g - C_e$ resonance must be at least three times the frequency of f_{BW} in order not to impair stability. Therefore, $L_{g,max}$ can be mathematically expressed as:

$$L_{g,max} = \frac{1}{3(2\pi f_{BW})^2 C_e}. \quad (3.71)$$

On the other hand, minimum value of the inductance $L_{g,min}$ is determined by peaking at the resonance since characteristic impedance of the filter reduces with decrease of L_g . The location of the minimum value is not a linear task and it is done by trial and error. The range that is covered in this work is from L_g equal to 35 μH up to 135 μH . For that span of L_g , the range in which impedance of L_d is at least ten times lower at maximum grid frequency f_{MAX} of 800 Hz and three times larger than R_d at resonant frequency f_0 does not exist. Nevertheless, as it is going to be soon shown, the highest priority should be given to optimization for minimum L_g , since then the characteristic impedance of $L_g - C_e$ is the lowest. Therefore, for $L_g = 35 \mu\text{H}$, $p = 3$ and $k = 10$ the range of $[L_{d,min}, L_{d,max}]$ given by (3.69)-(3.70) is [250 μH , 262 μH]. The value chosen is 260 μH . Finally, the analytical calculation of closed-loop input admittance $Y_{d,CL,EMI}(s)$, due to complexity of full dq model shown in Fig. 3.20, is not easily calculated and it is obtained numerically by linearizing mentioned circuit with Matlab/Simulink.

The overview of the parameters that are used for the closed-loop input admittance $Y_{d,CL,EMI}(s)$ with input $L_g - C_e$ filter are given in Table 3.4.

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Table 3.4: 10 kW three-phase buck-type rectifier parameters.

$V_{Ag,RMS}$ [V]	L_g [μ H]	C_e [μ F]	C_d [μ F]	R_d [Ω]
230	35-155	1.15	0.6	13.5-26
L_d [μ H]	L_{OUT} [μ H]	C_{OUT} [μ F]	V_{OUT} [V]	f_s [kHz]
320	200	400	400	100

Depending on the line inductance L_g , the optimal damping resistor $R_{d,opt}$ changes proportionally to the square root of the inductance as per (3.67). However, in the final design, one value of R_d must be chosen. The value chosen here is the optimal value for the minimum line inductance L_g , since that is when characteristic impedance of the filter is at minimum value provoking maximum peaking in $Y_{d,CL,EMI}(s)$. The final plot of $Y_{d,CL,EMI}(s)$ is given in Fig. 3.22a for the case of optimal R_d at L_g of 35 μ H. It can be seen that for the lowest value of line inductance, the closed-loop input admittance is very close to provoke the failure of compliance with the 10 % THD_v test. Moreover, the higher the L_g the higher the characteristic impedance of the filter, which translates into lower peaking in input admittance. In Fig. 3.22b, a zoom-in comparison is made of different optimal damping resistances R_d for each line inductance L_g . As it is expected, the farther the inductance L_g from the designed optimum, more deviation is present. Therefore, there exists a range of line inductances L_g for which the design is going to be compliant. Higher values than predicted by (3.71) would cause system stability concerns and ultimately reduction of current controller bandwidth. The plot of the current control loop gain for various L_g values is given in Fig. 3.23. It can be seen that, for the case of the line impedance of 135 μ H, due to the impact of the EMI filter on all transfer functions, the loop-gain exhibits a peak that is close to 0 dB in the frequency range of the resonance of EMI filter. Lastly, in order to demonstrate that the coupling admittances Y_{qd} and Y_{dq} do not significantly impact the limits previously derived in Section 3.2, the plot of all four admittances is given in Fig. 3.24 for the case L_g at 35 μ H.

In order to verify the proposed design methodology, a set of simulations is carried out in power electronics simulator GeckoCIRCUITS [72]. The results are presented at 10 kW output power and according to parameters from Table 3.4. For each line impedance analyzed in Fig. 3.22a, one figure that represents worst case line frequency of input voltages and currents under 10 % THD_v test is given. Moreover,

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Figure 3.22: Plot of the closed-loop input admittance $Y_{d,CL,EMI}(s)$ for various line impedances L_g with single resistor damping option for LC differential EMI filter with: (a) optimal R_d for $L_g = 35 \mu\text{H}$, (b) different optimal R_d dependent on L_g compared to (a).

Figure 3.23: Bode plot of current loop gain for various line impedances under optimal damping for $L_g = 35 \mu\text{H}$.

Figure 3.24: Bode plot of closed-loop input admittances Y_{dd} , Y_{qd} , Y_{dq} and Y_{qq} for $L_g = 35 \mu\text{H}$.

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Figure 3.25: Simulation results with line impedance $L_g = 35 \mu\text{H}$ of input three-phase voltages and currents for the worst case line frequency of 600 Hz under 10 % THD_v test.

Figure 3.26: Simulation results with line impedance $L_g = 35 \mu\text{H}$ of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

phase A current spectrum for frequencies 360, 400, 500, 600, 700 and 800 Hz against DO-160G limits is provided split into two figures for the sake of clarity.

As it is predicted by closed-loop input admittance $Y_{d,CL,EMI}(s)$ on the case of L_g of $35 \mu\text{H}$, the 10 % THD_v test is on the limit of compliance as shown by simulation results presented in Fig. 3.26, with time waveforms given in Fig. 3.25. Namely, for the line frequency of 600 Hz, the 37th harmonic is located at 22.2 kHz, and according to Fig. 3.26b is at the DO-160G limit. That is exactly the frequency region where closed-loop input admittance $Y_{d,CL,EMI}(s)$ from Fig. 3.22a exhibits its peak. The

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Figure 3.27: Simulation results with line impedance $L_g = 55 \mu\text{H}$ of input three-phase voltages and currents for the line frequency of 650 Hz under 10 % THDv test.

Figure 3.28: Simulation results with line impedance $L_g = 55 \mu\text{H}$ of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

voltage and current waveforms presented in Fig. 3.25, illustrate the case that is on the limit of compliance with 600 Hz line frequency.

Next analyzed case is with line impedance L_g of $55 \mu\text{H}$, where simulation results are given in Fig. 3.27 and Fig. 3.28. This case is fully compliant with the DO-160G 10 % THDv test, as it is predicted by closed-loop input admittance $Y_{d,CL,EMI}(s)$ from Fig. 3.22a. The peaking in $Y_{d,CL,EMI}(s)$ now occurs around 17 kHz. Consequently, in Fig. 3.28b the harmonics around 21st are amplified which is in the vicinity of 16.8 kHz for 800 Hz fundamental case. The voltage and current waveforms presented

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Figure 3.29: Simulation results with line impedance $L_g = 95 \mu\text{H}$ of input three-phase voltages and currents for the line frequency of 700 Hz under 10 % THD_v test.

Figure 3.30: Simulation results with line impedance $L_g = 95 \mu\text{H}$ of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

in Fig. 3.28, illustrate the performance of the 10 % THD_v test compliant design at 650 Hz line frequency.

Further increase of line impedance L_g to $95 \mu\text{H}$ and its impact on the 10 % THD_v test is presented in Figs. 3.29 and 3.30. This is another fully compliant DO-160G 10 % THD_v test design, as predicted by closed-loop input admittance $Y_{d,CL,EMI}(s)$ from Fig. 3.22a. Input admittance exhibits maximum values in the vicinity of 13 kHz which translates into harmonics around 19th for 700 Hz line frequency or 23rd for 500 Hz line frequency. That is confirmed by input current harmonic content given in Figs. 3.30a and 3.30b.

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Figure 3.31: Simulation results with line impedance $L_g = 135 \mu\text{H}$ of input three-phase voltages and currents for the line frequency of 800 Hz under 10 % THDv test.

Figure 3.32: Simulation results with line impedance $L_g = 135 \mu\text{H}$ of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

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Finally, the highest line impedance L_g , which is on the limit of impairing closed-loop system stability, as predicted by (3.71), is 135 μH . The simulation results for this case are given in Figs. 3.31 and 3.32. The compliance of this design is accurately predicted by closed-loop input admittance $Y_{d,CL,EMI}(s)$ from Fig. 3.22a. As it can be seen in Fig. 3.32b, the harmonics around 13th are amplified for 800 Hz case which translates into frequency range around 10 kHz. That is precisely where $Y_{d,CL,EMI}(s)$ exhibits maximum values. Lastly, the voltage and current waveforms presented in Fig. 3.31, illustrate the performance of the 10 % THD_v test compliant design at 800 Hz line frequency.

3.3.2 Summary and Discussion

To conclude this Section, a brief summary is provided. The previously developed dq admittance limits from Section 3.2 are applied on the three-phase buck-type topology and key points are addressed. First, a detailed development of the basic rectifier switching model is provided. Then, by introducing moving average operator, an average model is calculated in Stationary Reference Frame (abc domain). Afterwards, dq transformation of the average model is done and dq equivalent model is obtained. Next, output DC link LC filter is added and successfully modeled, followed by development of small-signal model. It allowed definition of key transfer functions necessary for the proposed design methodology. The two most important transfer functions are open-loop input admittance $Y_{dd}(s)$ and duty cycle to output inductor current $G_{ld}(s)$. It is realized that open-loop input admittance is above predicted 10 % THD_v test admittance limits. Therefore, input admittance is shaped by means of PI current control on the output inductor current. Analysis of various current controller bandwidths is addressed, as well as their impact on closed-loop input admittance $Y_{d,CL}(s)$. Also, transport delay T_d of $0.75T_s$ is introduced in order to model ADC sampling acquisition time, microcontroller code execution time and duty cycle update routine. Due to discontinuous input currents of three-phase buck-type rectifiers, input EMI capacitors C_e are added. Therefore, modeling of reactive components such as inductances and capacitances is done and their equivalent circuits in dq domain are provided. With the inclusion of C_e into the dq model, its influence of newly obtained closed-loop input admittance $Y_{d,CL,C_e}(s)$ is addressed. It is shown that there exists maximum capacitance C_e that will cause

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failure of the compliance with the 10 % THD_v test. Furthermore, inclusion of unavoidable line inductance L_g is done. Its addition created an unwanted resonance in the EMI filter and methods to minimize its impact are addressed. The method consists in passive damping of the newly obtained LC filter. Three passive damping methods are shown and their advantages and disadvantages addressed. The selected passive damping method is parallel $R_d - C_d$ since it yields minimum increment in overall system weight. In order to minimize unwanted line-frequency dissipation in the damping resistor, a shunt inductance L_d is introduced and its design guideline presented. Consequently, complete dq model with input EMI filter and output LC filter is provided. Finally, a range of line inductances that must be known beforehand is addressed and their impact on the design is analyzed. It is shown that there exists a minimum line inductance that causes failure of compliance with the 10 % THD_v test. The reason lies in reduction of characteristic impedance of the EMI filter which translates into higher peaking in the closed-loop input admittance. Therefore, optimum damping resistance value for the minimum line inductance L_g is selected, since increment of L_g reduces the peak in closed-loop input admittance. The maximum value of line inductance is limited by the desired current controller bandwidth. Further increments of line inductance above maximum value forces reduction of current controller bandwidth, as given by (3.71).

From the practical standpoint it is reasonable to focus on the higher values of L_g due to high-frequency conducted EMI issues not addressed in this Section. Apart from EMI concerns, lower values of C_e than already chosen for 10 % peak-to-peak voltage ripple calculated by (3.65) would violate the assumption that the voltage applied on the output inductors L_{OUT} is approximately constant during switching states. Therefore, it is highly likely that, by taking into account EMI issues, L_g would have to increase and/or addition of a second EMI filter stage would be necessary. Due to rectifier's rather low sensitivity to the current controller bandwidth, its reduction would offer design space for the high-frequency conducted EMI requirements as per Fig. 1.4, while maintaining compliance with the 10 % THD_v test.

3.4 Design Guidelines for a Three-Phase VIENNA Rectifier

Among boost-type rectifiers, VIENNA rectifier is selected to obtain the design guidelines to meet the 10 % THD_v regulation, thus it is thoroughly analyzed in this Section. Similarly, derivation of the average dq model valid up to half of the switching frequency of the rectifier is derived. Since in boost-type topologies the inductors are located on the AC side, shaping of the input admittance is done by closing the loop on two input currents in d and q axes. Due to duality of this rectifier compared to the buck-type, fundamental differences emerge during the design process. Namely, the most critical parameter is formed in the product of input three-phase inductance value with current controller bandwidth. For the same size of magnetic components compared with the buck-type case, higher bandwidth of current loop is mandatory for the 10 % THD_v test compliance. On the other hand, due to presence of inductors on the AC side, the addition of EMI filtering capacitance is relatively small, making boost-type topologies rather insensitive to differential EMI filter design. Finally, experimental results on a 10 kW SiC prototype are provided that back up proposed design methodology in a very close manner.

3.4.1 Three-Phase VIENNA Rectifier dq Model Derivation

In order to derive the valid model for the three-phase VIENNA rectifier, a focus is given to the rectifier circuit depicted in Fig. 3.33. As in all boost-type rectifiers, the basic idea is to modulate the switches in the manner that three-phase currents through the inductors L_r are sinusoidal, symmetrical and balanced when a moving average is applied on the switching period. The equivalent circuit on the AC side that illustrates that idea is given in Fig 3.34. The VIENNA rectifier is unidirectional three-level voltage-source topology where the voltage space vectors that can be attained are governed by the input current space vector. Namely, when input phase current i_k is positive, the switched node voltage v_{kr} can take only values of v_{C1} or 0 V, where $k \in \{A, B, C\}$. Similarly, for the negative currents v_{kr} takes values of $-v_{C2}$ or 0 V.

The set of equations that describes the VIENNA rectifier on the AC terminals can be obtained from circuit given in Fig. 3.34 as:

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Figure 3.33: The basic three-phase VIENNA rectifier.

Figure 3.34: The boost-type topologies equivalent AC terminal model.

$$\begin{aligned}
 L_r \frac{di_{Ar}}{dt} &= v_{Ag} - R_L i_{Ar} - v_{ArM} - v_M \\
 L_r \frac{di_{Br}}{dt} &= v_{Bg} - R_L i_{Br} - v_{BrM} - v_M, \\
 L_r \frac{di_{Cr}}{dt} &= v_{Cg} - R_L i_{Cr} - v_{CrM} - v_M
 \end{aligned} \tag{3.72}$$

where $v_{krM} = v_{kr} - v_M$, $k \in \{A, B, C\}$. With the constraint that the upper switches S_{k+} are active when the corresponding phase current i_{kr} is positive, and the lower switches S_{k-} when the current is negative, the switching function can be defined as

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Table 3.5: Dependency of the switched node voltage v_{krM} on the circuit states.

$\text{sgn}(i_{\text{kr}})$	S_{k}	v_{krM}
1	1	0
1	0	v_{C1}
0	1	0
0	0	$-v_{\text{C2}}$

follows:

$$S_{\text{k}} = \begin{cases} 1, & ((S_{\text{k}+} = 1) \wedge (i_{\text{kr}} > 0)) \vee ((S_{\text{k}-} = 1) \wedge (i_{\text{kr}} < 0)) \\ 0, & ((S_{\text{k}+} = 0) \wedge (i_{\text{kr}} > 0)) \vee ((S_{\text{k}-} = 0) \wedge (i_{\text{kr}} < 0)) \end{cases}. \quad (3.73)$$

Defining the total output voltage v_{OUT} and the output voltage unbalance Δv as:

$$\begin{aligned} v_{\text{OUT}} &= v_{\text{C1}} + v_{\text{C2}} \\ \Delta v &= v_{\text{C1}} - v_{\text{C2}} \end{aligned}, \quad (3.74)$$

the output capacitors voltage can be expressed as a function of total output voltage v_{OUT} and output voltage unbalance Δv as:

$$\begin{aligned} v_{\text{C1}} &= \frac{v_{\text{OUT}}}{2} \left(1 + \frac{\Delta v}{v_{\text{OUT}}} \right) \\ v_{\text{C2}} &= -\frac{v_{\text{OUT}}}{2} \left(-1 + \frac{\Delta v}{v_{\text{OUT}}} \right) \end{aligned}. \quad (3.75)$$

With these definitions, the value of voltage v_{krM} as a function of sign of corresponding current i_{kr} and a switching function S_{k} for all combinations is presented in Table 3.5. From Table 3.5 the voltage v_{krM} can be obtained as:

$$v_{\text{krM}} = \frac{v_{\text{OUT}}}{2} \left(\text{sgn}(i_{\text{kr}}) + \frac{\Delta v}{v_{\text{OUT}}} \right) (1 - S_{\text{k}}). \quad (3.76)$$

Under the assumption that the output voltage unbalance is much smaller than the total output voltage, (3.76) can be simplified as:

$$v_{\text{krM}} = \frac{v_{\text{OUT}}}{2} \text{sgn}(i_{\text{kr}}) (1 - S_{\text{k}}). \quad (3.77)$$

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Defining a phase duty cycle as:

$$d'_k = \text{sgn}(i_{kr})(1 - K_k) = d_k + d_0, \quad (3.78)$$

where K_k is moving average value of a switching function S_k , d_k differential component of the phase duty cycle and d_0 zero-sequence or common-mode duty cycle. Having in mind that this is a three-wire connected topology eg:

$$i_{Ar} + i_{Br} + i_{Cr} = 0, \quad (3.79)$$

it follows that zero-sequence in voltages and duty cycles cannot contribute to the power flow, which can also be concluded by observing the equivalent AC terminal circuit previously given in Fig. 3.34. Namely, the common-mode voltage v_M from Fig. 3.34 can be disregarded in the further average model derivation. Plugging in (3.78) and (3.77) into (3.72) the following average model in abc domain is obtained [73]:

$$\begin{aligned} L_r \frac{di_{Ar}}{dt} &= v_{Ag} - R_L i_{Ar} - d_A \frac{v_{OUT}}{2} \\ L_r \frac{di_{Br}}{dt} &= v_{Bg} - R_L i_{Br} - d_B \frac{v_{OUT}}{2}, \\ L_r \frac{di_{Cr}}{dt} &= v_{Cg} - R_L i_{Cr} - d_C \frac{v_{OUT}}{2} \end{aligned} \quad (3.80)$$

where common-mode duty cycle d_0 is disregarded. In order to easily make the transformation from abc to the dq domain, the AC terminal average model of VIENNA rectifier can be rewritten in compact matrix form as:

$$L_r \frac{d\mathbf{i}_r}{dt} = \mathbf{v}_g - R_L \mathbf{i}_r - \mathbf{d} \frac{v_{OUT}}{2}, \quad (3.81)$$

where $\mathbf{i}_r$, $\mathbf{v}_g$ and $\mathbf{d}$ were previously defined by (3.21) and (3.27). On the DC terminal side the state-space equations are:

$$\begin{aligned} 2C_{OUT} \frac{dv_{C1}}{dt} &= i_+ - \frac{v_{OUT}}{R_{OUT}}, \\ 2C_{OUT} \frac{dv_{C2}}{dt} &= i_- - \frac{v_{OUT}}{R_{OUT}} \end{aligned} \quad (3.82)$$

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where by first Kirchhoff's law:

$$\begin{aligned} i_+ &= i_{A+} + i_{B+} + i_{C+} \\ i_- &= i_{A-} + i_{B-} + i_{C-} \end{aligned} \quad (3.83)$$

Due to force-commutation nature of the VIENNA rectifier the currents through high-frequency diodes $D_{\text{HFk}+}$ and $D_{\text{HFk}-}$ are:

$$i_{k+} = \begin{cases} (1 - K_k) i_{kr}, & i_{kr} \geq 0 \\ 0, & i_{kr} < 0 \end{cases} \quad (3.84)$$

$$i_{k-} = \begin{cases} 0, & i_{kr} \geq 0 \\ -(1 - K_k) i_{kr}, & i_{kr} < 0 \end{cases} \quad (3.85)$$

Subtracting (3.85) from (3.84) gives:

$$i_{k-} - i_{k+} = \begin{cases} 0 - (1 - K_k) i_{kr}, & i_{kr} \geq 0 \\ -(1 - K_k) i_{kr} - 0, & i_{kr} < 0 \end{cases} = -(1 - K_k) i_{kr}, \quad (3.86)$$

while summing (3.85) and (3.84) gives:

$$i_{k-} + i_{k+} = \begin{cases} 0 + (1 - K_k) i_{kr}, & i_{kr} \geq 0 \\ -(1 - K_k) i_{kr} + 0, & i_{kr} < 0 \end{cases} = (1 - K_k) \text{sgn}(i_{kr}) i_{kr}. \quad (3.87)$$

Combining (3.78) and (3.87):

$$i_{k-} + i_{k+} = d'_k i_{kr} = (d_k + d_0) i_{kr}. \quad (3.88)$$

Summing up (3.82):

$$2C_{\text{OUT}} \frac{d(v_{c2} + v_{c1})}{dt} = 2C_{\text{OUT}} \frac{dv_{\text{OUT}}}{dt} = i_{k-} + i_{k+} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}}, \quad (3.89)$$

and by plugging in (3.83), (3.88):

$$\begin{aligned} 2C_{\text{OUT}} \frac{dv_{\text{OUT}}}{dt} &= d_A i_{Ar} + d_B i_{Br} + d_C i_{Cr} \\ &\quad + (i_{Ar} + i_{Br} + i_{Cr}) d_0 - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}}. \end{aligned} \quad (3.90)$$

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Due to (3.79), (3.90) finally becomes:

$$2C_{\text{OUT}} \frac{dv_{\text{OUT}}}{dt} = d_A i_{\text{Ar}} + d_B i_{\text{Br}} + d_C i_{\text{Cr}} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}}, \quad (3.91)$$

or rewritten in matrix form:

$$2C_{\text{OUT}} \frac{dv_{\text{OUT}}}{dt} = \mathbf{d}^T \mathbf{i}_r - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}}. \quad (3.92)$$

Applying similar method to AC terminal equation given by (3.81), as before for the three-phase buck-type rectifier, the AC side VIENNA rectifier dq model can be obtained:

$$L_r \frac{d(\mathbf{T}^T \mathbf{i}_{r,dq})}{dt} = \mathbf{T}^T \mathbf{v}_{g,dq} - R_L \mathbf{T}^T \mathbf{i}_{r,dq} - \mathbf{T}^T \mathbf{d}_{dq} \frac{v_{\text{OUT}}}{2}. \quad (3.93)$$

Expanding the derivative term and multiplying by $2/3\mathbf{T}$ from the left side:

$$\begin{aligned} L_r \frac{2}{3} \mathbf{T} \frac{d\mathbf{T}^T}{dt} \mathbf{i}_{r,dq} + L_r \frac{2}{3} \mathbf{T} \mathbf{T}^T \frac{d\mathbf{i}_{r,dq}}{dt} &= \\ &= \frac{2}{3} \mathbf{T} \mathbf{T}^T \mathbf{v}_{g,dq} - R_L \frac{2}{3} \mathbf{T} \mathbf{T}^T \mathbf{i}_{r,dq} - \frac{2}{3} \mathbf{T} \mathbf{T}^T \mathbf{d}_{dq} \frac{v_{\text{OUT}}}{2}. \end{aligned} \quad (3.94)$$

Utilizing previously calculated identities (3.32) and (3.56):

$$L_r \frac{d\mathbf{i}_{r,dq}}{dt} = \mathbf{v}_{g,dq} - R_L \mathbf{i}_{r,dq} + \begin{bmatrix} 0 & \omega L_r \\ -\omega L_r & 0 \end{bmatrix} \mathbf{i}_{r,dq} - \mathbf{d}_{dq} \frac{v_{\text{OUT}}}{2}, \quad (3.95)$$

or rewritten as a set of two equations:

$$L_r \frac{di_{rd}}{dt} = v_{gd} - R_L i_{rd} + \omega L_r i_{rq} - d_d \frac{v_{\text{OUT}}}{2} \quad (3.96)$$

$$L_r \frac{di_{rq}}{dt} = v_{gq} - R_L i_{rq} - \omega L_r i_{rd} - d_q \frac{v_{\text{OUT}}}{2}. \quad (3.97)$$

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Applying dq transformation on the DC side equation given by (3.92):

$$\begin{aligned}
 2C_{\text{OUT}} \frac{dv_{\text{OUT}}}{dt} &= (\mathbf{T}^T \mathbf{d}_{dq})^T \mathbf{T}^T \mathbf{i}_{r,dq} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}} \\
 &= \mathbf{d}_{dq}^T \mathbf{T} \mathbf{T}^T \mathbf{i}_{r,dq} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}} \\
 &= \frac{3}{2} \mathbf{d}_{dq}^T \mathbf{i}_{r,dq} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}} \\
 &= \frac{3}{2} d_d i_{rd} + \frac{3}{2} d_q i_{rq} - 2 \frac{v_{\text{OUT}}}{R_{\text{OUT}}}.
 \end{aligned} \tag{3.98}$$

On the other hand, by subtracting equations (3.82), the state-space equation considering DC link capacitors balancing is obtained as:

$$2C_{\text{OUT}} \frac{d(v_{C1} - v_{C2})}{dt} = 2C_{\text{OUT}} \frac{d\Delta v}{dt} = i_+ - i_-. \tag{3.99}$$

Combining (3.86) and (3.99):

$$\begin{aligned}
 2C_{\text{OUT}} \frac{d\Delta v}{dt} &= (1 - K_A) i_{Ar} + (1 - K_B) i_{Br} + (1 - K_C) i_{Cr} \\
 &= (1 - K_A) \text{sgn}(i_{Ar}) \text{sgn}(i_{Ar}) i_{Ar} \\
 &\quad + (1 - K_B) \text{sgn}(i_{Br}) \text{sgn}(i_{Br}) i_{Br} \\
 &\quad + (1 - K_C) \text{sgn}(i_{Cr}) \text{sgn}(i_{Cr}) i_{Cr}.
 \end{aligned} \tag{3.100}$$

Taking into account duty cycle definition from (3.78) and the relationship of sign function to the absolute value function, the following is obtained:

$$2C_{\text{OUT}} \frac{d\Delta v}{dt} = d_A |i_{Ar}| + d_B |i_{Br}| + d_C |i_{Cr}| + d_0 (|i_{Ar}| + |i_{Br}| + |i_{Cr}|). \tag{3.101}$$

In order to maintain output capacitors voltage balance, the net current injected into the M point should be equal to zero during switching period. From that condition, the optimal zero-sequence component $d_{0,\text{opt}}$ is obtained as:

$$d_{0,\text{opt}} = - \frac{d_A |i_{Ar}| + d_B |i_{Br}| + d_C |i_{Cr}|}{|i_{Ar}| + |i_{Br}| + |i_{Cr}|}. \tag{3.102}$$

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Assuming that total zero-sequence duty cycle d_0 is:

$$d_0 = d_{0,\text{opt}} + \Delta d_0, \quad (3.103)$$

where Δd_0 is small perturbation around ideally applied optimal zero-sequence duty cycle $d_{0,\text{opt}}$, then (3.101) can be rewritten as:

$$C_{\text{OUT}} \frac{d\Delta v}{dt} = \Delta d_0 \frac{|i_{\text{Ar}}| + |i_{\text{Br}}| + |i_{\text{Cr}}|}{2}. \quad (3.104)$$

The part $(|i_{\text{Ar}}| + |i_{\text{Br}}| + |i_{\text{Cr}}|)/2$ is equal to maximum instantaneous input current. Since it has a very strong DC component compared to higher order harmonics, it can be approximated by:

$$\frac{6}{T} \int_{-T/12}^{T/12} I_{\text{M}} \cos(\omega t) dt = \frac{3}{\pi} I_{\text{M}}, \quad (3.105)$$

where I_{M} equals to peak line current. Therefore, (3.104) is simplified as:

$$C_{\text{OUT}} \frac{d\Delta v}{dt} \approx \frac{3}{\pi} I_{\text{M}} \Delta d_0 = \frac{3}{\pi} i_{\text{rd}} \Delta d_0, \quad (3.106)$$

for unity PF case. Using (3.96), (3.97), (3.98) and (3.106), the dq model of a three-phase VIENNA rectifier considering DC link voltage capacitors balancing can be obtained and it is shown in Fig. 3.35. In order to obtain desired transfer functions of the system, a steady-state DC operating point must be determined beforehand. Solving the equivalent circuit given in Fig. 3.35, the following is obtained for the duty cycles in d and q axes:

$$D_{\text{D}} = \frac{4}{3} \frac{P_{\text{OUT}}}{I_{\text{RD}} V_{\text{OUT}}}, \quad D_{\text{Q}} = -\frac{2\omega L_{\text{r}} I_{\text{RD}}}{V_{\text{OUT}}}, \quad (3.107)$$

while the zero-sequence small perturbation ΔD_0 is equal to zero. The steady-state current in d -axis is:

$$I_{\text{RD}} = \frac{V_{\text{GD}}}{2R_{\text{L}}} \left(1 - \sqrt{1 - \frac{8}{3} \frac{R_{\text{L}} P_{\text{OUT}}}{V_{\text{GD}}^2}} \right), \quad (3.108)$$

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Figure 3.35: The three-phase VIENNA rectifier dq model considering DC link voltage balancing.

Figure 3.36: Small-signal dq model of a three-phase VIENNA rectifier considering DC link voltage balancing.

while $I_{RQ} = 0$ since the rectifier is controlled to emulate pure resistance at the input port. The linearized dq model is shown in Fig. 3.36, where $\hat{x}$ denotes averaged, small-signal value of a variable x . A set of equations that describes the linearized circuit is as follows:

$$L_r \frac{d\hat{i}_{rd}}{dt} = \hat{v}_{gd} - R_L \hat{i}_{rd} + \omega L_r \hat{i}_{rq} - \frac{1}{2} D_D \hat{v}_{out} - \frac{1}{2} V_{OUT} \hat{d}_d \quad (3.109)$$

$$L_r \frac{d\hat{i}_{rq}}{dt} = \hat{v}_{gq} - R_L \hat{i}_{rq} - \omega L_r \hat{i}_{rd} - \frac{1}{2} D_Q \hat{v}_{out} - \frac{1}{2} V_{OUT} \hat{d}_q \quad (3.110)$$

$$C_{OUT} \frac{d\hat{v}_{out}}{dt} = \frac{3}{4} D_D \hat{i}_{rd} + \frac{3}{4} D_Q \hat{i}_{rq} + \frac{3}{4} I_D \hat{d}_d + \frac{3}{4} I_Q \hat{d}_q - \frac{1}{R_{OUT}} \hat{v}_{out} \quad (3.111)$$

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$$C_{\text{OUT}} \frac{d\Delta\hat{v}}{dt} = \frac{3}{\pi} I_{\text{RD}} \Delta\hat{d}_0 + \frac{3}{\pi} \Delta D_0 \hat{i}_{\text{rd}}. \quad (3.112)$$

Applying Laplace transform on (3.109)-(3.111) and by plugging in (3.111) into (3.109) and (3.110) the following is obtained:

$$\begin{aligned} \left(sL_r + R_L + \frac{3}{8} D_D^2 Z_O(s) \right) \hat{i}_{\text{rd}} + \left(-\omega L_r + \frac{3}{8} D_D D_Q Z_O(s) \right) \hat{i}_{\text{rq}} = \\ \hat{v}_{\text{gd}} - \left(\frac{3}{8} D_D I_{\text{RD}} Z_O(s) + \frac{V_{\text{OUT}}}{2} \right) \hat{d}_d - \frac{3}{8} D_D I_{\text{RQ}} Z_O(s) \hat{d}_q \end{aligned} \quad (3.113)$$

$$\begin{aligned} \left(\omega L_r + \frac{3}{8} D_D D_Q Z_O(s) \right) \hat{i}_{\text{rd}} + \left(sL_r + R_L + \frac{3}{8} D_Q^2 Z_O(s) \right) \hat{i}_{\text{rq}} = \\ \hat{v}_{\text{gq}} - \frac{3}{8} D_Q I_{\text{RD}} Z_O(s) \hat{d}_d - \left(\frac{3}{8} D_Q I_{\text{RQ}} Z_O(s) + \frac{V_{\text{OUT}}}{2} \right) \hat{d}_q, \end{aligned} \quad (3.114)$$

where:

$$Z_O(s) = \frac{R_{\text{OUT}}}{sR_{\text{OUT}}C_{\text{OUT}} + 1}. \quad (3.115)$$

Similarly, by applying Laplace transform on (3.112), the output DC link balancing circuit in s -domain becomes:

$$sC_{\text{OUT}} \Delta\hat{v} = \frac{3}{\pi} I_{\text{RD}} \Delta\hat{d}_0 + \frac{3}{\pi} \Delta D_0 \hat{i}_{\text{rd}}. \quad (3.116)$$

From (3.113) and (3.114) many different transfer functions can be obtained, while (3.116) provides a simple transfer function that is used for controlling DC link voltage unbalance. For the sake of simplicity, (3.113) and (3.114) can be rewritten as:

$$a_{11}(s) \hat{i}_{\text{rd}} + a_{12}(s) \hat{i}_{\text{rq}} = \hat{v}_{\text{gd}} + b_{11}(s) \hat{d}_d + b_{12}(s) \hat{d}_q \quad (3.117)$$

$$a_{21}(s) \hat{i}_{\text{rd}} + a_{22}(s) \hat{i}_{\text{rq}} = \hat{v}_{\text{gq}} + b_{21}(s) \hat{d}_d + b_{22}(s) \hat{d}_q, \quad (3.118)$$

where coefficients a_{ij} , b_{ij} , $i, j \in \{1, 2\}$, can be obtained by comparison of (3.113) and (3.114) with (3.117) and (3.118). The system itself has four independent inputs $\hat{v}_{\text{gd}}$, $\hat{v}_{\text{gq}}$, $\hat{d}_d$ and $\hat{d}_q$. In order to obtain open-loop input admittances, $Y_{\text{dd}}(s)$, $Y_{\text{qd}}(s)$, $Y_{\text{dq}}(s)$ and $Y_{\text{qq}}(s)$, independent inputs $\hat{d}_d$ and $\hat{d}_q$ must be nullified. The admittances originating from $\hat{v}_{\text{gd}}$ that are $Y_{\text{dd}}(s)$ and $Y_{\text{qd}}(s)$ are obtained from (3.117) and (3.118)

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by nullifying $\hat{v}_{gq}$ as well:

$$Y_{dd}(s) = \frac{\hat{i}_{rd}}{\hat{v}_{gd}} = \frac{a_{22}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)} \quad (3.119)$$

$$Y_{qd}(s) = \frac{\hat{i}_{rq}}{\hat{v}_{gd}} = \frac{-a_{21}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)}. \quad (3.120)$$

Similarly, the admittances originating from $\hat{v}_{gq}$ that are $Y_{dq}(s)$ and $Y_{qq}(s)$ are obtained from (3.117) and (3.118) by nullifying $\hat{v}_{gd}$ instead of $\hat{v}_{gq}$ as:

$$Y_{dq}(s) = \frac{\hat{i}_{rd}}{\hat{v}_{gq}} = \frac{-a_{12}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)} \quad (3.121)$$

$$Y_{qq}(s) = \frac{\hat{i}_{rq}}{\hat{v}_{gq}} = \frac{a_{11}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)}. \quad (3.122)$$

In order to obtain open-loop duty cycle to inductor current transfer functions $G_{dd}(s)$, $G_{qd}(s)$, $G_{dq}(s)$ and $G_{qq}(s)$, in a dual manner, independent inputs $\hat{v}_{gd}$ and $\hat{v}_{gq}$ must be nullified. The open-loop transfer functions originating from d -axis duty cycle to inductor currents $\hat{i}_{rd}$ and $\hat{i}_{rq}$, $G_{dd}(s)$ and $G_{qd}(s)$ are obtained from (3.117) and (3.118) by nullifying q -axis duty cycle as well:

$$G_{dd}(s) = \frac{\hat{i}_{rd}}{\hat{d}_d} = \frac{b_{11}(s)a_{22}(s) - b_{21}(s)a_{12}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)} \quad (3.123)$$

$$G_{qd}(s) = \frac{\hat{i}_{rq}}{\hat{d}_d} = \frac{b_{21}(s)a_{11}(s) - b_{11}(s)a_{21}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)}. \quad (3.124)$$

Analogously, the open-loop transfer functions originating from $\hat{d}_q$ that are $G_{dq}(s)$ and $G_{qq}(s)$ are obtained from (3.117) and (3.118) by nullifying $\hat{d}_d$ instead of $\hat{d}_q$ as:

$$G_{dq}(s) = \frac{\hat{i}_{rd}}{\hat{d}_q} = \frac{b_{12}(s)a_{22}(s) - b_{22}(s)a_{12}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)} \quad (3.125)$$

$$G_{qq}(s) = \frac{\hat{i}_{rq}}{\hat{d}_q} = \frac{b_{22}(s)a_{11}(s) - b_{12}(s)a_{21}(s)}{a_{11}(s)a_{22}(s) - a_{12}(s)a_{21}(s)}. \quad (3.126)$$

In order to shape input admittance of the converter, a closed-loop control is imposed on the input inductor L_r currents in d and q axes by means of PI controller through

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Figure 3.37: Block diagram of closed current loop three-phase VIENNA rectifier.

$G_{dd}(s)$ and $G_{qq}(s)$ transfer functions. The block diagram of the closed-loop system with previously derived transfer functions and two identical PI regulators $K(s)$, is shown in Fig. 3.37. Applying Mason's gain rule, closed-loop input admittances $Y_{dd,cl}(s)$, $Y_{qd,cl}(s)$, $Y_{dq,cl}(s)$ and $Y_{qq,cl}(s)$ can be obtained as:

$$Y_{dd,cl}(s) = \frac{Y_{dd}(s)(1 + K(s)G_{qq}(s)) - Y_{qd}(s)K(s)G_{dq}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)} \quad (3.127)$$

$$Y_{qd,cl}(s) = \frac{Y_{qd}(s)(1 + K(s)G_{dd}(s)) - Y_{dd}(s)K(s)G_{qd}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)} \quad (3.128)$$

$$Y_{dq,cl}(s) = \frac{Y_{dq}(s)(1 + K(s)G_{qq}(s)) - Y_{qq}(s)K(s)G_{dq}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)} \quad (3.129)$$

$$Y_{qq,cl}(s) = \frac{Y_{qq}(s)(1 + K(s)G_{dd}(s)) - Y_{dq}(s)K(s)G_{qd}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)}. \quad (3.130)$$

The example of this design methodology is conducted on a 10 kW three-phase VIENNA rectifier. Assuming that the rectifier is around 98 % efficient and by concentrating all losses in inductor series resistance R_L , its value is selected to be 300 m Ω . Now, steady-state input current I_{RD} can be calculated by (3.108) which

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gives 20.9 A. With input line-to-neutral RMS voltage $V_{\text{Ag,RMS}}$ of 230 V and output voltage of 800 V, the steady-state duty cycle in d -axis can be calculated by (3.107) and is $D_D = 0.7997$. Before calculating value of D_Q , input three-phase inductor L_r value must be provided. In [47], assuming that the peak current ripple is present at $\omega t = \pm 30^\circ$, a formula is given which calculates minimum value of three-phase inductance L_r as a function of peak-to-peak current ripple Δi_{Ar} :

$$L_{r,\min} = \frac{V_{\text{OUT}}}{\Delta i_{\text{Ar}} f_s} \left(1 - D_D \frac{\sqrt{3}}{2} \right) \left(D_D \frac{\sqrt{3}}{2} - \frac{1}{3} \right). \quad (3.131)$$

Assuming Δi_{Ar} equal to 20 % of I_{RD} and switching frequency f_s of 100 kHz, the formula estimates minimum value of L_r to be 220 μH . The value chosen in this work is 220 μH . Compared to the value of the output inductors L_{OUT} in the three-phase buck-type rectifier case, given in Fig. 3.10, the total size of the inductors is expected to be approximately the same since they store same peak total energy. Namely, peak stored energy $E_{Lr,\max}$ is:

$$E_{Lr,\max} = \frac{1}{2} I_{\text{DR}}^2 L_r = 48 \text{ mJ}, \quad (3.132)$$

while for the three-phase buck-type rectifier designed in the Section 3.3.1:

$$E_{L_{\text{out}},\max} = \frac{1}{2} I_L^2 L_{\text{OUT}} = 62.5 \text{ mJ}, \quad (3.133)$$

from which it is observable that $3E_{Lr,\max} \approx 2E_{L_{\text{out}},\max}$. With selected value of L_r and assumed line frequency of 400 Hz, steady-state duty cycle in q -axis can be calculated by (3.107) which gives a value of -0.0305. Lastly, value of the output capacitors $2C_{\text{OUT}}$ is calculated using (3.49) with the same criteria as in the case of three-phase buck-type rectifier. Plugging in the values of output voltage and discharge current of 800 V and 12.5 A respectively, with the same hold-up time, the minimum value of output capacitance $C_{\text{OUT},\min}$ is 97.6 μF . The value selected in this work is 108 μF , which again is representing similar total output capacitor volume compared to the three-phase buck-type design.

With all operating point values calculated, open-loop duty cycle to inductor current transfer functions $G_{\text{dd}}(s)$, $G_{\text{qd}}(s)$, $G_{\text{dq}}(s)$ and $G_{\text{qq}}(s)$, assuming transport

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Figure 3.38: Plot of the three-phase VIENNA rectifier open-loop transfer functions: (a) $G_{dd}(s)$, $G_{qd}(s)$, $G_{dq}(s)$ and $G_{qq}(s)$, (b) $Y_{dd}(s)$, $Y_{qd}(s)$, $Y_{dq}(s)$ and $Y_{qq}(s)$.

delay of $T_d = 0.75/f_s$, are given in Fig. 3.38a while open-loop input admittances $Y_{dd}(s)$, $Y_{qd}(s)$, $Y_{dq}(s)$ and $Y_{qq}(s)$ are given in Fig. 3.38b.

As it can be observed from Figs. 3.38a and 3.38b there exists significant coupling between direct to quadrature axes and vice versa. The coupling can be considerably reduced by means of closed-loop current control applying two identical regulators on $G_{dd}(s)$ and $G_{qq}(s)$ transfer functions as previously shown in Fig. 3.37. The closed-loop coupling transfer functions $G_{qd,cl}(s)$ and $G_{dq,cl}(s)$ can be obtained from Fig. 3.37 by Mason's gain rule as:

$$G_{qd,cl}(s) = \frac{G_{qd}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)} \quad (3.134)$$

$$G_{dq,cl}(s) = \frac{G_{dq}(s)}{(1 + K(s)G_{dd}(s))(1 + K(s)G_{qq}(s)) - K(s)G_{dq}(s)K(s)G_{qd}(s)}. \quad (3.135)$$

As it can be observed, the coupling terms are attenuated by double zero at the origin coming from the integral parts of the regulators, while outside of the controller bandwidth they roll-off with -40 dB/dec. Therefore, as long as the cross-over frequency of the loop-gains is higher than twice the grid frequency, the loop-gain of the control loops in d and q axes can be approximated by $L_{dd} \approx K(s)G_{dd}(s)$ and $L_{qq} \approx K(s)G_{qq}(s)$. As a starting point, loop-gain crossover frequency for both channels is set to 4.4 kHz which is done by having proportional and integral parts of $K(s)$ at -0.01507 A^{-1} and -74.12 C^{-1} respectively. Bode plot

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Figure 3.39: Plot of the three-phase VIENNA rectifier transfer functions: (a) inverted loop-gains $L_{dd}(s)$ and $L_{qq}(s)$ with 4.4 kHz cross-over frequency, (b) open-loop cross-coupling transfer functions $G_{qd}(s)$ and $G_{dq}(s)$ against closed-loop transfer functions $G_{qd,cl}(s)$ and $G_{dq,cl}(s)$.

of inverted loop-gains $L_{dd}(s)$ and $L_{qq}(s)$ is given in Fig. 3.39a, while a comparison of open-loop cross-coupling transfer functions $G_{qd}(s)$ and $G_{dq}(s)$ against closed-loop transfer functions $G_{qd,cl}(s)$ and $G_{dq,cl}(s)$ is given in Fig. 3.39b. Bode plots of closed-loop input admittances $Y_{dd,cl}(s)$, $Y_{qd,cl}(s)$, $Y_{dq,cl}(s)$ and $Y_{qq,cl}(s)$ for two different controller bandwidths at 4.4 kHz and 7 kHz are given in Fig. 3.40a and 3.40b respectively. It can be seen that the coupling admittances $Y_{qd,cl}(s)$ and $Y_{dq,cl}(s)$, on the case of 4.4 kHz controller, are at least 20 dB lower than direct admittances $Y_{dd,cl}(s)$ and $Y_{qq,cl}(s)$. When the bandwidth is increased to 7 kHz, the direct admittances are almost 25 dB higher than coupled ones in the worst case scenario. Therefore, it can be concluded that coupling admittances are more than 10 times lower and do not significantly contribute to the total input admittance.

Ideally by neglecting transport delay in the system, the cross-coupling transfer functions can be completely eliminated by applying cross-coupling cancelation technique widely used in the three-phase boost-type rectifiers/inverters. If for example the standard dq frame duty cycles d_d and d_q are represented in the following manner:

$$d_d = d_d^* + \frac{2\omega L_r}{v_{OUT}} i_{rq} \quad (3.136)$$

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Figure 3.40: Plot of the three-phase VIENNA rectifier closed-loop input admittances $Y_{dd,cl}(s)$, $Y_{qd,cl}(s)$, $Y_{dq,cl}(s)$ and $Y_{qq,cl}(s)$ for controller bandwidths of: (a) 4.4 kHz, (b) 7 kHz.

$$d_q = d_q^* - \frac{2\omega L_r}{v_{OUT}} i_{rd}, \quad (3.137)$$

where d_d^* and d_q^* are new decoupled duty cycle inputs to the system, then by plugging in (3.136) and (3.137) into (3.96), (3.97) and (3.98), a completely decoupled system of equations that describes VIENNA rectifier is obtained as:

$$L_r \frac{di_{rd}}{dt} = v_{gd} - R_L i_{rd} - d_d^* \frac{v_{OUT}}{2} \quad (3.138)$$

$$L_r \frac{di_{rq}}{dt} = v_{gq} - R_L i_{rq} - d_q^* \frac{v_{OUT}}{2} \quad (3.139)$$

$$C_{OUT} \frac{dv_{OUT}}{dt} = \frac{3}{4} d_d^* i_{rd} + \frac{3}{4} d_q^* i_{rq} - \frac{v_{OUT}}{R_{OUT}}, \quad (3.140)$$

while output capacitor voltage balance equation remains unaffected. The decoupled circuit diagram of the VIENNA rectifier is shown in Fig. 3.41. For the purpose of obtaining small-signal transfer functions, the new decoupled steady-state operating point duty cycle in d -axis D_D^* is the same as the one in original circuit given by (3.107), while now D_Q^* is equal to zero. Similar as before, linearization can be applied and later Laplace transform in order to obtain the set of equations from which all desired open-loop transfer functions can be obtained. Namely, by plugging in $\omega L_r = D_Q = I_{RQ} = 0$ into (3.113) and (3.114), the system of equations that

Figure 3.41: The three-phase VIENNA rectifier decoupled dq model considering DC link voltage balancing.

describes decoupled small-signal dynamics of the VIENNA rectifier is obtained as:

$$\left(sL_r + R_L + \frac{3}{8}D_D^{*2}Z_O(s)\right)\hat{i}_{rd} = \hat{v}_{gd} - \left(\frac{3}{8}D_D^*I_{RD}Z_O(s) + \frac{V_{OUT}}{2}\right)\hat{d}_d^* \quad (3.141)$$

$$(sL_r + R_L)\hat{i}_{rq} = \hat{v}_{gq} - \frac{V_{OUT}}{2}\hat{d}_q^*. \quad (3.142)$$

It can be immediately observed that there is no coupling between duty cycles in d and q -axes with currents in q and d -axes since (3.141) does not contain any variable related to q -axis, while (3.142) does not depend on $\hat{d}_d^*$ nor $\hat{i}_{rd}$. Therefore, the decoupled open-loop transfer functions $G_{dd}^*(s)$ and $G_{qq}^*(s)$, obtained from (3.141) and (3.142) are:

$$G_{dd}(s) = \frac{\hat{i}_{rd}}{\hat{d}_d^*} = -\frac{\frac{3}{8}D_D^*I_{RD}Z_O(s) + \frac{V_{OUT}}{2}}{sL_r + R_L + \frac{3}{8}D_D^{*2}Z_O(s)} \quad (3.143)$$

$$G_{qq}(s) = \frac{\hat{i}_{rq}}{\hat{d}_q^*} = -\frac{1}{2} \frac{V_{OUT}}{sL_r + R_L}, \quad (3.144)$$

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Figure 3.42: Block diagram of decoupled closed current loop three-phase VIENNA rectifier.

while $G_{qd}^*(s)$ and $G_{dq}^*(s)$ are equal to zero. Similarly, decoupled open-loop input admittances $Y_{dd}^*(s)$ and $Y_{qq}^*(s)$ are:

$$Y_{dd}^*(s) = \frac{\hat{i}_{rd}}{\hat{v}_d} = \frac{1}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} \frac{sR_{OUT}C_{OUT} + 1}{s^2 \frac{L_r C_{OUT} R_{OUT}}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} + s \frac{L_r + R_L R_{OUT} C_{OUT}}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} + 1} \quad (3.145)$$

$$Y_{qq}^*(s) = \frac{\hat{i}_{rq}}{\hat{v}_q^*} = \frac{1}{sL_r + R_L}, \quad (3.146)$$

while $Y_{qd}^*(s)$ and $Y_{dq}^*(s)$ are equal to zero. The decupuled closed-loop system block diagram is given in Fig. 3.42. Applying Mason's gain rule, the closed-loop input admittances $Y_{dd,cl}^*(s)$ and $Y_{qq,cl}^*(s)$ are drastically simplified as:

$$Y_{dd,cl}^*(s) = \frac{Y_{dd}^*(s)}{1 + K(s)G_{dd}^*(s)} \quad (3.147)$$

$$Y_{qq,cl}^*(s) = \frac{Y_{qq}^*(s)}{1 + K(s)G_{qq}^*(s)} \quad (3.148)$$

A plot comparing the closed-loop input admittances $Y_{dd,cl}(s)$ and $Y_{qq,cl}(s)$ to closed-loop input admittances of decoupled system $Y_{dd,cl}^*(s)$ and $Y_{qq,cl}^*(s)$ with the same regulator employing cross-over frequency of 4.4 kHz is given in Fig. 3.43a. From the plot given in Fig. 3.43a an important conclusion can be drawn. Namely, the

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Figure 3.43: Plot of the three-phase VIENNA rectifier closed-loop input admittances for controller bandwidth of 4.4 kHz comparing: (a) coupled system direct admittances $Y_{dd,cl}(s)$ and $Y_{qq,cl}(s)$ to perfectly decoupled system admittances $Y_{dd,cl}^*(s)$ and $Y_{qq,cl}^*(s)$, (b) coupled system coupling admittances $Y_{qd,cl}(s)$ and $Y_{dq,cl}(s)$ to decoupled system admittances $Y_{qd,cl}^{**}(s)$ and $Y_{dq,cl}^{**}(s)$ with transport delay of $T_d = 0.75T_s$.

assumption from Section 3.2 that it is sufficient for the closed-loop input admittance in d -axis to be below the three-wire limit in order to guarantee compliance with the 10 % THD_v test, is now shown to be a valid one due to, indeed, very high level of similarity between $Y_{dd,cl}(s)$ and $Y_{qq,cl}(s)$. Even if cross-coupling cancellation is not applied, the closed-loop coupling admittances are attenuated severely, as shown in Fig. 3.40, and can, as again has been assumed in Section 3.2, be disregarded in the design which dramatically simplifies the procedure. Moreover, there is no practical deviation from closed-loop $Y_{dd,cl}(s)$ and $Y_{dd,cl}^*(s)$. Therefore, closed-loop input admittance of a system without cross-coupling cancellation $Y_{dd,cl}(s)$ can be successfully approximated by:

$$Y_{dd,cl}(s) \approx \frac{Y_{dd}(s)}{1 + K(s)G_{dd}(s)}, \quad (3.149)$$

and it is the determining factor regarding the rectifier compliance under 10 % THD_v test. Lastly, the inclusion of a delay effect of $0.75T_s$ into a decoupled system makes the coupling admittances non-zero. However, they are still severely attenuated compared to the closed-loop case as shown in Fig. 3.43b.

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Figure 3.44: Plot of the three-phase VIENNA rectifier closed-loop transfer functions including transport delay of $T_d = 0.75T_s$ with variable controller bandwidths comparing: (a) open-loop decoupled system input admittance $Y_{dd}^*(s)$ and closed-loop system admittances $Y_{dd,cl}(s)$ with controller bandwidths of 4.4 kHz, 7 kHz and 11 kHz against 3-wire 10 % THDv test admittance limits, (b) loop-gain of d -axis current controller for crossover frequencies of 3 kHz, 4.4 kHz, 7 kHz and 11 kHz.

Having established the 10 % THDv test design criteria by (3.149), the effect of the loop-gain cross-over frequency is analyzed next. In the Fig. 3.44a a comparison is made of various current controller bandwidths against the 3-wire limit derived in Section 3.2. What can be immediately observed is the difference in the input admittance shape compared to the three-phase buck-type rectifier case. The reason for this lies in the direct control of the input current in the boost-type rectifiers as opposed to the output current control in the buck-type case. Moreover, for the approximately same volume and weight of the total magnetic components, boost-type rectifiers require higher controller bandwidth in contrast to the buck-derived ones.

Finally, inclusion of single-stage differential EMI filter is analyzed assuming loop-gain cross-over frequency of 7 kHz. Moreover, a coupled system from Fig. 3.35 is used from this point onward, since it is shown that there are no significant deviations in the closed-loop transfer functions with respect to the perfectly decoupled system. Starting with a input capacitor C_e it can be concluded that, due to the same power level of 10 kW, the actual maximum input capacitance that will provoke the failure of the 10 % THDv test has exactly the same value as for the buck-type case which makes its value power level dependent rather than topology dependent. However,

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Figure 3.45: The three-phase VIENNA rectifier dq model considering DC link voltage balancing and input C_e three-phase star-connected capacitors.

due to presence of the inductors on the AC side, the practical value of the input C_e capacitance is typically going to be several times smaller as opposed to buck-type scenario. Utilizing (3.58) and (3.59), the dq model of the three-phase VIENNA rectifier including input EMI capacitor is obtained as shown in Fig. 3.45. The actual value of C_e would depend on the desired attenuation of the EMI filter at the switching frequency, and it must be calculated along with the line impedance L_g . As a starting value C_e is selected to be 268 nF. With the capacitor C_e chosen, the closed-loop input admittance in d -axis is simply given by:

$$Y_{dd,cl,C_e}(s) = Y_{dd,cl}(s) + sC_e, \quad (3.150)$$

where $Y_{dd,cl}(s)$ is given by (3.149). A comparison of the closed-loop input admittance in d -axis $Y_{dd,cl}(s)$ without input capacitor C_e and $Y_{dd,cl,C_e}(s)$ for different values of C_e , assuming the base value of 268 nF, is shown in Fig. 3.46. As it can be observed from the Fig. 3.46, there is no significant impact of the input capacitance to the pass/fail criteria of the 10 % THD_v test. It is worth mentioning that the value chosen as a base capacitance C_e of 268 nF is 4.3 times lower than the minimum recommended value in the buck-type case. This capacitance is assumed for the rest of this Section.

Due to relatively low input capacitance C_e the effect of the line inductance L_g is not as severe as in the buck-type case since the characteristic impedance of the filter is approximately twice as large for the same L_g . That translates to lower peaking

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Figure 3.46: Bode plot of closed-loop input admittance $Y_{dd,cl}(s)$ without C_e and closed-loop input admittance $Y_{dd,cl,Ce}(s)$ for different C_e values.

Figure 3.47: The three-phase VIENNA rectifier with differential EMI stage.

Figure 3.48: dq model of a three-phase VIENNA rectifier with differential EMI stage.

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Table 3.6: 10 kW three-phase VIENNA rectifier parameters.

$V_{Ag,RMS}$ [V]	L_g [μ H]	C_e [nF]	C_d [nF]	R_d [Ω]
230	20-500	268	350	50
L_d [μ H]	L_r [μ H]	C_{OUT} [μ F]	V_{OUT} [V]	f_s [kHz]
680	220	108	800	100

in the closed-loop input admittance making its damping less critical. Assuming the passive damping structure from Fig. 3.19a and by adding a small inductor L_d in parallel with the damping resistor R_d , the complete VIENNA rectifier and its dq model with included input differential EMI stage is given in Figs. 3.47 and 3.48 respectively. Since the EMI capacitor C_e is rather small, higher value damping capacitor can be chosen while still having minor impact on the rectifier PF at 800 Hz. The value chosen here for C_d is 350 nF. In order to demonstrate low sensitivity to the EMI filter resonance damping, a wide range of inductances is covered from 20 μ H to 500 μ H. Moreover, damping resistor is chosen to be optimal for the highest L_g which is where it is the least critical since the characteristic impedance of the filter has the highest value. At the critical point with minimum L_g the chosen damping resistor value R_d of 50 Ω is nearly five times larger than the optimal value, again demonstrating low impact of the EMI filter design. Lastly, the extra shunt inductance L_d with its value at 680 μ H, is chosen to prioritize reduction of the low frequency dissipation over damping effectiveness. The impedance of L_d is more than fourteen times smaller than the R_d at 800 Hz line frequency, bringing down total power loss in the damping resistor from 25 W to 0.1 W. Moreover, at lowest L_g the impedance of shunt inductance L_d is approximately six time larger than damping resistor R_d which does not impact the damping effectiveness substantially. However, at maximum line inductance L_g , even though damping resistance is optimal for that case, the impedance of L_d is equal to R_d severely diminishing its performance.

With this rather poor design of the EMI filter damping branch, its impact on the 10 % THD_v test is analyzed next. The rectifier parameters are given in Table 3.6, while the current controller bandwidths chosen are non-compliant 4.4 kHz and 7 kHz which is on the limit of compliance. With a selected bandwidth of a controller, results are presented for variable line inductance. The closed-loop input admittance including EMI filter $Y_{cl,EMI}(s)$ for various line inductances is given in Fig. 3.49a. As it

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Figure 3.49: Plot of the three-phase VIENNA rectifier transfer functions including transport delay of $T_d = 0.75T_s$ with 4.4 kHz controller bandwidth (without EMI) for various line inductances L_g : (a) closed-loop input admittance $Y_{dd,cl,EMI}(s)$ against 3-wire 10 % THDv test admittance limits, (b) inverted loop-gain $L_{dd}(s)$ of d -axis current controller.

can be observed, even though damping scheme is far from optimal with L_g at 20 μH , the resonance peak, shown by red plot, is outside of frequency range of interest for the 10 % THDv test. As inductance L_g increases, so does the characteristic impedance of the EMI filter, thus the peaking in the input admittance decreases. Moreover, up to line inductance of 500 μH , the resonance is always located outside of 10 % THDv test range. Also, the damping resistor R_d is getting closer to the optimal value as inductance increases. Its effectiveness, however, is reduced due to the EMI filter resonant frequency decrease, since impedance of the shunt inductance L_d decreases and starts being comparable to R_d . It can be concluded that the design does not comply with 10 % THDv requirement due to reduced controller bandwidth. Moreover, it is demonstrated that EMI filter has minor influence up to line impedance of 500 μH where it starts being beneficial by attenuating fifth harmonic for higher grid frequencies, making only 360 and 400 Hz grid frequencies non-compliant with the 10 % THDv test.

The d -axis loop-gain of the current controller with bandwidth of 4 kHz when no EMI filter is present for various line inductances L_g is shown in Fig. 3.49b. What can be immediately concluded is that there are pairs of complex-conjugate poles and zeros that are both located in the left half-plane, since the phase after and before the EMI filter resonance is at the same value, if transport delay is ignored.

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Figure 3.50: Plot of the three-phase VIENNA rectifier transfer functions including transport delay of $T_d = 0.75T_s$ with 7 kHz controller bandwidth (without EMI) for various line inductances L_g : (a) closed-loop input admittance $Y_{dd,cl,EMI}(s)$ against 3-wire 10 % THD_v test admittance limits, (b) inverted loop-gain $L_{dd}(s)$ of d -axis current controller.

That is opposite of the buck rectifier case, where there were two right half-plane zeros, due to the fact that the input current is directly controlled in the boost-type converters. That yields current source behaviour for the boost-type converters at the input port, as opposed to constant power source for the buck-type rectifiers in the respected converters controller bandwidths. Fundamentally, with appropriate damping scheme, the boost-type rectifier current loop bandwidth is theoretically only limited by the total transport delay in the system. Also, the actual current-loop bandwidth is decreased with respect to 4 kHz when there was no EMI filter, due to the interactions of the $L_g - C_e$ with $L_r - C_{OUT}$.

The closed-loop input admittance for the faster current controller with cross-over frequency of 7 kHz (without EMI filter) against DO-160G 10 % THD_v test limit is given in Fig. 3.50a. Similar conclusion that EMI filter has rather minor impact on the 10 % THD_v test holds for this scenario as well. In this case design in on the limit of compliance as it is shown in the latter simulation results. The loop-gain of the d -axis current controller for various line impedances is given in Fig. 3.50b.

In order to verify the proposed design methodology, a set of simulations is carried out in power electronics simulator GeckoCIRCUITS. The results are presented at 10 kW output power and according to parameters from Table 3.6. For each of the controller bandwidths of 4.4 kHz and 7 kHz, time domain voltage and current

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Figure 3.51: Simulation results with line impedance $L_g = 20 \mu\text{H}$ and controller bandwidth of 4.4 kHz (without EMI) of input three-phase voltages and currents for line frequency of 500 Hz under 10 % THDv test.

waveforms and input current spectrum are given for the cases of highest and lowest line impedance analyzed in Fig. 3.50a. Therefore, each combination of controller bandwidth and line impedance value, is equipped with three figures: one figure of time domain input voltages and currents under 10 % THDv test at 500 Hz line frequency, another figure comparing phase A current spectrum with fundamental frequencies of 360, 400, 500 Hz against DO-160G and lastly a figure comparing phase A current spectrum with fundamental frequencies of 600, 700 and 800 Hz against DO-160G. The results are present at non-compliant current controller bandwidth of 4.4 kHz and marginally compliant controller bandwidth of 7 kHz, previously illustrated in Fig. 3.44b with blue and green plots respectively.

As it is predicted by closed-loop input admittance $Y_{\text{dd,cl,EMI}}(s)$ on the case of L_g of 20 μH and controller bandwidth of 4.4 kHz, the 10 % THDv test is not complied regardless of the line frequency fundamental as shown in simulation results presented in Fig. 3.52, with time domain input voltage and current waveforms at 500 Hz grid frequency given in Fig. 3.51. Interestingly, the flatness of the input admittance $Y_{\text{dd,cl,EMI}}(s)$ around fifth harmonic for variable frequency range is reflected in the simulation results as it is remaining constant regardless of fundamental frequency. Moreover, the influence of EMI filter cannot be observed since the resonant frequency is well outside the range of interest of the 10 % THDv test.

In order to verify that line inductance L_g does not impact the results in a critical way, its value has been increased 25 times to 500 μH . The closed-loop input

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Figure 3.52: Simulation results with line impedance $L_g = 20 \mu\text{H}$ and controller bandwidth of 4.4 kHz (without EMI) of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

admittance $Y_{\text{dd,cl,EMI}}(s)$ for this case is given by magenta line in Fig. 3.49b, and it predicts that the fifth harmonic for 360 and 400 Hz fundamental is slightly above the limit. That is indeed verified by the simulation results given in Fig. 3.54. For the fundamental frequencies higher than 400 Hz, the large line impedance L_g of 500 μH helps attenuate the fifth harmonic even further as seen in Fig. 3.54b. Even though proportional and integral gains are exactly the same as for the 4.4 kHz bandwidth controller when EMI filter was not considered, the actual interaction of LC filters $L_g - C_e$ and $L_r - C_{\text{OUT}}$ moves their respective resonances which in turn reduces the bandwidth of the controller to only 1.55 kHz, as shown previously by magenta plot in Fig. 3.49b.

For the sake of ensuring that the design is compliant with the required admittance profile of the 10 % THD_v test, the bandwidth of the controller is increased to 7 kHz, when EMI filter is not considered. The closed-loop input admittance $Y_{\text{dd,cl,EMI}}(s)$ with line impedance L_g set to 20 μH , previously given by red plot in Fig. 3.50a, predicts that the design is narrowly compliant. That is indeed verified by simulation results given in Fig. 3.56. Again it is shown that low line impedance has very low impact on the design as it can be seen by red plot of the d -axis current controller loop-gain previously given in Fig. 3.50b. Also, flatness of the closed-loop input admittance $Y_{\text{dd,cl,EMI}}(s)$ around fifth harmonic is again manifested as its constant

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Figure 3.53: Simulation results with line impedance $L_g = 500 \mu\text{H}$ and controller bandwidth of 4.4 kHz (without EMI) of input three-phase voltages and currents for line frequency of 500 Hz under 10 % THDv test.

Figure 3.54: Simulation results with line impedance $L_g = 500 \mu\text{H}$ and controller bandwidth of 4.4 kHz (without EMI) of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

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Figure 3.55: Simulation results with line impedance $L_g = 20 \mu\text{H}$ and controller bandwidth of 7 kHz (without EMI) of input three-phase voltages and currents for line frequency of 500 Hz under 10 % THD_v test.

Figure 3.56: Simulation results with line impedance $L_g = 20 \mu\text{H}$ and controller bandwidth of 7 kHz (without EMI) of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

amplitude regardless of the line frequency. Lastly, the time domain waveforms of the input voltages and currents with 500 Hz line frequency are given in Fig. 3.55.

Finally, for the controller bandwidth of 7 kHz and line impedance L_g of 500 μH , a brief analysis of the results from Figs. 3.57 and 3.58 is provided. The closed-loop input admittance $Y_{\text{dd,cl,EMI}}(s)$ from Fig. 3.50a for this case is given by magenta plot. It predicts that the design is fully compliant with the lowest harmonic content of all analyzed cases due to high line inductance. The simulation results of input phase A current harmonic content justifies this claim as it is shown in Fig. 3.58. The actual

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Figure 3.57: Simulation results with line impedance $L_g = 500 \mu\text{H}$ and controller bandwidth of 7 kHz (without EMI) of input three-phase voltages and currents for line frequency of 500 Hz under 10 % THDv test.

Figure 3.58: Simulation results with line impedance $L_g = 500 \mu\text{H}$ and controller bandwidth of 7 kHz (without EMI) of phase A current I_A spectrum for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

bandwidth of the current controller is again dramatically reduced from 7 kHz to 2.2 kHz as it is previously shown by magenta plot in Fig. 3.50b.

In the following a 10 kW SiC VIENNA rectifier prototype is presented and a set of experimental results is given that verify the extensive analysis from this Section.

3.4.2 Experimental Results

In order to validate the presented analysis, a three-phase 10 kW VIENNA prototype shown in Fig. 3.59 is built with the power stage parameters given in Table 3.7. The

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Figure 3.59: Constructed 10 kW three-phase VIENNA prototype employing SiC devices.

Table 3.7: 10 kW VIENNA rectifier power stage devices and passives.

Device/Passive	Part number
$S_{A,B,C,\pm}$	C3M0065100K
$D_{HF,A,B,C,\pm}$	2x C5D50065D
$D_{LF,A,B,C,\pm}$	VS-60EPS08-M3
Gate driver	CRD-001
$2C_{OUT}$	10x B32678G6206K000
L_r	33 turn (5x 1 mm ²) 2x B66375G0000X187 air gap 3 mm
C_e	2x B32912A3104K000 B32912A3683K000
C_d	2x B32912A3104K000 B32912A3154K000
R_d	PWR220T-20-50R0F
L_d	7447480681
Current sensors	LAH 25-NP
Microcontroller	TI F28379D

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MOSFETs chosen are third generation SiC devices C3M0065100K from Wolfspeed. The gate driver used to drive the MOSFETs is CRD-001 again from Wolfspeed. The high frequency diodes D_{HF} are fifth generation SiC Schottky diodes C5D50065D also from Wolfspeed. Each D_{HF} diode consists of two C5D50065D diodes in parallel. The low-frequency diodes D_{LF} are VS-60EPS08-M3 manufactured by Vishay. Moving to reactive components, each of the $2C_{\text{OUT}}$ consists of ten parallel connected B32678G6206K000 MKP capacitors manufactured by EPCOS/TDK with total capacitance of 200 μF . The input inductors L_r are made using N87 ferrite E cores B66375G0000X187 with an air gap of the central leg of 3 mm. The winding consists of 33 turns, where each turn is made of five 1 mm² cross-section solid copper wires connected in parallel. The EMI capacitor C_e consists of a parallel connection of two 100 nF B32912A3104K000 MKP capacitors and one 68 nF B32912A3683K000 all manufactured by EPCOS/TDK. The damping branch capacitor C_d consists of parallel connection of two 100 nF B32912A3104K000 MKP capacitors and one 150 nF B32912A3154K000 capacitor. The damping resistor R_d is PWR220T-20-50R0F manufactured by Bourns. The shunt inductance L_d is 680 μH 7447480681 manufactured by Wurth Elektronik. The current sensors used are LEM LAH 25-NP with 200 kHz -1 dB bandwidth. Finally, the whole system is controlled by Texas Instruments F28379D dual-core microcontroller equipped with powerful hardware accelerators enabling low-latency calculations needed for minimization of current control loops transport delays T_d . The experimental measurement of the Bode transfer functions is done by the block diagram shown in Fig. 3.60. The analog current measurements i_{Ar} , i_{Br} and i_{Cr} obtained from the LEM sensors, after being adopted to the input ADC voltage level of 0-3 V, are sampled along with the perturbation signal $\hat{s}$ provided by Bode 100 network analyzer. Then, in the interrupt service routine (ISR) of the F28379D microcontroller, measurements acquisition, required dq transformation, control loops and PWM duty cycle updates are performed. The total ISR execution time from ADC start of the conversion until PWM register update is measured to be around 4 μs , which enables double updating of the duty cycles at the switching frequency of 100 kHz. That effectively halves the total computational delay from $1.5T_s$ to $0.75T_s$ to its theoretical minimum, assuming synchronous update of the duty cycles. In the ISR several digital signals are configured and sent via SPI interface to the external subsystem. The SPI data,

Figure 3.60: Block diagram of the experimental setup for transfer function measurements.

Figure 3.61: Block diagram of the experimental measurement of the d -axis current controller inverted loop-gain $L_{dd}(s)$.

clock and chip select signals are then isolated by means of fast digital isolators and fed to the four channel digital-to-analog converter with SPI input interface. These newly obtained analog signals can be seen on the oscilloscope for the purpose of debugging and verification or fed back to the Bode 100 network analyzer for transfer function measurements.

In order to measure open-loop transfer function $G_{dd}(s)$, the signals that have to be measured are the small-signal duty cycle in d -axis $\hat{d}_d$ and AC component of the rectifier current $\hat{i}_{rd}$. Therefore, the perturbation signal $\hat{s}$ from Bode 100 analyzer, after being scaled and added to the duty cycle in d -axis, is sent back via SPI interface along with the $\hat{i}_{rd}$. A frequency sweep is done from 10 Hz up to the Nyquist frequency of 100 kHz. The experimental measurement at full load of 10 kW compared to the analytical expression given by (3.123) is presented in the Fig. 3.62a. The measuring procedure of the current control loop loop-gain can be understood with the block

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Figure 3.62: Comparison of simulated against experimentally obtained transfer functions: (a) open-loop duty cycle in d -axis to inductor current $G_{dd}(s)$, (b) d -axis current controller inverted loop-gain $L_{dd}(s)$ with the controller bandwidth at 4.4 kHz (without EMI).

diagram given in Fig. 3.61. While the rectifier is running at nominal power and closed current loops in d and q axes, the perturbation $\hat{s}$ is injected into the d -axis loop for the purpose of measuring loop-gain $L_{dd}(s) = K(s)G_{dd}(s)$. The system from the block diagram has two independent inputs $\hat{i}_{rd,ref}$ and $\hat{s}$. By nullifying input $\hat{i}_{rd,ref}$ the following expression holds:

$$\hat{i}_{rd} = -K(s)G_{dd}(s)(\hat{s} + \hat{i}_{rd}) = -L_{dd}(s)(\hat{s} + \hat{i}_{rd}),$$

from which it follows:

$$-L_{dd}(s) = \frac{\hat{i}_{rd}}{\hat{s} + \hat{i}_{rd}}. \quad (3.151)$$

Therefore, inverted loop-gain $-L_{dd}(s)$ can be easily measured by sending via SPI interface AC perturbation of d -axis inductor current $\hat{i}_r$ along with the same value summed with the injected perturbation $\hat{s}$. The comparison of the simulated d -axis current controller loop-gain with cross-over frequency of 4.4 kHz (without EMI filter) previously given by blue plot in Fig. 3.44b and the experimental measurement is given in Fig. 3.62b. A clear delay effect of $0.75T_s$ is observable in the inverted loop-gain plot since the phase characteristics is equal to -180° at the Nyquist frequency of 100 kHz.

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Figure 3.63: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THD_v test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @360 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

The final part of the experimental results is obtained by Yokogawa WT1800 Precision Power Analyzer. The captures are given for all required frequencies for the 10 % THD_v test from DO-160G which are 360, 400, 500, 600, 650, 700 and 800 Hz with two plots, one that shows time waveforms of input three-phase voltages and currents and one that shows input power quality overview. Moreover, the results are presented with the controller bandwidth of 4.4 kHz and 7 kHz (without EMI) that represent the non-compliant and compliant design respectively. Finally, a spectrum of input currents are presented comparing phase A current harmonic content against the DO-160G limits for 4.4 kHz and 7 kHz controllers. It is shown that all experimental results follow the previously derived theory in a very close manner. Although zero-sequence harmonics are greatly present in the three-phase voltages due to three-wire connection and symmetry, they are practically negligible in the input current spectrum, justifying the relaxation of the limits from the Section 3.2.

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Figure 3.64: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @400 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.65: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @500 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.66: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @600 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.67: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @650 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.68: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @700 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.69: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) @800 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.70: Experimental results showing input phase A current spectrum against DO-160G limits under 10 % THDv test for slower controller, $f_{BW} = 4.4$ kHz (without EMI) for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

Figure 3.71: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @360 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.72: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @400 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.73: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @500 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.74: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @600 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.75: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @650 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

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Figure 3.76: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @700 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.77: Experimental results of 10 kW three-phase VIENNA rectifier steady-state operation under 10 % THDv test for faster controller, $f_{BW} = 7$ kHz (without EMI) @800 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 3.78: Experimental results showing input phase A current spectrum against DO-160G limits under 10 % THD_v test for faster controller, $f_{BW} = 7$ kHz (without EMI) for: (a) 360, 400, 500 Hz grid frequency, (b) 600, 700, 800 Hz grid frequency.

3.4.3 Summary and Discussion

The previously developed dq admittance limits from Section 3.2 are applied on the three-phase boost-type topology, specifically the VIENNA rectifier, and key points are addressed. First, a detailed development of the VIENNA rectifier switching model is provided. Then, by applying moving average operator, an average model is calculated in Stationary Reference Frame (abc domain). Afterwards, dq transformation of the average model is done and dq equivalent model is obtained considering DC link voltage capacitors balancing. Next, development of small-signal model is given. It allows definition of key transfer functions necessary for the proposed 10 % THD_v test compliance design methodology. Due to extensive coupling between d and q axes of boost-type topologies, the open and closed-loop transfer functions are rather complex. It is shown that, with sufficient current controller bandwidth, the coupling transfer functions can be disregarded and the approximate closed-loop input admittances in d and q axes are obtained. Also, decoupling strategy widely used in the literature is not necessary to be employed when controller bandwidths are sufficiently high, even when transport delay of $0.75T_s$ is taken into account. Moreover, due to high level of symmetry between closed-loop direct and quadrature admittances $Y_{dd,cl}(s)$ and $Y_{qq,cl}(s)$ it is shown that it is sufficient to satisfy that $Y_{dd,cl}(s)$ admittance is below three-wire limits from Section 3.2 in order to comply with the 10 % THD_v test. It is demonstrated

3.5. Conclusions

that, VIENNA rectifier requires rather fast current controllers in order for the design to be compliant with the 10 % THD_v test. Analyzing further, effect of the EMI filter is addressed. It is shown that boost-type rectifiers are rather insensitive to EMI filter design, since proposed design is fairly far from optimal. The impact of the filter on the rectifier is marginal due to presence of small filtering capacitors C_e . These small capacitors inherently yield high characteristic impedances of the EMI filter which translates into low peaking in the input admittance. The resonant frequency of the three-phase VIENNA rectifier differential EMI filter is very likely to be outside of the frequency range of interest for 10 % THD_v test. Since input current is directly controlled in boost-type rectifiers, the complex conjugate pairs of poles and zeroes in the loop-gain of the current controller are located in left-half-plane. Therefore, properly designed EMI filter is extremely unlikely to cause stability issues and higher bandwidths than the filter resonant frequency are achievable. The only theoretical limit present is related to total transport delay of the system T_d .

The obtained experimental results of the 10 kW SiC VIENNA rectifier follow the proposed analysis in a very close manner. The results are presented at all frequencies that are defined in the DO-160G and no significant deviations are observed. Moreover, a way of experimentally measuring transfer functions is presented and compared with the previously analytically calculated values. These results have also shown to align very well with the theoretical analysis.

3.5 Conclusions

The proposed design methodology in order to comply with DO-160G current distortion test is presented and analyzed in detail. It is based on translation of per-harmonic current limits into per-harmonic maximum input admittances that connected load is allowed to have over the whole variable frequency range in order to be compliant. Due to normalization, the obtained limits are valid for arbitrary power level by simple shifting with base admittance governed by equipment's nominal power as given by (3.4). The rather complicated DO-160G current distortion test requirement is drastically simplified by method proposed in this Chapter.

It is shown that buck-type rectifiers are rather insensitive to current controller bandwidth unlike the three-phase boost-type rectifiers, assuming the same size of

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magnetic components. On the other hand, the design of the input EMI filter used for differential filtering must be done carefully for the three-phase buck-type rectifier since it can cause both failure of compliance with THD_v test and/or stability issues. In the case of boost-type rectifiers, the differential EMI filter design is shown not to be problematic due to presence of smaller capacitances at the rectifier input, which translates into higher characteristic impedances of the filter compared to the buck-type case. Consequently, the resonant frequency of the EMI filter is located at higher frequencies for the same values of line inductance L_g previously used for three-phase buck-type rectifier and can be even located outside of frequency range of interest for the 10 % THD_v test.

In general, the design methodology presented in this Chapter can be performed on any standard that implies limitations on current harmonics relative to the corresponding voltage harmonics. Also, multistage EMI filters design can be successfully done employing this method. Moreover, the design methodology and the corresponding conclusions presented in this work are extendable to other buck-type topologies eg. SWISS rectifier, and to boost-type rectifiers eg. three-phase boost, NPC, Y rectifier etc., since their equivalent dq models are expected to be very similar to the basic three-phase buck-type and three-phase VIENNA rectifier models.

Analysis of Boost-type Rectifiers Under Input Phase Failure

4.1 Introduction

The main purpose of this Chapter is to provide a robust control strategy for a three-phase three-wire six-switch boost-type rectifier against arbitrary input phase failure scenario. The fundamental idea lies in control of positive and negative sequence components of the three-phase system after the failure occurrence. For that purpose two rotating reference frames are introduced that are tied to positive and negative sequence voltage vectors by means of Decoupled Double Synchronous Reference Frame Phase-Locked Loop (DDSRF-PLL). The mentioned PLL is an essential part of the control strategy since it provides accurate values of direct and quadrature components of positive and negative sequence that are used to control the rectifier under grid fault scenario. Therefore, the applied rectifier closed-loop current control consists of four identical PI controllers, two for each sequence d and q components. Since each grid fault case generates unique values of positive and negative sequence voltage vectors, a mathematical derivation of d and q components of each rotating sequence is calculated. The main contribution of this Chapter lies in precise mathematical extraction of necessary positive and negative sequence voltage and current components needed to cope with any grid fault scenario. The total number of analyzed failure cases is nine, where three are related to phase-to-phase short-circuit, three to open-phase case, and three to phase-to-neutral fault. Moreover, a mathematical link between instantaneous amplitudes of each individual phase and positive and negative sequence component values is also

Chapter 4. Analysis of Boost-type Rectifiers Under Input Phase Failure

provided. The derived link utilized on input three-phase voltages and currents provides a simple way of detecting the nine grid failure cases so that adequate current controller references can be provided which guarantee optimal power flow. Finally, the proposed analysis is backed up by simulation and experimental results, conducted on a full SiC 3.45 kW prototype.

This Chapter is organized as follows. First, a brief introduction into Double Synchronous Reference Frame (DSRF) is given, followed by DDSRF-PLL design. Then, by means of phasor theory, a mathematical link between positive and negative sequence d and q components and abc domain phase voltages/currents is derived. From it, instantaneous amplitudes of phase voltages/currents can be obtained as well as DDSRF current controller references. Afterwards, each of the nine failure cases is analyzed by means of phasor diagram and exact current references are obtained, as well as unique failure condition based on individual phase voltage and current amplitudes combination. Next, a 3.45 kW three-phase three-wire connected boost-type rectifier power stage is designed, along with four PI current controllers, one for each of the positive and negative sequence d and q components. Based on the previously derived mathematical expressions, a rectifier state machine is provided with total of nine failure states and one nominal state that reliably detects fault case and modifies the current references accordingly without the need of modifying PI controllers. Afterwards, a simulation for all nine case scenarios is done which includes transition from nominal to failure state and back. Finally, a set of experimental results is given based on a full SiC 3.45 kW prototype in order to verify the proposed simulations in practice.

4.2 The Decoupled Double Synchronous Reference Frame Phase-Locked Loop (DDSRF-PLL)

The fundamental part of the DDSRF control algorithm lies in the correct synchronization to the grid. The classical Synchronous Reference Frame PLL (SRF-PLL) structure [74] works very well under balanced case, however suffers from bandwidth limitations under mains unbalance. The extension to the SRF-PLL, which is the DDSRF-PLL, as presented in [75], is much more robust to the grid faults while at the same time offering information of the grid positive and negative

4.2. The Decoupled Double Synchronous Reference Frame Phase-Locked Loop (DDSRF-PLL)

Figure 4.1: General voltage vector $\mathbf{v}$ decomposed into positive and negative sequence vectors $\mathbf{v}^+$ and $\mathbf{v}^-$ in Double Synchronous Reference Frame (DSRF).

sequence voltage amplitudes. That information is useful for detection of potential grid failures and generation of proper control signals for safe compensation.

A general case of an unbalanced three-phase voltage represented by voltage space vector $\mathbf{v}$ decomposed by means of symmetrical components into positive sequence voltage vector $\mathbf{v}^+$ rotating in counter-clockwise direction and negative sequence voltage vector $\mathbf{v}^-$ rotating in clockwise direction in Double Synchronous Reference Frame (DSRF), is given in Fig. 4.1. After decomposition of vector $\mathbf{v}$ into $\mathbf{v}^+$ and $\mathbf{v}^-$ the two sequence vectors projections onto dq^+ and dq^- frames respectively have constant values, assuming that vector rotating speed ω is equal to SRF rotating speed ω' . However, in dq^+ reference frame vector $\mathbf{v}^-$ is seen as a component oscillating at frequency -2ω , since relative speed of dq^- with respect to dq^+ frame is equal to -2ω . Similarly, the reference frame dq^- sees voltage vector $\mathbf{v}^+$ as an

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oscillation at 2ω . Thus, PLL designed to operate under grid faults must be able to mitigate this coupling effect between $dq+$ and $dq-$ axes. Assuming that the $d+$ axis is perfectly aligned with positive sequence voltage vector $\mathbf{v}^+$, the dq components of $dq+$ frame can be expressed as:

$$\begin{aligned}
 \mathbf{v}_{dq}^+ &= \mathbf{T}_{dq+} \mathbf{v}_{\alpha\beta} \\
 &= \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \left(\begin{bmatrix} V_m^+ \cos \omega t \\ V_m^+ \sin \omega t \end{bmatrix} + \begin{bmatrix} V_m^- \cos(-\omega t + \theta_{0-}) \\ V_m^- \sin(-\omega t + \theta_{0-}) \end{bmatrix} \right) \\
 &= V_m^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + \begin{bmatrix} \cos 2\omega t & \sin 2\omega t \\ -\sin 2\omega t & \cos 2\omega t \end{bmatrix} \begin{bmatrix} V_m^- \cos \theta_{0-} \\ V_m^- \sin \theta_{0-} \end{bmatrix} \\
 &= V_m^+ \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_m^- \mathbf{T}_{dq+2} \begin{bmatrix} \cos \theta_{0-} \\ \sin \theta_{0-} \end{bmatrix},
 \end{aligned} \tag{4.1}$$

while for the $dq-$ frame:

$$\begin{aligned}
 \mathbf{v}_{dq}^- &= \mathbf{T}_{dq-} \mathbf{v}_{\alpha\beta} \\
 &= \begin{bmatrix} \cos \omega t & -\sin \omega t \\ \sin \omega t & \cos \omega t \end{bmatrix} \left(\begin{bmatrix} V_m^+ \cos \omega t \\ V_m^+ \sin \omega t \end{bmatrix} + \begin{bmatrix} V_m^- \cos(-\omega t + \theta_{0-}) \\ V_m^- \sin(-\omega t + \theta_{0-}) \end{bmatrix} \right) \\
 &= V_m^+ \begin{bmatrix} \cos 2\omega t \\ \sin 2\omega t \end{bmatrix} + V_m^- \begin{bmatrix} \cos \theta_{0-} \\ \sin \theta_{0-} \end{bmatrix} \\
 &= V_m^+ \mathbf{T}_{dq-2} \begin{bmatrix} 1 \\ 0 \end{bmatrix} + V_m^- \begin{bmatrix} \cos \theta_{0-} \\ \sin \theta_{0-} \end{bmatrix},
 \end{aligned} \tag{4.2}$$

where $\mathbf{T}_{dq+}$, $\mathbf{T}_{dq-}$, $\mathbf{T}_{dq+2}$, $\mathbf{T}_{dq-2}$ are dq transformation matrix, inverse dq transformation matrix, dq transformation matrix at double frequency, inverse dq transformation matrix at double frequency, while V_m^+ , V_m^- and θ_{0-} are amplitude of positive sequence voltage vector $\mathbf{v}^+$, amplitude of negative sequence voltage vector $\mathbf{v}^-$ and initial phase angle of negative sequence voltage vector respectively. Observing (4.1) and (4.2) it can be concluded that DC terms carry the desired information about respective sequence voltage vectors, while AC terms that oscillate at 2ω represent the undesired coupling between sequences. Moreover, the amplitudes of AC terms are equal to the amplitude of voltage vector of the opposite frame. In order to eliminate the coupling terms, the $\mathbf{v}_{dq}^+$ and $\mathbf{v}_{dq}^-$ can be passed through

4.2. The Decoupled Double Synchronous Reference Frame Phase-Locked Loop (DDSRF-PLL)

Figure 4.2: The DDSRF-PLL structure

low-pass filter with a cut-off frequency of ω_f which extracts the DC components of respective sequences, while attenuating the coupling terms. To these filtered values, inverse dq transformation at 2ω can be applied and the result subtracted from the opposing sequence dq transformation, which in turn attenuates even further the undesired oscillation at 2ω . In this manner, a perfect estimation of grid positive and negative sequence components is obtained, where the dynamic response depends on the filter cut-off frequency ω_f . In [75] an optimal compromise between response time and overshoot is found to be at $\omega_f = \omega_0/\sqrt{2}$, where ω_0 is grid frequency, which is the value used in this work assuming 400 Hz grid. Finally, PLL design can be approximated by a design of a basic SRF-PLL. The DDSRF-PLL employing the mentioned decoupling structure is shown in Fig. 4.2. The PI regulator values chosen are $k_p = -1.61 \text{ V}^{-1}$ and $k_i = -545 \text{ Wb}^{-1}$ which gives PLL bandwidth of 80 Hz. A simulation example of PLL performance under failure event of short-circuit between phases A and B is shown in Fig. 4.3. The actual values of v_d^+ , v_q^+ , v_d^- and v_q^- for this particular failure are calculated in the following Section.

Figure 4.3: The DDSRF-PLL tracking of positive and negative sequence dq components before and after sudden short circuit between phases A and B.

4.3 Control Logic Derivation Under Grid Faults

In this Section by means of phasor theory mathematical expressions are derived that link waveforms from a specific grid fault scenario in abc domain to dq components of positive and negative sequence. Based on these calculations, an expression that extracts per-phase instantaneous peak fundamental values is also provided. The calculations are then applied to nine single failure cases: phases AB, BC or CA short-circuit, phase A, B or C open-circuit and phase A, B or C short-circuit to neutral wire. As a result, a set of four current references is obtained in order effectively cope with the failure case. Moreover, unique failure condition utilized for its detection is provided by means of specific per-phase voltage and current instantaneous amplitudes combinations.

4.3.1 General Relationship Between abc and $dq\pm$ Sequence Components

The inverse dq transformation of the positive sequence voltage vector $\mathbf{v}^+$ is given by:

$$\mathbf{v}_{\alpha\beta}^+ = \begin{bmatrix} \cos \omega t & -\sin \omega t \\ \sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} V_d^+ \\ V_q^+ \end{bmatrix} = \begin{bmatrix} V_d^+ \cos \omega t - V_q^+ \sin \omega t \\ V_d^+ \sin \omega t + V_q^+ \cos \omega t \end{bmatrix}, \quad (4.3)$$

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and can be rewritten in more compact complex form as:

$$\mathbf{v}_{\alpha\beta+} = \begin{bmatrix} V_d^+ + jV_q^+ \\ -jV_d^+ + V_q^+ \end{bmatrix}. \quad (4.4)$$

Similarly for negative sequence component:

$$\mathbf{v}_{\alpha\beta}^- = \begin{bmatrix} \cos \omega t & \sin \omega t \\ -\sin \omega t & \cos \omega t \end{bmatrix} \begin{bmatrix} V_d^- \\ V_q^- \end{bmatrix} = \begin{bmatrix} V_d^- \cos \omega t + V_q^- \sin \omega t \\ -V_d^- \sin \omega t + V_q^- \cos \omega t \end{bmatrix}, \quad (4.5)$$

or in complex form:

$$\mathbf{v}_{\alpha\beta}^- = \begin{bmatrix} V_d^- - jV_q^- \\ jV_d^- + V_q^- \end{bmatrix}. \quad (4.6)$$

The total voltage vector represented in $\alpha\beta$ domain is obtained by summing (4.4) and (4.6):

$$\mathbf{v}_{\alpha\beta} = \mathbf{v}_{\alpha\beta}^+ + \mathbf{v}_{\alpha\beta}^- = \begin{bmatrix} V_d^+ + V_d^- + j(V_q^+ - V_q^-) \\ V_q^+ + V_q^- - j(V_d^+ - V_d^-) \end{bmatrix}. \quad (4.7)$$

By applying $\alpha\beta$ to abc transformation the voltages in abc domain are obtained as:

$$\begin{aligned} \mathbf{v}_{abc} = \mathbf{T}_{\alpha\beta \rightarrow abc} \mathbf{v}_{\alpha\beta} &= \begin{bmatrix} 1 & 0 \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} V_d^+ + V_d^- + j(V_q^+ - V_q^-) \\ V_q^+ + V_q^- - j(V_d^+ - V_d^-) \end{bmatrix} \\ &= \begin{bmatrix} V_d^+ + V_d^- + j(V_q^+ - V_q^-) \\ -\frac{1}{2}(V_d^+ + V_d^-) + \frac{\sqrt{3}}{2}(V_q^+ + V_q^-) + j\left(-\frac{\sqrt{3}}{2}(V_d^+ - V_d^-) - \frac{1}{2}(V_q^+ - V_q^-)\right) \\ -\frac{1}{2}(V_d^+ + V_d^-) - \frac{\sqrt{3}}{2}(V_q^+ + V_q^-) + j\left(\frac{\sqrt{3}}{2}(V_d^+ - V_d^-) - \frac{1}{2}(V_q^+ - V_q^-)\right) \end{bmatrix}. \end{aligned} \quad (4.8)$$

Since case study at hand are three-wire systems, only two out of three three-phase voltages/currents can be independently defined by their amplitudes and initial phases. That is in accordance with four independent variables V_d^+ , V_q^+ , V_d^- and V_q^- from dq frames. Therefore, direct and quadrature values of phase A and B are

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enough to uniquely define a desired three-phase voltage/current waveform, with an additional constraint in the case of loss of one phase.

Based on (4.8), the following set of equations fully describes a three-wire three-phase system of voltages or currents:

$$V_{ad} = V_d^+ + V_d^- \quad (4.9)$$

$$V_{aq} = V_q^+ - V_q^- \quad (4.10)$$

$$V_{bd} = -\frac{1}{2}(V_d^+ + V_d^-) + \frac{\sqrt{3}}{2}(V_q^+ + V_q^-) \quad (4.11)$$

$$V_{bq} = -\frac{\sqrt{3}}{2}(V_d^+ - V_d^-) - \frac{1}{2}(V_q^+ - V_q^-), \quad (4.12)$$

where V_{ad} and V_{aq} are direct and quadrature parts of voltage v_A , while V_{bd} and V_{bq} are direct and quadrature parts of voltage v_B . Normally, a set of desired voltages/currents in abc domain is defined and on that basis dq components are calculated. Therefore, solving (4.9)-(4.12) for V_d^+ , V_d^- , V_q^+ and V_q^- the following is obtained:

$$V_d^+ = \frac{1}{2}V_{ad} - \frac{1}{2\sqrt{3}}V_{aq} - \frac{1}{\sqrt{3}}V_{bq} \quad (4.13)$$

$$V_q^+ = \frac{1}{2}V_{ad} + \frac{1}{2\sqrt{3}}V_{aq} + \frac{1}{\sqrt{3}}V_{bq} \quad (4.14)$$

$$V_d^- = \frac{1}{2\sqrt{3}}V_{ad} + \frac{1}{2}V_{aq} + \frac{1}{\sqrt{3}}V_{bd} \quad (4.15)$$

$$V_q^- = \frac{1}{2\sqrt{3}}V_{ad} - \frac{1}{2}V_{aq} + \frac{1}{\sqrt{3}}V_{bd}. \quad (4.16)$$

The (4.13)-(4.16) form a base from which all failure cases current references can be obtained, while instantaneous amplitudes of phase voltages/currents are given by calculating modules for each phase from (4.8) as:

$$V_{am} = \sqrt{(V_d^+ + V_d^-)^2 + (V_q^+ - V_q^-)^2} \quad (4.17)$$

$$V_{bm} = \sqrt{\left(\frac{\sqrt{3}}{2}(V_q^+ + V_q^-) - \frac{1}{2}(V_d^+ + V_d^-)\right)^2 + \left(\frac{\sqrt{3}}{2}(V_d^+ - V_d^-) + \frac{1}{2}(V_q^+ - V_q^-)\right)^2} \quad (4.18)$$

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Figure 4.4: Case study of short-circuit event between phases A and B: (a) phasor diagram of three-wire voltage system, (b) power stage three-phase source structure.

$$V_{cm} = \sqrt{\left(\frac{1}{2}(V_d^+ + V_d^-) + \frac{\sqrt{3}}{2}(V_q^+ + V_q^-)\right)^2 + \left(\frac{\sqrt{3}}{2}(V_d^+ - V_d^-) - \frac{1}{2}(V_q^+ - V_q^-)\right)^2}. \quad (4.19)$$

4.3.2 DDSRF Current Controller References Generation Under Grid Faults

If for instance there is a short-circuit between phases A and B, then the phasor diagram shown in Fig. 4.4a can be drawn. Due to short-circuit, assuming that the three-phase source has output impedance L_g as in Fig. 4.4b, the short-circuit point has a voltage:

$$v_{A,sc,ab} = v_{B,sc,ab} = \frac{v_{Ag} + v_{Bg}}{2} = -\frac{v_C}{2}, \quad (4.20)$$

where voltage v_C remains unaffected. From phasor diagram values of $V_{ad,sc,ab}$, $V_{aq,sc,ab}$, $V_{bd,sc,ab}$ and $V_{bq,sc,ab}$ are obtained as:

$$V_{ad,sc,ab} = 0.5V_m \cos \frac{\pi}{3} = \frac{1}{4}V_m \quad (4.21)$$

$$V_{aq,sc,ab} = -0.5V_m \sin \frac{\pi}{3} = -\frac{\sqrt{3}}{4}V_m \quad (4.22)$$

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$$V_{bd,sc,ab} = 0.5V_m \cos \frac{\pi}{3} = \frac{1}{4}V_m \quad (4.23)$$

$$V_{bq,sc,ab} = -0.5V_m \sin \frac{\pi}{3} = -\frac{\sqrt{3}}{4}V_m. \quad (4.24)$$

Plugging in (4.21-4.24) into (4.13-4.16) the positive and negative sequence dq components are obtained:

$$V_{d,sc,ab}^+ = \frac{1}{2}V_m \quad (4.25)$$

$$V_{q,sc,ab}^+ = 0 \quad (4.26)$$

$$V_{d,sc,ab}^- = -\frac{1}{4}V_m \quad (4.27)$$

$$V_{q,sc,ab}^- = \frac{\sqrt{3}}{4}V_m. \quad (4.28)$$

In order to maintain the same power level as before short-circuit between phases A and B, the current references must be increased by a factor. There are many different ways to provide full power through combinations of positive and negative sequence components. The total average active power is governed by:

$$P = \frac{3}{2} (V_d^+ I_d^+ + V_q^+ I_q^+ + V_d^- I_d^- + V_q^- I_q^-) \quad (4.29)$$

where part coming from $V_q^+ I_q^+$ is equal to zero since rectifier DDSRF-PLL is assumed to be synchronized to positive sequence voltage vector $\mathbf{v}^+$. Therefore, the rectifier can be controlled to provide full power with just positive sequence, just negative sequence or a combination of both. Providing power with only positive or only negative sequence has an advantage of perfectly balanced three-phase currents despite the severe unbalance in input three-phase voltages. However, the same power can be provided with lower RMS current in the phases that have lower voltages. The reason lies in the fact that other sequence can provide power, therefore symmetrical currents with unbalanced voltages will generate more conduction losses reducing the converter efficiency. The approach used in this work is based on resistive sequence emulation. That means that current dq references are set in proportion to the respective voltage dq components. That guarantees minimum total RMS currents, minimizing converter conduction loss.

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Setting the current references in the exact proportion, relative to their nominal balanced case current of I_m , as for the voltage components would yield in only half of active power provided to the load. Therefore, the values obtained must be doubled as:

$$I_{d,sc,ab}^+ = I_m \quad (4.30)$$

$$I_{q,sc,ab}^+ = 0 \quad (4.31)$$

$$I_{d,sc,ab}^- = -\frac{1}{2}I_m \quad (4.32)$$

$$I_{q,sc,ab}^- = \frac{\sqrt{3}}{2}I_m. \quad (4.33)$$

This set of current references provides full power to the load, as in the case without grid fault, with global minimum per phase RMS current. The unique condition for this failure case is that absolute difference of peak instantaneous voltage amplitudes of phases A and B must be below some small ε value, and the difference of phase C peak voltage and twice the amplitude of phase A voltage must be below ε as:

$$(|V_{am} - V_{bm}| < \varepsilon) \wedge (|2V_{am} - V_{cm}| < \varepsilon). \quad (4.34)$$

Similarly, for the case of short-circuit between phases B and C, the direct and quadrature components of voltages in phase A and B are:

$$V_{ad,sc,bc} = V_m \quad (4.35)$$

$$V_{aq,sc,bc} = 0 \quad (4.36)$$

$$V_{bd,sc,bc} = -0.5V_m \quad (4.37)$$

$$V_{bq,sc,bc} = 0, \quad (4.38)$$

which gives dq components of three-phase voltage as:

$$V_{d,sc,bc}^+ = \frac{1}{2}V_m \quad (4.39)$$

$$V_{q,sc,bc}^+ = 0 \quad (4.40)$$

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$$V_{d,sc,bc}^- = \frac{1}{2}V_m \quad (4.41)$$

$$V_{q,sc,bc}^- = 0, \quad (4.42)$$

and the current references that guarantee resistive behaviour and full power are:

$$I_{d,sc,bc}^+ = I_m \quad (4.43)$$

$$I_{q,sc,bc}^+ = 0 \quad (4.44)$$

$$I_{d,sc,bc}^- = I_m \quad (4.45)$$

$$I_{q,sc,bc}^- = 0, \quad (4.46)$$

while the unique condition for this failure case is:

$$(|V_{bm} - V_{cm}| < \varepsilon) \wedge (|2V_{bm} - V_{am}| < \varepsilon). \quad (4.47)$$

Finally, the current references for the case of short-circuit between phases C and A that guarantee resistive behaviour and full power are:

$$I_{d,sc,ca}^+ = I_m \quad (4.48)$$

$$I_{q,sc,ca}^+ = 0 \quad (4.49)$$

$$I_{d,sc,ca}^- = -\frac{1}{2}I_m \quad (4.50)$$

$$I_{q,sc,ca}^- = -\frac{\sqrt{3}}{2}I_m, \quad (4.51)$$

while the unique condition:

$$(|V_{cm} - V_{am}| < \varepsilon) \wedge (|2V_{cm} - V_{bm}| < \varepsilon). \quad (4.52)$$

In order to analyze a grid fault case where phase A is left open, the equivalent power stage structure is provided in Fig. 4.5b. Due to open-circuit, the zero-sequence voltage v_0 is:

$$v_{0,oc,a} = \frac{v_B + v_C}{2} = -\frac{v_A}{2}. \quad (4.53)$$

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Figure 4.5: Case study of open-circuit of phase A: (a) phasor diagram of two-wire voltage system, (b) power stage three-phase source structure.

The zero-sequence does not affect the power flow due to lack of neutral connection, therefore it must be subtracted from the voltages in other two phases which yields:

$$v_{B,oc,a} = v_B - v_{0,oc,a} = \frac{\sqrt{3}}{2} V_m e^{-j\pi/2} \quad (4.54)$$

$$v_{C,oc,a} = v_C - v_{0,oc,a} = \frac{\sqrt{3}}{2} V_m e^{j\pi/2}. \quad (4.55)$$

Due to open-circuit of one phase, the system effectively degenerates into two-wire system where it must hold that currents in the operating phases must be of the same amplitude and opposing sign. As it can be concluded from the phasor diagram from Fig. 4.5a, the three-phase system of voltages degenerated into single-phase system with line-to-line voltage v_{BC} . Based on the phasor diagram, the direct and quadrature components in of voltages in phases A and B for this case are:

$$V_{ad,oc,a} = 0 \quad (4.56)$$

$$V_{aq,oc,a} = 0 \quad (4.57)$$

$$V_{bd,oc,a} = 0 \quad (4.58)$$

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$$V_{bq,oc,a} = -V_m \sin \frac{\pi}{2} = -\frac{\sqrt{3}}{2}V_m. \quad (4.59)$$

which gives dq domain sequence components:

$$V_{d,oc,a}^+ = \frac{1}{2}V_m \quad (4.60)$$

$$V_{q,oc,a}^+ = 0 \quad (4.61)$$

$$V_{d,oc,a}^- = -\frac{1}{2}V_m \quad (4.62)$$

$$V_{q,oc,a}^- = 0. \quad (4.63)$$

In this case there is no degree of freedom in the choice of current references meaning that half of the power must be transmitted by positive and half by negative sequence. If the same output power is to be provided while maintaining resistive behaviour of the rectifier, the current references must be:

$$I_{d,oc,a}^+ = I_m \quad (4.64)$$

$$I_{q,oc,a}^+ = 0 \quad (4.65)$$

$$I_{d,oc,a}^- = -I_m \quad (4.66)$$

$$I_{q,oc,a}^- = 0, \quad (4.67)$$

while the unique condition for this failure case is that absolute difference of peak instantaneous current amplitudes in phases B and C must be below some small ε value, and phase A current amplitude must be below ε as:

$$(|I_{bm} - I_{cm}| < \varepsilon) \wedge (I_{am} < \varepsilon). \quad (4.68)$$

Similarly, for the case of open-circuit of phase B, the direct and quadrature components of voltages in phase A and B are:

$$V_{ad,oc,b} = \frac{3}{4}V_m \quad (4.69)$$

$$V_{aq,oc,b} = -\frac{\sqrt{3}}{4}V_m \quad (4.70)$$

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$$V_{bd,oc,b} = 0 \quad (4.71)$$

$$V_{bq,oc,b} = 0, \quad (4.72)$$

which gives dq components of three-phase voltage as:

$$V_{d,oc,b}^+ = \frac{1}{2}V_m \quad (4.73)$$

$$V_{q,oc,b}^+ = 0 \quad (4.74)$$

$$V_{d,oc,b}^- = \frac{1}{4}V_m \quad (4.75)$$

$$V_{q,oc,b}^- = \frac{\sqrt{3}}{4}V_m, \quad (4.76)$$

and the current references that guarantee resistive behaviour and full power are:

$$I_{d,oc,b}^+ = I_m \quad (4.77)$$

$$I_{q,oc,b}^+ = 0 \quad (4.78)$$

$$I_{d,oc,b}^- = \frac{1}{2}I_m \quad (4.79)$$

$$I_{q,oc,b}^- = \frac{\sqrt{3}}{2}I_m, \quad (4.80)$$

while the unique condition for this failure case is:

$$(|I_{cm} - I_{am}| < \varepsilon) \wedge (I_{bm} < \varepsilon). \quad (4.81)$$

Finally, the current references for the case of open-circuit of phase C that guarantee resistive behaviour and full power are:

$$I_{d,oc,c}^+ = I_m \quad (4.82)$$

$$I_{q,oc,c}^+ = 0 \quad (4.83)$$

$$I_{d,oc,c}^- = \frac{1}{2}I_m \quad (4.84)$$

$$I_{q,oc,c}^- = -\frac{\sqrt{3}}{2}I_m, \quad (4.85)$$

Figure 4.6: Case study of short-circuit of phase A: (a) phasor diagram of three-wire voltage system, (b) power stage three-phase source structure.

while the unique condition:

$$(|I_{am} - I_{bm}| < \varepsilon) \wedge (I_{cm} < \varepsilon). \quad (4.86)$$

The last set of failure cases is short-circuit of one phase to source neutral. In order to analyze a grid fault case where phase A is short-circuited to source neutral, the equivalent power stage structure is provided in Fig. 4.6b. Due to short-circuit, the zero-sequence voltage v_0 is:

$$v_{0,sc,a} = \frac{v_B + v_C}{3} = -\frac{v_A}{3}. \quad (4.87)$$

Similarly, the zero-sequence does not affect the power flow due to lack of neutral connection, therefore it must be subtracted from the voltages in all three phases, as illustrated by phasor diagram in Fig. 4.6a, which yields:

$$v_{A,sc,a} = v_A - v_{0,sc,a} = \frac{1}{3}V_m \quad (4.88)$$

$$v_{B,sc,a} = v_B - v_{0,sc,a} \approx \frac{\sqrt{7}}{3}V_m e^{-j108^\circ} \quad (4.89)$$

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$$v_{C,sc,a} = v_C - v_{0,sc,a} \approx \frac{\sqrt{7}}{3} V_m e^{j108^\circ}. \quad (4.90)$$

Based on (4.88) and (4.89), the direct and quadrature components of voltages in phases A and B for this case are:

$$V_{ad,oc,a} = \frac{1}{3} V_m \quad (4.91)$$

$$V_{aq,oc,a} = 0 \quad (4.92)$$

$$V_{bd,oc,a} = -\frac{1}{6} V_m \quad (4.93)$$

$$V_{bq,oc,a} = -\frac{\sqrt{3}}{2} V_m, \quad (4.94)$$

which gives dq domain sequence components:

$$V_{d,oc,a}^+ = \frac{2}{3} V_m \quad (4.95)$$

$$V_{q,oc,a}^+ = 0 \quad (4.96)$$

$$V_{d,oc,a}^- = -\frac{1}{3} V_m \quad (4.97)$$

$$V_{q,oc,a}^- = 0. \quad (4.98)$$

Similar to the case of short-circuit between phases, the total average output power can be given by only positive, negative or a combination of both sequences. In this case, however, after a phase short-circuit event, the positive sequence vector has double the amplitude of the negative sequence. In order to maintain output power with only positive sequence, the current reference in $d+$ axis must be increased to 150 %. On the other hand, if all active power is to be provided by negative sequence, then the final value would be 300 % which would considerably increase system conduction loss. If the same output power is to be provided while maintaining resistive behaviour of the rectifier, the current references must be:

$$I_{d,sc,a}^+ = \frac{6}{5} I_m \quad (4.99)$$

$$I_{q,sc,a}^+ = 0 \quad (4.100)$$

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$$I_{d,sc,a}^- = -\frac{3}{5}I_m \quad (4.101)$$

$$I_{q,sc,a}^- = 0, \quad (4.102)$$

while the unique condition for this failure case is that absolute difference of peak instantaneous voltage amplitudes in phases B and C must be below some small ε value, and difference between phase B voltage amplitude and phase A voltage amplitude scaled by $\sqrt{7}$ must be below ε as:

$$(|V_{bm} - V_{cm}| < \varepsilon) \wedge \left(\left| \sqrt{7}V_{am} - V_{bm} \right| < \varepsilon \right). \quad (4.103)$$

Similarly, for the case of short-circuit of phase B, the direct and quadrature components of voltages in phase A and B are:

$$V_{ad,sc,b} = \frac{5}{6}V_m \quad (4.104)$$

$$V_{aq,sc,b} = -\frac{\sqrt{3}}{6}V_m \quad (4.105)$$

$$V_{bd,sc,b} = -\frac{1}{6}V_m \quad (4.106)$$

$$V_{bq,sc,b} = -\frac{\sqrt{3}}{6}V_m, \quad (4.107)$$

which gives dq components of three-phase voltage as:

$$V_{d,sc,b}^+ = \frac{2}{3}V_m \quad (4.108)$$

$$V_{q,sc,b}^+ = 0 \quad (4.109)$$

$$V_{d,sc,b}^- = \frac{1}{6}V_m \quad (4.110)$$

$$V_{q,sc,b}^- = \frac{\sqrt{3}}{6}V_m, \quad (4.111)$$

and the current references that guarantee resistive behaviour and full power are:

$$I_{d,sc,b}^+ = \frac{6}{5}I_m \quad (4.112)$$

$$I_{q,sc,b}^+ = 0 \quad (4.113)$$

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$$I_{d,sc,b}^- = \frac{3}{10} I_m \quad (4.114)$$

$$I_{q,sc,b}^- = \frac{3\sqrt{3}}{10} I_m, \quad (4.115)$$

while the unique condition for this failure case is:

$$(|V_{cm} - V_{am}| < \varepsilon) \wedge \left(\left| \sqrt{7} V_{bm} - V_{cm} \right| < \varepsilon \right). \quad (4.116)$$

Finally, the current references for the case of short-circuit of phase C that guarantee resistive behaviour and full power are:

$$I_{d,sc,c}^+ = \frac{6}{5} I_m \quad (4.117)$$

$$I_{q,sc,c}^+ = 0 \quad (4.118)$$

$$I_{d,sc,c}^- = \frac{3}{10} I_m \quad (4.119)$$

$$I_{q,sc,c}^- = -\frac{3\sqrt{3}}{10} I_m, \quad (4.120)$$

while the unique condition is:

$$(|V_{am} - V_{bm}| < \varepsilon) \wedge \left(\left| \sqrt{7} V_{cm} - V_{am} \right| < \varepsilon \right). \quad (4.121)$$

As a conclusion of this analysis summary of all nine failure scenarios, their current references for resistive case, as well as the cases where power is provided by only positive or negative sequence is given in Table 4.1. Moreover, per phase RMS currents are provided for the sake of comparison. All values are normalized to I_m .

4.4 Three-Phase Boost-Type Rectifier With Proposed Grid Fault Tolerant Logic

In this Section the previously derived control logic that presents robustness against grid faults is applied to a three-phase three-wire six-switch boost-type rectifier with output power rating of 3.45 kW. First, power stage parameters are

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Table 4.1: An overview and comparison of current references and peak per-phase currents for all analyzed grid fault scenarios assuming full output power by means of resistive case, only positive and only negative sequence case active power delivery (all values are normalized to I_m).

Fault	Resistive						Only $\mathbf{I}^+$		Only $\mathbf{I}^-$		
	I_d^+	I_d^-	I_q^-	I_{am}	I_{bm}	I_{cm}	I_d^+	$I_{abc,m}$	I_d^-	I_q^-	$I_{abc,m}$
Short AB	1	$-\frac{1}{2}$	$\frac{\sqrt{3}}{2}$	1	1	2	2	2	-1	$\sqrt{3}$	2
Short BC	1	1	0	2	1	1	2	2	2	0	2
Short CA	1	$-\frac{1}{2}$	$-\frac{\sqrt{3}}{2}$	1	2	1	2	2	-1	$-\sqrt{3}$	2
Open A	1	-1	0	0	$\sqrt{3}$	$\sqrt{3}$	/	/	/	/	/
Open B	1	$\frac{1}{2}$	$\frac{\sqrt{3}}{2}$	$\sqrt{3}$	0	$\sqrt{3}$	/	/	/	/	/
Open C	1	$\frac{1}{2}$	$-\frac{\sqrt{3}}{2}$	$\sqrt{3}$	$\sqrt{3}$	0	/	/	/	/	/
Short A	$\frac{6}{5}$	$-\frac{3}{5}$	0	$\frac{3}{5}$	$\frac{3\sqrt{7}}{5}$	$\frac{3\sqrt{7}}{5}$	$\frac{3}{2}$	$\frac{3}{2}$	-3	0	3
Short B	$\frac{6}{5}$	$\frac{3}{10}$	$\frac{3\sqrt{3}}{10}$	$\frac{3\sqrt{7}}{5}$	$\frac{3}{5}$	$\frac{3\sqrt{7}}{5}$	$\frac{3}{2}$	$\frac{3}{2}$	$\frac{3}{2}$	$\frac{3\sqrt{3}}{2}$	3
Short C	$\frac{6}{5}$	$\frac{3}{10}$	$-\frac{3\sqrt{3}}{10}$	$\frac{3\sqrt{7}}{5}$	$\frac{3\sqrt{7}}{5}$	$\frac{3}{5}$	$\frac{3}{2}$	$\frac{3}{2}$	$\frac{3}{2}$	$-\frac{3\sqrt{3}}{2}$	3

selected. Then, current controller structure based on the decoupling network presented in the Section 4.2 and four identical PI controllers is designed taking into account computational delay of $1.5T_s$. The introduced decoupling scheme enables independent design of positive and negative sequence subsystems which have identical dq models. With implemented proposed grid fault tolerant supervisory logic that modifies current controller references, a set of simulation results is presented that demonstrate the proposed control strategy. Lastly, experimental results conducted on a all-SiC prototype are given to verify the performance in practice.

4.4.1 Rectifier Design

The three-phase three-wire six-switch boost-type rectifier with differential EMI filter and rated output power of 3.45 kW analyzed in this Subsection is given in Fig. 4.7. Since the topology in question is of boost-type in nature, the output voltage must be at least higher than maximum line-to-line grid voltage, assuming Space Vector Modulation (SVM). Since in this work, various grid fault scenarios are analyzed, the selected modulation scheme is carrier based Sinusoidal Pulse Width Modulation

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Figure 4.7: The three-phase three-wire six-switch boost-type rectifier with DDSRF-PLL, current controller and the additional supervisor logic.

(SPWM). As a consequence, for assumed grid line-to-neutral RMS voltage $V_{Ag,RMS}$ of 230 V, the minimum DC link voltage that guarantees full controllability of the switches is:

$$V_{OUT,min} = 2\sqrt{2}V_{Ag,RMS} \approx 651 \text{ V}. \quad (4.122)$$

In order to have some margin during output voltage transients, the selected V_{OUT} is 800 V. In [76], an equation is given which calculates the minimum boost inductor inductance $L_{r,min}$ as a function of maximum allowed peak-to-peak ripple $\Delta I_{am,p-p}$ and rectifier parameters as:

$$L_{r,min} = \frac{\sqrt{6}V_{Ag,RMS,l-n}}{V_{OUT}} \frac{2/3V_{OUT} - \sqrt{2}V_{Ag,RMS,l-n} \cos \frac{\pi}{6}}{\Delta I_{am,p-p} f_s}. \quad (4.123)$$

With the switching frequency f_s chosen to be 50 kHz and maximum allowed peak-to-peak boost inductor current ripple $\Delta I_{am,p-p}$ equal to 20 % of peak nominal

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Table 4.2: 3.45 kW three-phase three-wire six-switch boost-type rectifier parameters.

L_g [μH]	C_e [nF]	C_d [nF]	R_d [Ω]	L_r [mH]	C_{OUT} [μF]	V_{OUT} [V]
500	100	100	70	2	17.5	800

Figure 4.8: The DDSRF current controller structure.

current I_{am} of $5\sqrt{2}$ A, the minimum value of inductance $L_{r,\text{min}}$ is obtained as 1.77 mH. The value of L_r chosen is 2 mH. The total output capacitance C_{OUT} chosen in this work is 17.5 μF . The three-phase output inductance assumed is 500 μH , while the EMI differential filtering capacitor C_e chosen is 100 nF. The location of the EMI resonant peak is at:

$$f_r = \frac{1}{2\pi\sqrt{L_g C_e}} \approx 22.5 \text{ kHz}, \quad (4.124)$$

which is passively damped by damping branch containing C_e and R_d at 100 nF and 70 Ω respectively. The overview of the power stage parameters is given in Table 4.2.

The DDSRF current controller structure is shown in Fig. 4.8. First, the measured L_r inductor currents are transformed to $\alpha\beta$ frame and dq transformations of positive and negative sequence are done by means of $\mathbf{T}_{dq}^+$ and $\mathbf{T}_{dq}^-$ matrices previously used in (4.3) and (4.5). Then, the same decoupling network is introduced as

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Figure 4.9: The three-phase three-wire six-switch boost-type rectifier dq model assuming perfect cross-coupling cancelation.

in the design of DDSRF-PLL from Section 4.2. Afterwards, four identical PI controllers are utilized that control four decoupled currents $i_d^{+'}$, $i_q^{+'}$, $i_d^{-'}$ and $i_q^{-'}$ by actuating over the corresponding duty cycles d_d^{+} , d_q^{+} , d_d^{-} and d_q^{-} . Due to decoupling structure between the positive and negative sequence dq frame currents, the regulator design can be successfully approximated by focusing only on the positive sequence. Moreover, EMI filter dynamics are disregarded since attainable cross-over frequency is predominantly limited by computational delay of the system of $1.5T_s$. Thus, realistic controller bandwidth is in the range of few kHz as opposed to 22.5 kHz resonance of the EMI filter based on (4.124). The equivalent dq model of the three-phase three-wire six-switch boost-type rectifier is identical to the VIENNA rectifier previously given in Fig. 3.35, with the exception of the output capacitor balancing subcircuit, since there is no access to the DC link midpoint. As it is concluded by extensive analysis from Section 3.4.1, the decoupled model from Fig. 3.41 can be used with no significant impact on the loop-gains of the controllers. For the sake of brevity, the three-phase model of the boost-type rectifier is given in Fig. 4.9. Similar to the VIENNA rectifier case, the d -axis duty cycle to inductor

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Figure 4.10: Plot of the three-phase boost rectifier transfer functions with transport delay of $T_d = 1.5T_s$: (a) open-loop transfer functions $G_{dd}^*(s)$ and $G_{qq}^*(s)$, (b) inverted loop-gains $L_{dd}(s)$ and $L_{qq}(s)$ with 2 kHz cross-over frequency.

current transfer function is given by:

$$G_{dd}(s) = -\frac{\frac{V_{OUT}}{2} + \frac{3}{8}D_D^*I_{RD}R_{OUT}}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} \frac{s^2 \frac{\frac{V_{OUT}}{2}R_{OUT}C_{OUT}}{\frac{V_{OUT}}{2} + \frac{3}{8}D_D^*I_{RD}R_{OUT}} + 1}{s^2 \frac{L_r C_{OUT} R_{OUT}}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} + s \frac{L_r + R_{OUT}C_{OUT}R_L}{R_L + \frac{3}{8}D_D^{*2}R_{OUT}} + 1}, \quad (4.125)$$

while q -axis duty cycle to inductor current transfer function is:

$$G_{qq}(s) = \frac{\hat{i}_{rq}}{\hat{d}_q^*} = -\frac{V_{OUT}}{2R_L} \frac{1}{s \frac{L_r}{R_L} + 1}. \quad (4.126)$$

In order to emulate converter efficiency of around 98.5 %, all losses are concentrated in R_L with the resistance of 650 mΩ. Based on the (3.107) previously given for VIENNA rectifier, the duty cycle in d -axis is calculated to be 0.8015. With all parameters defined, the open-loop transfer function plots of $G_{dd}(s)$ and $G_{qq}(s)$ are given in Fig. 4.10a. Analyzing the open-loop transfer functions for the case at hand, the same PI regulator is chosen for d and q axes with proportional and integral part of -0.062515 A^{-1} and -143.347 C^{-1} respectively, which yields current loop bandwidths of 2 kHz in both cases, as it can be verified in Fig. 4.10b. The same current regulators and bandwidths are used for the negative sequence.

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4.4.2 Simulation Results

In order to verify the proposed design methodology, a simulation is carried out in power electronics simulator GeckoCIRCUITS. The results are presented at 3.45 kW output power and according to parameters from Table 4.2 at 400 Hz grid frequency. The supervisor logic state machine implements current references for each failure case as per Table 4.1, while the conditions for entering the corresponding state are calculated in Subsection 4.3.2. In order to reliably detect the failure state, the corresponding condition must be fulfilled for k number of consecutive regulation execution cycles of 20 μ s. The value chosen is 50 which gives minimum detection time of 1 ms. For each of nine failure cases, set of plots is given that illustrate transition from nominal to failure state and vice-versa. The results follow the evolution of measured input voltages, rectifier input currents and output DC link voltage.

The waveforms concerning grid failure in the form of phase-to-phase short-circuit for all three possible combinations are given in Figs. 4.11-4.13. As it can be seen from the results, the rectifier is able to successfully control these cases with reaction time inside two grid cycles, mostly determined by the additional minimum detection time of 1 ms.

The waveforms concerning grid failure in the form of single phase open scenario for all three possible combinations are given in Figs. 4.14-4.16. Again, the rectifier is able to successfully control these cases with reaction time inside two grid cycles.

Lastly, the waveforms concerning grid failure in the form of single phase short-circuit to source neutral scenario for all three possible combinations are given in Figs. 4.17-4.19. Again, the rectifier is able to successfully control these cases with reaction time inside two grid cycles.

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Figure 4.11: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phases A and B grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Figure 4.12: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phases B and C grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

4.4. Three-Phase Boost-Type Rectifier With Proposed Grid Fault Tolerant Logic

Figure 4.13: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phases C and A grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Figure 4.14: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for open-circuit of phase A grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

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Figure 4.15: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for open-circuit of phase B grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Figure 4.16: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for open-circuit of phase C grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

4.4. Three-Phase Boost-Type Rectifier With Proposed Grid Fault Tolerant Logic

Figure 4.17: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phase A and source neutral grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Figure 4.18: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phase B and source neutral grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Chapter 4. Analysis of Boost-type Rectifiers Under Input Phase Failure

Figure 4.19: Simulation results of the three-phase three-wire six-switch boost-type rectifier input voltages, input currents and output DC link voltage for short-circuit between phase C and source neutral grid failure: (a) evolution of the waveforms from nominal to failure case, (b) evolution of the waveforms from failure to nominal case.

Figure 4.20: 3.45 kW experimental setup.

4.5 Experimental Results

In order to validate the discussed theory, a three-phase three-wire six-switch three-phase boost-type rectifier prototype with nominal output power of 3.45 kW is developed shown in Fig. 4.20. MOSFETs used are with on-resistance of 160 m Ω C2M0160120D manufactured by Wolfspeed. Inductors value is chosen to be 2 mH and it is designed using litz wire with 93 turns. The inductor core is PC40 90/90/30 from TDK with an air gap of 3 mm. Output DC link capacitors are 7x 2 times

4.5. Experimental Results

Table 4.3: 3.45 kW three-phase three-wire six-switch three-phase boost-type rectifier power stage devices and passives.

Device/Passive	Part number
$S_{A,B,C,\pm}$	C2M0160120D
Gate driver	CRD-001
$2C_{OUT}$	7x B32674D6505K
L_r	93 turn (litz wire) PC40 90/90/30 air gap 3 mm
Current sensors	LAH 25-NP
Microcontroller	TI F28335

in series of 5 μ F EPCOS B32674D6505K capacitors with equivalent capacitance of 17.5 μ F. Output DC link voltage is set to 800 V. Input current sensors are LA25-NP from LEM. The control is done by Texas Instruments F28335 Delfino microcontroller with switching frequency of 50 kHz.

The results of the rectifier operating at nominal power at 400 Hz as well as at 800 Hz are presented in Figs. 4.21 and 4.22 respectively. It can be seen that the rectifier operation under nominal conditions is unaffected by negative sequence coupling due to decoupling methods previously discussed in Section 4.2. The results of the rectifier operating with phase C as a short-circuit is shown in Fig. 4.23. Since the power provided is chosen to be with only positive sequence currents, the input currents RMS rise is at 50 %, as it is predicted in Table 4.1. The rectifier is able to provide full power with minor impact on the mains current quality. The phase C open test is shown in Fig. 4.24. The provided power is limited to 85% due to sharp saturation behaviour of the input boost inductors L_r . The steady-state behaviour is in very good agreement to the previous analysis.

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Figure 4.21: Experimental results of 3.45 kW three-phase three-wire six-switch boost-type rectifier steady-state nominal operation @400 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 4.22: Experimental results of 3.45 kW three-phase three-wire six-switch boost-type rectifier steady-state nominal operation @800 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

4.5. Experimental Results

Figure 4.23: Experimental results of 3.45 kW three-phase three-wire six-switch boost-type rectifier steady-state phase C short-circuit operation providing power with only positive sequence currents @800 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

Figure 4.24: Experimental results of 3.45 kW three-phase three-wire six-switch boost-type rectifier steady-state phase C open-circuit operation providing 85% power @800 Hz: (a) three-phase input voltages and currents, (b) input and output power quality overview.

4.6 Conclusions

Based on the presented analysis in this Chapter, a set of conclusions can be derived. The main contribution of this Chapter is to provide a robust control strategy for a three-phase three-wire six-switch boost-type rectifier against arbitrary input phase failure scenario. The fundamental idea of controlling positive and negative sequence components of the three-phase system after the failure occurrence that is used in 50/60 Hz grid inverter applications is adopted to the rectification process for avionic systems. By creating an unified current controller structure that takes inputs in direct and quadrature components of positive and negative sequence currents, the simple and robust controller is created that only needs to change its current references in order to cope with the arbitrary grid fault scenario. Each of the nine failure scenarios, three phase-to-phase short-circuits, three open-phase cases and three phase-neutral short-circuits is shown to have unique combination of input voltages and currents combinations that is advantageously used to reliably detect the corresponding failure. The mathematical extraction of necessary positive and negative sequence components needed to cope with any grid fault scenario is extensively verified by simulation results. Finally, the proposed analysis is backed up by experimental results, conducted on a full SiC 3.45 kW prototype.

Conclusively, a rather simple, low component three-phase three-wire six-switch boost-type rectifier presents a very flexible solution regarding response to the mains failures. This type of rectifier and proposed control can be a very good future candidate for the variable frequency, highly robust three-phase grid applications in the More Electric Aircraft.

Contributions and Future Work

5.1 Conclusions and Contributions

In this dissertation, a survey is first performed on the state-of-the-art three-phase rectifiers intended for use in aircraft applications. Moreover, a brief overview of the topologies and their control strategies under three-phase mains fault scenario for 50/60 Hz grid applications is also addressed since it forms a basis for one of the contributions of this work. This thesis aims to contribute in the field of three-phase active rectifier systems for aircraft application bearing in mind specific requirements of most comprehensive avionic standard DO-160G [15].

The first main set of contributions lies in the design methodology for the three-phase active rectifiers in order to comply with the DO-160G current distortion test under 10 % THD of the three-phase voltage. An analysis of systematic design methodology for three-phase buck-type and boost-type rectifiers in order to meet with the voltage distortion test requirement is performed. For a given voltage harmonic profile, the current harmonic limits that must be satisfied are translated into equivalent per-harmonic admittances in abc domain and a profile of maximum rectifier input admittance versus frequency is obtained. Since the control of the rectifiers is performed in the Synchronous Reference Frame (dq domain), translation of the admittance limits into dq domain is proposed. The newly defined dq admittance profile, due to normalization, is applicable to arbitrary power level with simple shifting by the base admittance governed by the converter nominal power. It is shown that for the buck-type rectifier main limitation lies in the input LC filter design used for differential EMI filtering, while for the boost-type rectifiers there exists a trade-off between current controller bandwidth and input inductor size. At the end, the experimental results conducted on a SiC three-phase 10 kW VIENNA rectifier are shown to tightly back up the proposed theoretical analysis.

The second set of contributions, reflected in Chapter 4, is to provide a robust control strategy for a three-phase three-wire six-switch boost-type rectifier against arbitrary input phase failure scenario in order to meet with the DO-160G phase loss requirement. The fundamental idea lies in control of positive and negative sequence components of the three-phase system after the failure occurrence. For that purpose, two rotating reference frames are used that are tied to positive and negative sequence voltage vectors by means of Decoupled Double Synchronous Reference Frame Phase-Locked Loop (DDSRF-PLL). The mentioned PLL is an essential part of the control strategy since it provides accurate values of direct and quadrature components of positive and negative sequence that are used to control the rectifier under grid fault scenario. Therefore, the applied rectifier closed-loop current control consists of four identical PI controllers, two for each sequence d and q components. Since each grid fault case generates unique values of positive and negative sequence voltage vectors, a mathematical derivation of d and q components of each rotating sequence is calculated. The main contribution of Chapter 4 lies in precise mathematical extraction of necessary positive and negative sequence voltage and current components needed to cope with any grid fault scenario. The total number of analyzed failure cases is nine, where three are related to phase-to-phase short-circuit, three to open-phase case, and three to phase-to-neutral fault. Moreover, a mathematical link between instantaneous amplitudes of each individual phase and positive and negative sequence component values is also provided. The derived link utilized on input three-phase voltages and currents provides a simple way of detecting the nine grid failure cases so that adequate current controller references can be provided which guarantee optimal power flow. Finally, the proposed analysis is backed up by simulation and experimental results, conducted on a full-SiC 3.45 kW prototype.

5.2 Future Work

There are several tasks that can be done in order to further enhance the contributions of this work in the field of AC/DC power conversion intended for use in the future More Electric Aircraft.

5.2. Future Work

- **Utilization of PR+PI controller instead simple PI for boost-type rectifiers under 10 % THDv test.** In Section 3.4 it is shown that high controller bandwidths are necessary in order to cope with the most demanding fifth harmonic. By adding an adaptive PR controller adjusted to the fifth harmonic, this problem could be alleviated.
- **Application of the design methodology for THDv test using control in stationary frame.** For Chapter 3 in this work control in dq domain is selected and thoroughly analyzed. If control in stationary $\alpha\beta$ frame is to be selected, it would be interesting compare it with proposed method. The main advantage in control in $\alpha\beta$ frame is reduced computational effort since there are no trigonometric calculations in this approach.
- **Application of proposed design methodology for THDv test to other active rectifiers.** Even though it is expected for other boost or buck-type rectifiers to behave in the manner closely analyzed on three-phase VIENNA and buck-type rectifiers, it would be interesting to research further along this line and obtain a practical verification.
- **Application of the robust grid fault tolerant current controller on the case of VIENNA rectifier.** After successfully verifying the performance of the proposed control on the three-phase three-wire six-switch boost-type rectifier, it would be interesting to apply it to the three-phase VIENNA rectifier. Since it is a unidirectional converter, modifications are expected to be applied to the method due to inherent reduced space vector choices.
- **Design a three-phase rectifier that complies all mentioned DO-160G requirements from Section 1.2.** This thesis focused on providing a possible solution for compliance with the 10 % THDv test and how to successfully handle single phase loss. A possible extension of this work could be the design that addresses all mentioned DO-160G requirements. As a result, a prototype would be obtained that would bring active rectifiers a step closer to the actual applications in MEA.

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