Space III-V Multijunction Solar Cells on Ge/Si virtual substrates

Iván García

Ignacio Rey-Stolle

Manuel Hinojosa

Iván Lombardero

Luis Cifuentes

Carlos Algora

Huy Nguyen

Aled Morgan

Andrew Johnson

Abstract— Virtual substrates based on thin Ge layers on Si substrates by direct deposition have recently achieved high quality. In this work, their application as low cost, removable substrates for the growth of high efficiency, lightweight and flexible multijunction solar cells for space applications is analyzed. Experimental Ge single-junction solar cells and GaInP/Ga(In)As/Ge triple-junction solar cells using the Ge/Si virtual substrate as an active bottom junction (being the Si inactive), are implemented using medium quality Ge/Si virtual substrates with a 5 μm Ge layer thickness. A lower quality in the Ge material, as compared to standard substrates, but enough carrier collection efficiency for a standard triple-junction, are shown. The expected formation of cracks during growth, due to the large thermal expansion coefficient mismatch with the Si substrate, is confirmed, and is found to be a major limiting factor for the performance of the solar cells. Strategies such as thinning the Ge + III-V structure and minimizing the thermal cycling during growth are discussed. Using an embedded porous Si layer to serve as buffer for the strain is being investigated. This porous layer could also serve as sacrificial layer for high throughput mechanical epitaxial lift-off in the manufacturing of lightweight and flexible multijunction cells. These embedded porous Si layers need to be engineered for optimum performance and compatibility with the Ge and III-V deposition processes.

Keywords—III-V multijunction solar cell, lightweight solar cell, virtual substrate, porous silicon

I. INTRODUCTION

Substituting the conventional Ge growth template by an alternative, which allows for reducing the use of Ge upfront while maintaining or even improving BOL and EOL efficiencies of today's III-V multijunction solar cells, is a topic of great interest for some space applications. Obtaining "virtual substrates" based on Ge deposited on Si substrates is an appealing approach since they would conceptually allow the integration of high efficiency III-V multijunction structures, including the mature GaInP/Ga(In)As/Ge architecture [1]. The use of SiGe metamorphic buffers to fabricate these templates has demonstrated promising performances in single and dual-junction GaInP/GaAs solar

cells [2], [3]. A disadvantage of this approach is the thick ($>10 \mu\text{m}$) metamorphic buffer required. Otherwise, the direct growth of thin Ge films on Si substrates is under development and its potential for the fabrication of high efficiency III-V solar cells has been experimentally demonstrated by growing GaAs and GaInP solar cells on top, with promising results [4], [5]. Given the thin Ge layers used ($< 5 \mu\text{m}$ typically), this approach offers an attractive potential for low substrate cost and eases on Ge material scarcity concerns.

Minimizing the weight of the solar panels is of central importance for space applications. In addition, despite the $\sim 2\times$ higher density of Ge as compared to Si, virtual substrates based on Si are heavier than standard Ge substrates because of the typical thicknesses used for these substrates in order to achieve enough mechanical robustness (175 μm in Ge versus 525 μm in Si, for 4" substrates). Therefore, being able to efficiently remove the substrate is of interest for standard substrates and particularly in the case of virtual substrates based on Si. For this purpose, Ge/Si virtual substrates with an embedded, shallow Si porous layer could function as a release layer to remove the Si substrate using mechanical epitaxial lift-off (ELO). Thanks to the tunable mechanical properties of the porous layer, the lift-off of the epilayer could be carried out by a mechanical "peeling" process which would take just a few minutes, as compared to the much longer times required in the case of chemical ELO. This provides a potential technique for high throughput ELO to manufacture lightweight solar cells. Moreover, the porous layer is expected to help accommodating the thermal expansion coefficient mismatch between the silicon substrate and the Ge and III-V layers deposited on top, mitigating the formation of cracks, which is currently a major issue in this technology [6], [7].

In any case, the development of high efficiency solar cells on Ge/Si virtual substrates poses a series of challenges that need to be tackled. The reader is referred to our previous introductory work on the use of these virtual substrates for high efficiency III-V cells, including a discussion of the potential applications to different solar cell architectures and preliminary experimental results in the context of terrestrial concentrator applications [7]. In this work we examine the use

of Ge/Si virtual substrates as an alternative to standard Ge for the manufacturing of lattice-matched GaInP/Ga(In)As/Ge triple junction solar cells for space, and we discuss the potential of virtual substrates with embedded porous Si layer as release layer for efficient substrate removal.

II. METHODS

The details about the methods used for the theoretical and experimental work presented in this work can be found in our previous work on this topic [7]. Briefly, the modelling work was carried out using a numerical approach by means of the TCAD tool Silvaco Atlas. The experimental semiconductor structures were grown at IES-UPM (Madrid) by MOVPE on Ge/Si virtual substrates developed and provided by IQE plc (Cardiff). The virtual substrates used for this work are medium quality, with a threading dislocation density (TDD) of around $4 \cdot 10^6 \text{ cm}^{-2}$. Higher quality virtual substrates, with TDD below $1 \cdot 10^6 \text{ cm}^{-2}$ are available now and will be used in subsequent experiments. Solar cells were fabricated using standard photolithography, wet etching techniques, and gold electroplated contacts. External quantum efficiency (EQE) and I-V curves measurements are based on standard methods and were taken using custom made systems.

III. THEORETICAL ANALYSIS

The replacement of Ge substrates with Ge/Si virtual substrates to function as the bottom cell in standard GaInP/Ga(In)As/Ge triple-junction (3JSC) space solar cells involves rethinking the design of the semiconductor structure. The Ge bottom cell does not limit the photocurrent in standard 3JSC structures. The open circuit voltage (V_{oc}) is mostly defined by the emitter properties and the bulk recombination properties in the base [8]. However, in virtual Ge/Si substrates, the Ge photoactive layer is only a few microns thick, and the back interface with the Si substrate is expected to be highly recombining, due to the misfit dislocation network formed there, as schematically depicted in Fig. 1, which raise questions about their effect on the short circuit current density (J_{sc}) and V_{oc} . Given the location of the highly recombining interface in the Ge/Si virtual substrate, applying passivation techniques is not straightforward. Removing the Si substrate would provide access to this highly recombining

Fig. 1. Sketch comparing the bottom cell structure in a GaInP/Ga(In)As/Ge solar cell grown on Ge and on Ge/Si substrates.

Fig. 2. Calculated contour plots of the J_{sc} (top) and V_{oc} (bottom) of a Ge bottom cell in a GaInP/Ga(In)As/Ge triple-junction solar cell, vs. the back Ge/Si interface recombination velocity ($S_{rec, Ge/Si}$) and the Ge subcell thickness. The dashed line indicates the (approximate) condition of current matching in a typical triple-junction under AM0 spectrum.

back surface, enabling the utilization of passivation techniques. This can be facilitated by the virtual substrates with embedded porous Si layer, as commented in the Introduction.

Assuming that the highly recombining interface at the back of the Ge subcell will be present, we have carried out a simulation study to understand the implications on the performance of these subcells and quantify the thickness and surface recombination ranges where the optimum performance can be expected. In Fig. 2 we present some selected results of this theoretical study. The graphs show the calculated J_{sc} and V_{oc} of the Ge subcell in a lattice-matched GaInP/Ga(In)As/Ge triple-junction solar cell [9] under 1-sun of AM0 spectrum. The J_{sc} and V_{oc} parameters are plotted vs. the Ge subcell thickness and the Ge/Si interface recombination velocity ($S_{rec, Ge/Si}$). The other parameters of the Ge subcell are taken from our previous works [8]–[10]. Note that the simulation assumes a standard anti-reflection coating (ARC) for this kind of solar cells, which typically exhibits a significant reflectance in the range of the Ge bottom cell ($>10\%$), but which does not affect the overall J_{sc} in the 3JSC given the much higher photocurrent produced in this subcell. However, a thin Ge bottom cell can limit the overall J_{sc} , and, therefore, a broadband ARC would give rise to more

optimistic results of the calculation shown in Fig. 2., allowing for thinner Ge thicknesses and/or higher $S_{\text{rec,Ge/Si}}$.

For the interface recombination velocity values expected (well above 10^5 cm/s) a J_{sc} of 18.5 mA/cm² or more (for current matching with the other subcells under AM0 spectrum) can be attained using a thickness in the Ge layer over 3 μm . If reducing the $S_{\text{rec,Ge/Si}}$, the thickness needed can be lowered down to ~ 1 μm . At this range of thicknesses the $S_{\text{rec,Ge/Si}}$ affects the V_{oc} importantly, which has to be taken into account when trying to reduce the Ge thickness.

The Ge/Si virtual substrates we are working with have thicknesses ranging 3-5 μm . Therefore, according to these modelling results, the J_{sc} that can be achieved in the bottom cell is higher than required for a standard 3JSC. This can compensate for possible losses, such as lower minority carrier properties in the Ge material of virtual substrates, as will be shown in next sections. Obviously, for other solar cell designs other than the standard 3JSC, such as the upright metamorphic, where the upper subcells bandgaps are lower and, therefore, less light is transmitted to the bottom cell, the minimum Ge thickness required increases, similarly as in the case of cells for terrestrial applications [7]. In the case of a typical 4JSC designed by inserting a 1eV subcell in the standard 3JSC, the minimum thickness for the Ge bottom cell is found to be too high (tens of microns) to be realizable using Ge/Si virtual substrates.

IV. EXPERIMENTAL RESULTS

In this work, we focus on the experimental results obtained so far for GaInP/Ga(In)As/Ge 3JSC grown on Ge/Si virtual substrates. The virtual substrates used for these experiments have a 5 μm thick Ge layer. Other Ge layer thicknesses are available and will be tested in future works. The purpose of these preliminary experiments was to implement the first prototype solar cells and gauge the potential to achieve high efficiencies. No issue was found when growing III-V structures on these Ge/Si virtual substrates, which behave similarly as standard Ge substrates, as long as surface readiness for epitaxy and first nucleation steps are concerned, as observed during in-situ spectrometry measurements (details in [7]).

Ge single-junction solar cell structures were fabricated using the virtual substrates. In Fig 3 we show the EQE and light I-V of these solar cells compared to single-junction Ge solar cells fabricated using standard substrates (170 μm thick). A significantly lower EQE is observed for the virtual substrate case. The modelling of these EQE carried out in previous works demonstrated that this is not due to a lower light absorption in the thinner Ge layer of the virtual substrate, but to worse minority carrier properties. However, as noted in the graph, the J_{sc} attained under the AM0 spectrum, assuming a perfect ARC, is still above 22 mA/cm², which is amply enough for the application in a 3JSC with typical ARCs. The light I-V curves show a leaky behavior in the case of the cells made with virtual substrates, and a significantly lower V_{oc} , of about 160 mV. We believe this is due to the shunting behavior of the TDs present in the structure, the microcracks (not visible to the naked eye or under the optical microscope, tough) caused by the thermal expansion coefficient mismatch and the worse electronic quality of the Ge material, as compared to the standard substrates. In order to analyze the impact of the back surface recombination and the minority carrier lifetime degradation on these results, the J_{sc} and V_{oc} of

Fig. 3. Measurement of Ge single-junction solar cells fabricated using Ge/Si virtual substrates. Top: external quantum efficiency and reflectivity. Bottom: 1-sun light I-V curves. The J_{sc} indicated in the EQE graph correspond to the absorption band of the Ge bottom cell in a 3JSC, while the I-V curves were taken with unfiltered spectrum.

these 5 μm Ge subcells were modeled for a range of $S_{\text{rec,Ge/Si}}$ and minority carrier lifetimes in the emitter and base. The resulting contour plots are shown in Fig. 4. The minority carrier lifetime is expressed as a factor multiplying the baseline minority carrier lifetimes used to fit the data for the standard Ge substrate. As can be seen, the J_{sc} and V_{oc} measured can be reproduced in the simulation by drastically reducing the minority carrier lifetimes by about three orders of magnitude. In this situation, the effect of the back surface recombination is weak. The two take home messages here are, first, that there is a large room for improvement in the quality of the Ge layers. In fact, it is expected to improve considerably with available higher quality and thinner Ge/Si virtual substrates, which we plan to use in next development steps. But, second, with the results so far we have not been able to estimate the impact of the $S_{\text{rec,Ge/Si}}$ on the performance, and it is possible that as the quality of the Ge layer improves, the $S_{\text{rec,Ge/Si}}$ will start to limit the performance.

Complete GaInP/Ga(In)As/Ge 3JSC were also grown on the virtual substrates, and solar cells fabricated, characterized, and compared to our standard 3JSC. We have first used a baseline growth process among our available catalogue and applied it to Ge substrates and Ge/Si templates using identical growth runs for both cases. The Ge/Si templates available for this preliminary study had also a 5 μm thick Ge layer. We found that, as expected, such thick Ge layers and the III-V structure grown on top gave rise to visible cracks across the

Fig. 4. Contours of the J_{sc} and V_{oc} against the $S_{rec, Ge/Si}$ and a factor multiplying the emitter and base minority carrier lifetime of the standard Ge substrate case. The dashed lines correspond to the measured values and the red markers indicate the simultaneous fit of J_{sc} and V_{oc} .

Fig. 5. Electroluminescence map of a 3JSC grown on a virtual Ge/Si substrate. The detected emission corresponds to the GaInP top cell. The middle cell shows a similar emission pattern (not shown for brevity) caused by cracks along the cell area.

Fig. 6. Measurement results of the 3JSC grown on Ge/Si virtual substrates compared to the case of standard Ge substrates. Top: EQE; bottom: 1-sun light I-V curves.

surface because of the thermal expansion coefficient mismatch with the silicon substrate. Electroluminescence map measurements reveal also the presence of these cracks, which affect both the top and middle cells (Fig. 5).

These 3JSC devices were measured, and the EQE and light I-V results are shown in Fig. 6. The EQE response shows two main aspects. First, the Ge bottom cell could not be properly measured, given its leaky behavior, as shown in Fig. 3. Second, the Ga(In)As middle cell shows a degraded EQE response, while the GaInP top cell shows a virtually identical EQE to the standard substrate case. This indicates that, leaving cracks aside, the Ge/Si virtual substrates behave as high quality templates for the growth of III-V solar cell structures. Concerning the formation of cracks, it appears that it affects more the middle cell than the top cell. We hypothesize with the possibility that most of the cracking occurs during the growth of the middle cell, which is thick. Moreover, the middle cell is submitted to a thermal cycling during the growth of the top tunnel junction, which can enhance the formation of cracks. It is possible that the top cell is less affected by cracks, since they are already formed before its growth. Obviously, more experimental work is required to understand these results. The light I-V curves shown in Fig 6 bottom reveal the expected lower J_{sc} in the case of the virtual substrate, although the relative drop in J_{sc} is lower than in the case of the concentrator application [7], due to the differences in relative content of the AM0 and AM1.5d spectra in the top and middle cell ranges. The V_{oc} shows a drop of around 500 mV, which

Fig. 7. Sketch of the mechanical ELO process.

points to more than one junction being affected by the cracks, TDs, etc. This is also in agreement with the lower EQE of the middle subcell.

In [7], an extended discussion on these results can be found, but it is clear that a priority now is to reduce the cracking in order to obtain high quality structures on Ge/Si virtual substrates. Total Ge + III-V layer thicknesses below 3 μm are desirable, since that is the maximum thickness reported not to produce cracking in structures grown on Si [11]. The immediate approach we are considering is to use available Ge/Si templates with Ge layers thinner than 5 μm and lower TDD, which will exhibit higher minority carrier properties. Reducing the total thickness of the monolithic III-V structure while maintaining the photocurrent in the subcells seems challenging unless photonic techniques are used to increase the absorption path length. In addition, minimizing the impact of the thermal cycling during growth of the tunnel junctions and during the cooling of the samples after the deposition process, is also under investigation. Finally, we think that virtual substrates with embedded porous Si layers offer a promising route to mitigate the effect of the thermal expansion coefficient mismatch, if the porous layer is appropriately engineered so that it can function as a buffer (confine cracks in the porous layer) for the inevitable mechanical strain that appears between the Si substrate and the rest of Ge and III-V structure [6]. This requires an extensive modeling and experimental work.

V. ELO OF STRUCTURES GROWN ON VIRTUAL SUBSTRATES WITH EMBEDDED POROUS SILICON LAYERS.

As explained in the Introduction, embedding a porous silicon layer in the Ge/Si virtual substrate would enable the development of mechanical ELO processes with high throughput, in addition to serving as a buffer for the strain generated by the thermal expansion coefficient mismatch commented in the previous section. In Fig. 7, the ELO process is sketched. Note that no chemical process is conceptually involved in this technique and, therefore, the full release of a wafer could take just a few minutes. In this case, as compared to the standard ELO where a sacrificial layer is etched, a rough layer of porous Si is expected to remain on the surface of the silicon substrate and the lifted-off epitaxial structure. The silicon substrate could be reused, extending this rough porous layer with a new anodization process, and then fabricating the virtual substrate by deposition of Ge. In the lifted-off epilayers, the rough porous silicon layer can be removed chemically.

Using the embedded porous layer to achieve high throughput ELO is conceptually simple. However, it must be pointed out that the silicon porous layers are kinetically active and the arrangement of the pores and their properties change dramatically when the samples are submitted to thermal loads, which is inevitable during the epitaxial processes used to deposit the Ge and III-V layers. Therefore, the porous layer must be designed taking into account the properties needed for an efficient ELO process and the changes occurring during the epitaxial deposit of the Ge and III-V layers. Fortunately, the anodization process for the formation of the porous layer is very controllable [12], with non-uniform porosity profiles attainable, and which depend on the properties of the original silicon substrate such as the doping level or the orientation. These can be used to engineer the porous layer and obtain the desired properties, which is a work underway.

VI. CONCLUSIONS

Ge/Si virtual substrates offer a variety of potential advantages in the context of high efficiency solar cells. Using low cost Si substrates and a much reduced usage of scarce Ge is attained. In addition, they allow to use embedded porous Si layers, which offer the potential to serve as a buffer for the differences in thermal expansion coefficient in the structure, and would enable the application of high throughput mechanical ELO techniques for substrate detachment in the fabrication of lightweight and flexible solar cells. For the cases where the virtual substrate is to function as an active bottom cell, we have done a simulation study that shows the range of thicknesses and back surface recombination velocities that allow to achieve the required performance in a Ge bottom cell for a GaInP/Ga(In)As/Ge triple-junction cell. We have also shown the first experimental results obtained using medium quality Ge/Si virtual substrates. Functional Ge single-junction cells, and triple-junction cells have been demonstrated, which, when compared to devices grown on standard Ge substrates, show an important room for improvement. Firstly, they reveal a worse electronic quality of the Ge material, as compared to the standard Ge substrates, which is ascribed to the threading dislocations and a high recombination velocity at the back of the Ge layer. Secondly, the expected formation of cracks due to the large thermal expansion coefficient mismatch with the silicon substrate is confirmed, which is probably the main limitation to the performance of the devices developed so far. In order to mitigate the formation of cracks, we are investigating the possibility of thinning the semiconductor structure, minimizing the thermal cycling during the epitaxial deposition processes and using embedded porous Si layers. In the immediate future we will be working with higher quality Ge/Si virtual substrates, which are expected to boost the performance of the solar cell devices grown on top. We will also investigate the relation between the formation of cracks and the characteristics of the porous layers, in addition to make them compatible with efficient mechanical ELO processes, which will allow to achieve high efficiency, lightweight space solar cells grown of cheap substrates.

ACKNOWLEDGMENT

The authors acknowledge the technical support by J. Bautista and useful discussions with L. Barrutia.

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