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*Single-stage single-phase inverter
with multimode modulation and
ZVS for PV applications*

TESIS DOCTORAL

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Abstract

Photovoltaic energy has grown rapidly over the last few decades driven by the decrease in cost and volume of the photovoltaic systems. These systems are composed of solar panels, batteries, and power converters. This tendency has driven the research for more compact and efficient solar inverters for residential applications. To push the research in this field, Google and the IEEE cosponsored the Little Box Challenge in 2014–2015, a contest with a million-dollar prize for the designers of the smallest 2 kVA single-phase inverter in the world. The goal was to obtain a ten times reduction in size compared to commercially available inverters. To obtain this dramatic size reduction, most teams participating in the competition used wide-bandgap devices in their designs and proposed different architectures. The *CEI@UPM* team proposed an innovative but complex solution. Unfortunately, the concept was not ready for the date of the competition. Nevertheless, the research group has continued to develop the architecture to prove that high efficiency and power density are achievable.

A key component in the design of single-phase inverters is the storage element needed to decouple the input and output power. This storage element is typically a bulky capacitor that comprises a large part of the total volume of the inverter. Recently, converters to interface the input port and the capacitor are emerging, allowing a higher voltage swing in the capacitor to lower its volume. The novelty of the studied topology is that it integrates the inverter and the converter for the storage capacitor in a single power stage. Therefore, instead of interfacing just the input and output ports, as conventional inverters do, this inverter has an additional port for the storage capacitor. As a result, the topology can be considered a three-port inverter.

The power stage is simple since it requires only one inductor and six switches. Besides the reduced component count, the topology and modulation are designed aiming to reduce the size and losses of the inductor through the minimization of the indirect power. The indirect power is a measure of the energy stored or delivered by reactive components in a switching cycle.

The modulation of the inverter is divided into several operation modes used in different sectors of the line cycle to allow the inverter to interface the three ports with minimum indirect power. More than one operation mode can be used in each point of the line cycle, and, for the modulation, those with minimum indirect power in the inductor are selected.

Regarding the control, three-port inverters require two control variables. As a result, the current in the inductor in the different operation modes is divided into three or four different states, as opposed to common architectures where the waveform is divided into just two states. The inverter can work under resistive, inductive, and capacitive loads, with different sets of operation modes in each case. As a result, this inverter has a multi-mode modulation. All operation modes work ideally in boundary conduction mode and with variable switching frequency.

The modulation is designed to achieve Zero Voltage Switching (ZVS) in all transitions to improve the efficiency of the inverter. ZVS not only helps to reduce the losses in switching devices, but it reduces the electromagnetic noise introduced in the grid. For ZVS purposes, the current in the inductor is used to discharge the drain-source capacitance of MOSFETs before the turn-on

event. ZVS transitions in this inverter are challenging to analyze due to the different voltages withstood by switching devices, and because more than a device can be turned off at once. In this dissertation, the modulation is modified to achieve ZVS in the transitions where the inductor current is zero. This modification includes additional states when the inductor current is between a positive and negative threshold value. As a result, this modified modulation is based on triangular conduction mode. The proposed modulation also solves some issues associated with the wide variations in switching frequency along the line cycle and for different loads.

As the topology integrates both the DC-AC conversion and the power decoupling functions and the modulation is divided into several operation modes, the control of the inverter is sophisticated. A decoupling network is used to enable the use of conventional control loops and make the control independent of the operation mode. This decoupling network solves a set of equations that relate the time each state lasts in the different modes with the desired currents in the three ports. To improve the previous solution, a numerical method is proposed to solve these equations. This control is implemented in an FPGA.

One of the challenges of nonisolated photovoltaic inverters is the leakage current generated in the parasitic capacitance of the solar panels to ground due to the common-mode voltage between the input and output ports. This leakage current is limited by legislation. In this topology, a filter is required to limit the leakage current.

This dissertation details technical advancements since the end of the competition in the research of this inverter. The multi-mode modulation is explored in detail to obtain all the operation modes required to operate the inverter under any load condition. Also, the ZVS transitions are analyzed, aiming to obtain the current in the inductor needed for ZVS purposes in all possible scenarios. With this information, a complex modulation based on triangular conduction mode is proposed. The modulation is seamless, obtains ZVS in all transitions, and helps limiting the switching frequency variations during the operation. This work also describes how the modulation is implemented. Finally, the design of the leakage current filter is also covered. The concepts discussed in the dissertation are validated through simulations and a 1 kVA proof-of-concept prototype.

Resumen

En las últimas décadas la energía fotovoltaica ha crecido rápidamente, fundamentalmente debido a la bajada del coste y el volumen asociados a los sistemas fotovoltaicos, compuestos de paneles solares, baterías y convertidores de potencia. Esta tendencia está promoviendo el desarrollo de nuevas tecnologías para obtener inversores más eficientes y compactos para aplicaciones residenciales. En este ámbito, Google y el IEEE patrocinaron el concurso *Little Box Challenge* en 2014-2015, donde se premió con un millón de dólares al equipo que diseñó el inversor monofásico más pequeño del mundo con una potencia de 2 kVA. El concurso buscaba reducir el tamaño de los inversores en un factor de diez con respecto a los inversores comerciales en ese momento. Para obtener esta reducción drástica en el tamaño de los inversores, los diferentes equipos que participaron emplearon semiconductores de banda prohibida ancha y presentaron diferentes topologías.

El equipo *CEI@UPM* propuso una solución innovadora y diferente, pero bastante compleja. Desafortunadamente, el concepto no estaba listo para la fecha de la competición. No obstante, este grupo de investigación ha continuado con el desarrollo de la topología, con el objetivo de probar que esta nueva arquitectura es capaz de lograr alta eficiencia con un volumen reducido.

Un componente esencial en el diseño de inversores monofásicos para aplicaciones fotovoltaicas es el elemento de almacenamiento para desacoplar la potencia de entrada de la de salida. Normalmente, este elemento es un condensador que ocupa gran parte del volumen total del inversor. En la actualidad, se utilizan convertidores que conectan este condensador con el puerto de entrada del inversor con el fin de aumentar el rizado en el condensador, lo que permite reducir considerablemente el tamaño de este. La novedad de esta topología es que integra el convertidor para el condensador de almacenamiento con el inversor en una sola etapa de potencia. Por tanto, esta arquitectura no solo interconecta la entrada y la salida del inversor, sino que incluye el condensador de almacenamiento, por lo que puede considerarse un inversor de tres puertos.

La etapa de potencia es relativamente sencilla ya que solo requiere seis transistores y una única bobina, además, la topología está diseñada para minimizar la potencia indirecta en la bobina con el fin de reducir sus pérdidas y su volumen. La potencia indirecta es una medida de la energía almacenada y cedida por componentes reactivos en un ciclo de conmutación.

Para interconectar los tres puertos y minimizar la potencia indirecta de la bobina, la modulación del inversor se divide en varios modos de operación empleados en los diferentes sectores del ciclo de red. Dado que se puede utilizar más de un modo de operación en cada instante del ciclo de red, se seleccionan aquellos modos que minimizan la potencia indirecta.

En lo que al control se refiere, se necesitan dos variables para controlar convertidores de tres puertos. Debido a esto, la corriente en la bobina en cada uno de los modos de operación se divide en tres o en cuatro estados diferentes, mientras que en convertidores convencionales se dividen únicamente en dos estados. El inversor puede operar con cargas resistivas, capacitivas o inductivas, con modos de operación diferentes para cada caso. Por tanto, la modulación de este inversor es

multi-modo, todos estos modos de operación trabajan idealmente en modo de conducción crítico y con frecuencia de conmutación variable.

Para maximizar la eficiencia del inversor, la modulación está diseñada para obtener transiciones suaves en todas las transiciones, concretamente se utiliza la técnica conocida como *Zero-Voltage Switching* (ZVS). Además de disminuir las pérdidas, esta técnica permite reducir el ruido electromagnético inducido en la red. Para obtener transiciones con ZVS, se utiliza la corriente en la bobina para descargar la capacidad parásita entre drenador y fuente de los transistores antes del encendido. Las transiciones con ZVS en este inversor son difíciles de estudiar ya que la tensión que bloquean los distintos dispositivos es distinta, y, además, hay transiciones donde más de un dispositivo se apaga simultáneamente. Para obtener ZVS en aquellas transiciones donde la corriente en la bobina es cero, la modulación se ha modificado para incluir estados adicionales cuando la corriente de la bobina está comprendida entre un límite superior y un límite inferior. Se puede considerar por tanto que la modulación opera en modo de conducción triangular. Esta modulación, además de obtener ZVS, soluciona los problemas asociados con la gran variación en la frecuencia de conmutación de este inversor a lo largo del ciclo de red y cuando se utilizan distintas cargas.

Ya que esta topología integra en una sola etapa la función del inversor y de desacoplo de la potencia de entrada y de salida, y además la modulación está dividida en varios modos de operación, el control resulta complejo. Para utilizar lazos de control convencionales y hacer que el control sea independiente del modo de operación empleado, una red de desacoplo es necesaria. La red de desacoplo utilizada en este trabajo resuelve una serie de ecuaciones que relacionan el tiempo que dura cada estado en los distintos modos con las corrientes en los tres puertos. Estas ecuaciones se resuelven por medio de métodos numéricos. En este trabajo se explica cómo se ha adaptado este método para tener en cuenta la modulación propuesta. Además, el control se ha implementado en una FPGA.

Uno de los retos en el diseño de inversores para paneles solares es la corriente de fuga generada por la tensión de modo común entre la entrada y la salida aplicada a la capacidad parásita que presentan los paneles solares a tierra. Esta corriente de fuga está limitada por legislación, por lo que, en esta topología, un filtro de modo común es necesario para mantener la corriente de fuga por debajo de la máxima especificada.

En esta tesis se tratarán los avances técnicos en el desarrollo de la topología desde el fin de la competición. Se examinará en detalle la modulación multi-modo con el objetivo de encontrar todos los modos de operación necesarios para que el inversor pueda trabajar con cualquier tipo de carga. Además, se analizarán las transiciones con ZVS para obtener la corriente necesaria en la bobina en todos los posibles escenarios con el fin de asegurar que las transiciones sean suaves. Con esta información, se propone una nueva modulación basada en el modo de conducción triangular, que es continua, tiene ZVS en todas las transiciones, y además ayuda a reducir las variaciones en la frecuencia de conmutación. En este trabajo se describirá también como implementar la modulación propuesta. Finalmente, se incluirá el diseño del filtro para minimizar las corrientes de fuga. Los conceptos estudiados a lo largo de este trabajo han sido validados mediante simulaciones y las pruebas realizadas con un prototipo de 1 kVA de potencia.

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Nomenclature

List of abbreviations:

ADC	Analog-to-Digital Converter
BCM	Boundary Conduction Mode
CCM	Continuous Conduction Mode
CEC	California Energy Commission
CM	Common Mode
CSI	Current-Source Inverter
DAB	Dual Active Bridge
DCM	Discontinuous Conduction Mode
DM	Differential Mode
ECPE	European Center for Power Electronics
EMC	Electromagnetic Compliance
EMI	Electromagnetic Interference
FPGA	Field-Programmable Gate Array
GaN	Gallium Nitride
IGBT	Insulated-Gate Bipolar Transistor
LBC	Little Box Challenge
LISN	Line Impedance Stabilization Network
MOSFET	Metal Oxide Silicon Field Effect Transistor
MPPT	Maximum Power Point Tracking
OVC	Over-Current
PF	Power Factor
PI	Proportional Integral
PLL	Phase-Locked Loop
PR	Proportional Resonant
PV	Photovoltaic
Si	Silicon
SiC	Silicon Carbide
T	Triangular (Mode)
T^n	Triangular Negative (Mode)
T^p	Triangular Positive (Mode)
TCM	Triangular Conduction Mode
THD+N	Total Harmonic Distortion plus Noise
TIBuck	Two-Input Buck
Tra	Trapezoidal (Mode)
Tra^n	Trapezoidal Negative (Mode)
Tra^p	Trapezoidal Positive (Mode)
UPS	Uninterruptible Power Supply
VSI	Voltage-Source Inverter
WGB	Wide-Bandgap
ZCS	Zero Current Switching
ZVS	Zero Voltage Switching

The average value of a variable is represented with an overline:

$$a_{mean} = \bar{a} = \int_0^T a(t) dt \quad (1)$$

The rms value is given by:

$$a_{rms} = \sqrt{\frac{1}{T} \int_0^T a(t)^2 dt} \quad (2)$$

Finally, the $||$ operator is defined as:

$$a||b = \frac{a \cdot b}{a + b} \quad (3)$$

In this work, bold variables represent vector and matrices. Uppercase variables stand for the time average over a switching cycle; it should not be interpreted as the time average over the complete line cycle. This is not the standard definition for uppercase variables, but it is more practical in the context of this single-phase inverter. For instance, the inductor current in a switching cycle is defined as $i_L(t)$, the evolution of its average value along the line cycle is defined as $I_L(\omega \cdot t)$. Therefore, in a switching cycle $I_L = \overline{i_L}$.

Moreover, in the thesis, the subscript $_g$ refers to the input port, from *generator*, it should not be mistaken with *grid*. The subscript $_o$ is used for the output port and $_s$ for the storage capacitor port.

Finally, when the horizontal axis in a figure is an angle, it always represents the line cycle. In other words, the axis always represents $\omega_{line} \cdot t$.

Introduction and state of the art

1.1 Motivation

Renewable energy represented 26 % of the global power generation in 2018, rising from 18 % in 2008. Although photovoltaic (PV) power only represented 2.2 % of the electricity output of the world in 2018, it shows the most significant annual increase in installed power among renewable energies. In 2018, Europe added 11.3 GW, a 21 % rise over the power installed in 2017 [2]. These numbers show that solar energy is rising worldwide, but a faster increase is still needed as CO₂ emissions are still growing year after year. The main reason for the increase in solar power is the reduction of costs, and, together with the decrease in the cost of batteries, is making the combination of energy storage and PV energy a more suitable option compared to other renewable and nonrenewable sources [3].

As solar systems and batteries are becoming cheaper, solar installations in residential homes are increasing. PV systems for households play an important role as buildings represent around 30 % of the energy consumption worldwide [2]. In general, a PV system is comprised of the solar panels, a battery to store energy, the inverter, and the loads. Depending on the configuration of the system, additional converters might be necessary, such as DC-DC stages to obtain the maximum power from the panels, which may come in several configurations, DC-DC converters to interface the battery and panels, protections, or smart controllers.

The energy from a PV panel cannot be utilized directly. A power inverter is required to transform the DC power provided by the panel into AC power that can be consumed by electric appliances. The design of the inverter depends on the power level. There are utility-scale three-phase inverters, used in PV plants ranging from hundreds of kilowatts to megawatts and also single-phase micro-inverters interfacing a single or a few PV panels, rated from hundreds of watts to few kilowatts.

With the growth in the PV market, so has increased the research for more cost-effective, lightweight, small, and efficient inverters. This trend is driving the industry to find new architectures, and to use new devices. High efficiency is a desired feature in inverters for two reasons, first, to minimize the number of PV panels required for a given amount of power, second, a considerable amount of space is usually employed to evacuate the heat generated due to the losses in power devices. Hence, lower losses can lead to smaller and more compact designs. Moreover, compact and light inverters are preferred by the users and also decrease maintenance and installation costs.

1.1.1 Little Box Challenge

In July 2014, *Google* and *IEEE* launched the *Little Box Challenge* (LBC) competition, where industries and universities had the opportunity to design a single-phase inverter of 2 kVA with a size reduction of approximately then times compared to state-of-art inverters at that time. The award for the winners was a 1 million \$ prize. The motivation of the competition was to raise interest in PV energy by means of smaller and more efficient inverters and to promote the use of Wide-Bandgap (WBG) devices [1], [4], [5]. Additional goals of this competition were to increase efficiency in Uninterruptible Power Supplies (UPS), help to lower the cost of microgrids in parts of the world where the grid is not available, make Google’s data centers more efficient, or even to use electric vehicle’s batteries as a backup in the event of a blackout [6], [7].

The winner of this competition was the team that designed the smallest inverter while complying with the strict requirements of the competition [8]. Over two thousand teams participated, and, among those, *Google* and *IEEE* selected eighteen finalists based on the technical documents they delivered [1], [5]. The finalists had to deliver a working prototype in October 2015 to the Energy Systems Integration Facility in Golden, Colorado, USA from the National Renewable Energy Laboratory. Their prototypes were submitted to tests to validate the operation and check that all the specifications were met. A list of the finalists can be found in [9]. Among the inverters that successfully passed the tests, the smallest three were the inverter from the *Future Energy Electronics Center* team from *VirginiaTech*, USA in the third position, followed by *Schneider Electric* team, France, and the winner was the *Red Electrical Devils* team from the company *CE+T* from Belgium. The inverter from *Red Electrical Devils* achieved a volume of 14 in³, considerably lower than the 40 in³ specified [10].

Once the competition was over, papers and articles summarized the work done by the finalist as well as the design challenges and how different teams dealt with them [4], [11]. In most of the proposed solutions, the inverter shared three features:

- Transformerless inverters were used for their superior efficiency and power density. These architectures avoid the transformer typically used to step-up the voltage and provide isolation. The specification was prone to the use of transformerless inverters as isolation was not specified and input and output voltages were in the same range. The problem is that certain transformerless topologies, like the one described in this work, generate large leakage current through the parasitic capacitance of PV panels, and this current has to be suppressed with filters. This aspect is further detailed in Section 1.4.2.
- Single-phase inverters for PV applications require nearly constant input power, but the output power pulsates at twice the line frequency. Converters specifically designed to mitigate this twice-line-frequency power pulsation problem were proposed. These converters are intended to replace the bulky electrolytic capacitor placed in the input port with a smaller capacitor with a higher voltage swing. A more detailed explanation can be found in Section 1.5.
- Most teams employed WBG semiconductors, namely Silicon Carbide (SiC) and Gallium Nitride (GaN) devices. The introduction of WBG semiconductors to replace Silicon (Si)

1.2. Organization of the dissertation

devices was key to obtain this tenfold decrease in size compared to commercially-available inverters [7], [12].

One of the participants of this competition was the *CEI@UPM* team, integrated by Pedro Alou, Rafael Asensi, Víctor Cordón, Jorge Cortés, Helena Cristóbal, Angel de Castro, Jesús A. Oliver, Jorge Ramírez, Regina Ramos, Miroslav Vasić, Alberto Sánchez, Marcelo Silva, Vladimir Sviković, Carlos Ucha and led by professor José Antonio Cobos [13]. The solution they proposed was very different compared to those proposed by the rest of the teams, and the team received the *Little box challenge award for academics* grant for it [14]. Also, the team received the *European Center for Power Electronics (ECPE) award* for their work [15]. Unfortunately, the team did not qualify as a finalist because a working prototype was not ready for that date [15].

This dissertation describes the solution proposed by the *CEI@UPM* team and the improvements since the end of the competition, trying to reduce the gap between the initial idea and a prototype that could meet the specifications.

1.2 Organization of the dissertation

This section describes the structure of this and the following chapters of this work.

In the rest of the chapter, first, the specifications of the Little Box Challenge are discussed, as it is the target of the research project in which this dissertation is framed. The specific considerations in the design of inverters for PV applications are discussed later. Also, the research related to the topic of single-phase inverters to date is reviewed. Two of these aspects, namely the power pulsation and the leakage current, are explained in detail as they are important throughout the thesis. The leakage current problem is briefly explained, together with a description of the problems and advantages that transformerless inverters present compared to isolated inverters. The leakage problem is elaborated in Chapter 6. As a review, common transformerless inverters are described. Later, the twice-line-frequency power pulsation issue is extensively covered. Architectures are classified depending on how they deal with the power pulsation. The literature on this topic for nonisolated inverters is reviewed. This review leads to the concept of the single-stage three-port inverter, a type of architecture where the circuit to handle the power pulsation is integrated with the inverter. This concept is the basis of the topology analyzed in this work. A brief review of general aspects of three-port conversion and the challenges these architectures usually face is included later. The solutions proposed by the finalists of the LBC are included as a part of the literature review. Then, the previous work regarding the studied architecture is detailed, highlighting the operation principle and how the topology was derived. The chapter ends with the objectives of the dissertation and its contributions to the research line in the *CEI@UPM* group.

The rest of the dissertation is organized as follows:

Chapter 2 describes how the modulation for the studied inverter was derived, introducing the work of José A. Cobos in [16]. The topology is designed to integrate a storage capacitor used for power pulsation into the inverter. A single inductor is used to perform output voltage regulation and power balance among the input, storage capacitor, and output ports. The goal of the modulation is to decrease the power processed by this inductor, namely P_{indL} .

Chapter 3 analyzes the Zero Voltage Switching (ZVS) transitions in this inverter. This technique reduces losses in switching devices and decreases EMI filter requirements. The chapter is introduced before the final modulation of the inverter is presented as ZVS plays an essential role in shaping the current in the inductor.

Chapter 4 describes the different operation modes that this converter uses along the line cycle, considering only transitions where ZVS can be achieved. The range of operation of each mode is described too. The modulation described in Chapter 2 is modified as it cannot be directly implemented.

Chapter 5 describes how the control is implemented. First, the complete control structure is shortly reviewed. Then, how *control times* are obtained is extensively described, emphasizing the *inversion-based control* used for the modulation described in Chapter 4.

Chapter 6 includes an extensive description of the leakage current issue in the studied topology, describing the causes, and the guidelines to design a filter to mitigate this problem.

Chapter 7 includes a simulation of the inverter and experimental validation. In this chapter, a 1 kVA prototype, the setup, and the performed tests are described.

Chapter 8 summarizes the conclusion, the reach of this work, and the future lines of this research line.

1.3 Specifications for the Little Box Challenge

This research line and this thesis are about the implementation of the topology proposed by Prof. José A. Cobos for the LBC and the general goal is to meet the specifications for this competition. A summary of the specifications is included below, extending those sections related to the topics of this dissertation. The specifications for the contest were published in [8], unfortunately, the original publication is no longer available, and the document cited here is an archived version. The scope of the contest is to design a 2 kVA inverter with a volume below 40 in³. The inverter has to endure 100 h of continuous operation and meet the specifications listed below:

- **Volume and enclosure requirements:** The inverter has to be contained within a rectangular enclosure in a volume of less than 40 in³, or 655 cm³. Therefore, the power density must be above 50 W/in³, or 3 kW/dm³.
- **Efficiency:** The efficiency, measured as $\eta = P_{out\ AC}/P_{in\ DC}$, should be above 95 % at full power. Moreover, the *California Energy Commission* (CEC) efficiency should also be above 95 %. The CEC efficiency is given by:

$$0.04 \cdot \eta|_{10\ \%} + 0.05 \cdot \eta|_{20\ \%} + 0.12 \cdot \eta|_{30\ \%} + 0.21 \cdot \eta|_{50\ \%} + 0.53 \cdot \eta|_{75\ \%} + 0.05 \cdot \eta|_{100\ \%} \quad (1.1)$$

- **Maximum exposed outer device temperature:** All finger-accessible parts of the chassis should be below 60 °C for an ambient temperature up to 30 °C.
- **Input voltage:** The input of the inverter is a 450 V voltage source with a 10 Ω resistor in series with the positive terminal of the source. This configuration is used to model the I-V

1.3. Specifications for the Little Box Challenge

curve of solar panels. The Common Mode (CM) current from the DC supply has to be below 50 mA rms for a CM capacitance below 200 nF (120 nF is the expected value).

- **Output voltage:** The single-phase output voltage must be $240\text{ V} \pm 12\text{ V}$ rms with a line frequency of 60 Hz within $\pm 3\text{ Hz}$.
- **Load profile:** Passive resistive, capacitive, and inductive loads are used to test the inverter. The load is connected to the inverter through an isolation transformer. The maximum load is 2 kVA, with a Power Factor (PF) between 0.7 and 1, leading or lagging. The load will vary from 0 to 2 kVA with load steps as high as 500 VA for resistive loads. 100 VA steps are used for capacitive and inductive loads.
- **Total harmonic distortion + noise:** The quality of the output sinewave is measured with the Total Harmonic Distortion plus Noise (THD+N), defined as:

$$V_{THD+N} = \frac{\sqrt{V_{noise}^2 + \sum_{i=2}^{i=\infty} V_i^2}}{V_1} \quad I_{THD+N} = \frac{\sqrt{I_{noise}^2 + \sum_{i=2}^{i=\infty} I_i^2}}{I_1} \quad (1.2)$$

V_1 and I_1 are the amplitude at the fundamental frequency, in this case, the 60 Hz component. V_i and I_i is the amplitude of the i^{th} harmonic. Finally, V_{noise} and I_{noise} are the rms value of all components that are not a multiple of the fundamental. The output THD+N for the voltage and current must be lower than 5 % regardless of the load.

- **Input ripple current and voltage:** Both the input voltage (after the $10\ \Omega$ resistor) and input current are measured to ensure that the output power ripple is not reflected in the input port. This 120 Hz ripple is defined as $\Delta I_{in}|_{120\text{ Hz}}/I_{in\text{ avg}}$ for the current and $\Delta V_{in}|_{120\text{ Hz}}/V_{in\text{ avg}}$ for the voltage. The input current ripple must be below 20 % for loads over 500 VA, and 250 mA peak to peak below that power. The input voltage ripple is specified to be below 3 %, although it is less stringent than the current ripple [5].
- **Electromagnetic compatibility:** The inverter must meet the Electromagnetic Compliance (EMC) standard *FCC Part 15 B for unintentional radiators* for conducted and radiated emissions [17]. Conducted emissions are measured on the AC side of the inverter. Conducted limits at different frequencies are shown in Figure 1.1 a). Both the average amplitude and the quasi-peak are measured. How it is measured is detailed later in Figure 1.5. The limits for radiated emissions are represented in Figure 1.1 b).
- **Grounding:** Galvanic isolation is not required; however, the output has to be grounded. Two grounding connections are allowed, namely: *240 V split phase configuration* where ground is connected to the midpoint of the output isolation transformer. Alternatively, *240 V to ground configuration*, where ground is connected to the neutral terminal. In other words, earth is connected either to one of the AC terminals, like in European and other households in the world, or to the midpoint, like in North America households.
- **Ground current limit:** The chassis of the inverter has to be grounded as well. The current flowing through the chassis connection, or the wire used to ground the output cannot be larger

Figure 1.1: Conducted and radiated limits specified in the standard *FCC Part 15 B* for *unintentional radiators* [17].

than 50 mA rms. As mentioned in the input voltage section, the common-mode current in the input supply caused by the parasitic capacitance to earth must be below 50 mA rms too.

- **Other requirements:** There are additional requirements that are not going to be detailed here and can be found in [8]. These requirements specify the wiring, additional connections, safety requirements or requirements related to undervoltage, overcurrent, or overtemperature.

Figure 1.2: Summary of the main specification of the LCB competition, [1].

The specifications from the above list are summarized in Figure 1.2 for clarity. From the list of specifications, some critical challenges can be identified. First, the volume, case temperature, and efficiency requirements are rigorous and closely related. Due to the volume limitation and the low temperature rise allowed, heat extraction is a major concern. Efforts are required to both reduce heat generation and improve heat extraction. By maximizing efficiency, the power dissipated is minimized, hence reducing temperature and heat-sinking requirements. Also, proper thermal management and packaging are critical factors for the design of the inverter. In this work, the thermal issue is mostly addressed by trying to obtain an inverter with extremely high efficiency, well above the 95 % specified. Aiming for low losses simplifies the thermal management problem and makes the inverter a better solution at the same time.

The 20 % input current ripple specification is a second challenge. Because of the difference between the input and the output power in single-stage inverters, a storage element has to handle

1.4. Single-phase inverters for photovoltaic applications

the difference in power. This important aspect is described in detail in Section 1.5, and it is one of the important differences between the studied inverter and the inverters proposed by other teams.

Additionally, limiting the ground current to 50 mA rms is a problem when considering topologies without galvanic isolation, as the one studied in this work. For the selected topology, a filter is needed to maintain the ground current below the specified value.

Maximizing efficiency, reducing EMI, maintaining a low input current ripple, and limiting the ground current are the challenges that make the topology selection and optimal modulation essential to comply with the specifications successfully.

1.4 Single-phase inverters for photovoltaic applications

This section describes the particularities of single-phase inverters for PV applications. In general, single-phase inverters find applications, in UPSs, renewable energy, home appliances, motor drives, and distributed grids, among others [18]. From a topology perspective, there are inverters designed as Voltage-Source Inverters (VSI) or as Current-Source Inverters (CSI). In this application, the DC voltage is nearly constant, therefore, only VSIs are considered hereafter.

Regarding the function of the inverter, two types can be considered, *Grid Forming* and *Grid Following* inverters [19]. Although topologies are the same in both cases, their functions and control structures are different. The objective of *Grid Following* inverters is to inject current to the grid with a high power factor, which is typically the case of grid-connected PV inverters. Therefore, this type of inverters usually employ Phase-Locked Loops (PLLs) and require zero-cross detection of the AC voltage to synchronize the output current with the grid voltage. Additional features sometimes found in these types of inverters are to provide reactive power or to maximize the power drawn from the PV panel through Maximum Power Point Tracking (MPPT). In contrast, *Grid Forming* inverters generate the sinusoidal voltage directly, instead of supplying current to the existing grid. Therefore, features as PLLs and zero-cross detection are not required. This type of operation is referred to as *autonomous operation mode* in [20] or *stand-alone mode* in [21]. In these inverters, the power provided depends on the load. As a result, the MPPT function cannot be implemented as the input power cannot be freely adjusted. For the LBC, a *Grid Forming* inverter has to be designed because one of the goals of the control of the inverter is to generate a 240 V rms output at 60 Hz. Therefore, the control in *Grid Following* inverters is not further detailed in this work; only the control for *Grid Forming* inverters is studied.

PV inverters can also be classified as isolated or nonisolated, also known as transformerless. There are two main aspects in favor of isolated topologies. First, with a transformer, the gain is easily adjusted by selecting the appropriate turn ratio of the transformer. These types of inverters are commonly used when the input voltage is low [22]. Second, the transformer provides galvanic isolation. Isolation can be achieved either by using line-frequency transformers or high-frequency transformers. In the first case, due to the low operation frequency, the transformer is usually bulky, lossy, and expensive [22]. When the transformer is a part of the inverter and works at switching frequency, the size and cost are considerably reduced [23]. Yet, the smallest, lightest,

most cost-effective, and most efficient solution often is to use transformerless topologies when it is possible [21], [24], [25], [26].

1.4.1 Transformerless inverters

As the objective of this work is to design an inverter with extremely low volume and the input and output voltages are in the same range, topologies with transformer are not considered, and they are not further discussed. The most widespread topology for transformerless inverters when the input voltage is higher than the output voltage is the Full Bridge [27], [28]. This topology and a few more common topologies for transformerless inverters are reviewed. This review is used for comparison and discussion of the solutions proposed by LBC participants. A list of four conventional inverters used in this competition is found below:

- **Full Bridge:** Also named H-Bridge. It is represented in Figure 1.3 a) with the inductor split in the two legs. A single inductor can be placed in either leg if desired. The Full-Bridge is the most popular solution because of its simplicity [29].

Several modulation schemes can be applied, the most common ones being the bipolar modulation and the unipolar modulation [24]. When bipolar modulation is applied, the operation is divided into two states. In the first state, Q_1 and Q_4 are closed. In the second state, Q_2 and Q_3 are closed. Therefore, in a switching cycle, the voltage applied to the inductor is $V_g - V_o$ and $-V_g - V_o$ respectively. With PWM modulation, the output voltage can be adjusted by controlling the duty cycle. With unipolar modulation, besides the two previous states, there are two additional states, with Q_1 and Q_2 closed or with Q_3 and Q_4 closed. Hence, the voltage in the inductor can also take the value $-V_o$ and the modulation has three levels [26]. The selection of the modulation leads to different inductor sizes. The volt-second applied to the inductor is lower in the case of unipolar modulation because of the additional level and because the effective frequency in the inductor is two times the switching frequency. This leads to a more compact and efficient design [30]. However, the unipolar modulation also leads to problems related to the leakage current as it is elaborated in Chapter 6.

- **Two buck converters:** Another common option is to use two separate buck converters to generate two voltages with a difference of V_o , as shown in Figure 1.3 b). A possible modulation is to keep constant the voltage of the midpoint of the load at $V_g/2$ with respect to the negative terminal of the input [31]. This topology is also based on the H-Bridge. In fact, in [31] it is called *symmetric* Full-Bridge.
- **Buck + unfold:** A different option is to use a buck converter to generate the rectified output voltage and then an unfolder to change the polarity of the output at line frequency. The function of the unfolder is equivalent to the diode bridge in a rectifier. Another alternative is to use just two switches for unfolding purposes, as depicted in Figure 1.3 d), one connected to the positive terminal of the input and the other to the negative terminal. This topology is called Full-Bridge with *hybrid modulation* in [30] and $DC/|AC| + \text{unfolder}$ in [31]. In [24], the modulation is called *single-phase chopping scheme*.

1.4. Single-phase inverters for photovoltaic applications

Figure 1.3: Common single-phase transformerless inverters. Q transistors operate at switching frequency while M transistors are switched at line frequency. a) Full-Bridge, b) two buck converters, c) Buck + 4-switch unfolded, d) Buck + 2-switch unfolded.

The selection of the inverter influences the design of the inductor and CM and DM filter. More advanced architectures can be found in [24], where examples of commercial topologies are given. In this short review, only topologies that fit the voltage specifications of LBC have been included ($V_{o\ peak} < V_g < 2 \cdot V_{o\ peak}$). Therefore, microinverters, with low input voltage [32] are not described, further information can be found in [23].

1.4.2 Leakage current and common mode filter

Due to the lack of isolation of transformerless inverters, leakage current or ground current is an important issue in PV systems [22]. PV panels have a considerable parasitic capacitance between their terminals and ground. This capacitance is connected between the input and output terminals of the inverter when the output of the inverter is grounded. Then, large variations on the CM voltage between input and output can generate large leakage current through this parasitic capacitance. This parasitic capacitance and the path of the leakage current is represented in Figure 1.4. The leakage current generates losses, harmonics injected to the grid, and conducted and radiated emissions [26]. Therefore, it is limited by different standards in the world. Hence, limiting the ground current is not only convenient but mandatory. This requirement implies that topologies and modulation should be selected carefully to avoid a varying CM voltage, or CM filters would be required to reduce the amplitude of this current. This issue is addressed in Chapter 6.

Regarding EMI considerations, Figure 1.5 shows how the noise is measured according to the LBC specifications. In the figure, the Line Impedance Stabilization Network (LISN) is shown [33]. Two options for the grounding of the inverter are included in dashed lines. In the LBC specification, a line transformer is used to isolate the output for testing purposes. Figure 1.5 shows

Figure 1.4: Leakage current, i_{lk} , induced in the PV parasitic capacitance by the CM voltage between the input and output ports, v_{cm} .

the different connections to ground, to give an idea of the different paths the leakage current and other ground currents can take. To limit conducted noise, DM and CM filters can be added. The design of the EMI filter is out of the objectives of the thesis, although a few comments are given in Chapter 6.

Figure 1.5: Connection of the LISN for EMI measurements, showing the different connection of the system to ground.

1.5 Power pulsation and storage capacitor

One major issue of inverters intended for PV applications, whether they are isolated or not, is the effect of the power pulsation on the input side. In PV applications, constant input power is convenient because AC components degrade the solar panel performance at maximum power. Due to the V-I curve, the solar panel would operate around the maximum power point if its voltage contains 120 Hz ripple, hence the total power supplied by the PV panel is decreased [34], [35], [36], [37]. In other words, to obtain the maximum power of a solar panel, its voltage and current must be constant. This problem not only affects solar panels, but it is also present in fuel cells, batteries chargers, and LED drivers applications [34]. This issue is caused by the difference between input and output power, not the direction of the power, nor the selected topology or modulation [38].

For an inverter with constant input power equal to the average output power, there is a difference between the input power and output power that can be easily obtained if a lossless

1.5. Power pulsation and storage capacitor

inverter is considered [38]. Let the output voltage be $V_o = V \sin(\omega_{line} \cdot t)$ and the output current be $I_o = I \sin(\omega_{line} \cdot t - \phi)$. The output power is then given by:

$$P_o = \frac{V \cdot I}{2} (\cos(\phi) - \cos(2 \cdot \omega_{line} \cdot t - \phi)) \quad (1.3)$$

If the inverter is considered lossless, $P_g = |P_o|$, then the input power is:

$$P_g = \frac{V \cdot I}{2} \cos(\phi) \quad (1.4)$$

As a result, the inverter must include a storage element or *buffer* to compensate for the twice line frequency ($2 \cdot \omega_{line}$) pulsation power, $P_s = P_o - P_g$. In this work, P_s is defined positive when the storage element supplies power to the load. P_s is negative when the storage element is charged from the input. With this definition, P_s is given by:

$$P_s = -\frac{V \cdot I}{2} \cos(2 \cdot \omega_{line} \cdot t - \phi) \quad (1.5)$$

Figure 1.6 shows the shape of P_s and the variables used in this analysis.

Figure 1.6: Power pulsation in single-phase inverters with constant input power including P_s , and the energy variation in the buffer, ΔE_s .

P_s is defined solely by the input and output power and defines the energy variation that the storage element has to handle. The energy stored or delivered in the storage element is given by:

$$\Delta E_s = \frac{V \cdot I}{2 \cdot \omega_{line}} \quad (1.6)$$

Therefore, the storage element is sized based on the apparent power and the line frequency of the output port [1], which is the shaded area in Figure 1.6. To illustrate the magnitude of this value, for an apparent power of 1 kVA at 60 Hz, the energy variation is $\Delta E_s \approx 2.65$ J.

This energy can be stored in inductors or capacitors. As the energy density is orders of magnitude higher in capacitors than in inductors, the former is typically employed for this purpose.

In this work, only the case of capacitive energy storage is analyzed. This capacitor is named *storage capacitor*, C_s , in this dissertation, although it can also be found as *decoupling capacitor* in the literature [23]. If a capacitor is used to decouple the input and output power, its voltage and current are defined by the following relations: $I_s = -C_s \cdot dV_s/dt$ and $V_s \cdot I_s = P_s$. The minus sign in the voltage-current relationship is added because P_s is defined positive when the current flows out of the capacitor. As a result, I_s is positive when the capacitor is being discharged. This nomenclature is employed to match our previously published work [16], [39], [40].

The solution of these equations is a function of the initial capacitor voltage, but, for convenience, it can be expressed in terms of the maximum voltage, V_{smax} . The solution for V_s considering the voltage positive is given by:

$$V_s = \sqrt{\frac{V \cdot I}{2 \cdot \omega_{line} \cdot C_s} (\sin(2 \cdot \omega_{line} \cdot t - \phi) - 1) + V_{smax}^2} \quad (1.7)$$

In this equation, V_{smax} is a degree of freedom. This analysis can be found in a variety of articles about energy decoupling such as [5],[35], [41], [42], [43], or [44]. For $V_s > 0$, the minimum voltage is reached at $2 \cdot \omega_{line} \cdot t - \phi = 3\pi/2$, defined as V_{smin} . Hence, the following relation is obtained for the value of the capacitor [29]:

$$\frac{V \cdot I}{\omega_{line} \cdot C_s} = V_{smax}^2 - V_{smin}^2 \quad (1.8)$$

The capacitance required for a given power can be calculated given the maximum and minimum voltage allowed in the storage capacitor from Equation 1.8. The minimum capacitance is obtained for $V_{smin} = 0$. In this case, the maximum energy in the capacitor is equal to ΔE_s [38], [42]. For instance, for 1 kVA and $V_{smax} = 400$ V, the minimum capacitance is 33.2 μ F.

The volume of the storage capacitor is usually proportional to its maximum energy, although this relation is not valid for all capacitor technologies, it is enough to give a reasonable idea of the capacitor size. From Equation 1.6, this maximum energy is given by:

$$E_{smax} = \frac{1}{2} \cdot C_s \cdot V_{smax}^2 = \Delta E_s \frac{V_{smax}^2}{V_{smax}^2 - V_{smin}^2} \quad (1.9)$$

The capacitance and maximum energy as a function of V_{smax} and the ratio $(V_{smax} - V_{smin})/V_{smax}$ are shown in Figure 1.7 for $\Delta E_s \approx 2.65$ J. The point for $V_{smax} = 400$ V and $V_{smin} = 0$ discussed before is marked with a red square on the top of the plots. As illustrated in this figure, the maximum energy is not a function of the maximum voltage but to the percentage of voltage swing. A very small voltage swing leads to extremely high energy requirements because most of the energy in C_s is not used for energy buffering.

To summarize this section, the key to size reduction of the capacitor is a high voltage swing [29], [45]. The question is how to design topologies that allow high voltage swing in C_s .

1.5. Power pulsation and storage capacitor

Figure 1.7: Contour plot for C_s and E_s as a function of V_{smax} and the percentage of voltage swing for 1 kVA and 60 Hz.

1.5.1 Architectures classified according to the position of the storage capacitor

This section discusses the possible configurations of the storage capacitor in the inverter. The arrangement of the storage capacitor has a considerable impact on the performance and control of the architecture. Architectures can be sorted based on how the power decoupling function is implemented [35]. This classification is helpful for introducing the origin of the topology investigated in this work. A high-level description is provided because discussing the specific details of each topology is not the goal of this section.

1.5.1.1 Traditional solution: large input capacitor

The classic solution to the power pulsation problem is to use a large input capacitor. It has to be sized so that the 120 Hz input voltage swing is small for the voltage and current in the solar panel to be nearly constant. This solution is shown in Figure 1.8 a), and it is sometimes referred to as a single-stage inverter [22]. The drawback is that the capacitor is bulky if the specifications for the 120 Hz voltage and current ripple are restrictive.

To illustrate how the limit in the voltage swing in the input voltage affects its size, the maximum energy in C_s can be obtained for 1 kVA and a 3 % ripple as specified for the LBC. For a 1 kVA the input can be modeled as a 450 V source in series with a 20 Ω resistor so the input voltage of the inverter at 1 kW is 400 V. In these conditions, the input capacitance calculated using Equation 1.8 and assuming that I_g is constant (which is a valid assumption as the allowed voltage ripple is just 12 V) is $C_s \approx 560 \mu\text{F}$. This capacitor has a maximum energy of $\approx 45 \text{ J}$ using $V_{smax} = 400 \text{ V}$, from which only 2.65 J are used for power decoupling purposes. In Figure 1.7 this design is marked as a red dot on the bottom of the plots.

Figure 1.8: Architectures classified according to the connection of the storage capacitor, a) passive solution with large input capacitor, b) cascaded configuration, c) parallel input active filter, d) single-stage solution.

For this C_s connected in the input, electrolytic capacitors are usually employed as they offer high energy density at reasonable low prices. However, one of the flaws of electrolytic capacitors is their low current ripple capability and short lifetime [41], [46], [47].

An advantage of passive solutions is simplicity. Since the power pulsation problem is solved passively, the objective of the power stage and control is solely to generate the output voltage. There are other passive solutions for power decoupling, but, in general, these solutions occupy a large volume and are not further investigated in this work [31].

1.5.1.2 Two-stage architectures

To reduce the size of the storage capacitor, a larger voltage swing should be allowed. Therefore, the storage capacitor should not be placed at the input port. This section describes the solutions based on two power stages, the inverter, and an additional converter with C_s in the output to allow higher voltage swing. Therefore, the additional stage controls the storage capacitor port.

Since a second stage is added, the control becomes more complex compared to passive solutions. Not only the output voltage has to be controlled, but constant input current must be achieved too. Additionally, V_s should be kept under the desired values. Hence, a storage capacitor voltage loop is usually implemented. Each stage serves a purpose, the inverter controls V_o and the additional stage controls V_s , while ensuring constant I_g . This concept is elaborated in Chapter 5.

Two-stage cascaded

A common architecture in this category is the two-stage cascaded converter composed of the DC-DC converter, that maintains the input ripple constant, and the inverter, that creates the sinusoidal output [32]. This architecture is shown in Figure 1.8 b). The purpose of the input DC-DC converter, besides maintaining the input current constant, is to adapt the input voltage

1.5. Power pulsation and storage capacitor

of the inverter. For the inverter, topologies as the ones reviewed in Section 1.4.1 can be used. The storage capacitor is also known as *DC-link capacitor* when placed between the stages. As the power of the DC-DC stage is P_g and the power of the inverter is P_o , the difference is handled by the storage capacitor as discussed in Section 1.5. The DC-DC stage can be either buck based, boost based, or buck-boost based, and the inverter usually requires a higher input voltage than the output voltage, which limits the range of V_s . The capacitor value can be decreased if a large voltage swing is allowed, however, this voltage is constrained by the selection of the DC-DC and inverter topologies [1].

A review of two-stage cascaded topologies where the first stage is used to boost the PV voltage can be found in [22]. Because two converters are cascaded, this architecture may not be attractive because the number of components is increased and the efficiency may be penalized, even though C_s is reduced. Nevertheless, for limited overall volume, the cascaded architecture is usually preferred over passive solutions.

Two-stage with active filter

Another type of two-stage solution is the combination of an inverter and an *active filter*. Active filters are converters to interface the storage capacitor only. In the literature, the active filter is sometimes referred to as *active power pulsation buffer* or *power decoupling circuit* among others. In [48], these converters are called *Active Power Decoupling stages*. These converters are named *active capacitive DC-links* in [49], and are subdivided in passive or active, DC-DC or DC-AC, and integrated or separated circuits. A complete review of the different types of active filters can be found in [34], where capacitive and inductive topologies based on buck, boost, or buck-boost converters are described. In [35] another extensive literature review can be found, in this paper architectures are classified according to the connection of the active filter to the input or output port, and as *series* or *parallel* converters. In [49], these architectures are classified according to how the storage element and the additional converter are connected.

The most common configuration is to connect the active filter to the input port. It can be either connected in series between the input port and the inverter or connected in the input in parallel with the inverter, as shown in Figure 1.8 c). This latter can be found in many of the designs proposed for the LBC. In the architecture of Figure 1.8 c), the inverter is chosen independently of the active filter. Since the DC-DC converter is designed for P_s only, the voltage swing in C_s is only constrained by the topology used as input active filter. Therefore, a wide voltage swing can be employed to decrease the size of the storage capacitor. However, designing converters to interface large voltage swings in the capacitor typically implies higher losses and volume compared to converters designed to work for a narrowly defined voltage. Not always the minimum capacitance leads to the best overall solution [21], [41].

To conclude this section, the advantage of two-stage active filters over two-stage cascaded solutions is that, in general, V_s is less constrained, and that higher efficiency can be achieved.

1.5.1.3 Single-stage inverters

Lately, there is a trend to integrate the active filter within the inverter. This solution is referred to as single-stage inverters as it uses a single stage for both output voltage regulation and to obtain

constant input current. In this architecture, a single power stage interfaces three ports, the input, output, and storage capacitor, as depicted in Figure 1.8 d). Unfortunately, the passive solution (Figure 1.8 a)) is sometimes named single-stage too. In this work, single-stage inverters refer to three-port solutions, where high voltage swing in the storage capacitor is allowed. As this is not a mature concept, different authors name this concept differently, for instance, in [50] it is called *integrated series pulsation buffer*, in [44] it is named *series-connected active buffer* and in [51] it is labeled *embedded pulsating power buffering*. The idea behind this solution is usually to reduce the component count by reusing common elements such as switches or inductors that can be shared between the active filter and the inverter. This idea can be used to generate new topologies as discussed in [49]. In [49] the possible connections of the storage capacitor in single-stage inverters are discussed, although the solution is called *integrated active DC-link*. These architectures are termed *dependent decoupling topologies* in [34].

Most topologies are designed by inspection, trying to find elements that can be shared between the inverter and active filter, usually switching legs and inductors. Examples of single-stage topologies can be found in [20], [21], [29], [52], or [53]. This concept can be applied to isolated topologies too and a review on this topic can be found in [23].

Yet, there are some topologies directly designed as single-stage inverter rather than the combination of active filter and inverter [49]. In [54], an inverter is proposed where the storage capacitor is connected to the positive rail of the input, with a voltage bigger than the input voltage. The output port is connected to the negative terminal of the input, and, as a result, there is no leakage current generated. With a small modification of the part of the converter that interfaces the input with the storage capacitor, the topology proposed in [55] is obtained. In [48] and [56], two similar boost type PFC single-phase are proposed with a flying capacitor replacing the boost converter, although the flying capacitor voltage is larger than the output voltage. The key feature of these last solutions is that the flying capacitor acts as the storage capacitor too.

The flying capacitor also acts as the storage capacitor in the topology investigated in this thesis. It should be noted that there is not a clear difference between those topologies designed as single-stage directly and those resulting from the integration of active filters and inverters.

Both two-stages and single-stages architectures are often represented as three-port systems (Figure 1.8 d)) to interface the input, output, and storage capacitor [32]. However, it should be noted that the concepts of *three-port systems* and a *three-port power stage* are different. The former refers to any system where three different ports can be identified, regardless of the number of power stages. For instance, two-stage inverters can be considered three-port systems [38]. The latter is only applicable when a single-stage is used. With this definition, the solution with a large input capacitor described at the beginning of this section is considered a two-port solution.

In general, in three-port systems, there are two control variables, independently of the number of power stages used. Then, one of the three ports is not controlled but it is the result of the power balance: $P_g + P_s = P_o$ [43]. The modulation in single-stage inverters with a single power stage is usually complex because some components have dual purposes: output voltage regulation and power decoupling [34]. Further details regarding the control of single-stage three-port inverters are given in Chapter 5.

1.6. Solutions proposed for the LBC

Single-stage architectures have the advantage of reduced storage capacitor size as in two-stage converters, and, additionally, a reduced number of components. This, in turn, can lead to lower cost, higher power density, and higher efficiency.

1.5.2 Three-port converters in the literature

This section includes a brief discussion of the general aspect of three-port systems. It should be clarified that the applications of three-port systems are not restricted to inverters only. There is a wide variety of DC-DC applications for three-port systems too.

In general, these DC-DC converters are useful when the power demanded by the load does not match the power generated, and additional storage, such as a battery, is needed. *Multi-port* converters find applications in hybrid vehicles for regenerative braking, fuel-cells and battery systems, aerospace power systems, PV with battery backup among others [57], [58]. These DC-DC converters can be classified in isolated or non-isolated [58], [59]. For instance, three-port DC-DC converters are proposed in [57], [58], [59] and [60] to interface a PV panel, a DC load, and a battery.

In [59], the advantages and defects of multi-port conversion are stated clearly: in general, they feature lower weight, more compact packaging, lower cost, and improved reliability. However, in multi-port converters, the number of control variables is equal to the number of ports minus one, which results in a more complex control scheme. Moreover, when the same power stage is shared, proper decoupling of the control loops is required so variations in one variable do not affect the other [60]. The coupling of control variables gets intricate as more devices are shared for more than one purpose. Note that a *three-port converter* refers to converters where two ports can be controlled independently in this work. For instance, a Flyback with two outputs is not considered a three-port converter.

1.6 Solutions proposed for the LBC

Different architectures were proposed in the LBC to achieve the highest power density possible while complying with the specifications. Some solutions proposed by the finalists are qualitatively described in this section. The review includes the power stage used as inverter and how the power pulsation and leakage current were addressed. Other aspects as the thermal management, component selection, or the achieved efficiency or power density are out of the scope of this short review. These aspects can be found in [11] and [31]. The goal of this section is to present the state of the art at the time of the competition. It will be helpful in the following chapters to highlight the differences in the solutions from different participants compared with the one studied in this work.

Some of the finalists have published articles regarding their work for the LBC competition, unfortunately, this is not the general case. The author has not been able to find any published work for some of the finalists: *AHED*, *AMR*, *Cambridge Active Magnetics*, *Energylayer*, *OKE-Services*, *Rompower*, *Tommasi - Bailly*, and *Venderbosch*. Moreover, three teams dropped out of the competition before testing: *Adiabatic Logic*, *Helios*, and *LBC1*. Therefore, only the work of seven out of the eighteen finalists is summarized here.

The team that won the competition is *Red Electrical Devils* from CE+T. Their solution is a two-stage converter with a parallel input active filter for power decoupling [61]. Their input active filter is a buck converter supplied from the input (Figure 1.8 c)) with the negative terminal of the storage capacitor connected to the negative terminal of the input. Ceramic capacitors are used for the storage capacitor, and a large voltage swing (from 200 V to 400 V) is allowed, leading to a very low volume. For the inverter stage, a Full-Bridge with two interleaved legs per bridge is used. A special phase-shift modulation with variable switching frequency is used to minimize the total size and losses of the inductor and the choke. Because of the phase-shift modulation, a large CM voltage at switching frequency is present. This CM voltage is filtered with a choke to avoid large leakage currents. The input active filter and the inverter are operated in Triangular Conduction Mode (TMC). With it, the inductor current is positive and negative in a switching cycle and ZVS can be achieved in all transitions. TCM is explained in detail in Chapter 2 as it is used for the modulation of the inverter studied in this work.

The second place was for the *Schneider Electric Team*. They proposed a two-stage solution based on an inverter and input active filter too. However, in their case, the input active filter is connected in series with the input. The inverter is a Full-Bridge with PWM modulation and SiC devices hard-switching at 45 kHz [18]. The PWM modulation generates high frequency CM voltage that has to be filtered to meet the specifications for the leakage current. In [5], the active filter used by this team is compared with the one used by the winners.

The *Future Energy Electronics Center* team from Virginia Tech finished third. They selected a two-stage cascaded solution [62], [63]. The first stage is a buck converter, and the DC-link capacitor is used as the storage capacitor to reduce the size of the input filter. For the inverter, an interleaved buck converter with two switches for unfolding purposes is used (Figure 1.3 d)). As a result, there is no high frequency leakage problem. It should be mentioned that according to [11], in their technical approach a HERIC inverter was selected.

The team *Fraunhofer IISB* proposed a two-stage solution with a parallel input active filter based on a buck converter. The storage capacitor voltage ranged from 190 V to 380 V [64]. Two buck converters are used for the inverter (Figure 1.3 b)). The switching frequency is 140 kHz and the buck converters are modulated so that the midpoint of the load is at $V_g/2$ with respect to the negative terminal of the input. By phase-shifting each leg, the effective frequency of the filter is 280 kHz so its size can be reduced.

The only finalist that used a passive solution for power decoupling was the *University of Tennessee*. Instead of a large input capacitor, they used a resonant circuit formed by the storage capacitor and an inductor [65]. The inverter is a hard-switched Full-Bridge with unipolar modulation. Therefore, the switching frequency is doubled for the DM filter, and lower voltage is applied to the inductor, a large CM filter is required to filter the CM voltage at switching frequency.

The *UIUC Pilawa Group* proposed a two-stage architecture with extremely high power density. It is based on an active filter connected in series with the input capacitor, similar to the passive filter but the converter together with the storage capacitor act as an active inductor [66]. The inverter is a *7-Level Flying Capacitor* switching at 120 kHz and then a 4-switch unfolded. The multilevel

1.7. CEI@UPM single-stage inverter

converter reduces the inductor size considerably as the effective frequency in the inductor is 720 kHz [67].

Finally, the team *Inverter* from ETH also proposed a two-stage with input active filter solution. As the winners, for power decoupling, they used a parallel input active filter buck converter operated in TCM with variable switching frequency (200 kHz to 1 MHz) [42]. For the inverter, a structure composed of two buck converters, as in Figure 1.3 b) but with two interleaved stages per buck is used [31]. The modulation ensures a constant CM voltage of $V_g/2$, hence no leakage current is present [68]. They selected this architecture because when the LBC began because the specification for leakage current was 5 mA rms. It was only months later, when they had already designed the inverter, that the specification was relaxed to 50 mA rms. In [68] it is found that a buck converter with a 4-switch unfolded is a better solution if the maximum leakage current is specified at 50 mA rms.

As mentioned in Section 1.1.1, most teams used GaN semiconductors. These devices switch much faster than their Si counterparts because of their lower $\sqrt{R_{ds(on)} \cdot C_{gd}}$ [52]. Even for applications with Zero-Voltage Switching (ZVS), GaN devices are better. They feature a much lower $\sqrt{R_{ds(on)} \cdot C_{oss}}$ for a given breakdown voltage compared to Si or SiC devices [69]. ZVS is described in detail in Chapter 3.

For the leakage current issue, the solution adopted was either to select topologies with inherent no-generation of CM voltage at high frequency or to include filters to mitigate the leakage current if the topologies or modulation generates high frequency CM voltage.

Regarding the power pulsation, it can be concluded that most teams used input active filters for the power decoupling. It proves that a large voltage swing in C_s is desirable. At the time of this competition, three-port single-stage transformerless inverters were an emerging concept, and to the author's knowledge, only the *CEI@UPM* team proposed one [13]. It is the objective of this research line to prove if the single-stage inverter studied in this work is a great candidate compared to two-stage solutions.

1.7 CEI@UPM single-stage inverter

The topology studied in this work was first introduced by Prof. José A. Cobos in 2015 for the LBC competition. The architecture was designed to minimize the inductor size and losses by taking advantage of the integration of the storage capacitor and the inverter in a single power stage. This topology has a single inductor used to control that the storage capacitor performs the power decoupling function, and, at the same time, to generate the sinusoidal output voltage.

In this section, the inverter is introduced, together with the main ideas behind its modulation and control. The explanation begins with the metric used to synthesize the topology.

1.7.1 *Indirect and differential power*

A comparison between architectures was the first step to find a topology suitable for this competition. To do a high-level comparison of inverters, a metric was needed. The nominal power of the different stages is sometimes used to compare architectures. However, to optimize

volume and losses it is found not to be a reliable metric. Instead, the comparison was carried out using the *differential power*, P_{diff} [16].

This paragraph illustrates the problem of using nominal power as a rough estimate for efficiency and volume in a converter. It is a common misconception to think that a converter with a nominal power two times higher than the other will have either higher volume or losses or both. This is not always the case. Consider two buck converters with the same input power, input voltage, inductance, switching frequency, and, in both cases, operated at Continuous Conduction Mode (CCM), stepping down the voltage to 1/4 and 3/4 respectively. The volt-second applied to the inductor when the gain is 1/4 and 3/4 is the same, but the inductor current in the case of 1/4 gain is three times higher, leading to a worse design. Even if the input power of the buck with the 3/4 gain is doubled, it may still have a smaller inductor compared with the original solution with 1/4 gain. The bottom-line of this discussion is that input or output power is not reliable when it comes to the comparison of passive components, as gain has an important impact too.

A usual argument to claim that the two-stage cascaded solutions are worse in terms of volume and losses than inverters with input active filters is that the first stage of the cascaded converter has to be rated to P_g , whereas the input active filter is only rated to $P_g - P_o$. This can be misleading because nominal power is not the only important metric, the gain of the stages should also be considered as discussed previously.

Opposite to the nominal power, the *differential power* accounts for the effect of the gain as well as nominal power. Hence, it is a better metric when it comes to system-level comparison of architectures in terms of volume and losses of passive components.

Prof. J. A. Cobos defined P_{diff} in [70] as the theoretical minimum power that has to be processed by reactive components in converters. In this context, *power processed* is defined as the power stored or delivered by reactive components in a switching cycle. The power processed is termed indirect power, P_{ind} in [13]. It is defined later.

The differential power can be calculated directly from the nominal power and the voltage gain of the power stage, as described in [13]. For a two port converter, it is:

$$P_{diff} = P \cdot \max\left(\frac{G_v - 1}{G_v}, \frac{G_i - 1}{G_i}\right) \quad (1.10)$$

Where P is the input or output power assuming a lossless converter, G_v is voltage gain, $|V_o|/|V_g|$, and G_i is the current gain, $|I_o|/|I_g|$ [71].

The idea is that architectures with reduced P_{diff} may lead to more efficient and power-dense designs. Comparing architectures based on this metric instead of nominal power helps to understand why a higher gain typically leads to more bulky or lossy designs. This concept is also helpful to understand misconceptions when it comes to the concept of *partial power processing* [72].

Calculating P_{diff} in three-port systems is not straightforward. It depends on the instantaneous voltage and power of the three ports. To obtain the equations the port variables can be represented as *Volt-Amp* areas where P_{diff} is the area that is not shared among ports [70]. Moreover, in inverters, as the voltage and current of the ports change along the line cycle, the value of P_{diff}

1.7. CEI@UPM single-stage inverter

changes depending on the instant of time along the line cycle. In three ports systems, different equations may be required to obtain P_{diff} depending on the point of the line cycle studied [70].

In [16] P_{diff} is used to compare the two-stage cascaded, the two-stage input active filter, and the single-stage three-port architecture for different storage capacitor values and voltages. It shows that the latter achieves the minimum P_{diff} of all possible architectures. The differential power is reduced roughly by half with a single-stage inverter. Therefore, a considerable impact in volume and losses is expected when the correct single-stage inverter is used. This is why the *CEI@UPM* team opted for a single-stage solution.

Nevertheless, to understand P_{diff} , the concept of power processed, or *indirect power*, should be clearly defined. The indirect power in any reactive component is defined as:

$$P_{ind} = \frac{1}{2 \cdot T} \int_0^T |v(t) \cdot i(t)| dt \quad (1.11)$$

For transformers, v and i can be either the primary or secondary current and voltage. The total indirect power in all capacitors, inductors, and transformers in a converter is always equal or above the *differential power* [70]:

$$\sum P_{indL} + \sum P_{indC} + \sum P_{indT} \geq P_{diff} \quad (1.12)$$

P_{ind} gives insight into the fundamental operation of reactive components in a topology. The indirect power in the inductor is considered a limiting factor compared to the indirect power in capacitors as the energy density is much higher in capacitors than in inductors. Unless several capacitors are used for power processing (as in multilevel converters), P_{indL} should be minimized. P_{indL} is independent of switching frequency, or inductance value (which depend on optimization results), therefore, it can be obtained directly given the port values and modulation.

Note that the storage capacitor is considered as one of the three ports and its size is determined by the power it has to buffer, not its indirect power. For the design of the architecture, the topology and modulation that minimized P_{indL} were selected. This process is discussed in the following section.

It should be noted that this metric is not supposed to substitute an optimization process for the design, but it is complementary. The topology and modulation can be selected based on this metric, and then optimization is required comprising all the different elements, from active elements (MOSFETs, IGBTs, diodes), capacitors, EMI filter, and even auxiliary circuits, not only the inductor, to minimize the volume and losses. Then, the modulation or topology can be modified to try to obtain better results. Minimizing P_{indL} gives a good starting point for the topology selection. To summarize, P_{indL} was used to design the topology and its modulation as it is a simple metric containing the fundamental information on how the power is processed. Of course, further optimization is required to validate the effectiveness of solutions proposed based on this method.

1.7.2 Synthesis of the topology

To design a topology with minimum P_{indL} , first, the minimum P_{indL} possible was obtained, which is P_{diff} . Then, the topology was selected based on equivalent circuits for different sectors of the line cycle. Here, only a summary is given, for further clarification of the concept mentioned below and a detailed description refer to [13].

As mentioned before, P_{diff} is defined by different equations depending on the voltage and current of the ports for three-port inverters. These equations are different for different sectors of the line cycle. For each one of these sectors with different P_{diff} equations, an equivalent circuit where $P_{indL} = P_{diff}$ was proposed, those equivalent circuits can be found in [13]. These equivalent circuits use power sources to represent the indirect and direct power and are labeled *continuous power model* [70]. These circuits with equivalent power sources were then represented as DC-DC converters with a single inductor. Then, for each sector of the line cycle, there was an equivalent DC-DC converter with a single inductor where the inductor processed the differential power. The last part of the process was to combine each equivalent DC-DC converter into a single DC-AC converter that could operate as each of them depending on the current and voltage in the ports. Along this *synthesis* process, some modifications were necessary to reduce the number of switches, and limitations such as ZVS were considered too. Therefore, the resulting topology is not directly a combination of the equivalent DC-DC circuits. As acknowledged in [16], there are regions along the line cycle where the storage capacitor can be used as a flying capacitor, thus making $P_{indL} < P_{diff}$ at the expense of higher P_{indC} in the storage capacitor port. Those cases are not considered when the methodology for synthesis briefly described above is followed but came later. For a complete explanation of the synthesis of this inverter, please refer to [13] and [70].

1.7.3 Selected single-stage inverter

The result of this synthesis is the topology depicted in Figure 1.9. The power stage requires just six switches and a single inductor to interface the input, output, and storage capacitor. Moreover, the storage capacitor acts as flying capacitor in some sectors of the line cycle. Since the inverter is designed as the combination of different equivalent circuits, its operation is divided into what is termed *operation modes*. Each operation mode is applied in a different sector of the line cycle and is defined as a sequence of *switching states*. Switching states define the connection of the inductor to the ports, obtained by turning on and off certain switches. These concepts are illustrated in Figure 1.9 for clarity.

It should be clarified that operation modes did not follow directly from the equivalent circuits that were used to synthesize the topology. Some equivalent circuits could not be implemented and operation modes that performed the same functions as these circuits were proposed by Prof. J. A. Cobos to synthesize an inverter with just six switches and a single inductor, without increasing P_{indL} in the process.

Operation modes were designed to achieve ZVS in all the transitions between switching states. For such purpose, only certain combinations of switching states are possible. To obtain ZVS in the transitions when the current in the inductor was near zero, switching states were extended so

Figure 1.9: Studied inverter and representation of the concept of multimode modulation.

their current was enough for ZVS, or additional states were added if the previous solution was not sufficient. A detailed explanation of how much current in the inductor is required for ZVS given in Chapter 3 as it is important to describe the general solution proposed for ZVS given in Chapter 4.

For the modulation, two types of operation modes were considered, both operating in Boundary Conduction Mode (BCM): *trapezoidal* modes, that are the combination of three states with either positive or negative inductor current, and *triangular* modes, with two states with positive current and two states with negative current (in Figure 1.9 the first two operation modes are trapezoidal and the last one triangular). As mentioned earlier, depending on the voltage and current of the ports, a different operation mode is used, leading to the concept of *multimode* modulation. The operation modes used prior to this work were described in [39]. As a continuation of the work in [39], in this dissertation, a complete analysis of the possible operation modes is provided. From this analysis, a few new operation modes are proposed to allow the inverter to operate seamlessly and in the whole voltage and current range of the three ports. This analysis is covered in Chapters 2 and 4.

One important design parameter that shaped the modulation was the selection of the storage capacitor value and voltage swing. As discussed in Section 1.5.1.2, the voltage swing of the storage capacitor impacts the power stage performance. For low values of V_s , I_s can take large values. Therefore, solutions with high voltage swing are less attractive. In general, it is accepted that

converter working under a wide range of voltages and currents are generally less efficient than those designed for precise operation points. Therefore, a relatively low voltage swing is preferred from the power stage standpoint. The optimum capacitance is not the value that attains the lower volume in the storage capacitor, but the one that minimizes the size and losses of both the storage capacitor and the inverter.

The optimum storage capacitor swing was found to be around 30 %, which led to $C_s = 70 \text{ } \mu\text{F/kVA}$ [13]. However, to allow some margins for the control in the event of a load step, the value was increased to $90 \text{ } \mu\text{F/kVA}$ and a voltage ranging from $V_{smin} = 295 \text{ V}$ to $V_{smax} = 380 \text{ V}$ in steady state at maximum load. Figure 1.10 shows the power, voltage, and current of the three ports with the design mentioned above for the storage capacitor for 1 kVA and $PF = 1$. For comparison purposes, this value is also shown in the contour plots in Figure 1.7 as a black dot. Throughout this thesis, the storage capacitor port has a value of $90 \text{ } \mu\text{F}$ and an average voltage of 340 V . Further analysis of which is the exact capacitance value and voltage swing that minimizes volume and losses would require an extensive and detailed optimization process that is out of the scope of this work.

Figure 1.10: Port variables for 1 kVA resistive load with $C_s = 90 \text{ } \mu\text{F}$.

Not only the modulation is complex, but the control of the inverter is difficult too. The control of the inverter has been investigated in detail by Regina Ramos. The inverter uses two voltage loops to control V_o and V_s , two inner current loops to control I_g and I_o , and a decoupling stage. A technique called *plant-inversion* was applied to decouple the loops. A summary of the control strategy is included in Chapter 5. For a more detailed explanation refer to [40], [73], and [74]. The *plant-inversion*, also named *inversion-based control* in this work, is used to translate the target I_g and I_o into the time each switching state has to last and the operation mode that should be used for each point of the line cycle. Chapter 5 explains in detail the proposed equations for the *inversion-based control* to account when the modulation for ZVS is considered.

Several students participated in the development of this research project and defended their degree's thesis and master's thesis in 2015 and 2016. First, in "*Inversor de alta densidad de potencia y bajo rizado de corriente de entrada*" from Helena Cristóbal Losada, the optimization of the topology and the design of the inductor were explained. In "*Control de una nueva topología de inversor de potencia con dispositivos GaN y técnicas de conmutación suave (ZVS)*" from Víctor

1.8. Specific objectives of the thesis

Cordón García, the earlier modulation and ZVS transitions and the implementation of the first prototype were covered. In "*Inversor de 2kVA de alta densidad de potencia y control en espacio de estados*" from Iñigo Zubitur Sasturain, the design of the drivers together with the description of the operation modes to minimize P_{indL} were explained. Finally, María Regina Ramos Hortal described the control of the inverter in detail in "*Control de un inversor de potencia diseñado para la competición The Little Box Challenge*". Citations to these works are not added in the bibliography as the documents are not available online.

1.8 Specific objectives of the thesis

This thesis continues with the work that the *CEI@UPM* team started, with specific goals different from the initial objective of the research line. The general objective is to obtain a small inverter complying with the LBC specifications. To do so, the first thing required is to be able to implement such inverter and modulation. This is the goal of the dissertation: to analyze the details required to implement this complex three-port single-stage inverter, which presents several challenges compared to traditional inverters. The operation is different from any conventional inverter because several operation modes are used and because the modulation has two control variables. Most of the dissertation is dedicated to the modulation, where soft-switching plays an important role. A detailed analysis of ZVS transitions is developed, and a modification of the modulation is proposed to address several practical issues. Modifications to the *plant-inversion* and its implementation in an FPGA are also discussed in this work. Nevertheless, the details of the control loops are out of the scope of this thesis, further information will be available in the Ph.D. dissertation of Regina Ramos to be presented this year. A downside of this topology is the CM voltage between the input and ground, which generates large leakage current because of the parasitic capacitance of the PV panel. Hence, a filter is needed to comply with the 50 mA rms limitation. The design considerations for this filter are also described in this work. The proposed modulation is validated experimentally, for such purpose, a 1 kVA prototype is designed and built. A future line is to have two inverters of 1 kVA working in parallel to meet the 2 kVA target. A brief discussion on this topic is given in Chapter 6. As the prototype is built for half the nominal power of the LBC specifications, for the rest of the work the input port is modeled as a 20 Ω resistor in series with the 450 V voltage source, instead of 10 Ω , so the input voltage range is defined between 400 V and 450 V depending on the load is not modified. To summarize: **the objective of this thesis is to analyze, implement, and validate a modulation that can operate this inverter properly.** This work will enable the future optimization and integration of the inverter in a little box.

1.9 Conclusion

In this chapter, a review of the design considerations of single-phase inverters for *grid forming* PV applications is provided, namely the leakage current and power pulsation issues. A literature review of the possible solutions for the power pulsation at a high level is provided, highlighting

the advantages of single-stage inverters and introducing the concept of three-port systems. Then, different solutions proposed by several finalists for the LBC have been reviewed to show the state of the art in 2015. The chapter ends with a short description of the topology proposed by the *CEI@UPM* team for this competition. The topology was proposed aiming to reduce the number of components and the size and volume of the inductor, by taking advantage of the integration of the storage capacitor.

Since the proposed inverter is an original idea of prof. J. A. Cobos for the LBC competition, there is no available literature of this specific topology other than the one generated by the *CEI@UPM* research group. Some topologies resemble the one analyzed here. Those are flying-capacitor based architectures where the flying capacitor works as the storage capacitor. For instance, in [50], a cell formed by a flying capacitor and four semiconductors is placed in series with the inductor in a buck-boost rectifier. This PFC rectifier can operate in buck or boost mode transitioning seamlessly between the two modes. In [44], the same structure formed by the storage capacitor and four switches is added in series with the output inductor in a current-source inverter. This inverter has two operation modes to charge and discharge the storage capacitor. Another similar architecture is proposed in [51], this one is a buck rectifier where the buck stage is replaced with a flying capacitor stage used for power decoupling purposes too. In this architecture, the output voltage can be controlled even when the rectified voltage is below V_o thanks to the flying capacitor. CCM operation divided into two operation modes is used, depending on the power direction of the storage capacitor port. The same authors proposed a similar architecture but based on buck-boost in [75]. In [45], a buck type PFC rectifier is proposed, where a flying-capacitor based structure replaces the buck. Note that not all these architectures are valid for the voltage specified in the LBC, nor the main goal is the reduction of the inductor size.

The number of publications on three-port systems and the trend to integrate the active filter and inverter has been increasing over the last few years, mostly after the LBC competition. Finally, the objective of this thesis is to propose a modulation and to study the details to solve the problems associated with this topology and the previous modulation, to enable the experimental validation of the concept.

Indirect power applied to the single-stage inverter

A systematic approach to derive the modulation of the analyzed single-stage inverter is described in this chapter. The modulation that minimizes the indirect power in the inductor along the line cycle is employed, following the methodology proposed in [16]. The analysis is included in the thesis as it is helpful to understand how the modulation was proposed and to show how the new operation modes are obtained. A script in *Matlab* is used to obtain the indirect power for all possible operation modes in different sectors of the line cycle.

The analysis of this chapter is restricted to nominal power, and a storage capacitor of 90 μF with an average voltage of 340 V. Therefore, the values of the current and voltage in the three ports of Figure 1.10 are considered. The analysis is completed in Chapter 4, including different loads, once the restrictions of ZVS are considered.

Nevertheless, before the analysis is applied to the inverter, the physical meaning of the indirect power is discussed since it is not a concept commonly employed to design converters, and it has played a very important role in this research line. The calculation of P_{indL} in a couple of three-port DC-DC converters and the Full-Bridge with unipolar and bipolar modulation are included to clarify the concept.

This chapter is structured as follows. First, the indirect power for different inductor current waveform is discussed, to understand what it represents. Then, to become familiar with P_{indL} , this concept is applied to more common inverters and three-port DC-DC converters. It is then applied to this single-stage inverter, leading to the modulation with minimum power is processed in the inductor.

2.1 Indirect power in the inductor as a high-level metric

The indirect power is a measure of how much power is stored or delivered in a reactive component, as described in Equation 1.11. It is defined for steady-state conditions where the average power in the reactive component is zero. Since the integral of the absolute value of power is just the sum of the variations of energy Equation 1.11 can be elaborated as:

$$P_{ind} = \frac{1}{2 \cdot T} \int_0^T |p(t)| dt = \frac{1}{2 \cdot T} \sum_{i=1}^{N^o \text{ of increments}} |\Delta E_i| \quad (2.1)$$

Therefore, the indirect power is also a measure of the variations of energy in the reactive components over the switching period. Given the voltage and current in the reactive element, the indirect power can be obtained with Equation 1.11. Equation 1.11 is repeated here for inductors as it is used throughout the analysis.

$$P_{indL} = \frac{1}{2 \cdot T} \int_0^T |v_L(t) \cdot i_L(t)| dt \quad (2.2)$$

The equation can be simplified in converters where the voltage applied to the inductor is constant, V_i , in each switching state. Switching states are named *states* for simplicity in this analysis. This is the case of converters whose operation is not based on the resonance of capacitors and inductors, i.e., inductor-based converter. Equation 2.2 for a constant voltage for the different states is:

$$P_{indL} = \frac{1}{2 \cdot T} \sum_{i=1}^{N^o \text{ of states}} |V_i| \int_{T_{i-1}}^{T_i} |i_L(t)| dt \quad (2.3)$$

Where T_{i-1} is the time when the i^{th} state starts and T_i when it ends. Moreover, if the direction of the inductor current does not change during the switching state, the integral of the absolute value of the current is just the average current in that state. Then, the indirect power is just the sum of the voltage times the average current times the duty cycle of each switching state.

Equation 2.2 can be expressed in terms of the volt-seconds in the inductor, VS_L . The volt-seconds in the inductor in this work are defined as the positive or negative area under the $v_L(t)$ function since the average $v_L(t)$ is zero in a switching cycle:

$$VS_L = \frac{1}{2} \int_0^T |v_L(t)| dt \quad (2.4)$$

If the average current in the inductor in all states is the same, then, Equation 2.2 becomes:

$$\text{if } \int_{T_{i-1}}^{T_i} i_L(t) dt = I_L \text{ for any } i \rightarrow P_{indL} = \frac{I_L \cdot VS_L}{T} \quad (2.5)$$

Although this equation is not always valid, it is helpful to give an idea of the meaning of P_{indL} for most converters. With the previous considerations, if an inductor with a given indirect power is compared to one with higher indirect power, the latter has either higher current, higher volt-seconds applied, or higher frequency. Then, selecting topologies and modulations that minimize the indirect power can help reducing the inductor size and losses.

To find a more general equation for P_{indL} that does not require that the inductor current is the same in different states, the *current in a state*, I_i , is defined. The inductor current in a state is defined as the average current over the whole switching cycle, not over the time the switching state lasts, to avoid including the duty cycle in the equation for P_{indL} . Therefore, the "information" about the duty cycle is already included in the definition of *current in the state*:

$$I_i = \frac{1}{T} \int_{T_{i-1}}^{T_i} i_L(t) dt \quad (2.6)$$

2.1. Indirect power in the inductor as a high-level metric

This current can be usually calculated directly from the current in the different ports. Therefore, the duty cycle is not even required to obtain these currents in general. Moreover, with this definition, the average inductor current directly is:

$$I_L = \sum_{i=1}^{N^o \text{ of states}} I_i \quad (2.7)$$

This concept is clarified with the examples given in the following section. Using this definition, P_{indL} can be written as:

$$P_{indL} = \frac{1}{2} \sum_{i=1}^{N^o \text{ of states}} |V_i \cdot I_i| \quad (2.8)$$

Furthermore, as the average power in the inductor is zero, and the same power is stored and delivered in a switching cycle, either can be used to calculate P_{indL} :

$$P_{indL} = \sum_{i=1}^{N^o \text{ of states}} \max(V_i \cdot I_i; 0) = \sum_{i=1}^{N^o \text{ of states}} \max(-V_i \cdot I_i; 0) \quad (2.9)$$

2.1.1 Indirect power applied to DC-DC two-port converters

Before P_{indL} is calculated in three-port systems, the concept is applied to two-port systems, in this case, a buck converter in CCM. The operation of the buck converter is briefly described here only to clarify the definition of the variables used to obtain P_{indL} . V_g and I_g stand for the input voltage and current, respectively, and V_o and I_o for the output. The operation is divided into two states. In the first one, the voltage in the inductor is $V_1 = V_g - V_o$, and in the second state is $V_2 = -V_o$. The average current over the whole switching cycle in the first state is $I_1 = I_g$. As the average inductor current is $I_L = I_1 + I_2 = I_o$, the current of the second state is $I_2 = I_o - I_g$. I_1 and I_2 are easily obtained without solving Equation 2.6, this is why this definition of the current in the states is preferred. Then, the indirect power is calculated using Equation 2.9, $P_{indL} = V_1 \cdot I_1 = -V_2 \cdot I_2$, leading to:

$$P_{indL} = P \cdot \left(1 - \frac{V_o}{V_g}\right) \quad (2.10)$$

Where $P = P_g = P_o$ considering a lossless converter. As mentioned in [76], when $d = V_o/V_g$ is large, the energy stored and released in the inductor is low, which is a well-known fact. A remarkable feature of P_{indL} is that it is not a function of the inductance value or switching frequency, only the variables of the input and output ports. As mentioned in [77], to accomplish step-down DC-DC conversion with the minimum amount of *AC power* (or P_{ind}) requires the use of buck converters. The reason is that $P_{indL} = P_{diff}$, as it can be checked by comparing Equations 2.10 and 1.12.

To show how this metric can be used to compare the inductor in different topologies, the buck converter can be compared with the buck-boost converter in terms of P_{indL} . In the buck-boost converter, the voltage in the first state is $V_1 = V_g$ and the current is $I_1 = I_g$, in the second state,

they are $V_2 = -V_o$ and $I_2 = I_o$. Then, from Equation 2.9 $P_{indL} = V_g \cdot I_g = P$. For the same V_g , I_g , V_o , and I_o as for the buck converter described before, P_{indL} in the buck-boost converter is always bigger than in the buck converter (Equation 2.10). The result is expected, it is widely accepted that the buck-boost converter has higher volume/losses in the inductor compared to the inductor in a buck converter for the same specifications. This brief comparison shows that the differences in performance in the inductor are reflected in the value of P_{indL} .

Equation 2.10 was obtained assuming that the buck converter operated in CCM, although the same result would have been obtained if other types of waveform were considered, such as Discontinuous Conduction Mode (DCM) or Boundary (or Critical) Conduction Mode (BCM). However, in Triangular Conduction Mode (TCM), the current in the inductor is negative in a part of the switching cycle. Therefore, Equation 2.10 is no longer valid as the direction of the current changes in the two states. To clarify the meaning of P_{indL} when different waveforms are considered, these four types of waveforms are shown in Figure 2.1 for the same conditions. The voltage, current, power, and energy waveforms for the inductor are shown. In this plot V_1 , V_2 , I_1 , and I_2 are also included. TCM results in higher P_{indL} compared with the other types of waveforms, higher the more negative the negative current peak is. Since the inductor gives some energy back to the input when the current is negative in the first state, more energy has to be stored in the inductor for the same total input power. The same happens with the output energy: when the current in the inductor is negative, the inductor is retrieving energy from the output port. In Figure 2.1, the instantaneous inductor power is shown, including its absolute value and the average of the positive or negative part, which is defined as P_{indL} . A remarkable property of P_{indL} is that it is independent of the number of switching cycles used to calculate it.

Figure 2.1: Common inductor waveforms in CCM, BCM, DCM, and TCM. The indirect power and its relationship with the energy in the inductor is included.

It should be noted that the indirect power is not related to the maximum energy in the inductor, E_L , but with its variations, ΔE_L , as shown in the energy plots of Figure 2.1. In CCM, the maximum energy is higher than the variations of energy because a portion of it is not used for power conversion. In DCM and BCM, the maximum energy and variations of energy are equal,

2.1. Indirect power in the inductor as a high-level metric

therefore $E_L = P_{indL} \cdot T$. Finally, in TCM, E_L is below $P_{indL} \cdot T$, because $P_{indL} \cdot T$ is the sum of the variation in energy when the current is positive and when it is negative. As a result, in TCM, the peak energy in the inductor may be smaller than in CCM, even with a higher value of P_{indL} . This plot concludes that the relation between maximum energy and P_{indL} depends on the type of waveform considered. The relation between E_L , P_{indL} and volume and losses in the inductor also depends on the waveform considered. To summarize, P_{indL} is a good and straightforward metric for comparison when the same type of waveform is considered.

2.1.2 Indirect power applied to DC-AC two-port inverters

For DC-DC conversion, the indirect power is a constant value that relates frequency and variations of energy. However, for DC-AC systems, the indirect power is no longer a constant as the voltage and current in the ports change along the line cycle. Moreover, in DC-AC systems, the energy at the beginning and end of the switching cycle in the inductor is not usually the same. In other words, some energy is stored at line frequency. For this analysis, the variations of energy at low frequency are omitted as they are usually small compared with the energy of the ports, so it is assumed $P_g = P_o$. Moreover, quasistatic DC ports are assumed: the voltage and current in a switching cycle are assumed constant. The Full-Bridge with bipolar and unipolar modulations are compared to illustrate the calculation of P_{indL} in DC-AC inverters. For this comparison, a constant input voltage, V_g , is assumed. For the output, $PF = 1$ is considered; the output voltage and current are given by $V_o = V \cdot \sin(\omega_{line} \cdot t)$ and $I_o = I \cdot \sin(\omega_{line} \cdot t)$ respectively.

In bipolar modulation, the operation is divided into two states. In the first one, the voltage applied to the inductor is $V_1 = V_g - V_o$, while in the second state, the voltage is $V_2 = -V_g - V_o$. For the currents, since the inductor is in series with the output, $I_L = I_1 + I_2 = I_o$, and, since the input current is $I_g = I_1 - I_2$, therefore $I_1 = (I_g + I_o)/2$. Using the first state to calculate the indirect power with Equation 2.9, the result is $P_{indL} = |V_g - V_o| \cdot |I_g + I_o|/2 = P/2 \cdot (V_g/|V_o| - |V_o|/V_g)$. The indirect power along a line cycle is plotted in Figure 2.2 for $V_g = 400$ V, $V = 340$ V, and the average output power of 1 kW.

Then, the same process can be applied to unipolar modulation. Only the first half cycle ($V_o > 0$) is calculated here. From the inductor standpoint, the operation in the first half of the cycle is like in a buck converter. Therefore, $V_1 = V_g - V_o$, $V_2 = -V_o$, $I_1 = I_g$, and $I_2 = I_o - I_g$, leading to $P_{indL} = (V_g - V_o) \cdot I_g$. The same result is obtained for the negative part of the cycle but replacing V_o with $-V_o$. As a result, the indirect power with unipolar modulation is given by $P_{indL} = P(1 - |V_o|/V_g)$. Figure 2.2 shows the indirect power with unipolar modulation along the line cycle too.

P_{indL} is lower when unipolar modulation is applied. In fact, with bipolar modulation, there are parts of the line cycle where the power processed by the inductor is above the nominal power. As in the Full-Bridge $I_L = I_o$, the average inductor current is the same regardless of the modulation, the difference in P_{indL} comes from the volt-second part. It is well known that with bipolar modulation, VS_L is higher than in unipolar modulation. It should be noted that P_{indL} does not reflect the relationship between switching frequency and the frequency seen by the inductor. In bipolar modulation, these frequencies coincide, but with unipolar modulation, the inductor frequency is

Figure 2.2: P_{indL} in a Full-Bridge inverter for unipolar and bipolar modulations.

two times the switching frequency, leading to a further reduction on the inductor requirements if the same switching frequency is applied. The frequency factor is not a part of the plot in Figure 2.2, as P_{indL} is not a function of the switching frequency. In general, it is concluded that bipolar modulation is worse in terms of the inductor size and losses. However, to decide which modulation to apply, other considerations such as CM voltages or control complexity should be taken into account too. The takeaway from this short comparison is that P_{indL} gives a measure of the product of the variations of energy and frequency, but the selection of the switching frequency and type of current waveform has an important impact on the design too.

In DC-AC conversion, P_{indL} changes during the line cycle, hence its relation to energy or volume and losses is more subtle compared to DC-DC conversion where P_{indL} is a constant value. The problem with DC-AC conversion is that not only P_{indL} changes along the line cycle, but the relationship between the maximum energy and the variations of energy in the inductor changes too. For instance, if CCM with PWM modulation is used for the Full-Bridge, the worst point in terms of energy in the inductor is reached near the peak output current, at $\pi/2$ in Figure 2.2, which is not the point where P_{indL} is maximum. The reason is that P_{indL} is related to ΔE_L not E_L , as mentioned before

The indirect power is more meaningful in BCM instead of CCM, because $E_L = P_{indL} \cdot T$. In this case, the P_{indL} plot gives the relation between maximum energy and frequency in the inductor. In BCM, the maximum energy in the inductor is given by $E_L = 2 \cdot L \cdot I_o^2$ because the peak inductor current is $2 \cdot I_o$. As a result, P_{indL} gives information about the inductor frequency because ΔE_L is known. Therefore, for two converters with the same inductance and average current in BCM, the higher P_{indL} , the higher the frequency, and higher losses or volume can be expected.

2.1. Indirect power in the inductor as a high-level metric

Regardless of the type of waveform, P_{indL} only gives the ratio $\Delta E_L/T$. How these two quantities are distributed along the line cycle is not derived from P_{indL} and depends on the specific topology and modulation. With PWM modulation, as the frequency of the inductor is fixed, P_{indL} is directly related to ΔE_L . However, for BCM operation, the frequency applied to the inductor depends on the inductance value. Therefore, the inductor shifts the product towards the frequency or the energy for a given P_{indL} . In general, in BCM, the value of the inductance and P_{indL} determine the shape of ΔE_L and T along the line cycle once L is set.

2.1.3 Indirect power in three-port systems

Obtaining the indirect power in three-port systems is not a problem since Equation 2.8 can be used directly. Although, usually in three-port systems, more than two states are applied. In this section, two DC-DC three-port converters are described to introduce the methodology. The operation of these converters resembles to the operation of the inverter analyzed in this work in two sectors of the line cycle. Also, the concepts of CCM, DCM, BCM, and TCM are extended to three-port converters.

2.1.3.1 Two-Input Buck converter

An interesting yet simple DC-DC converter designed to obtain a small and efficient inductor is the Two-Input Buck (TIBuck), described in [78]. The converter is shown in the bottom of Figure 2.3. The TIBuck uses two separate input sources to provide power to the output, provided $V_{g1} > V_o > V_{g2}$. It should be mentioned that this converter is not technically a three-port converter as defined in the previous chapter, because only one port can be controlled independently.

Figure 2.3: Comparison of a Buck and a Two-Input Buck.

This converter is described to show the reduction of P_{indL} that can be obtained when a third port is added. In the first state, $V_1 = V_{g1} - V_o$ and $I_1 = I_{g1}$. In the second state, $V_2 = V_{g2} - V_o$ and $I_2 = I_{g2}$. Here, V_{g1} and I_{g1} are the port values of the input source with the higher voltage and V_{g2}

and I_{g2} the ones of the other input source. The indirect power is given by $P_{indL} = (V_{g1} - V_o) \cdot I_{g1}$, which can be rewritten as $P_{indL} = I_o \cdot (V_{g1} - V_o) \cdot (V_o - V_{g2}) / (V_{g1} - V_{g2})$. As mentioned in [78], the efficiency of the converter is exceptionally high when the two input voltages are close. The indirect power, as compared to the nominal power, is lower the higher the output voltage and lower the difference between the input voltages [13].

The indirect power in the inductor can be compared in this converter and the buck converter to highlight the advantages of this topology. For this brief comparison, the selected specifications for the buck converter are $V_g = 400$ V, $V_o = 300$ V and $I_o = 1$ A and for the TIBuck, $V_{g1} = 400$ V, $V_{g2} = 200$ V, $V_o = 300$ V and $I_o = 1$ A. Both converters and their waveforms are shown in Figure 2.3. From Equation 2.10, the buck converter processes $P_{indL} = 75$ W while the TIBuck processes only $P_{indL} = 50$ W. This improvement is highly dependent on the port parameters. The inductor in the TIBuck is expected to be smaller if the same switching frequency and type of waveforms are considered in both cases.

For this converter to be a three-port converter, an additional freewheeling state can be added. As explained in [13], the modified topology to add the freewheeling state together with the waveforms are shown in Figure 2.4. With this modification, this converter represents the operation of the analyzed inverter when the storage capacitor is providing power.

Figure 2.4: Two-Input Buck with freewheeling state.

The operation is divided into three states; therefore, the power flow among the three ports can be controlled independently of the output voltage. However, there are limits to how much current can be drawn from each input, for instance, this converter cannot accomplish $V_o > V_{g2}$ with all power coming from the input with lower voltage, V_{g2} . This type of limitation is addressed in Chapter 4 since it has an important role in the selection of the modulation for the studied topology.

For the indirect power, the voltage and current in the states are $V_1 = V_{g1} - V_o$, $I_1 = I_{g1}$, $V_2 = V_{g2} - V_o$, $I_2 = I_{g2}$, $V_3 = V_o$ and $I_3 = I_o - I_{g1} - I_{g2}$. Equation 2.5 is not valid as different states have different average current, Equation 2.8 is used as before. It implies that P_{indL} is not directly related to the volt-seconds in the inductor. The indirect power can be calculated using the states storing power in the inductor or the states delivering power. If $V_o > V_{g2}$ as in the waveform of Figure 2.4, the only state with positive power in the inductor is the first one, then $P_{indL} = (V_{g1} - V_o) \cdot I_{g1}$. If instead $V_o < V_{g2}$, the voltage in the second state is positive and the only state with negative power is the last one, then $P_{indL} = V_o \cdot (I_o - I_{g1} - I_{g2})$. The bottom

2.1. Indirect power in the inductor as a high-level metric

line is that the analysis of the indirect power can sometimes be straightforward if the voltage and current of all ports are known.

With three states, the current waveform in the inductor is more complicated, but the same types of waveforms as in two-port converters are found. This kind of waveform, with a trapezoidal shape, is also found in two-ports converters, although an additional control variable is required [79], [80]. Below, a brief discussion of the different waveforms that i_L can take is included. The waveforms are depicted in Figure 2.5.

Figure 2.5: Possible modulations of the modified Two-Input Buck, a) CCM, b) CCM with a different sequence of states, c) TCM, d) DCM, e) BCM.

- **Continuous Conduction Mode (CCM):** Figure 2.5 a) shows the waveform when the inductor current is always above 0. As the waveform is separated into three states, the order of the states (or sequence) affects the shape of the inductor current. There are two possible sequences of states, as shown in Figure 2.5 a) and b). Any other possible sequence can be represented through the waveforms in a) or b) but starting with a different state. When $V_1 > V_2 > V_3$, as in Figure 2.5 a), the shape of i_L is more "squared" compared with the case of $V_1 > V_3 > V_2$ in b). These two sequences have a different total current ripple, leading to a different peak and rms current for the same I_L , and the difference is more pronounced as the operation tends to BCM. Therefore, the sequence with $V_1 > V_2 > V_3$ is preferred. Note that these two sequences have the same indirect power.
- **Triangular Conduction Mode (TCM):** When the inductor value is low, the inductor current can be negative, as shown in Figure 2.5 c). Again, the sequence of states can be different, but only the one equivalent to case a) is shown. In TCM, P_{indL} is higher than in CCM, and the rms current and peak inductor current are also higher, like in two-port converters. A great feature of this kind of waveform is that it can be used in some converters to perform ZVS [68], [61]. The volume of the inductor could be assumed to be proportional to the inductance, the rms current, and the peak current in the inductor as mentioned in [61]. Accordingly, TCM is a good trade-off between these parameters and the switching-loss reduction because of ZVS. In this work, the modulation of the inverter is based on TCM too. The modulation is described in Chapter 4 after the ideal modulation based on a BCM modulation is explained.

- **Discontinuous Conduction Mode (DCM):** This type of waveform is divided into four states, as shown in Figure 2.5 d). DCM features the same P_{indL} as CCM. However, due to the higher peak current and rms current, the inductor design is penalized.
- **Boundary Conduction Mode (BCM):** BCM is the limit between CCM and DCM or CCM and TCM, where the inductor current is zero at the beginning and end of the switching cycle, as shown in Figure 2.5 e). It features lower rms and peak current compared to DCM or TCM, yet not as low as in CCM. Nevertheless, as the inductance value is not as high as in CCM, the maximum energy in the inductor is minimized. As mentioned earlier, the optimum sequence is the one where the voltages decrease gradually from a state to the next as it is convenient to have a waveform as close to a square as possible to reduce rms current. BCM is used to describe the modulation of the analyzed inverter first, as described in [13].

2.1.3.2 Dual Active Bridge

Another DC-DC converter that is going to be helpful to explain the modulation of this inverter when the output power is low is the Dual Active Bridge (DAB). First, the optimum modulation in terms of P_{indL} is obtained. Then, the topology is modified to include a third port to represent the operation of the studied inverter.

To describe the fundamental operation of the DAB and the indirect power of the inductor, L_m is assumed infinite and the transformer is omitted. The topology without the transformer is shown in Figure 2.6.

Figure 2.6: Dual Active Bridge without the transformer and waveform in BCM, with this modulation, secondary switches can be replaced with diodes.

Many different modulations can be applied to the DAB. It is not required to analyze every possible modulation to obtain the one that features minimum P_{indL} . In Section 2.1.1, it was found that the buck converters operate with $P_{indL} = P_{diff}$ (the minimum achievable). Therefore, if the voltage on the primary side is higher than in the secondary side (accounting for the number of turns), as in Figure 2.6, the DAB operating with the same states as a buck already features minimum P_{indL} . First the inductor should be connected between the input and output, and then only to the output. No other state should be used, or the indirect power would increase. For instance, the classical phase shift modulations would result in higher P_{indL} because the input is always connected to the inductor, in one direction or the other. These two states have to be applied first with positive current and then with negative to ensure that the average current in the

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inductor is zero. This is required to ensure I_{Lm} in the transformer equal to zero. Moreover, the magnetizing state should start with $i_L = 0$ and the demagnetizing state should end with $i_L = 0$. Otherwise, i_L would change direction in a given state, increasing the indirect power, implying that BCM modulation should be used; the result is the modulation of Figure 2.6. Note that this modulation would require variable frequency and has the advantage of no circulating currents but no ZVS. For the values of Figure 2.6, with this modulation the indirect power is $P_{indL} = 0.25 \cdot P$ for $V_g = 400$ V and $V_o = 300$ V using Equation 2.10.

This converter is introduced to show that BCM is required to minimize P_{indL} while ensuring an average current in the inductor of zero. In any other modulation with different states or additional states, the indirect power would increase. BCM is used in the studied inverter for this reason, among others [13].

This converter can be modified to include a third port to represent the operation of this inverter when the output power is low. This concept is shown in Figure 2.7, where the load is connected in series with the inductor and the transformer is removed as the converter would not work with L_m .

Figure 2.7: Three-port modification for the DAB, showing the topology and the waveforms for $V_g > V_{o2} > V_{o1}$ (as before, secondary switches can be replaced by diodes).

By controlling how long the first and third states last, how much current flows from V_g to V_{o2} can be controlled, and it is also possible to control the average current through V_{o1} .

P_{indL} can be calculated as $V_1 \cdot I_1 + V_3 \cdot I_3$ from Equation 2.8 since energy is stored in the inductor in the first and third states, and released in the second and fourth. The voltages are easy to obtain, $V_1 = V_g - V_{o2} - V_{o1}$ and $V_3 = -V_g + V_{o2} - V_{o1}$. However, the currents are far more complicated, the following relations are not sufficient: $I_g = I_1 + I_3$, $I_{o2} = -I_1 - I_2 + I_3 + I_4$, and $I_{o1} = I_1 + I_2 + I_3 + I_4$ following the sign criteria of Figure 2.7. To obtain I_1 and I_3 , an additional constrain is needed. Since i_L at the beginning of the first and third states is 0, the following relation between the voltage and the time the states last is found: $V_1/L \cdot T_1 = -V_2/L \cdot T_2$ where T_1 and T_2 is the time the first and second state last respectively. The current of the first state is given $I_1 = V_1/L \cdot T_1/2 \cdot T_1/T$ and the current in the second state by $I_2 = -V_2/L \cdot T_2/2 \cdot T_2/T$. Together with the previous relation, it leads to $I_1/I_2 = T_1/T_2 = -V_2/V_1$. With this equation and $I_3/I_4 = V_4/V_3$, and the relation between port currents and state currents found before, I_1 and I_3 can be obtained. Then, with these values, P_{indL} can be calculated. The result is not shown here as it is going to be calculated again when the analyzed inverter is studied, the goal is to show that obtaining the state currents is not always straightforward when it comes to waveforms divided into several states. This is elaborated in Appendix B.

It should be noted that this modified DAB and the modified TIBuck described in Section 2.1.3.1 can only work under certain conditions. The modified TIBuck of Figure 2.4 only works for $V_o > 0$ and can only achieve a certain sharing of power among port. This type of waveform in Figure 2.5 e), divided into three states with positive current, is referred to as *trapezoidal* modulation. Two control variables define the waveform unequivocally. The modified DAB of Figure 2.7 seems more inserting as it can have positive or negative V_o , but the modulation of Figure 2.7 b) is only valid for power flowing from the right port to the left port and $V_g > V_{o2} > V_{o1}$. This type of waveform, with two states with positive current and two states with negative current, is referred to as *triangular* modulation. Again, with two control variables, the waveform is completely defined since it is constrained to BCM operation. In this work, BCM modulation is considered as it is required in those *triangular* modes, and it leads to minimum indirect power [16].

2.2 Description of the analyzed inverter

In this section, the topology proposed in [16] and its operating principles are extensively described. The topology is shown in Figure 2.8, highlighting the three ports. The power stage requires three pairs of complementary switches, named d^+ and d^- , h^+ and h^- in the branch with the storage capacitor, and q^+ and q^- in the other leg. Therefore, the storage capacitor is connected as a flying capacitor in this structure. The current in the storage capacitor is defined as positive when flowing out of the capacitor, as noted in the previous chapter. Moreover, the output capacitor is considered a part of the output port for the analysis of P_{indL} . Therefore, the output current is defined as the average inductor current.

Figure 2.8: Analyzed topology highlighting the three ports.

2.2.1 Switching states

With three pairs of complementary switches, this topology can be configured in eight switching states, states for short. A state defines the voltage in the inductor and how the current is flowing among ports. The states are shown in Figure 2.9. In this section, the nomenclature used to define the states is discussed. The dead time to transition from one state to the next is going to be described in the following chapter.

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Figure 2.9: Circuits for the eight switching states named after the switches configuration $[dhq]$ and the port configuration $[g \quad s]$.

Instead of numbering the states one to eight, a more meaningful name is given to each state. States can be named according to the configuration of the switches as a set of three digits, namely $[dhq]$. When d^+ is closed, the d digit is equal to 1, and when d^- is closed instead, the number is 0. The same rule defines the h and q digits. This set of numbers is shown in the top-left of each circuit in Figure 2.9. This nomenclature is used in the following chapter, as it is helpful to describe ZVS processes [81].

A different nomenclature is also defined based on how the input and storage capacitor ports are connected to the inductor. This nomenclature is useful to describe the modulation and to calculate the indirect power, as it defines which ports are connected to the inductor in the state. For this nomenclature, two values are defined, g and s . These numbers can take the values $+1$, 0 , or -1 and define how the input and storage capacitor are connected to the inductor, respectively. When $g = +1$, the input is connected to the inductor, when it is 0 the input is not connected, and when it is -1 the input is connected with the opposite polarity. The same applies to the storage capacitor, $s = +1$ means that the storage capacitor is connected to the inductor, -1 means that it is connected in the opposite direction and 0 that it is not connected. As the output port is always connected in series with the inductor, a third number is not required, states can be defined with the string $[g \ s]$. This nomenclature is shown in the top-right of each circuit in Figure 2.9. Note that two switching states give rise to the same connections of the ports, namely $[110]$ and $[001]$. In both cases, the input and storage capacitor are not connected; this is $[0 \ 0]$ in terms of the $[g \ s]$ nomenclature.

The current and voltage in the inductor in each state can be obtained either through the g and s numbers according to:

$$v_L = g \cdot V_g + s \cdot V_s - V_o \quad (2.11)$$

$$i_L = g \cdot i_g = s \cdot i_s = i_o \quad (2.12)$$

This nomenclature is very useful for this reason. The two nomenclatures are summarized in Table 2.1, where the voltage applied to the inductor and the relation between the current in the ports is included for the eight states.

$[g \ s]$	Voltage	Current		$[dhq]$
$[+1 \ 0]$	$v_L = V_g - V_o$	$i_L = i_g = i_o$	$i_s = 0$	$[111]$
$[0 \ 0]$	$v_L = -V_o$	$i_L = i_o$	$i_g = i_s = 0$	$[110]$
$[+1 \ -1]$	$v_L = V_g - V_s - V_o$	$i_L = i_g = -i_s = i_o$		$[101]$
$[0 \ +1]$	$v_L = V_s - V_o$	$i_L = i_s = i_o$	$i_g = 0$	$[011]$
$[0 \ -1]$	$v_L = -V_s - V_o$	$i_L = -i_s = i_o$	$i_g = 0$	$[100]$
$[-1 \ +1]$	$v_L = -V_g + V_s - V_o$	$i_L = -i_g = i_s = i_o$		$[010]$
$[0 \ 0]$	$v_L = -V_o$	$i_L = i_o$	$i_g = i_s = 0$	$[001]$
$[-1 \ 0]$	$v_L = -V_g - V_o$	$i_L = -i_g = i_o$	$i_s = 0$	$[000]$

Table 2.1: Available switching states, named after the configuration of the port and the configuration of the switches.

2.2. Description of the analyzed inverter

These switching states are combined in sequences to create the *operation modes* that shape the current in the inductor.

2.2.2 Introduction to the operation modes

Each different sequence of switching states is called *operation mode*, *mode* for short. Modes are named according to the sequence of states as $[g_1 \ s_1] \rightarrow [g_2 \ s_2] \rightarrow \dots$ or as $[d_1 h_1 q_1] \rightarrow [d_2 h_2 q_2] \rightarrow \dots$ depending on the situation. In the literature, the meaning of *modes* and *states* are often interchanged. As it is not standardized, modes are composed of states in this work.

For instance, the operation modes and equivalent circuits of the modified TiBuck converter (Figure 2.4) and modified nonisolated DAB (Figure 2.7) explained previously are depicted in Figure 2.10 replacing V_{g1} with V_g and V_{g2} with V_s for the modified TiBuck and replacing V_{o1} with V_o and V_{o2} with V_s for the modified DAB. The operation mode for the modified TiBuck with the $[g \ s]$ nomenclature would be $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$. The operation mode of the modified DAB would be $[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$. These modes are used in the modulation of the inverter and are called $Tra4^+$ and $T0$ respectively in Chapter 4. The complete modulation of this converter requires nineteen modes like the ones shown in this figure.

Figure 2.10: Operation modes of the modified TiBuck and modified DAB, with states named using the $[g \ s]$ nomenclature. The area shaded in green in i_L represents i_g , and the area shaded in purple represents i_s .

For the modulation of the inverter, there are three types of modes classified according to the shape of the inductor current waveform [13], [16]. These types of modes are labeled *trapezoidal positive* (Tra^p), as the one in Figure 2.10 a), *trapezoidal negative* (Tra^n), also divided into three states but with negative current in the inductor, and *triangular* (T), as the one in Figure 2.10 b). The three types of modes are shown in Figure 2.11. Along this section, how to obtain the indirect power in these types of modes is detailed. Further study in the types of modes and on how the modulation could be obtained in a general three-port inverter is provided in [82].

Figure 2.11: Different types of BCM modes considered for the modulation. a) *Trapezoidal positive* modes: Tra^p . b) *Trapezoidal negative* modes: Tra^n . c) *Triangular* modes: T .

2.2.2.1 BCM trapezoidal modes

There are many combinations of states that can give rise to different Tra^p modes, besides the one used in the modified TIBuck. In Tra^p modes, the first state start with $i_L = 0$ and the voltage in the inductor is positive. The voltage of the third state is negative, and the state has to end with $i_L = 0$. Two variables (duty cycle, on-time, peak currents, or any other) are required to define the waveform unambiguously. Moreover, only Tra^p modes, where $V_1 > V_2 > V_3$ are considered in this work, leading to the shape is shown in Figure 2.11 a). As discussed in Section 2.1.3, if the mode is defined so that $V_2 > V_1 > V_3$ or $V_1 > V_3 > V_2$, the rms and peak current in the inductor would increase for the same current in the ports compared to $V_1 > V_2 > V_3$.

For the modulation, there are modes dual to Tra^p modes, the Tra^n modes. In these modes the first state has a negative slope of the inductor current slope while the last one has positive slope; the inductor current starts and ends with $i_L = 0$ and $V_1 < V_2 < V_3$ as shown in Figure 2.11 b). Tra^p and Tra^n modes are referred together as Tra modes.

To calculate the indirect power and be able to compare modes, the voltage and current of the three states are required. To obtain the current and voltage in the states, the parameters g_1, s_1, g_2, s_2, g_3 , and s_3 used. Therefore, the results are valid regardless of the specific mode analyzed. The voltage in the inductor in the three states, V_1, V_2 , and V_3 respectively, are obtained applying Equation 2.11:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} = \begin{bmatrix} g_1 & s_1 & -1 \\ g_2 & s_2 & -1 \\ g_3 & s_3 & -1 \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_s \\ V_o \end{bmatrix} \quad (2.13)$$

The relation between the average current over a switching cycle in every state, I_1, I_2 , and I_3 and the current can be obtained from Equation 2.12. Defining I_g as the average value of i_g and I_s the average of i_s in a switching cycle, following the nomenclature used throughout the dissertation, the relation obtained is:

$$\begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} = \begin{bmatrix} g_1 & g_2 & g_3 \\ s_1 & s_2 & s_3 \\ 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \quad (2.14)$$

To obtain I_1, I_2 , and I_3 , the inverse of the previous matrix is required, resulting in:

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$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \frac{\begin{bmatrix} s_2 - s_3 & g_3 - g_2 & g_2 \cdot s_3 - g_3 \cdot s_2 \\ s_3 - s_1 & g_1 - g_3 & g_3 \cdot s_1 - g_1 \cdot s_3 \\ s_1 - s_2 & g_2 - g_1 & g_1 \cdot s_2 - g_2 \cdot s_1 \end{bmatrix}}{g_1 \cdot s_2 + g_2 \cdot s_3 + g_3 \cdot s_1 - g_1 \cdot s_3 - g_2 \cdot s_1 - g_3 \cdot s_2} \cdot \begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} \quad (2.15)$$

For the indirect power, depending on the sign of the voltage of the second state, there is a single state where energy is stored in the inductor or a single state where the inductor delivers energy. As a result, Equation 2.9 can be easily computed:

$$P_{indL} = \max(|V_1 \cdot I_1|, |V_3 \cdot I_3|) \quad (2.16)$$

These equations are valid for Tra^p modes and Tra^n modes. The indirect power at any point of the line cycle can be calculated for any given mode (any combination of g_1, s_1, g_2, s_2, g_3 , and s_3) with Equations 2.13, 2.15 and 2.16.

2.2.2.2 BCM triangular modes

T modes are divided into four states, two with positive current in the inductor and two with negative current (Figure 2.11 c)). The first and third states start with $i_L = 0$ and the second and fourth end with $i_L = 0$. The first and fourth states have positive slope while the second and third have negative slope. Keep in mind that these modes do not need to have an average inductor current of zero; the average current is used to control I_o . As before, voltages and currents can be obtained as a function of the g and s values for each state of the mode. For the voltages:

$$\begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix} = \begin{bmatrix} g_1 & s_1 & -1 \\ g_2 & s_2 & -1 \\ g_3 & s_3 & -1 \\ g_4 & s_4 & -1 \end{bmatrix} \cdot \begin{bmatrix} V_g \\ V_s \\ V_o \end{bmatrix} \quad (2.17)$$

And for the currents:

$$\begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} = \begin{bmatrix} g_1 & g_2 & g_3 & g_4 \\ s_1 & s_2 & s_3 & s_4 \\ 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} \quad (2.18)$$

The problem with Equation 2.18 is that there is no inverse matrix. To find I_1 to I_4 additional equations are required. This condition is obtained from the BCM condition, as applied when the modified DAB modulation was described in Section 2.1.3. Since the current is zero between the states two and three and states four and one, the following relations are always valid $V_1 \cdot T_1 + V_2 \cdot T_2 = 0$ and $V_3 \cdot T_3 + V_4 \cdot T_4 = 0$ where T_1, T_2, T_3 , and T_4 are the times each state last. In Tra modes, this condition is $V_1 \cdot T_1 + V_2 \cdot T_2 + V_3 \cdot T_3 = 0$, but it is not necessary as Equation 2.14 is invertible.

The peak current in the inductor is a function of the voltage and time in the states and the inductance value. The positive peak current is given by $V_1/L \cdot T_1 = -V_2/L \cdot T_2$ and the negative

peak by $V_3/L \cdot T_3 = -V_4/L \cdot T_4$. With these peak currents and the duty cycle of each step, the currents in the states can be obtained easily:

$$I_1 = \frac{V_1}{2 \cdot L} \frac{T_1}{T_1+T_2+T_3+T_4} \quad I_2 = \frac{V_2}{2 \cdot L} \frac{T_2}{T_1+T_2+T_3+T_4} \quad I_3 = \frac{V_3}{2 \cdot L} \frac{T_3}{T_1+T_2+T_3+T_4} \quad I_4 = \frac{V_4}{2 \cdot L} \frac{T_4}{T_1+T_2+T_3+T_4} \quad (2.19)$$

Dividing I_1 over I_2 and I_3 over I_4 the following relations are obtained: $I_1/T_1 = I_2/T_2$ and $I_3/T_3 = I_4/T_4$. Together with $V_1 \cdot T_1 = -V_2 \cdot T_2$ and $V_3 \cdot T_3 = -V_4 \cdot T_4$, it leads to:

$$-I_1 \cdot V_2 = I_2 \cdot V_1 \quad -I_3 \cdot V_4 = I_4 \cdot V_3 \quad (2.20)$$

This additional relation between the current in the states can be used in Equation 2.20 to obtain $I_1 + I_2$ and $I_3 + I_4$ as:

$$\begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} = \begin{bmatrix} g_1 & g_2 & g_3 & g_4 \\ s_1 & s_2 & s_3 & s_4 \\ 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} \frac{I_1+I_2}{1-\frac{V_1}{V_2}} \\ \frac{I_1+I_2}{1-\frac{V_2}{V_1}} \\ \frac{I_3+I_4}{1-\frac{V_3}{V_4}} \\ \frac{I_3+I_4}{1-\frac{V_4}{V_3}} \end{bmatrix} \quad (2.21)$$

In this new matrix, the number of output variables has been reduced from four to just $I_1 + I_2$ and $I_3 + I_4$. However, now, as there are more equations than variables, one of the three conditions can be removed. For instance, if I_s is removed, rearranging Equation 2.21 leads to:

$$\begin{bmatrix} I_g \\ I_o \end{bmatrix} = \begin{bmatrix} \frac{V_2 \cdot g_1 - V_1 \cdot g_2}{V_2 - V_1} & \frac{V_4 \cdot g_3 - V_3 \cdot g_4}{V_4 - V_3} \\ 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 + I_2 \\ I_3 + I_4 \end{bmatrix} \quad (2.22)$$

Finally, the inverse matrix of this function leads to:

$$\begin{bmatrix} I_1 + I_2 \\ I_3 + I_4 \end{bmatrix} = \frac{\begin{bmatrix} (V_2 - V_1) \cdot (V_4 - V_3) & -(V_2 - V_1) \cdot (V_4 \cdot g_3 - V_3 \cdot g_4) \\ -(V_4 - V_3) \cdot (V_2 - V_1) & (V_4 - V_3) \cdot (V_2 \cdot g_1 - V_1 \cdot g_2) \end{bmatrix}}{(V_2 \cdot g_1 - V_1 \cdot g_2) \cdot (V_4 - V_3) - (V_4 \cdot g_3 - V_3 \cdot g_4) \cdot (V_2 - V_1)} \cdot \begin{bmatrix} I_g \\ I_o \end{bmatrix} \quad (2.23)$$

I_1 to I_4 are obtained using Equations 2.20 and 2.23. In T modes, the power in the inductor is positive in the first and third states and negative in the second and fourth. Therefore, P_{indL} can be calculated as:

$$P_{indL} = V_1 \cdot I_1 + V_3 \cdot I_3 = -V_2 \cdot I_2 - V_4 \cdot I_4 \quad (2.24)$$

2.2.2.3 Interpretation of the indirect power in triangular and trapezoidal modes

In this section, the relation between P_{indL} , switching frequency, and energy in the inductor for Tra and T modes is discussed. The voltage, current, power, and energy in the inductor for T and Tra^p are shown in Figure 2.12. In Figure 2.12 a) $V_2 < 0$, a similar drawing can be obtained for Tra^p

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with $V_2 > 0$ or Tra^n modes. In the case of trapezoidal modulation when $V_2 < 0$, the maximum energy in the inductor is reached after the first state, and it is given by $E_L = V_1 \cdot I_1 \cdot T$. Therefore $E_L = P_{indL} \cdot T$ as in the BCM modulation of the buck converter. This relation is valid regardless of the sign of V_2 and also for Tra^n modes. In Tra modes, P_{indL} relates the maximum energy in the inductor through the switching frequency. In these modes, $\Delta I_L < 2 \cdot I_L$, meaning that the rms to average current and peak to average current is improved compared to the BCM modulation in a buck converter.

Figure 2.12: Indirect power, period, and energy for the types of modes considered in this inverter, a) trapezoidal modes b) triangular modes.

For triangular modes, the relation between P_{indL} , E_L , and T is not direct as shown in Figure 2.12 b). The reason is that there are two peaks for the energy in the inductor. Note that P_{indL} does not relate the maximum peak and the frequency, but the sum of the two peaks and the frequency.

When selecting the modulation, it is desired to minimize P_{indL} in triangular and trapezoidal modes, as it minimizes the energy processed in the inductor or reduces the switching frequency.

2.2.2.4 BCM modes not considered

It should be clarified that not every Tra or T mode can be used for the modulation; two additional conditions must be met:

- In at least one of the switching states of the mode, $s \neq 0$. And in at least one of the switching states $g \neq 0$. Otherwise, the storage capacitor or input current would be zero, and the mode could not control the power flow among ports. Consider for instance the Tra^p mode $[+1 \ 0] \rightarrow [0 \ 0] \rightarrow [-1 \ 0]$, regardless the control variables, the current in the capacitor is always zero.
- Modes with $I_g < 0$ are not considered since the inverter is not intended to operate as a rectifier. Therefore, Tra^p modes where g is not equal to $+1$ in at least one of the three states are not considered. Tra^n modes where g is not equal to -1 in any of the three states are not considered either. It also applies to T modes, in this case, either $g = +1$ in the first or second state or $g = -1$ in the third and fourth (or both) for the input current to be positive. The operation as a rectifier is described as a future line in Chapter 8.

The modes considered in this work are those initially described in [16], yet there are other possible types of modes that are not considered because the inverter and its control were developed only for T and Tra modes. A brief discussion to justify why these modes are not used is provided. Examples of the types of modes not considered are shown in Figure 2.13.

Figure 2.13: Types of modes not considered, a) T modes with just three states, b) $TTra^p$ modes, c) Tra^p modes with four states, d) TT^p modes.

In Figure 2.13 a), a different type of BCM mode with only three states is included. It is a triangular mode where the second and third (or the fourth and first) states are the same. These modes are considered as T modes, and its operation is divided into four states, so the same equations as T modes can be applied.

A type of mode that is not considered is shown in Figure 2.13 b) and c). These modes are divided into more than four or three states, respectively. In both cases, there is an additional degree of freedom to define the shape of i_L . Therefore, a third control variable would be required in this case. As a result, an additional criterion for the modulation would have to be defined, increasing the complexity of the modulation. Moreover, the additional state would imply higher P_{indL} than the minimum achievable, hence it is not recommended. Finally, another interesting option is to have two triangles with positive current only or negative current only. These types are named T^p , as shown in Figure 2.13 d) or T^n when both triangles are negative. T^p and T^n modes can lead to lower indirect power in certain parts of the line cycle. These modes are described in the future lines in Chapter 8. Unfortunately, these types are not considered for the proposed modulation as the modification adopted in this work to obtain ZVS in all transitions is not directly applicable to these modes; this modification is discussed in Chapter 4.

2.2.3 Modulation to minimize the indirect power along the line cycle

The inverter was proposed to reduce indirect power in the inductor, and for that purpose, different operation modes used in different sectors of the line cycle are required [13]. Yet, the modes were proposed based on what seemed logical from the power processing standpoint at each point of the line cycle. As a result, most of the modes proposed achieved minimum indirect power, but not all of them. In this work, instead of relying on experience, all possible modes are considered. Those with lower P_{indL} are selected, which complements those already proposed in [16]. It should be noted that the modes proposed in [16] accounted for transitions with soft-switching; this consideration is addressed in Chapter 4.

For the selection of the modulation, a *Matlab* script has been developed. The script calculates P_{indL} along the line cycle for every possible operation mode. For this purpose, first, all possible

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modes are defined in terms of the g and s parameters for their switching states. Given the voltages of the three ports, the voltage of each state for each possible mode is obtained using Equation 2.11. Then, Tra^p modes that do not comply with $0 < V_1 > V_2 > V_3 < 0$ are discarded. Tra^n that do not meet $0 > V_1 < V_2 < V_3 > 0$ and T modes that do not comply with $0 > V_1, V_4$ and $0 < V_2, V_3$ are removed too. For the remaining modes, the current of each state is calculated using Equations 2.15 and 2.23 for trapezoidal and triangular modes, respectively. Finally, the script calculates P_{indL} for each mode using Equation 2.16 for Tra modes and Equation 2.24 for T modes. This process is repeated for different points in the line cycle to show how P_{indL} evolves along the cycle, and how it changes for different modes. With this plot, the mode with minimum P_{indL} in each point of the line cycle can be selected.

In this section, only the operation for 1 kVA and resistive load is considered. The analysis is extended to all types of loads in Chapter 4. The input voltage and current for this power is $V_g = 400$ V and $I_g = 2.5$ A. The output is $V_o = 340 \cdot \sin(2\pi \cdot 60 \text{ Hz} \cdot t)$ V and there is no phase shift between input and output current, so the output current amplitude is 5.9 A. The effect of the output capacitor is neglected so far. The power pulsation at twice line cycle is fully buffered by the storage capacitor, with a value of 90 μF and swinging between $V_{smin} = 295$ V and $V_{smax} = 380$ V as described in Section 1.7.3. Figure 1.10 showed the three-port variables used in this analysis.

2.2.3.1 Indirect power in specific points of the line cycle

Before the results along the line cycle are discussed, the concept is clarified by investigating two specific points of the line cycle, the points of maximum and minimum output power, at $\omega \cdot t = \pi/2$ and $\omega \cdot t = 0$ respectively.

At $\omega \cdot t = \pi/2$, the output power is 2 kW, and both the input and storage capacitor are providing 1 kW each. In this specific point, the storage capacitor voltage is ≈ 340 V.

For this example, only Tra^p modes are considered because the output current is high. T modes are not interesting for this point as they have two states with negative current, not useful when aiming for high output current. Tra^n modes cannot work in this point $I_L = I_o > 0$. Figure 2.14 shows the three Tra^p modes with lower indirect power in this specific point. The waveforms in the figure only represent the sequence of states and the input and storage capacitor current of the different states, but the time each state lasts and the slope of the inductor current in each state is not representative.

Figure 2.14: The three trapezoidal positive modes with lower P_{indL} at $\omega \cdot t = \pi/2$. The time each state lasts and the slopes do not correspond with the drawing.

The mode that achieves the lowest P_{indL} is $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [+1 \ -1]$ with a value of 123.5 W at this point. In this mode $P_{indL} < P_{diff}$ as discussed in [16], the reason is that the storage capacitor is also processing indirect power. Since it is charged and discharged in the switching cycle, this operation mode uses the storage capacitor as a flying capacitor. Unfortunately, as it is going to be discussed in Chapter 3, this mode cannot achieve ZVS and it has to be replaced with a mode with higher P_{indL} . The following mode in terms of indirect power is $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$ with 150 W, which is the modulation of the modified TIBuck discussed in Section 2.1.3. Finally, the mode $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ -1]$ has also $P_{indL} = 150$ W but the ripple current in the storage capacitor is higher.

At $\omega \cdot t = 0$ (or $\omega \cdot t = \pi$) $P_o = 0$ and all the input power goes to the storage capacitor port, $P_g = -P_s = 1$ kW. In this specific point, the storage capacitor voltage is ≈ 340 V as before. For this point of the line cycle, only T modes can be used because $I_o = 0$ and Tra^p modes are only valid for $I_L = I_o > 0$ and Tra^n modes for $I_L = I_o < 0$. The triangular modes with the minimum indirect power are shown in Figure 2.15.

Figure 2.15: The three triangular modes with minimum P_{indL} at $\omega \cdot t = 0$ or $\omega \cdot t = \pi$.

The best mode in terms of indirect power is $[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$ with a value of $P_{indL} = 150$ W, which is the same mode used for the modified DAB in Section 2.1.3.2. Two similar modes with slightly higher indirect power result from the replacement of $[0 \ +1]$ with $[+1 \ 0]$ in the previous mode, and $[0 \ -1]$ in the with $[-1 \ 0]$ respectively. Both modes lead to $P_{indL} = 162.3$ W.

2.2.3.2 Indirect power along the line cycle

The same process can be used to compare operation modes for all points along the line cycle. For that purpose, the script in *Matlab* is used to calculate P_{indL} for Tra^p , Tra^n , and T modes for the port voltages and currents in Figure 1.10. The results are shown in Figure 2.16 where the voltage and current of the three ports are included too. In this plot, every line represents the indirect power of a different operation mode. There are short lines for modes that can only work in reduced sectors of the line cycle and lines that extend almost half a cycle. All modes have been drawn with the same color, so it is hard to distinguish where each mode starts and ends. The goal of the plot is not to describe every single mode that can be applied, but to show why it is important to select the modulation carefully to avoid processing more power than the minimum required. A large number of possible T modes are obtained because there are many possible combinations of states. As a

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result, in the plot of P_{indL} for T modes, the lines are barely distinguishable. The discussion about the limits of each operation mode is included in Chapter 4 once the final modulation is introduced.

Figure 2.16: P_{indL} along the line cycle for all the possible operation modes, a) voltage in the three ports, b) currents in the three ports, c) P_{indL} of all possible Tra^P modes, d) P_{indL} of all Tra^N modes, e) P_{indL} in T modes. The grey dots represent the P_{indL} of the modes of Figures 2.14 and 2.15.

As expected, Tra^P modes are used in the regions of the line cycle where high and positive I_L is required. Each Tra^P mode has a corresponding Tra^N mode, and they are used for negative and

high I_L . Finally, T modes are only well suited for the operation when I_L is low, regardless of the sign. There are T modes that can work with higher I_L , but the indirect power of those modes is much higher than the minimum, and those modes are not depicted in the figure as their P_{indL} is out of the scale.

The line with minimum P_{indL} in the Tra^p modes correspond to the mode $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [+1 \ -1]$ marked in a dashed line and described earlier. In the case of Tra^n modes, the dashed line corresponds to $[-1 \ 0] \rightarrow [0 \ -1] \rightarrow [-1 \ +1]$. Finally, for T modes, the dashed line is formed by different modes. For instance, at $\omega \cdot t = \pi$ and its vicinity, the mode is $[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$ as described before. To its right, the mode with minimum P_{indL} is $[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ 0] \rightarrow [-1 \ +1]$ and to its left $[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$.

Combining the five modes mentioned before, the minimum indirect power in this inverter is obtained. These five modes together draw the line of minimum indirect power in the inductor, $\min(P_{indL})$, which is shown as a black dashed line in Figure 2.17. The figure also includes the P_{indL} of the Full-Bridge with unipolar and bipolar modulations from Figure 2.2 for the same specifications, although in the Full-Bridge the input current is not constant. It is included to highlight how the correct selection of the topology and modulation can lead to reduced P_{indL} in single-stage inverters. In this inverter, P_{indL} is lower compared to the Full-Bridge but for the points where the output power is near zero. The reason is that in this inverter, the storage capacitor is charged from the input port during that part of the line cycle.

Figure 2.17: Minimum indirect power in this inverter compared with a Full-Bridge with bipolar and unipolar modulations from Figure 2.2.

This plot should be read carefully. As mentioned in Section 2.1.2, the indirect power is not directly related to E_L unless the same type of waveform is considered. Moreover, this plot does not tell which part of P_{indL} corresponds to ΔE_L and how much to T . Nevertheless, the conclusion from this plot is that this topology achieves a very low indirect power, lower than a Full-Bridge, which is impressive as the analyzed inverter integrates the storage capacitor. The Full-Bridge solution would require either a large input capacitor or an input filter to achieve constant input current. The conclusion is that the analyzed inverter is very attractive from the power processed standpoint.

2.3. Conclusion

2.2.3.3 Indirect power in other elements

An important drawback of the inverter and its modulation is that it generates a considerable CM voltage at the switching frequency between the input and output ports. This voltage generates leakage current as mentioned in Section 1.4.2 and has to be filtered with a CM choke. Because of the CM voltage between the input and output, the inverter cannot be directly interleaved. This issue discussed in Chapter 6. As stages cannot be interleaved in principle, the ripple current in the input, output, and storage capacitor can be high, mainly because a BCM modulation is used. The ripple is significant when the inductor current flows both ways in a port. For instance, in the Tra^p mode $[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [0 \ +1]$ shown in Figure 2.14, the current in the inductor flows through C_s in one direction in the second state and the opposite direction in the third state. therefore the capacitor is submitted to large and high-frequency currents. The same happens in C_o when T modes are applied. Even with low output current, the ripple in the output capacitor is high because of the shape of the inductor current. This effect should be considered in the design of C_o and C_g (not drawn in the schematic yet), but it is not a problem for C_s as the energy it has to buffer determines its size.

This effect can also be interpreted in terms of the indirect power of each capacitor, and, it should be noted that although P_{indC} has not been plotted, it can be considerable. Once P_{indC} is considered, the total indirect power in the inductor, capacitors, and even the CM choke can be well above P_{diff} in total. Nevertheless, in general, the power processed by capacitors or transformers has a much lower impact compared with the power processed by inductors in terms of volume and losses [72]. For this reason, only P_{indL} has been used to select the appropriate combination of modes.

2.3 Conclusion

As a summary, in this chapter, the concept of P_{indL} has been explained in detail and applied to two-port DC-DC and DC-AC converters, and three-port DC-DC converters. This metric has also been applied to Tra and T modes in this topology. Also, the relation between P_{indL} , energy, and frequency has been discussed for different types of inductor current waveform in two-port and three-port converters.

A *Matlab* script has been used to calculate the indirect power of every possible mode along the line cycle for the analyzed inverter. The modulation selected is the combination of the Tra^p , Tra^n , and T modes that minimize the indirect power in the inductor. The result is a modulation that performs both DC-AC inversion and energy buffering with reduced power processed by the inductor.

This modulation has been selected without considering ZVS transitions in this chapter. In the following chapter, the conditions required to achieve soft-switching are described in detail. Then, in Chapter 4, the modulation considering only transitions where ZVS is achievable is elaborated.

Zero-Voltage Switching analysis

Soft-switching techniques increase the efficiency of power converters by decreasing switching losses in semiconductors. The soft-switching technique consisting of discharging the drain-source capacitance of the MOSFETs before the device is turned on is called Zero-Voltage Switching (ZVS).

In the previous chapter, the modulation of the inverter was obtained aiming to minimize P_{indL} . However, another target of the modulation is to achieve soft-switching transitions. For such purposes, the modulation previously described is modified in the following chapter based on the results obtained in this one.

In this chapter, how to obtain ZVS transitions in this inverter is explained. The chapter begins with the description of the concept of ZVS, why it is important, and how TCM modulation can be used to obtain ZVS transitions with the current in the inductor. First, transitions are analyzed considering only the direction of the inductor current. Then, a detailed analysis considering not only the direction of the inductor current required to achieve ZVS but also the value of this current is performed. The results obtained in this chapter are later used to determine how much current is required to obtain ZVS transitions for the TCM modulation. The voltage dependence of the parasitic capacitance of transistors is accounted for in the analysis. The chapter ends with the verification through simulation of the proposed equations.

3.1 Soft-switching and its importance

In this section, the advantages of soft-switching are reviewed, defining ZCS and ZVS, and discussing how it is achieved. The impact of ZVS in switching losses and dv/dt is discussed too. Also, the advantages of WBG devices for applications with ZVS are highlighted.

3.1.1 Soft-switching, ZCS, and ZVS

A transition is *soft* when a device is turned on or off when its voltage or its current is zero before the transition. When soft-switching is achieved, switching losses are decreased because the product of voltage and current in the switching devices along the transition is zero.

When a device is switched on and its current right after the switching event is zero, or when a device is turned off when its current is already zero, the transition achieves Zero-Current Switching (ZCS). As the current in the transition is zero, there are no switching losses due to voltage and current coexistence. ZCS is naturally obtained in some resonant converters or converters operated in DCM or BCM in transitions with $i_L = 0$.

ZVS, on the other hand, is obtained when the voltage in the device is zero before it is turned on or when the voltage right after the turn off transition is still zero. ZVS transitions can reduce dv/dt in the switching node, losses due to the coexistence of voltage and current, and the losses associated with the sudden discharge of C_{oss} . Although the latter statement is not entirely true because there are losses associated with the charging and discharging process of the C_{oss} even with ZVS [1], [68]. ZVS can be achieved using external circuits to discharge the C_{oss} before the transition, or it can be achieved naturally in converter with BCM or TCM modulation using the current in the inductor. This is described in detail in Section 3.1.4.

3.1.2 Switching losses in MOSFETs

The impact on switching losses is briefly discussed to understand the advantages of soft-switching. Losses in MOSFETs are usually separated in conduction losses due to the R_{dson} of the device and switching losses that depend on the switching frequency.

Typically, when a transistor is turned on, its current rises before the drain-source voltage falls, generating power losses. In the same way, the turn-off process is lossy; the current decreases only after the drain-source voltage has reached the bus voltage. This type of transition is known as hard-switching, as opposed to soft-switching, where the coexistence of voltage and current is negligible. These losses can drop the efficiency of converters, especially when the turn on/off time is long and the switching frequency is high, ultimately setting a limit to how high the switching frequency can be.

High switching frequency is usually preferred as it decreases the size of passive components. For a given indirect power, the higher the frequency, the lower the variations in energy in reactive components. High switching frequency is also limited by reverse recovery losses in the diodes or the body diodes of the MOSFETs. The charge stored in the junction of the diode must be removed from the device to be turned off. This charge generates losses when removed while high voltage is present in the complementary device. Also, the energy stored in the parasitic capacitance between drain and source (C_{oss}) is dissipated in the channel in the turn-on event, increasing switching losses. Finally, driving losses due to the charge and discharge of the gate capacitance are also related to switching frequency.

3.1.3 Advantages of wide bandgap devices

WBG semiconductors, namely, Gallium-Nitride (GaN) and Silicon-Carbide (SiC) devices, have outperformed Silicon (Si) MOSFETs for most applications. Mainly, the only drawback of WBG devices now is cost. For a given blocking voltage and R_{dson} , WBG devices usually have lower gate charge, which, besides reducing the driving losses considerably, can increase the turn-on and turn-off speed significantly. Because of the fast turn on/off nature of these devices, switching losses are not a major concern, and converters can be designed with high switching frequency to reduce the size of passive components even with hard-switching transitions.

However, short turn-on and turn-off times lead to high dv/dt and di/dt transitions. These fast transitions generate severe EMI noise in turn [61]. Moreover, high dv/dt can couple the noise

3.1. Soft-switching and its importance

from the drivers to the controller [62]. It can also couple the noise to analog circuitry if the layout is not carefully designed [67]. As a result, this noise can lead to a failure of the inverter. Also, as mentioned in [61], the dv/dt reached with WBG devices imposed a serious concern since gate drivers were not reliable enough at the time of the LBC. Therefore, ZVS is important even when WBG devices are used, not only to reduce switching losses but to reduce dv/dt . ZVS was among the design considerations of many of the teams that participated in the LBC as mentioned in Chapter 1 [11].

GaN devices feature low C_{oss} , which is beneficial both in hard-switching transitions because of the lower losses and in soft-switching transitions because of the reduced energy required to discharge the capacitance before the turn-on event. Moreover, opposed to SiC and Si devices, GaN devices do not have body diode. Hence, there are no losses associated with the reverse recovery process. For these reasons, GaN devices are considered for this work.

3.1.4 ZVS using the inductor current

In this section, how to use the inductor current to achieved ZVS is reviewed. For this purpose, the ZVS transitions in a buck converter are used as an example. In this example, the inductor is considered large enough so that the inductor current does not change during the transition. The variation of the current in the inductor along the transition is considered later in the chapter. The ZVS transition in the buck converter is depicted in Figure 3.1. In the circuits, the inductor has been replaced with a current source for simplicity. For the ZVS process, first, the high side switch is turned off, the inductor (current source in the picture) forces a current that charges the high side C_{oss} and discharges the low side C_{oss} . Once the low side is fully discharged, the body diode of the low side switch takes the current. Finally, after the dead time, the low side switch is turned on and ZVS is obtained because its drain-source voltage is zero (or technically the drop of the diode) before the switch is turned on.

Figure 3.1: ZVS transition in a buck converter showing the different parts of the process.

In the turn-on process with ZVS, there is no coexistence of voltage and current, therefore switching losses are zero. Also, its C_{oss} is already discharged. Hence the energy stored in this parasitic capacitance is not dissipated. The turn-off losses of the high side switch can also be reduced with the ZVS transition, depending on what determines the dv/dt in the switching node. If the turn-off time is much faster than the time it takes for I_L to discharge the C_{oss} , it can be assumed that the drain-source voltage barely charges along the turn-off time and switching losses are negligible because the current decreases when the voltage is almost zero. On the other hand, if the transition time is close to the turn-off time, the drain-source voltage is determined by the driver

and the switching device instead of I_L . If this is the case, there is a coexistence of voltage and current, and switching losses can be considerable. As a summary, if the transition time because of the interaction of the inductor current and C_{oss} is much slower than the turn-off time of the device, turn-off losses are negligible too. This concept is explained in detail in [83].

The transition time, T_{tr} , is defined in this work as the time it takes to discharge the low side switch and charge the high side switch to the bus voltage. The dead time should be slightly longer than T_{tr} for the transition to achieve ZVS, or the low side switch would be turned on before its voltage is zero. However, the dead time should not last too much, to avoid the conduction of the diode for a long time. The transition time is directly proportional to the C_{oss} and the bus voltage, and inversely proportional to the magnitude of the inductor current, $T_{tr} \propto C_{oss}, V_{dd}, 1/I_L$ assuming the turn-off time is much faster than T_{tr} .

If both devices are equal and the charge in the C_{oss} at V_{dd} is defined as Q_{oss} , then $T_{tr} = 2 \cdot Q_{tr}/I_L$. In this case, $dv/dt = V_{dd}/T_{tr} = V_{dd} \cdot I_L/(2 \cdot Q_{tr})$. As a result, transitions with high current and low values of C_{oss} can be fast too. In the case of GaN devices, due to the low value of C_{oss} , the transition can be very fast, and the issues related to high dv/dt can be a problem even when ZVS is achieved. With high dv/dt , regardless of the transition is hard or soft, the loop inductance (shown in gray in Figure 3.1) can cause ringing in the switching node. When the inductor current is low and the transitions are slow, no ringing is generally observed.

In the buck converter from Figure 3.1, ZVS can only be achieved in the transition where the high side switch is opened. If the current in the inductor flows from the input to the output, the transition where the low side is opened would be hard.

To achieve ZVS in the transition where the low side switch is opened, the inductor current should be negative. In such conditions, when the low side switch is turned off, the inductor current would discharge the high side switch and ZVS could be obtained. For this reason, ZVS cannot be achieved in all transitions if the inductor current is always positive or negative. To obtain ZVS in both transitions, TCM modulation should be used. As shown in Figure 2.1 d) in the previous chapter, the current has the correct direction for ZVS purposed in the two transitions, at the expense of higher current ripple and power processed in the inductor.

3.2 ZVS transitions in this inverter

In this section, the direction of the current that allows ZVS for every possible transition between switching states is analyzed in the studied inverter. Later in this analysis, how to obtain the required dead time and current for ZVS is discussed, to extend the work presented in [81]. Switching states can be labeled according to the configuration of the ports or the configuration of switches as mentioned in Section 2.2.1. For this analysis, the latter nomenclature is selected. The eight switching states are labeled according to three numbers ($[dhq]$), 1 or 0 depending on whether d^+ , h^+ , and q^+ are on or off, respectively. Transitions are labeled with the initial and final switching state as $[d_1h_1q_1 \rightarrow d_2h_2q_2]$.

ZVS transitions are only possible when the direction of the inductor current discharges the C_{oss} that is initially charged and charges the complementary one. As a simple rule to check if ZVS is

3.2. ZVS transitions in this inverter

possible, a transition can have ZVS only if the inductor current after the dead time flows through the body diode of the MOSFET that is about to be opened, or, more simply, if the inductor current does not flow through the body diode of the opened device. It should be noted that the current direction is a necessary but not a sufficient condition. It is only valid if the inductor current is not reversed in the transition. This statement is discussed in the following section.

Determining which transition can achieve ZVS with positive or negative current in the inductor is easily accomplished by finding which body diode would take the current after the switch is turned off. For positive current in the inductor, ZVS is only possible in transitions where d^+ , h^+ , or q^+ are opened, but not in those where d^- , h^- or q^- are. With the $[dhq]$ nomenclature, this means that ZVS can only be achieved with positive current only when a digit 1 changes to 0. The opposite is true when the inductor current is negative. This is the reason why $[dhq]$ nomenclature is preferred in this chapter. The transitions with ZVS with positive current are listed in Equation 3.1 to clarify this idea. The list is divided into three columns according to the number of transistors switched simultaneously. There are transitions where more than a switch is opened at once, two switches can be switched at the same time (the second column of Equation 3.1), and even three switches can be turned off at once (third column). The same list can be obtained for negative inductor current by replacing all zeros for ones and ones for zeros.

$$i_L > 0 \rightarrow \left\{ \begin{array}{l} [111 \rightarrow 110] \\ [111 \rightarrow 101] \\ [111 \rightarrow 011] \\ [110 \rightarrow 100] \\ [110 \rightarrow 010] \\ [101 \rightarrow 100] \\ [101 \rightarrow 001] \\ [011 \rightarrow 010] \\ [011 \rightarrow 001] \\ [100 \rightarrow 000] \\ [010 \rightarrow 000] \\ [001 \rightarrow 000] \end{array} \right. ; \left\{ \begin{array}{l} [111 \rightarrow 100] \\ [111 \rightarrow 010] \\ [111 \rightarrow 001] \\ [110 \rightarrow 000] \\ [101 \rightarrow 000] \\ [011 \rightarrow 000] \end{array} \right. ; [111 \rightarrow 000] \quad (3.1)$$

A representation of the transitions that can achieve ZVS depending on the direction of i_L is included in Figure 3.2. The diagram is based on the previous list shown in Equation 3.1. The same diagram but using the $[g \ s]$ nomenclature is also included, as it is going to be helpful in the following chapter.

This diagram is helpful to determine which operation modes have ZVS. For instance, it can be applied to the Tra^p mode with minimum indirect power of Figure 2.14, $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [+1 \ -1]$. This mode, with the $[dhq]$ nomenclature is $[111] \rightarrow [011] \rightarrow [101]$. The transition $[111 \rightarrow 011]$ can achieve ZVS because d^+ is opened and the inductor current is positive, but the transition $[011 \rightarrow 101]$ cannot because h^- is opened with $i_L > 0$. Therefore, this mode cannot achieve ZVS

Figure 3.2: Possible ZVS transitions with switching states labeled using the $[dhq]$ and $[g \ s]$ nomenclature, depending on the direction of the inductor current [81].

in all the transitions and should not be used. To summarize, Figure 3.2 can be used to determine directly which modes from the previous chapter can achieve ZVS in the transitions with $i_L > 0$ and $i_L < 0$.

3.2.1 Minimum current and dead time for ZVS

However, the condition for ZVS is only valid provided the direction of the inductor current does not change during the transition. Unfortunately, this is not always the case. Sometimes, the inductor current may be too low and reach zero during the transition before the voltage in the C_{oss} drops to zero. This scenario should be avoided, and it is why it is important to quantify this minimum current in the inductor for ZVS purposes. In this section, this minimum current and dead time required for ZVS are analyzed. There are scenarios where the inductor current may be not enough for ZVS. For instance, in PFC boost converters in BCM, full ZVS can only be achieved when the rectified grid voltage is above half the output voltage, otherwise, only partial ZVS is obtained [84]. To obtain full ZVS transitions, the transition should start when i_L is slightly negative; it should be operated with TCM modulations.

The parasitic capacitances are labeled as C_{d+} instead of $C_{oss_{d+}}(v_{ds_{d+}})$ to avoid extensive nomenclature. Moreover, the dependence of the capacitance as a function of the voltage is neglected in this part of the analysis. Nevertheless, this nonlinearity has an importation role in shaping the transitions, and neglecting it would lead to an inaccurate estimation of the current required for ZVS. The nonlinear effects are introduced in Section 3.3.

As the transitions are considered much shorter than the switching cycle, the voltage in the ports is assumed constant during the transition. Therefore, the following equations relate the voltage in the complementary switches:

$$v_{d-}(t) + v_{d+}(t) = V_g - V_s \quad v_{h-}(t) + v_{h+}(t) = V_s \quad v_{q-}(t) + v_{q+}(t) = V_g \quad (3.2)$$

Also, the inductor current is always flowing through a switch, the complementary switch, or their parasitic capacitances. Put into equations:

$$i_L(t) = i_{d+}(t) - i_{d-}(t) = i_{h+}(t) - i_{h-}(t) = i_{q+}(t) - i_{q-}(t) \quad (3.3)$$

Moreover, in this analysis, the same devices are considered for the six switches, so their C_{oss} is the same. Also, the charge and discharge processes of parasitic capacitances are considered lossless.

3.2. ZVS transitions in this inverter

3.2.2 Transitions where a single device is turned off

In this section, the transitions in which a single switch is opened and the complementary is closed later are explained. The transitions are explained through the example in Figure 3.3, $[111 \rightarrow 110]$ with $i_L > 0$. Then, it is generalized for any transition involving a switch and its complementary. In the figure, the part of the transition where the body diode is conducting current is not drawn as it is not relevant for the analysis. The transition is considered to end when V_{q-} reaches 0. The time the diode conducts is considered as a part of the state after the transition, $[110]$ in this case.

Figure 3.3: $[111 \rightarrow 110]$ transition with positive current in the inductor. The first circuit shows the state before the transition, and the last one the state after the transition. The circuit in the transition and its equivalent circuit are shown in the middle of the figure.

In this section, the time the transition takes to end, $t = T_{tr}$, is calculated, defining $t = 0$ when q^+ is opened. The other objective of the section is to determine whether the current in the inductor when the transition started, $i_L(0)$, is enough to fully discharge C_{q-} . To analyze the transition, the circuit formed by the inductor and the parasitic capacitances in the middle of Figure 3.3 should be analyzed. In this case, $v_L(t) + V_o = v_{q-}(t)$ because d^+ and h^+ are closed, and $i_L(t) = i_{q+}(t) - i_{q-}(t)$ according to Equation 3.3. Therefore, $i_L(t) = -(C_{q+} + C_{q-}) dv_{q-}(t)/dt$ although this equation is only valid if the capacitances are not a function of their voltage. To simplify the notation, the equivalent capacitance seen from the inductor in the transition is named

C_{eq} , and, in this case, $C_{eq} = C_{q+} + C_{q-}$. The equivalent circuit for the transition is shown in the right part of Figure 3.3. The expression for the inductor voltage in this circuit is therefore $v_L(t) = v_{q-}(t) - V_o = -L \cdot C_{eq} \cdot d^2 v_{q-}(t)/dt^2$. This equation can be solved using the initial conditions of the inductor current and inductor voltage in the transition, leading to $v_{q-}(t) = V_o - i_L(0)\sqrt{L/C_{eq}} \sin(t/\sqrt{L \cdot C_{eq}}) + (V_g - V_o) \cos(t/\sqrt{L \cdot C_{eq}})$. The transition time can be obtained from the definition, $v_{q-}(T_{tr}) = 0$. Depending on $i_L(0)$, the transition can be short of fast, and it may happen that $v_{q-}(t) \neq 0$ and ZVS is not achievable if $i_L(0)$ is not high enough.

The same equations can be obtained if any other transition involving two complementary switches is considered. To generalize the analysis, v_{tr} is defined as the voltage in the MOSFET being discharged, in the previous case, $v_{tr} = v_{q-}$. Therefore, in general $v_{tr}(t) = v_L(t) - v_L(T_{tr})$. Also, C_{eq} is defined as the total capacitance involved in the transition, as mentioned before. Then, transitions can be analyzed as before considering the equivalent circuit formed by the inductor, C_{eq} , and the input, store capacitor, and output ports. With these definitions, the voltage and current in the inductor are described by the following equations:

$$\begin{cases} v_L(t) = v_L(0) \cos\left(\frac{t}{\sqrt{L \cdot C_{eq}}}\right) - i_L(0) \sqrt{\frac{L}{C_{eq}}} \sin\left(\frac{t}{\sqrt{L \cdot C_{eq}}}\right) \\ i_L(t) = v_L(0) \sqrt{\frac{C_{eq}}{L}} \sin\left(\frac{t}{\sqrt{L \cdot C_{eq}}}\right) + i_L(0) \cos\left(\frac{t}{\sqrt{L \cdot C_{eq}}}\right) \end{cases} \quad (3.4)$$

These equations can be used to determine whether $i_L(0)$ is enough for ZVS or not, and the value of T_{tr} for $v_L(T_{tr}) = 0$. It is also possible to obtain the inductor current after the transition, $i_L(T_{tr})$. The mathematical expressions to obtain these values can be significantly simplified by realizing that the quantity $v_L(t)^2 + L/C_{eq} \cdot i_L(t)^2$ is conserved during the transition.

This property can be used to obtain a relationship between the initial and final variables:

$$i_L(T_{tr})^2 + \frac{C_{eq}}{L} v_L(T_{tr})^2 = i_L(0)^2 + \frac{C_{eq}}{L} v_L(0)^2 \quad (3.5)$$

It is important to note that the sum of the inductor and capacitor energies is not what it is constant during the transition, which is a common misconception. There is also a certain amount of energy moved to or from the ports, as noted in [69].

The analysis is developed for the transitions with positive inductor current first. The mathematical expressions for the transitions with negative i_L can be obtained similarly. If $i_L(t) > 0$ is assumed, the final current can be directly calculated as:

$$i_L(T_{tr}) = \sqrt{\frac{C_{eq}}{L} (v_L(0)^2 - v_L(T_{tr})^2) + i_L(0)^2} \quad (3.6)$$

When $i_L(0)^2 \gg C_{eq}/L (v_L(0)^2 - v_L(T_{tr})^2)$, $i_L(T_{tr}) \approx i_L(0)$, and $i_L(t)$ is practically constant in the transition. In this case, the transition time is given by $T_{tr} = C_{eq} \cdot v_{tr}(0)/i_L(0)$, which is just the relation between the charge involved in the transition and the inductor current. This equation is commonly found in the literature; unfortunately, sometimes it is applied even when $i_L(0)^2 \approx C_{eq}/L (v_L(0)^2 - v_L(T_{tr})^2)$ as mentioned in [85].

However, if $i_L(0)^2$ is comparable to $C_{eq}/L (v_L(0)^2 - v_L(T_{tr})^2)$, the inductor current can change a lot in the transition. In fact, when $-v_L(T_{tr}) > v_L(0)$ and $i_L(0)^2 < C_{eq}/L (v_L(T_{tr})^2 - v_L(0)^2)$,

3.2. ZVS transitions in this inverter

Equation 3.6 has no solution, meaning that ZVS cannot be obtained. From this inequality, the minimum initial inductor current for ZVS is obtained:

$$i_{L \min}(0) = \begin{cases} \sqrt{\frac{C_{eq}}{L} (v_L(0)^2 - v_L(T_{tr})^2)} & \text{if } i_L(t) > 0 \text{ and } -v_L(T_{tr}) > v_L(0) \\ 0 & \text{if } i_L(t) > 0 \text{ and } v_L(0) > -v_L(T_{tr}) \end{cases} \quad (3.7)$$

For a transition to have ZVS, $i_L(0) > i_{L \min}(0)$. For $i_L(0) = i_{L \min}(0)$ and $-v_L(T_{tr}) > v_L(0)$, $i_L(T_{tr}) = 0$ from Equation 3.5. Therefore, when the current after the transition is exactly zero and $-v_L(T_{tr}) > v_L(0)$, the initial current has the minimum value possible.

Besides this important conclusion, Equation 3.5 can be used to obtain $i_L(T_{tr})$ if $i_L(0)$ is set. This value is used in the next chapter to quantify the variations in the inductor current during the transition, which impact the control of the inverter as discussed in Chapter 5. As mentioned before, sometimes $i_L(T_{tr}) = 0$ if the transition start with $i_{L \min}(0)$. But there are other cases where $i_L(0) = 0$ and ZVS is achieved, as Equation 3.7 states. In those cases, the current after the transition is minimum. These two cases are summarized as:

$$i_{L \min}(T_{tr}) = \begin{cases} 0 & \text{if } i_L(t) > 0 \text{ and } -v_L(T_{tr}) > v_L(0) \\ \sqrt{\frac{C_{eq}}{L} (v_L(T_{tr})^2 - v_L(0)^2)} & \text{if } i_L(t) > 0 \text{ and } v_L(0) > -v_L(T_{tr}) \end{cases} \quad (3.8)$$

Therefore, there are two types of transitions with ZVS, those that can start with $i_L(0) = 0$ and those that can end with $i_L(T_{tr}) = 0$. If $|v_L(0)| > |v_L(T_{tr})|$ then ZVS can be obtained with $i_L(0) = 0$. If, on the other hand, $|v_L(0)| < |v_L(T_{tr})|$, there has to be at least $i_{L \min}(0)$ to get ZVS and, with $i_{L \min}(0)$, $i_L(T_{tr}) = 0$. To clarify this idea, Figure 3.4 shows the different transitions with $i_L > 0$ for different initial and final voltages with minimum current for ZVS.

Figure 3.4: Types of transitions depending on the inductor voltage before and after the transition with minimum inductor current and positive i_L .

In transitions where $v_L(0) > 0 > v_L(T_{tr})$ the maximum current is not found at $t = 0$ or $t = T_{tr}$, but in between, when $v_L(t) = 0$. This is also shown in Figure 3.4. This peak current in the transition is given by:

$$i_{L \text{ pk}} = \sqrt{v_L(0)^2 \frac{C_{eq}}{L} + i_L(0)^2} \text{ if } i_L(t) > 0 \text{ and } v_L(0) > 0 > v_L(T_{tr}) \quad (3.9)$$

The peak current is important to determine the shape of the waveform because even transition where $i_L(0)$ and $i_L(T_{tr})$ are near zero can have a relatively large $i_{L\ pk}$. $i_{L\ pk}$ is important for the the experimental results of Chapter 7, as some operation modes suffer from large peak current in the transitions.

The last parameter that should be obtained from this analysis is T_{tr} . This value is required to determine the minimum dead time needed for the transition. The mathematical process to obtain T_{tr} is skipped, but it is calculated from Equations 3.4 and using the relation in Equation 3.5. The result is:

$$T_{tr} = \sqrt{L \cdot C_{eq}} \cos^{-1} \left(\frac{v_L(0) \cdot v_L(T_{tr}) + i_L(0) \cdot i_L(T_{tr}) \frac{L}{C_{eq}}}{v_L(0)^2 + i_L(0)^2 \frac{L}{C_{eq}}} \right) \quad (3.10)$$

If $i_L(0) = 0$ or $i_L(T_{tr}) = 0$, this equation can be simplified. In these cases, the current is the lowest possible for ZVS, which corresponds to the maximum transition time [1]. The result is:

$$T_{tr\ max} = \begin{cases} \sqrt{L \cdot C_{eq}} \cos^{-1} \left(\frac{v_L(T_{tr})}{v_L(0)} \right) & \text{if } |v_L(0)| > |v_L(T_{tr})| \\ \sqrt{L \cdot C_{eq}} \cos^{-1} \left(\frac{v_L(0)}{v_L(T_{tr})} \right) & \text{if } |v_L(T_{tr})| > |v_L(0)| \end{cases} \quad (3.11)$$

This equation concludes the analysis required to define any transition with a single switch turned off.

3.2.3 Transitions with more switches involved

In this inverter, there are transitions with more than a switch turned off at once. Analyzing these transitions is complicated because multiple capacitances are involved. Moreover, the inductor current waveform is different if a pair of transistors is switched first and then the second pair of transistors instead of switching all transistors at the same time. Unlike other types of converters like the Full-Bridge with bipolar modulation where both branches are charged at the same voltage and it takes the same time to perform ZVS in the two branches, in this inverter the three complementary switches withstand different voltages. Therefore, the transition in each branch takes a different time to complete. As transitions take different times, the whole process should be split into *parts*.

The transitions where more than a device is turned off at the same time are listed in the second and third column of Equation 3.1 for $i_L > 0$. When two pairs of devices are switched at once, the transition is divided into two parts. The transition $[111 \rightarrow 100]$ depicted in Figure 3.5 is used to illustrate the concept. In the first part of this transition, $i_L = i_{h+} - i_{h-} = i_{q+} - i_{q-}$ and the four parasitic capacitances resonate with the inductor. As a result, the pair of switches with the lower charge, in this case, the h branch, is discharged first. Therefore, this part of the transition ends when C_{h-} is fully discharged. The total charge involved in the first part of the transition is named Q^i in this analysis. To describe the first part of the transition Equations 3.7, 3.8, and 3.11 are still valid but considering that the equivalent capacitance seen from the inductor is $C_{eq}^i = (C_{q+} + C_{q-}) || (C_{h+} + C_{h-})$ and replacing the total transition time, T_{tr} , with the one of the first part, namely T_{tr1} .

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Figure 3.5: [111 → 100] transition, divided into two parts.

The challenge with these types of transitions is that $v_L(T_{tr1})$ is not known beforehand. It depends on the voltage left in the q branch. It can be calculated if constant and equal capacitances are considered. Since both branches would be discharged the same amount, in this example, it would mean $v_{q-}(T_{tr1}) = V_g - V_s$. However, this is not the case once the nonlinear behavior of the capacitances is introduced. This issue is addressed in the next section.

Then, the second part of the transition starts once h^- is discharged. The current flows through the body diode of h^- and, at the same time, it moves the charge left in the q branch. In this part, only the q capacitors resonate with the inductor. This transition can be analyzed again with equations from the previous section but replacing $t = 0$ with T_{tr1} . Note that for this part of the

analysis $v_L(T_{tr1})$ is required too. Once h^- is fully discharged, at $t = T_{tr}$, full ZVS is obtained. This transition takes place in the modes $T2^-$ and $T3^-$ described in the following chapter.

Finally, the most complex ZVS transitions are $[111 \rightarrow 000]$ with $i_L > 0$ or $[000 \rightarrow 111]$ with $i_L < 0$, because three switches are turned off at once. To clarify the process, the transition $[111 \rightarrow 000]$ with positive current in the inductor, shown in Figure 3.6, is described. This transition is divided into three different parts with different capacitances involved each.

In this transition, the q branch has the highest charge stored, as it withstands the highest voltage. For $V_s > V_g/2$, the second devices with the higher charge are h^+ and h^- . Finally, the pair of switches with the lowest charge is the d branch. That is why d^- is discharged first, followed by h^- and finally q^- .

When d^+ , h^+ , and q^+ are turned off, the inductor current flows through the parasitic capacitances of the six devices. Thus, in this first part of the transition, the same charge is moved in the three pairs of complementary switches, named Q^i . The previous equations remain valid if $C_{eq}^i = (C_{q^+} + C_{q^-}) || (C_{h^+} + C_{h^-}) || (C_{d^+} + C_{d^-})$ is considered. As before, $v_L(T_{tr1})$ is required to solve Equations 3.7, 3.8 and 3.11. $v_L(T_{tr1})$ depends on how much h^- and q^- are discharged in this part of the transition. Those voltages would be $v_{h^-}(T_{tr1}) = V_s - (V_g - V_s)$ and $v_{q^-}(T_{tr1}) = V_g - (V_g - V_s)$ assuming constant capacitances.

Then, once d^- is discharged and its body diode conducts the current, the second part of the transition starts. Now the inductor resonates with $C_{eq}^{ii} = (C_{q^+} + C_{q^-}) || (C_{h^+} + C_{h^-})$, until h^- is fully discharged. At this point, the voltage left in q^- is required for the equations, which, with the simplification of constant and equal capacitance, would be $v_{q^-}(T_{tr2}) = V_g - V_s$.

In the last part of the transition, the inductor moves the charge left in the q branch, and again the same equations apply but using $C_{eq}^{iii} = C_{q^+} + C_{q^-}$ and replacing $t = 0$ with $t = T_{tr2}$.

With the analysis divided into three parts, $i_L(T_{tr})$ can be obtained given $i_L(0)$, or the minimum $i_L(0)$ that is required to ensure ZVS transitions can be calculated. The total time of the transition can be obtained as well. It is concluded that all transitions can be analyzed using Equations 3.7, 3.8, and 3.11 if applied separately to each part of the transition. Note that when more than a branch is involved, it is not possible to determine whether a transition can start or end with $i_L = 0$ only based on the initial and final voltages.

3.3 Effects of nonlinear capacitances

So far, analytic equations have been obtained and applied to transitions considering a constant C_{oss} . Unfortunately, this is not the case as C_{oss} strongly depends on v_{ds} . This section describes how to obtain the parameters required to be able to use Equations 3.4 and the previous analysis when nonlinear capacitances are considered.

Since there is no analytic relationship between C_{oss} and v_{ds} , analytic solutions cannot be obtained. For an accurate estimation of the ZVS current and dead time, simulations or iterative processes would be required. However, the modulation of the inverter has many different transitions that are different along the line cycle. Therefore, it would be very hard to obtain meaningful results out of a reduced number of simulations for instance. Moreover, it is not practical to realize

3.3. Effects of nonlinear capacitances

Figure 3.6: [111] → [000] transition with $i_L > 0$.

simulations for every possible point of operation. An approximation to $C_{oss}(v_{ds})$ is preferred in this case.

3.3.1 Time-related capacitance to model the parasitic capacitances

The analysis can be simplified using the *time-related capacitance* for the value of C_{oss} to overcome this problem, as described in [69]. A constant capacitance for the transition (or part of the transition) is considered instead of accounting for the variations of capacitance with v_{ds} . The *time-related capacitance* is defined as the charge in the C_{oss} over the voltage applied to the switch in the transition or part of the transition. Given $C_{oss}(v_{ds})$, the drain-source charge can be calculated as:

$$Q_{oss}(v_{ds}) = \int_0^{v_{ds}} C_{oss}(u_{ds}) du_{ds} \quad (3.12)$$

Then, the time-related capacitance of a switch charged or discharged from zero to V_{dd} is given by:

$$C_{tr}|_0^{V_{dd}} = \frac{Q_{oss}(V_{dd})}{V_{dd}} \quad (3.13)$$

This is the average value of the capacitance in the transition. Figure 3.7 a) and b) shows the C_{oss} and Q_{oss} of two GS66516T devices from *GaN Systems* in parallel, as this used for the experimental validation in Chapter 7. These data points are obtained from the datasheet of the device, available in [86]. Figure 3.7 c) shows the value of C_{tr} as a function of V_{dd} . The interpretation of C_{tr} at 200 V and 400 V is shown in the Q_{oss} plot to clarify the idea. This work is based on [69], where a similar plot and description can be found. Although, in that paper, the analysis is only valid when the initial inductor voltage is zero and a single switch is turned off.

Figure 3.7: Drain-source capacitance and charge for two GS66516T GaN devices in parallel,[86], based on [69].

Using C_{tr} instead of C_{oss} in the equations of the previous section can approximate the behavior of transitions involving a switch and its complementary (Section 3.2.2). If the same devices are used, the C_{tr} of the high and low side device is the same as the voltage of one device goes from 0 to V_{dd} and the voltage in the complementary goes from V_{dd} to 0. Therefore, the equivalent capacitance is $C_{eq} = 2 \cdot C_{tr}|_0^{V_{ds}}$. If the total charge of the transition is defined as Q_{tr} , then the equivalent capacitance can also be expressed as $C_{eq} = Q_{tr}/V_{dd}$, where $Q_{tr} = \int_0^{T_{tr}} i_L(t) dt$.

3.3. Effects of nonlinear capacitances

However, analyzing a part of a transition where the final voltage is not zero requires a more general definition for C_{tr} . C_{tr} is then defined as the average capacitance between two values of drain-source voltage, namely V_{dd1} and V_{dd2} :

$$C_{tr}|_{V_{dd1}}^{V_{dd2}} = \frac{Q_{oss}(V_{dd2}) - Q_{oss}(V_{dd1})}{V_{dd2} - V_{dd1}} \quad (3.14)$$

This C_{tr} is only the value of the high side or the low side switch capacitance. Both capacitances have to be obtained to calculate the equivalent capacitance of the branch. In this case, the charge of the high side and low side capacitances would be different; one device is charged from 0 to $V_{dd1} - V_{dd2}$ and the other is discharged from V_{dd1} to V_{dd2} . The total charge in the branch, in that case, is, therefore:

$$Q_{eq} = Q_{oss}(V_{dd1}) - Q_{oss}(V_{dd2}) + Q_{oss}(V_{dd1} - V_{dd2}) \quad (3.15)$$

For the capacitance shown in Figure 3.7, the value of this charge is in Figure 3.8 b) for different values of V_{dd1} and V_{dd2} . The equivalent capacitance of the branch for this charge would be:

$$C_{eq} = C_{tr}|_{V_{dd2}}^{V_{dd1}} + C_{tr}|_0^{V_{dd1}-V_{dd2}} = \frac{Q_{oss}(V_{dd1}) - Q_{oss}(V_{dd2}) + Q_{oss}(V_{dd1} - V_{dd2})}{V_{dd1} - V_{dd2}} \quad (3.16)$$

Figure 3.8: Charge between two voltages and its associated *time-related capacitance*, for $V_{dd1} > V_{dd2}$ a) Q_{eq} b) C_{eq} , when $V_{dd2} = 0$ the values are equivalent to the plot in Figure 3.7.

The equivalent capacitance for different values of V_{dd1} and V_{dd2} is shown in Figure 3.8 b). Equation 3.16 and this plot are required to calculate the equivalent capacitance seen from the inductor in transitions divided into parts when devices are not fully discharged. This value can also be used to model *incomplete* or *partial* ZVS transitions, where less charge than Q_{tr} is moved in the transition, and the capacitances are not fully discharged/charged.

An additional problem of transition involving four or six switches is to obtain $v_L(T_{tr1})$ and $v_L(T_{tr2})$ as they are a function of how much each parasitic capacitance is discharged. For instance, in the transition of Figure 3.5, the voltage in the q branch after the first part depended on the total charge of the q branch minus the h branch. This charge can be easily obtained. Unfortunately, the voltage has to be calculated through a look-up table that relates voltage with the remaining charge in the branch. This concept is clarified in the example given in the following subsection.

With these considerations, the capacitances and voltages required for Equation 3.5 can be obtained even when the capacitances are not fully discharged or fully charged.

3.3.2 Detailed analysis of the $[111 \rightarrow 000]$ transition

The transition $[111 \rightarrow 000]$ of Figure 3.6 in a specif operation point is analyzed in detail to clarify how to account for the nonlinear C_{oss} . The goal is to obtain the transition times and initial or final inductor current, given the port voltages, the inductance value, and the value of C_{oss} from Figure 3.7. For this purpose, a sequence of operations is required. This sequence is shown in the diagram in Figure 3.9, as a more extensive description of what was described in [81]. First, the charge of the three complementary switches is calculated, as it determines the charge involved in each part of the transition. Then, the voltage across devices at the end of each part is obtained. With this information, the equivalent capacitances can be determined. Finally, T_{tr} and $i_L(T_{tr})$ are obtained given L , $i_L(0)$, and V_o by applying Equations 3.7, 3.8, and 3.11 in each part of the transition.

Figure 3.9: Sequence of operations used to analyze the $[111 \rightarrow 000]$ transition.

A similar diagram could be used to calculate other transitions with two and four switches involved. The rest of the section is dedicated to calculating those parameters for the example $[111 \rightarrow 000]$ following the diagram in Figure 3.9. This transition is very important as it takes place in all Tra^n modes, and its $i_{L \min}(0)$ considerably impacts the proposed TCM modulation. For this example $V_g = 400$ V and $V_s = 300$ V, $V_o = -200$ V, and $L = 80$ μ H are considered.

3.3. Effects of nonlinear capacitances

Charges involved in each part of the transition

In the first part of the transition, labeled i , d^+ is fully discharged. Since $v_{d^-}(0) = V_g - V_s = 100$ V, the total charge stored in the d devices is $Q_d = 2 \cdot Q_{oss}(V_g - V_s) \approx 2 \cdot 122.5$ nC from Figure 3.7 b). Q_d is the charge involved in this part of the transition as it is the lower, named as Q_{tr}^i . The charge associated with the second part of the transition, ii , is the charge left in the h branch once d^- is fully discharged, this is $Q_h - Q_d$, where $Q_h = 2 \cdot Q_{oss}(V_s) \approx 269.5$ nC. Therefore $Q_{tr}^{ii} \approx 147$ nC. Finally, the remaining charge in the q branch for part iii is $Q_q - Q_h$ where $Q_q = 2 \cdot Q_{oss}(V_g) \approx 322.5$ nC, leading to $Q_{tr}^{iii} \approx 53$ nC.

Calculate the voltages for the transition

Once the charges involved in the parts of the transitions are known, the next step is to obtain the voltages at the end of each part. Given the charge in the devices and the initial voltage, the voltage at the end can be directly obtained since the data in Figure 3.8 determine the relationship between charge and voltage for the C_{oss} .

In part i , Q_{tr}^i is the charge moved in the h and q pair of switches. It means that in the q branch $Q_{oss}(V_s) - Q_{oss}(v_{h^-}(T_{tr1})) + Q_{oss}(V_s - v_{h^-}(T_{tr1})) = Q_{tr}^i$. From this relation $v_{h^-}(T_{tr1})$ can be identified Figure 3.8 a). For $V_{dd1} = V_s = 300$ V and $Q = Q_{tr}^i \approx 245$ nC, $V_{dd2} = v_{h^-}(T_{tr1}) \approx 95$ V. Similarly, for the q branch $Q_{oss}(V_g) - Q_{oss}(v_{q^-}(T_{tr1})) + Q_{oss}(V_g - v_{q^-}(T_{tr1})) = Q_{tr}^i$, then $v_{q^-}(T_{tr1}) \approx 166$ V. At the end of part ii , the voltage in q^- , $v_{q^-}(T_{tr2})$, can be obtained from $Q_{oss}(v_{q^-}(T_{tr1})) - Q_{oss}(v_{q^-}(T_{tr2})) + Q_{oss}(V_g - v_{q^-}(T_{tr2})) - Q_{oss}(V_g - v_{q^-}(T_{tr1})) = Q_{tr}^{ii}$, in this case, approximately 25 V.

To obtain the voltage after each part of the transition, a look-up table, which is equivalent to use the first plot in Figure 3.8. With these values, the initial and final voltage in the inductor for each part can be calculated: $v_L(0) = V_g - V_o = 600$ V, $v_L(T_{tr1}) = -V_g - V_o + v_{h^-}(T_{tr1}) + v_{q^-}(T_{tr1}) = 61$ V, $v_L(T_{tr2}) = -V_g - V_o + v_{q^-}(T_{tr2}) = -59$ V and $v_L(t_{tr}) = -V_g - V_o = -200$ V.

Obtain the equivalent capacitances

With the voltages after each part and the charges involved, the equivalent capacitances for every switch can be obtained, and then the total C_{eq} can be calculated.

For part i , $C_{d^+}^i + C_{d^-}^i = Q_{tr}^i / (V_g - V_s) \approx 2.45$ nF, $C_{h^+}^i + C_{h^-}^i = Q_{tr}^i / (V_s - v_{h^-}(T_{tr1})) \approx 1.20$ nF, and $C_{q^+}^i + C_{q^-}^i = Q_{tr}^i / (V_g - v_{q^-}(T_{tr1})) \approx 1.05$ nF. Therefore, the equivalent capacitance of the first part is $C_{eq}^i = 2.45$ nF || 1.20 nF || 1.05 nF ≈ 0.45 nF. In part ii , $C_{h^+}^{ii} + C_{h^-}^{ii} = Q_{tr}^{ii} / (V_g - v_{h^-}(T_{tr1})) \approx 1.54$ nF, and $C_{q^+}^{ii} + C_{q^-}^{ii} = Q_{tr}^{ii} / (v_{q^-}(T_{tr1}) - v_{q^-}(T_{tr2})) = 1.04$ nF. Therefore $C_{eq}^{ii} = 0.62$ nF. Finally, in the last step $C_{q^+}^{iii} + C_{q^-}^{iii} = Q_{tr}^{iii} / v_{q^-}(T_{tr2}) = 2.14$ nF, which is directly C_{eq}^{iii} .

Obtain the currents and transition times

The transition is analyzed for $i_L(0) = 0$. For the first part, applying Equation 3.5, $i_L(T_{tr1}) \approx 1.42$ A, and, using Equation 3.10, $T_{tr}^i = T_{tr} \approx 280$ ns. Again with the same equations, but replacing $t = 0$ with T_{tr1} and T_{tr} with T_{tr2} , $i_L(T_{tr2}) \approx 1.35$ A in a time of $T_{tr}^{ii} \approx 104$ ns,

leading to $T_{tr2} = T_{tr}^i + T_{tr}^{ii} \approx 384$ ns. In part *ii*, the minimum current is reached, $i_{Lpk} \approx 1.43$ A, given by Equation 3.9. Finally, in the third part $i_L(T_{tr}) \approx 1.25$ A and $T_{tr}^{iii} \approx 41$ ns; therefore, the total transition time is $T_{tr} \approx 425$ ns. The transition is represented in Figure 3.10, showing the different parts, and the approximate shape of the waveform based on the values described here.

Figure 3.10: Voltage and current waveform of the $[111 \rightarrow 000]$ transition, for $V_g = 400$ V, $V_s = 300$ V, $V_o = -200$ V, $i_L(0) = 0$, $L = 80$ μ H and two GS66516T per switch.

This methodology can be extended to obtain T_{tr} , the minimum $i_L(0)$, or the minimum $i_L(T_{tr})$ for any transition and under different conditions of V_g , V_s , and V_o . For this purpose, a *Matlab* script is designed that outputs these values given the initial and final states and the port values. It should be noted that the analysis is complicated because of the multimode and multiport nature of this inverter. The minimum current for different transitions and different port values are included in Appendix A. Not all the possible transitions are used in the modulation proposed, so only the transitions of interest are studied.

3.3.3 Validation through simulation

A simulation in *Gecko Circuit* for the $[111 \rightarrow 000]$ transition exemplified before has been developed to prove the validity of the methodology described in this chapter and to quantify the error due to the assumption of constant capacitance in the parts of the transition. In the simulation, each parasitic capacitor is modeled with the data-points of Figure 3.7 a). The simulation consists of capacitances and diodes to model the switches in the transition, voltage sources for the three ports, and the inductor. The initial condition for the inductor is set to $i_L(0) = 0$, and the capacitor voltages are set so $v_{d+}(0) = v_{h+}(0) = v_{q+}(0) = 0$, coinciding with the point where d^+ , h^+ and q^+ are opened. The circuit and simulation results are plotted in Figure 3.11.

The transition is very similar to the one obtained theoretically in Figure 3.10. The nonlinear behavior of the capacitances causes small mismatches. The voltages in the simulation after each

3.4. Conclusion

Figure 3.11: Simulation of the $[111 \rightarrow 000]$ transition, for $V_g = 400$ V, $V_s = 300$ V, $V_o = -200$ V, $L = 80$ μ H and $i_L(0) = 0$.

part of the transitions are $v_{h-}(T_{tr1}) \approx 94$ V, $v_{q-}(T_{tr1}) \approx 165$ V and $v_{q-}(T_{tr2}) \approx 25$ V. These values perfectly match the theoretical ones as they come from the charge analysis through look-up tables, which is not an approximation. The following times are measured in simulation: $T_{tr1} \approx 272$ ns, $T_{tr2} \approx 98$ ns, and $T_{tr3} \approx 39$ ns, so the total transition time is $T_{tr} \approx 409$ ns. The measured currents in those times are $i_L(T_{tr1}) \approx 1.52$ A, $i_L(T_{tr2}) \approx 1.42$ A, and $i_L(T_{tr}) \approx 1.33$ A. The measured time is 16 ns shorter than the expected value, which is a 4 % error, and the current is 8 mA above the expected value, a 6 % error. Therefore, it can be concluded that the results are accurate even when the *time-related capacitance* is used.

3.4 Conclusion

In this chapter, a methodology to obtain the current and dead time required to achieve ZVS transitions is proposed, detailing what is explained in [81]. The analysis can be applied to any transition in this inverter and under different voltages in the three ports. It uses the *time-related capacitance* to model the nonlinear behavior the C_{oss} as a function of the drain-source voltage. With this simplification, analytic equations can be used to obtain the different parameters that define the transition. Analytic equations are useful to reduce the computational cost when many transitions are calculated and to avoid the use of simulations or iterative processes. Also, the concept has been validated in simulation showing a small error due to the nonlinear C_{oss} ; other sources of error such as tolerances can have a larger impact in the calculation of the current and the transition time.

This analysis is required to determine the current for the TCM modulation that is going to be described in the following chapter. For the buck converter with TCM modulation of Figure 2.1, the negative current should be minimized to reduce rms and peak current and indirect power, but it should be large enough to guarantee ZVS. A similar concept applies for the TCM modulation of this inverter, a certain amount of current is required for ZVS, but higher values lead to higher

rms and peak current in the inductor. In other words, as little current for ZVS as possible should be used to maximize efficiency. The analysis proposed here is useful for that purpose.

This methodology is an extension of the work in [69], to include transitions with more than a switch turned off simultaneously and different voltages in devices, so that it can be applied to any other converter with these features. ZVS in converters does not often require such a complex treatment, as bus voltages can be considered constant, or no more than a device is switched at once, or all devices withstand the same voltage and the transitions do not have to be divided into parts.

Multimode modulation with ZVS

The description of the modulation of the inverter to obtain a sinewave output voltage and constant input current along the line cycle was described in Chapter 2. The modulation selected was the combination of the triangular and trapezoidal modes with lower indirect power in the inductor along the line cycle [16]. In Chapter 3, ZVS transitions were introduced, describing which transitions from a switching state to the next one can achieve ZVS depending on the direction of the current. The dead time and minimum current required for this purpose are covered in Appendix A and the results are directly used in this chapter.

This chapter continues with the description of the modulation but restricted to operation modes with ZVS in all transitions. First, the operation modes used in the BCM modulation are described, considering ZVS only in the transitions with $i_L \neq 0$. The modulation for different loads, including inductive and capacitive is described. Then, the range of operation for different modes is identified, obtained as a function of the voltage and current of the three ports. Later in this chapter, a TCM modulation is proposed to achieve ZVS in the transitions where i_L is zero in the BCM modulation. This TCM modulation has additional benefits that are also discussed in the chapter.

4.1 BCM modulation with ZVS when $i_L \neq 0$

For the modulation, only Tra^p , Tra^n and T modes shown in Figure 2.11 are considered as described in Section 2.2.2. In these modes, there are two transitions with current equal to zero and two transitions with positive or negative current. For instance, in Tra^p modes there are two transitions with positive current in the inductor (Figure 2.11 a)), while in T modes one transition has positive current and the other negative current (Figure 2.11 c)). In this section, the modes with the lowest indirect power that also achieve ZVS in the transitions where the current is not zero are identified. How to achieve ZVS transitions when $i_L = 0$ is described later in Section 4.3.

To select operation modes with ZVS, the diagram of Figure 3.2 is used. The transitions with ZVS from one state to another are listed as a function of the direction of the current in that diagram. It can be directly applied to those transitions with positive or negative current in the inductor in the different operation modes. In these transitions with $i_L \neq 0$, it is assumed that the current is high enough, and ZVS can be achieved. Also, the dead time is considered negligible compared with the time different states last. Finally, the variations of the inductor current along the transitions are neglected [79]. These assumptions are not valid in general, but they are helpful in introducing the modulation. The assumptions are reconsidered once the TCM modulation is introduced in Section 4.4.

Considering only transitions with ZVS reduces substantially the number of possible operation modes. Most of the lines that represented an operation mode in Figure 2.16 are removed because of the lack of ZVS transitions. The number of possible Tra^p modes is reduced to just twelve, listed in Table 4.1. This table is included to clarify how ZVS restricts the possible operation modes in this inverter. The same table could be obtained for Tra^n modes or T modes, although in this last case, the number of possible operation modes is still large.

$[dhq]$ nomenclature	$[g \ s]$ nomenclature
$[111] \rightarrow [110] \rightarrow [100]$	$[+1 \ 0] \rightarrow [0 \ 0] \rightarrow [0 \ -1]$
$[111] \rightarrow [110] \rightarrow [010]$	$[+1 \ 0] \rightarrow [0 \ 0] \rightarrow [-1 \ +1]$
$[111] \rightarrow [101] \rightarrow [100]$	$[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [0 \ -1]$
$[111] \rightarrow [101] \rightarrow [001]$	$[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [0 \ 0]$
$[111] \rightarrow [101] \rightarrow [000]$	$[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [-1 \ 0]$
$[111] \rightarrow [011] \rightarrow [010]$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [-1 \ +1]$
$[111] \rightarrow [011] \rightarrow [001]$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$
$[111] \rightarrow [011] \rightarrow [000]$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [-1 \ 0]$
$[111] \rightarrow [100] \rightarrow [000]$	$[+1 \ 0] \rightarrow [0 \ -1] \rightarrow [-1 \ 0]$
$[111] \rightarrow [010] \rightarrow [000]$	$[+1 \ 0] \rightarrow [-1 \ +1] \rightarrow [-1 \ 0]$
$[101] \rightarrow [100] \rightarrow [000]$	$[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ 0]$
$[101] \rightarrow [001] \rightarrow [000]$	$[+1 \ -1] \rightarrow [0 \ 0] \rightarrow [-1 \ 0]$

Table 4.1: All Tra^p modes that can attain ZVS in the two transitions with $i_L > 0$ using $[dhq]$ nomenclature in the left and $[g \ s]$ nomenclature in the right.

The Tra^p mode $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [+1 \ -1]$ with minimum indirect power described in Chapter 2 is not in the list as ZVS cannot be achieved in the transition $[0 \ +1] \rightarrow [+1 \ -1]$ because $i_L > 0$ (as it is not in the diagram from Figure 3.2). Then, this mode is not considered for the modulation.

4.1.1 Indirect power in the inductor applied to modes with ZVS

To obtain the modulation of the inverter considering ZVS, the *Matlab* script employed in Section 2.2.3.2 can be used to determine the indirect power of each mode, but this time only considering the operation modes with ZVS transitions. The indirect power in the inductor of this reduced number of modes can be plotted against the line angle. As before, more than a mode that can work at each point of the line cycle. This plot is shown in Figure 4.1, for resistive load and at full power (1 kVA). The ports voltages and currents with this load were shown in Figure 1.10 and are not repeated in this one.

Since the ZVS condition was not applied to the modulation described in Chapter 2, comparing the results obtained in this chapter with the one obtained before shows the cost that soft-switching has in terms of P_{indL} . The indirect power of the modulation when ZVS was not considered is depicted as a black dashed line in this plot. The results with and without ZVS are similar. The fundamental difference is that the Tra^p and Tra^n modes with minimum indirect power cannot be applied as they do not feature ZVS as mentioned earlier. As for the T modes, those with minimum indirect power are still appropriate.

4.1. BCM modulation with ZVS when $i_L \neq 0$

Figure 4.1: P_{indL} along the line cycle for the modes with ZVS for all possible Tra^p , Tra^n and T . The dashed line represents the minimum indirect power in this inverter obtained in Chapter 2 when ZVS was not considered.

The modulation selected is the combination of the operation modes with minimum P_{indL} and ZVS. To clarify this concept, Figure 4.2 shows only the modes with minimum indirect power. The sectors of the line cycle where the modes are used are also shown. These sectors are a function of the voltage and current of the three ports. In this plot, the modes are labeled independently, as is more comfortable to refer to specific operation modes with their name instead of using the sequence of states. Only the modes with minimum indirect power have been named, and their corresponding sequence of states is included later in Table 4.2.

In Figure 4.2, the sinewave starts with $T0$, the mode with minimum indirect power described in Section 2.2.3.1 when the output voltage and current are zero. Then, once $V_o = V_g - V_s$ (the first vertical line in the plot), $T0$ can no longer be applied, and $T1^+$ has to be used instead. When $I_g = I_o$, this mode finds a boundary, and $Tra3^+$ is applied. This mode lasts until $I_s = 0$, and then $Tra4^+$ is used. $Tra4^+$ is equivalent to the operation of the modified TIBuck described in Section 2.1.3. This one is used when the input and storage capacitor provide power to the output, so it lasts until $I_s = 0$ is reached again. Then $Tra3^+$, followed by T_1 and $T0$, are applied one more time. For the second half-cycle, where the output voltage is negative, the same process is repeated but replacing the positive modes ($^+$) with negative modes ($^-$).

Figure 4.2 shows the modes required when resistive loads are used; however, capacitive and inductive loads require a few more modes than the seven listed here. The same plot as before can be obtained but for a $PF = 0.7$ capacitive load and 1 kVA. The result is shown in Figure 4.3, including the voltage and current in the ports. Unlike the previous case, in Figure 4.3 the sinewave starts directly in $T1^-$ when $I_o = 0$. Because of the 45° phase between the output current and voltage, in this point, $V_o < -V_g + V_s$. After $T1^-$, a new mode, $Tra1^+$, is used (since $I_s > I_g$ and, in that case, $Tra3^+$ cannot be applied). $Tra1^+$ works until $I_o = -I_g - 2I_s$ when $Tra2^+$, another mode that is not used for resistive loads, is applied. After this one, once $I_g > I_s$, $Tra3^+$ is applied.

Figure 4.2: P_{indL} of the selected modes for 1 kVA, resistive load ($PF = 1$).

Then, again, when I_s reaches zero, $Tra4^+$ starts. This time, the first quarter of the cycle does not use the same modes as the second quarter. Between $Tra3^+$ and $T1^+$, $T2^+$ appears shortly, a mode that was not used for resistive loads because $T1^+$ can only work for $V_o < V_s$. Finally, the positive part of the cycle ends with $T1^+$. The sequence is repeated with the complementary modes for the second half of the line cycle.

The results for $PF = 0.7$ inductive load at 1 kVA are shown in Figure 4.4. The phase between output current and voltage is not the only difference compared to the previous case; the storage capacitor voltage is shifted too. In the previous case, V_s was at its minimum when the output voltage was almost at its maximum. Now $V_s > V_o$ the whole line cycle, explaining why $T2^+$ and $T2^-$ are not required in this case. The rest is very similar, although the first mode is $T1^+$ instead of $T1^-$ this time.

Finally, the light load is illustrated in Figure 4.5 for 250 VA $PF = 1$, which is 25 % of the maximum load specified. The same modes used in Figure 4.2 are applied, although the sectors of the cycle where the different modes are used are slightly different. The reason is that the storage capacitor voltage swing is smaller because the power is low, and also that the input voltage is high (as mentioned in the specifications, the input voltage is given by $V_g = 450 \text{ V} - 20 \Omega \cdot I_g$). Also, as

4.1. BCM modulation with ZVS when $i_L \neq 0$

Figure 4.3: P_{indL} of the selected modes for 1 kVA, $PF = 0.7$ capacitive load.

the swing in V_s is small, the first and second quarters of the line cycle are very symmetric. The modes are the same because their limits do not depend on the power, just on the relation between port voltages or port currents.

A total of thirteen modes are required to operate this inverter under different loads.

4.1.1.1 Effects of the storage capacitor voltage

Before this analysis is concluded, the design of the storage capacitor port is discussed. As mentioned in Chapter 2, a 90 μF storage capacitor swinging around 340 V was selected. A smaller capacitor and a larger voltage swing could be considered to reduce the size of the storage capacitor for the same amount of energy buffered. If that were the case, the voltage swing would be higher, and the current in the capacitor would be increased substantially, and a different set of operation modes would be required. This is represented in Figure 4.6 for 1 kVA resistive load, where the capacitance has been reduced from $C_s = 90 \mu\text{F}$ to $C_s = 37 \mu\text{F}$, near the minimum possible. Compared to Figure 4.2, the indirect power increases considerably and the inductor would probably be oversized; this is the main reason why the storage capacitor is not decreased.

 Figure 4.4: P_{indL} of the selected modes for 1 kVA $PF = 0.7$ inductive load.

In this plot, there are six new modes, four T modes used for high output current, when Tra^p or Tra^n modes cannot be used, marked in yellow and named Th . The other two new modes are T modes that only work for $V_s < V_g/2$, used when the output voltage is low.

The main problem with the modulation with low C_s is that Th modes are required. The only difference compared to the other T modes is that they are applied when the output current is very high. Therefore, to get a high average current in the inductor, modes where the inductor current has two switching states with negative current have to be used. Hence, a large inductor ripple is expected. The peak inductor current is higher than $2 \cdot I_o$, leading to higher conduction losses in devices and worse performance of the inductor.

For this reason, Th modes should be avoided and $C_s = 90 \mu\text{F}$ selected. As shown in Figures 4.2, 4.3, 4.4, and 4.5, under normal conditions, Th modes are not applied. However, in a load step or abnormal voltage in the storage capacitor, these modes may be required. Moreover, $Th1^+$ and $Th1^-$ are used when there is no load, and the only *effective* load is the output capacitor; this is elaborated in Chapter 7.

With the analysis of the inverter under different loads and storage capacitor conditions, nineteen different modes performing minimum P_{indL} have been found. To conclude this section, these modes

Figure 4.5: P_{indL} of the selected modes for 250 VA resistive load.

and their sequence of switching states are listed in Table 4.2 showing the $[g \ s]$ nomenclature of their states, as it is convenient now that ZVS has already been considered. A representation of the inductor current in these modes is depicted in Figure 4.7.

4.1.2 Voltage and current limits of the operation modes

With this modulation, operation modes are not always followed by the same mode in the line cycle. For instance, $Tra3^+$ can come after $T1^+$ or $Tra2^+$, depending on the conditions. The range of operation where a mode is applied is constrained to certain currents and voltages in the ports. This section explains the voltage and current limits of the modes, to extend the work of Regina Ramos and Iñigo Zubitur presented in [39] and completed in [87].

4.1.2.1 Voltage limits in modes

Modes must satisfy certain voltage conditions. As discussed in Section 2.2.2, Tra^p modes can only work if $V_1 > 0$ and $V_3 < 0$. Interestingly, ZVS transitions enforce this situation. There are no ZVS transitions with $i_L > 0$ where the voltage after the transition is higher than the voltage before it.

Figure 4.6: P_{indL} for 1 kVA resistive load with $C_s = 37 \mu\text{F}$ and the same maximum voltage $V_{smax} \approx 380 \text{ V}$.

The voltage in a switching state as a function of the g and s values are given by Equation 2.11: $v_L = g \cdot V_g + s \cdot V_s - V_o$. As a result, the mode $Tra4^+$, $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$ for instance only works for $V_g - V_o > 0$ for the first state to have a positive slope in i_L . This condition is always met. Nevertheless, for the third state to have a negative voltage, $-V_o < 0$, which limits the operation of the mode.

Similar conditions apply to T and Tra^n modes as described in Chapter 2. For instance, $T0$ ($[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$) can only operate for $V_g + V_s > V_o$, $-V_s < V_o$, $-V_g + V_s < V_o$ and $V_s > V_o$, the conditions for each state respectively. For $V_s > V_g/2$ all the voltage limits in $T0$ can be written as $V_g + V_s > V_o > -V_g + V_s$. The inductor current waveform in the limits is depicted in the top part of Figure 4.8 b), for $V_g + V_s = V_o$ (left) or $V_o = -V_g + V_s$ (right). In both cases, the BCM waveform is no longer defined as the slope of one of the switching states is zero. In these limits, the inductor current waveform is not defined. This issue is elaborated in Section 4.3.2.

The conclusion from this short discussion is that operation modes have a limited range of voltage in the three ports where they are defined. Table 4.3 summarizes the voltage limits in each

4.1. BCM modulation with ZVS when $i_L \neq 0$

Mode	[g s] sequence
$Th2^+$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ -1] \rightarrow [+1 \ -1]$
$Th1^+$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [+1 \ -1] \rightarrow [+1 \ 0]$
$Tra4^+$	$[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$
$Tra3^+$	$[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [0 \ 0]$
$Tra2^+$	$[+1 \ -1] \rightarrow [0 \ 0] \rightarrow [-1 \ 0]$
$Tra1^+$	$[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ 0]$
$T3^+$	$[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [0 \ +1] \rightarrow [+1 \ 0]$
$T2^+$	$[0 \ +1] \rightarrow [+1 \ -1] \rightarrow [0 \ +1] \rightarrow [+1 \ 0]$
$T1^+$	$[0 \ +1] \rightarrow [+1 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$
$T0$	$[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$
$T1^-$	$[+1 \ -1] \rightarrow [0 \ -1] \rightarrow [-1 \ 0] \rightarrow [-1 \ +1]$
$T2^-$	$[0 \ -1] \rightarrow [-1 \ 0] \rightarrow [-1 \ 0] \rightarrow [-1 \ +1]$
$T3^-$	$[0 \ -1] \rightarrow [-1 \ 0] \rightarrow [-1 \ +1] \rightarrow [0 \ +1]$
$Tra1^-$	$[-1 \ +1] \rightarrow [0 \ +1] \rightarrow [+1 \ 0]$
$Tra2^-$	$[-1 \ +1] \rightarrow [0 \ 0] \rightarrow [+1 \ 0]$
$Tra3^-$	$[-1 \ 0] \rightarrow [-1 \ +1] \rightarrow [0 \ 0]$
$Tra4^-$	$[-1 \ 0] \rightarrow [0 \ -1] \rightarrow [0 \ 0]$
$Th1^-$	$[-1 \ +1] \rightarrow [-1 \ 0] \rightarrow [-1 \ 0] \rightarrow [0 \ -1]$
$Th2^-$	$[0 \ +1] \rightarrow [-1 \ +1] \rightarrow [-1 \ 0] \rightarrow [0 \ -1]$

Table 4.2: List of selected modes and their sequence of states.

mode. The topology itself imposes some limits. For instance, in this topology $V_g > V_o$, V_s always, regardless of the mode used.

4.1.2.2 Current limits in modes

Modes are not only bound to certain voltage conditions; they also find a limit when one of their states last zero. For instance, in $Tra4^+$, when the second state lasts zero the mode becomes $[+1 \ 0] \rightarrow [0 \ 0]$ while if the last state lasts zero it becomes $[+1 \ 0] \rightarrow [0 \ +1]$. In both cases, the inductor current becomes a triangle only divided into two states. These limits are drawn in Figure 4.8 a) to clarify this idea. There is another boundary when the first state lasts zero, although in this case, I_g would be zero, so it is not considered.

All Tra modes have three boundaries associated with how long states last. Each one associated with one of the three states lasting zero, while T modes only have two. In T modes, if the first state lasts zero, so does the second state, and if the third state lasts zero, the fourth state lasts zero too. As a result, the current waveform is always a triangle with two states in these limits.

These limits can be expressed in terms of the three ports currents. In the example given before (Figure 4.8 a)), when the second state lasts zero and the mode is $[+1 \ 0] \rightarrow [0 \ 0]$, it is found that $I_s = 0$. Therefore, $Tra4^+$ can only work for $I_s > 0$. In other words, the storage capacitor cannot have negative current if this mode is applied. In the second case ($[+1 \ 0] \rightarrow [0 \ +1]$), the inductor waveform happens to be a triangle where $I_g + I_s = I_o$. Therefore $Tra4^+$ can only work when $I_o > I_g + I_s$. In the operation mode $T0$, if the third and fourth states last zero, the mode becomes a triangle with positive current and the states $[+1 \ -1] \rightarrow [0 \ -1]$. In this case, $-I_s = I_o$. Therefore, $T0$ can only be used when $-I_s > I_o$. A similar case is obtained when the first and second state last zero. These limits are represented in the bottom-right part of Figure 4.8.

Figure 4.7: Representation of the nineteen operation modes. Voltages and currents do not represent any specific point. Switching states are labeled with the $[dhq]$ values.

It is better to write these kinds of boundaries in terms of the current in the ports, as it is helpful to distinguish and compare the operation ranges of different modes. The fact that some state lasts zero may mean a different thing depending on the mode discussed. The current limits of the nineteen modes are shown in Table 4.4. There are certain current limits that are not applicable (NA); those are the limits that imply $I_g < 0$ and are never reached.

To summarize, operation modes can only be applied in specific sectors of the line cycle, depending on the relation between the voltages of the three ports and the relation between the current of the three ports. Some of the limits mentioned above can be found in Figures 4.2 to 4.6 as vertical lines separating two modes to clarify the idea.

4.1. BCM modulation with ZVS when $i_L \neq 0$

Figure 4.8: Examples of the limits for $Tra4^+$ and $T0$. Current limits are found when one of the states last zero. In the voltage limits of a mode, the inductor current is no longer defined.

Mode	Voltage limits			
$Th2^+$	$V_o < V_g$	$V_o > V_s$	$V_o > -V_s$	$V_o < V_g - V_s$
$Th1^+$	$V_o < V_g$	$V_o > V_s$	$V_o > V_g - V_s$	$V_o < V_g$
$Tra4^+$	$V_o < V_g$		$V_o > 0$	
$Tra3^+$	$V_o < V_g$		$V_o > 0$	
$Tra2^+$	$V_o < V_g - V_s$		$V_o > -V_g$	
$Tra1^+$	$V_o < V_g - V_s$		$V_o > -V_g$	
$T3^+$	$V_o < V_g - V_s$	$V_o > -V_s$	$V_o > V_s$	$V_o < V_g$
$T2^+$	$V_o < V_g$	$V_o > V_g - V_s$	$V_o > V_s$	$V_o < V_g$
$T1^+$	$V_o < V_g$	$V_o > V_g - V_s$	$V_o > -V_g + V_s$	$V_o < V_s$
$T0$	$V_o < V_g - V_s$	$V_o > -V_s$	$V_o > -V_g + V_s$	$V_o < V_s$
$T1^-$	$V_o < V_g - V_s$	$V_o > -V_s$	$V_o > -V_g$	$V_o < V_g - V_s$
$T2^-$	$V_o < -V_s$	$V_o > -V_g$	$V_o > -V_g$	$V_o < V_g - V_s$
$T3^-$	$V_o < -V_s$	$V_o > -V_g$	$V_o > -V_g + V_s$	$V_o < V_s$
$Tra1^-$		$V_o > -V_g + V_s$		$V_o < V_g$
$Tra2^-$		$V_o > -V_g + V_s$		$V_o < V_g$
$Tra3^-$		$V_o > -V_g$		$V_o < 0$
$Tra4^-$		$V_o > -V_g$		$V_o < 0$
$Th1^-$	$V_o < -V_g + V_s$	$V_o > -V_g$	$V_o > -V_g$	$V_o < -V_s$
$Th2^-$	$V_o < V_s$	$V_o > -V_g + V_s$	$V_o > -V_g$	$V_o < -V_s$

Table 4.3: Voltage limits of each operation mode.

4.1.3 Representation of the limits for the modes

Now that the regions where the nineteen modes can operate are identified, the question is whether there is an operation mode for all possible combinations of V_g , V_s , V_o , I_g , and I_o . In other words, is there is an operation point where an additional mode is required? It is hard to answer this question using Tables 4.3 and 4.4, as there are six variables involved. Therefore, this problem can be addressed graphically. For this purpose, an advanced version of an XY plot typically used to represent trajectories of the output current and voltage is employed [39].

Mode	Current limits		
<i>Th2</i> ⁺	$I_s = -I_o$ (NA)		$I_g + I_s = I_o$
<i>Th1</i> ⁺	$I_g = I_o$ (NA)		$I_g + I_s = I_o$
<i>Tra4</i> ⁺	$I_g = 0$	$I_s = 0$	$I_g + I_s = I_o$
<i>Tra3</i> ⁺	$I_g = -I_s$	$I_s = 0$	$I_g = I_o$
<i>Tra2</i> ⁺	$I_s = 0$ (NA)	$2I_s + I_g = -I_o$	$I_g = -I_s$
<i>Tra1</i> ⁺	$I_g + I_s = -I_o$ (NA)	$2I_s + I_g = -I_o$	$I_s = -I_o$
<i>T3</i> ⁺	$I_g + I_s = I_o$ (NA)		$I_s = -I_o$
<i>T2</i> ⁺	$I_g = I_o$		$I_g + I_s = I_o$ (NA)
<i>T1</i> ⁺	$I_g = I_o$		$I_s = I_o$
<i>T0</i>	$I_s = -I_o$		$I_s = I_o$
<i>T1</i> ⁻	$I_s = -I_o$		$I_g = -I_o$
<i>T2</i> ⁻	$I_g + I_s = -I_o$ (NA)		$I_g = -I_o$
<i>T3</i> ⁻	$I_s = I_o$		$I_g + I_s = -I_o$ (NA)
<i>Tra1</i> ⁻	$I_g + I_s = I_o$ (NA)	$2I_s + I_g = I_o$	$I_s = I_o$
<i>Tra2</i> ⁻	$I_s = 0$ (NA)	$2I_s + I_g = I_o$	$I_g = -I_s$
<i>Tra3</i> ⁻	$I_g = -I_s$	$I_s = 0$	$I_g = -I_o$
<i>Tra4</i> ⁻	$I_g = 0$	$I_s = 0$	$I_g + I_s = -I_o$
<i>Th1</i> ⁻	$I_g + I_s = -I_o$		$I_g = -I_o$ (NA)
<i>Th2</i> ⁻	$I_g + I_s = -I_o$		$I_s = I_o$ (NA)

Table 4.4: Current limits of each operation mode. Those limits that also imply $I_g < 0$ are labeled (NA).

Nevertheless, before the representation is discussed, the XY plot is reviewed to clarify the idea. Figure 4.9 a) shows a typical XY plot for V_o and I_o , including the trajectories for different loads. For reference, the line where $P_o = 1$ kW is plotted too. In this map, a resistive load is represented as a line in the first and third quadrant. A pure reactive load would be a circle centered in zero, and the maximum capacitive and inductive load specified for this inverter are represented with an oval shape ($PF = 0.7$). However, drawing the limits between modes in such a map is not possible, as it contains only the information of V_o and I_o .

Since the limits of the operation modes do not depend on the magnitude of the port voltages but in their relation, normalization is useful. Therefore, instead of V_o and I_o for the axis of the XY plot, V_o/V_g and I_o/I_g can be used. The result is shown in Figure 4.9 b), containing the same information as Figure 4.9 a) and a few more lines where P_o is constant. In this map, the limits of between modes can be plotted for a given V_s , these plots can be found in [39]. The limits of the modes in this plot were extensively studied for the modes applied when the load is resistive by Regina Ramos and Iñigo Zubitur.

To cover the whole current range, the y -axis can be replaced by $I_o/(|I_o| + I_g)$, as shown in Figure 4.9 c). In this case, when $I_o/I_g \rightarrow \infty$ then $I_o/(|I_o| + I_g) \rightarrow 1$, and $I_o/(|I_o| + I_g) = 0.5$ when $I_o = I_g$. In this plot, the whole range of output voltage and current are mapped between -1 and 1 in the two axes. The lines showing constant output power can be used to understand how the map is modified with the normalization of the axis, and it is also helpful to understand the regions where the inverter normally operates. This last XY plot would be sufficient to represent all possible port variables if a two-port inverter were considered. However, in this three-port inverter, the storage

4.1. BCM modulation with ZVS when $i_L \neq 0$

Figure 4.9: I-V curve of the output variables for the loads used in Figures 4.2 to 4.5, a) as a function of V_o and I_o , b) normalized to the input variables, c) normalized for the range of operation to be contained between -1 and 1 .

capacitor voltage and current are also required to identify the operation point and represent the boundaries between modes.

A z -axis is required to include the storage capacitor port in this type of map. This axis can be used to represent V_s or I_s . In this work, V_s is selected for that purpose. I_s does not have to be included as it can be calculated from $P_s = P_o - P_g$ in each point of the plot. In other words, the information provided by I_s would be redundant once V_s is plotted. Therefore, this is a normalized XY plot for the output port with the addition of V_s in the z -axis. The z -axis is normalized to V_s/V_g , so the range of operation is defined between 0 and 1 .

In this modified XY plot, that could be named XYZ plot, the boundaries of the modes would be represented as surfaces, and the operation modes would be contained in volumes limited by these surfaces. The voltage and currents in the ports during the operation of the inverter are still represented as a line in these plots. Figure 4.10 a) to d) shows how the three ports variables are mapped in this XYZ plot for different loads.

Figure 4.10: Projection of the variables of the storage capacitor and output ports in the XYZ , a) for the port variables in Figure 4.2 (1 kVA $PF = 1$), b) for the variables in Figure 4.3 (1 kVA $PF = 0.7$ capacitive), c) for the variables in Figure 4.4 (1 kVA $PF = 0.7$ inductive), d) for the variables in Figure 4.5 (250 VA $PF = 0.1$), e) a slice of the volumes representing the operation modes.

The last plot of Figure 4.10 shows how a slice of the plot of the different modes for $V_s/V_g = 0.85$ would look like, using the same colors of Figure 4.2 to 4.6 for the modes. As it is a surface of the 3-D plot, the limits between modes are lines instead of surfaces and the regions where modes are applied are areas instead of volumes. This surface is redrawn in Figure 4.11 a) including the name of the operation modes and their limits.

To understand how the limits between the modes change with V_s , surfaces for $V_g = 400$ V when $V_s \approx 295$ V and $V_s \approx 380$ V have also been represented in Figure 4.11 b) and c). These three values of V_s correspond to the average, minimum, and maximum voltage in the storage capacitor at full power, respectively. With light load, V_g increases but the average V_s is kept at 340 V; the map is shifted towards the representation in b).

Combining the plots in Figure 4.11 and the trajectories in Figure 4.9 c), the sequence of operation modes used along the line cycle for different loads could be found. Also, in Figure 4.11, the limit between $Tra4^+$ and $Th1^+$ can be identified, for low values of V_s the boundary $I_g + I_s = I_o$ can be easily crossed. As mentioned earlier, the storage capacitor is designed to avoid Th modes, in other words, to meet $I_g + I_s < I_o$.

This XYZ map can also be used to identify if there is any region for which an operation mode is not defined. As it is not possible to show the map in 3D, some other interesting surfaces of the map are shown in Figure 4.12, this time without the labels for the limits. This figure shows the 3D map from different angles. It should be noted that the three surfaces shown in Figure 4.11 are situated between the $V_s = V_g$ and $V_s = V_g/2$ surfaces in this plot.

This plot also shows the modes $Th2^+$, $Th2^-$, $T3^+$, and $T3^-$ that are only used in case $V_s < V_g/2$. To conclude the analysis, these cuts show that there is an operation mode for every possible operation point of the inverter; this implies that there are no combinations of V_g , V_s , V_o , I_g , and I_o for which a mode is not defined. Therefore, it is proven that with the nineteen modes of Figure 4.7 the inverter can work even in abnormal conditions.

4.1.4 Seamless modulation

An interesting feature of this modulation is that the selected modes are used in their whole operation range. All the selected modes are bounded to a specific volume of the XYZ plot,

4.1. BCM modulation with ZVS when $i_L \neq 0$

Figure 4.11: Surfaces of the XYZ plot showing the modes and their limits for: a) $V_g = 400$ V and $V_s = 340$ V, b) $V_g = 400$ V and $V_s = 295$ V, c) $V_g = 400$ V and $V_s = 380$ V.

and the nineteen together fill the whole operation range. As a result, boundaries are shared. The fact that boundaries are shared is a very important property of the modulation. It implies that the shifts between modes are seamless. In this context, *shift* refers to the transitions between modes; the term *transition* is not used to avoid confusion with the transitions between switching states described in the previous chapter.

Current limits are associated with states lasting zero, as described in Section 4.1.2.2. In those boundaries, the current waveform is always a triangle with two states only. Regardless of the mode before and after the limit, each current limit is associated with a single combination of two states. This concept is clarified through an example; the boundary $I_s = 0$ of the first quadrant. This is the boundary between $Tra3^+$ ($[+1 \ 0] \rightarrow [+1 \ -1] \rightarrow [0 \ 0]$) and $Tra4^+$ ($[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [0 \ 0]$) shown in Figure 4.11 a). In $Tra3^+$ and $Tra4^+$, this boundary is met when the second state last zero, and the mode becomes $[+1 \ 0] \rightarrow [0 \ 0]$ in both cases, so the shift between modes is

4.2. Limitations of the BCM modulation

Figure 4.13: Example of the shift from a mode to the following one at $I_s = 0$ for $V_o > 0$. a) *Seamless* shift from $Tra3^+$ to $Tra4^+$. b) *Abrupt* shift from $Tra3^+$ to a mode with higher indirect power not selected, $[+1 \ 0] \rightarrow [0 \ +1] \rightarrow [-1 \ 0]$.

smoothly from one operation point to the next, the error signals of the control loops are continuous too; this is explained in Chapter 5 once the control loops are introduced. Also, for the control of the inverter, the time each switching state lasts is controlled. For the calculation of control of the times proposed in Chapter 5, an iterative process based on the control times of the previous switching cycle is used. For this purpose, it is imperative that the time each state last changes only slightly from a switching cycle to the next; this is discussed in detail in that chapter too.

Regarding the leakage current, to suppress the current through the parasitic capacitance of the PV panel, a common-mode choke is required as it is going to be detailed in Chapter 6. For the design of the choke, the *average* common-mode voltage should not have steps. These steps would be generated by abrupt changes in the average voltage between the input and the output port and would lead to a high current through the common mode choke that can lead to saturation. With the selected modulation, there are no abrupt changes in the average common-mode voltage because the duty cycle of the different switches changes smoothly along the line cycle. An example of this property is shown in Figure 4.13. In the case of seamless shifts in a), the average voltage in q^- does not change between modes. Meanwhile, in the case of an abrupt shift, shown in Figure 4.13 b), the average v_{q^-} changes from a switching cycle to the following one. A complete description of this issue is given in Chapter 6.

Seamless modulation is not only beneficial for this inverter. The control described in [59] also features smooth operation between modes. In [80], seamless (or *continuous*) modulation is preferred too for reasons related to the digital control implementation and to avoid system instabilities.

4.2 Limitations of the BCM modulation

So far, the operation of the inverter considering BCM modes has been described. The modulation is composed of nineteen operation modes used in different sectors of the line cycle depending on the voltage and current of the three ports and featuring the minimum indirect power in the inductor.

However, in these BCM modes, ZVS is not achieved in all the transitions between switching states. First, ZVS is not achieved in some transitions with $i_L = 0$. Second, there are transitions with $i_L \neq 0$ where the inductor current may not be high enough to achieve ZVS. Both cases are illustrated in the example of Figure 4.14 with the mode $Tra3^+$. In this example, I_g is slightly lower than I_o and only one of the three transitions achieves full ZVS. The following sections describe the problem in detail and possible solutions to ensure ZVS in all transitions.

Figure 4.14: Example of transitions without ZVS; $Tra3^+$ operating close to the $I_g = I_o$ boundary.

Even if ZVS is not considered, there is an issue with this modulation related to the variations in switching frequency along the line cycle and for different loads. With BCM modulation in the case of light load or no load, the inverter would work with an inadmissible high switching frequency. Also, in those voltage limits where the inductor current waveform is not defined it would operate with very low switching frequency. The switching frequency of the inverter, f_{sw} , along the line cycle, for different resistive loads, is depicted in Figure 4.15 to clarify this idea. In two points near $\omega t = 0$ and π , coinciding with voltage limit $V_g - V_s = V_o$ and $-V_g + V_s = V_o$, f_{sw} reach zero. Also, as the load is reduced f_{sw} increases drastically. The switching frequency has been calculated using the analysis included in Appendix B for the time that each state lasts.

Figure 4.15: Switching frequency along the line cycle for different resistive loads and $L = 80 \mu\text{H}$.

These two issues, together with the lack of ZVS, are detailed in the following subsections. All calculations are done considering $L = 80 \mu\text{H}$ and that two *GS66516T* devices in parallel are used per switch, as in the previous chapter.

4.3. Transitions with inductor current equal to zero

4.2.1 Transitions where the inductor current is not enough

ZVS transitions are important and one of the goals of the modulation. So far, it has been assumed that ZVS is achieved in those transitions where $i_L \neq 0$, relying on the diagram of Figure 3.2. However, as discussed in Chapter 3 this is not always the case as there is a minimum amount of inductor current required to perform ZVS. Then, if one of the states is not long enough, the current in the transition may be too close to zero, and below the minimum current for ZVS. If that is the case, as in the transition $[101 \rightarrow 001]$ in Figure 4.14, only *incomplete* ZVS would be achieved [69].

A simple solution to solve this issue could be to limit the minimum time that some states last, for instance, to set a minimum time for the last state in the example in Figure 4.14. This concept is equivalent to set a minimum current where the state has to end, namely I_{th} . Then, with a careful selection of I_{th} , ZVS could be guaranteed in these transitions. However, if this solution is applied, the current limits of modes would no longer be the ones described in Table 4.4 since the modes would not be limited to waveforms with two states, but to trapezoids where one of the states is very short but not zero. This is, the modes would be able to operate close to their current limits, but not in the current limits. With a solution like this, there would be regions of the XYZ plot where the inverter could not operate. Moreover, this solution would not work for light loads, when the current in the inductor is below the minimum for ZVS.

In the following section, how modulation is modified to ensure ZVS in these types of transitions for any type of load while ensuring that the current limits are not modified is explained.

4.3 Transitions with inductor current equal to zero

When $i_L = 0$, ZCS transitions are achieved, helping to reduce switching losses. However, dv/dt and C_{oss} are not reduced. Therefore, it is more convenient to obtain ZVS transitions, as mentioned in the previous chapter. Although some of the transitions can achieve ZVS when the transistor is opened when $i_L = 0$, this is not the general case, and a minimum current for ZVS is required. The process to obtain this $i_{Lmin}(0)$ is described in Chapter 3, and it is applied to the transitions along the line cycle in Appendix A. The results show that some transitions require an $i_{Lmin}(0)$ up to 2.6 A, which is comparable to I_g with the devices used for the prototype.

A practical solution to this problem would be to modify each mode slightly to ensure ZVS in the transitions with $i_L = 0$, as suggested in [70]. For instance, for Tra^p modes, the solution would be to switch with a certain negative current value instead of $i_L = 0$ when it is required. If i_L is negative enough, the transitions $[001 \rightarrow 111]$ of $Tra4^+$ and $Tra3^+$ and the transitions $[000 \rightarrow 101]$ of $Tra2^+$ and $Tra1^+$ would have ZVS. Figure 4.16 a) shows the transition $[001 \rightarrow 111]$ when the minimum current for ZVS is used. The value of $i_{Lmin}(0)$ depends on C_{oss} , L , and the voltage of the ports, as described in Chapter 3. As a result, it changes depending on the transition considered and the point of the line cycle.

The same could be done for Tra^n modes, just allowing some positive i_L before the transition. For T modes it is more complicated as there are two transitions with $i_L = 0$ per mode and the direction of the current before and after the transition is different. For instance, there are transitions as $[100 \rightarrow 000]$ in $T1^-$ where the transition should start with a certain positive current

Figure 4.16: Examples of transitions for $i_L = 0$, a) solution for Tra^p modes with minimum current, b) simple transitions for T modes with minimum current, c) transitions for T modes that require an intermediate step with the minimum current for both transitions, d) the previous example but with a higher current in the inductor in both transitions.

in the inductor, Figure 4.16 b) shows this case using $i_{Lmin}(0)$. Unfortunately, transitions can be more complicated than this one. The transition $[101 \rightarrow 011]$ in $T2^+$ cannot achieve ZVS neither with positive nor or negative current in the inductor, as shown in the diagram of Figure 3.2. Therefore, obtaining ZVS is a bit tricky. An intermediate state to cross $i_L = 0$ could be used. As a result, this transition is composed of two different transitions. For this example, a solution would be to use the transition $[101 \rightarrow 001]$ when the inductor current is positive, and later, once the current is zero $[001 \rightarrow 011]$. This process is shown in Figure 4.16 c) using the minimum amount of current for both transitions.

To summarize this discussion, some transitions only require switching before the current reach zero, but other transitions require the use of intermediate states. However, this solution comes with its own problems. First, if $i_{Lmin}(0)$, $i_{Lmin}(T_{tr})$, and T_{tr} are not negligible compared with current and time switching states last. As a result, it can no longer be assumed that a state starts when the previous state ends. The Equations 2.14 and 2.18, that describe the relation of the current in the three ports with the current in each state, are no longer be valid in this case. The implication is that the operation of the inverter would have to be redefined, and this is not convenient as it would make the control of the inverter more complicated.

Moreover, the current limits for the modes would no longer be valid as they are based on a model that neglects the effects of the transition. Also, the modulation would no longer be seamless as the operation of the inverter in the limits between modes would depend on the mode used before and after the limit is met. The magnitude of this effect depends on how high the current required for ZVS is, compared with the magnitude of i_L . If the current for ZVS is negligible so are the problems associated with this solution. Unfortunately, this is not the case for the devices selected ($L = 80 \mu\text{H}$ and two *GS66516T* devices).

Finally, a solution like this would be complex from the control and implementation standpoints. The equations required to calculate the minimum current and maximum dead time for ZVS are complex, far too complex to be implemented in real-time, and extensive look-up tables considering different port voltages and transitions would have to be used.

4.3. Transitions with inductor current equal to zero

This solution is perfect for efficiency and power density, as the modification for ZVS has the minimum possible impact on the modulation. Unfortunately, the conclusion is that this solution is not feasible because of the additional complexity and because the current for ZVS is not negligible.

A fixed threshold current

A solution that is easier to implement would be to use a fixed value for $i_L(0)$ and dead-time instead of switching with the optimum current in each specific point of the line cycle, regardless of the transition considered or the value of the port voltages. This fixed value of $i_L(0)$ is termed *threshold current*, I_{th} . If I_{th} is sufficiently high, ZVS is guaranteed in all transitions at the expense of higher current. This solution would have a negative impact on volume and losses of the inductor as it implies higher rms and peak current. With a solution like this, the transitions with $i_L = 0$ would be done with $i_L = I_{th}$ or $i_L = -I_{th}$ instead. If the positive and negative levels (I_{th} and $-I_{th}$) are set to the same value, the example in Figure 4.16 d) would replace the one in Figure 4.16 c).

An advantage of this solution is that the portion of the inductor current between I_{th} and $-I_{th}$ does not have a net effect on the current in the ports. In other words, neglecting the effect of the ZVS transitions, the average current of the inductor between I_{th} and $-I_{th}$ is zero, as expected. Therefore, if modes are defined so their transitions "with $i_L = 0$ " are implemented at $i_L = I_{th}$ or $i_L = -I_{th}$, Equations 2.14 and 2.18 are still valid if the transitions are neglected. Moreover, if I_{th} and $-I_{th}$ are defined to be high enough (considerably higher than the minimum for ZVS) the effect of the transitions on the current waveform can be neglected. Then, it would be valid to use Equations 2.14 and 2.18 meaning that the limits of the modes in Figure 4.11 remain unchanged. This effect can be seen in Figure 4.16 c) and d), the higher I_{th} , the shorter the transition time, and the lower the variation of the inductor current during the transitions.

Using a constant value for ZVS in these transitions would make the BCM of the inverter look like a TCM modulation. This solution can be found in converters where TCM is used. For instance, in the inverter of the *Inverter* team from ETH, a constant threshold is used [42], [68].

However, this solution has a significant drawback, besides the increase in rms and peak inductor current. The higher I_{th} , the higher the step when shifting between operation modes. Since the states used for ZVS between I_{th} and $-I_{th}$ depends on the mode, when the operation changes from a mode to a different one, the inductor current waveform changes. As a result, the duty cycles and switching frequency change abruptly in these boundaries. Therefore, with a solution like this, the modulation would no longer be seamless.

The proposed solution based on the idea of a fixed threshold current is described in Section 4.4.

4.3.1 Limiting high-frequency operation

Since the modulation is based in BCM, when the load is light, the current in the three ports is low. Therefore, the current in the different states and the time each state lasts are low as well. This leads to higher switching frequency, and theoretically, with no load at all ($I_g = I_s = I_o = 0$), the switching frequency tends to infinity.

The frequency tending to infinity is a common problem of converters operated in BCM, and solutions are easily found in the literature. The technique named *pulse-skipping*, consisting of

allowing some time where the inductor is not connected to any port and $i_L = 0$ is a very typical solution for converters working in light load conditions. With this solution, the energy is transferred in bursts to the different ports, thus reducing the switching frequency. Another possible solution would be to switch to DCM modulation when the load is light. These solutions would require a control a little bit more complicated, and ZVS would not be achievable after the state where $i_L = 0$.

An alternative based on what is discussed in the previous subsection is to switch the inductor current between two threshold currents at the same level, from I_{th} to $-I_{th}$. Since states switched between I_{th} and $-I_{th}$ have an average current of zero, they do not add any net current to the ports. Therefore, switching states between I_{th} and $-I_{th}$ can lower the switching frequency while achieving $I_g = I_s = I_o = 0$. The frequency would depend on the states selected, the inductance value, and how high I_{th} is set. The problem of this solution is that the inductor would be moving energy from the ports back and forth, so the efficiency at light load is penalized. In Section 4.4, the implementation of this idea is discussed.

4.3.2 Limiting low-frequency operation

One of the most critical limitations of the BCM modulation is the fact that modes are not defined in the voltage limits. Unlike current limits, where the number of states is reduced to two, in the voltage limits, the inductor current waveform does not exist. The reason is that a voltage that should be either positive or negative is zero (see Figure 4.8).

As a mode gets near its voltage limit, the voltage of one of the states gets lower and the time that state lasts becomes much longer. The reason is that it takes a long time to get reasonable current in the state when the voltage is nearly zero and the current starts or ends with $i_L = 0$. Therefore, in those cases, the switching frequency is reduced. In the boundary where the voltage in a state is zero, the state tends to last an infinite amount of time as it cannot build-up the necessary current. These points in the line cycle can be identified in Figure 4.15. Therefore, in all voltage limits described in Section 4.1.3, the switching frequency tends to zero.

This problem can be found in Multilevel inverters working in BCM when the output voltage approaches the different input voltage levels ($V_{in}/2$ in a 3-level, for instance) [88]. In [43], buck, boost, and buck-boost families of inverters with a single switch are proposed. The buck family suffers from frequency near zero at $V_c = |V_o|$, which makes this family less attractive.

When the switching frequency is too low, the assumptions used to describe the operation of the inverter are not valid. The inverter has been described considering that the voltage applied to the inductor in the switching states is constant, but this is only valid when the switching frequency is higher than the resonant frequency of inductor and the input capacitor, output capacitor and the storage capacitor (the input capacitor is included in Figure 6.3 and described once the leakage current filter is introduced). At low frequency, this resonance causes the voltage applied to the inductor to change during the switching state. In such cases, the description of the modes is not accurate, and the control that is going to be described in Chapter 5 is not valid. Therefore, a minimum switching frequency is required for the correct operation of the inverter.

4.3. Transitions with inductor current equal to zero

Before this dissertation, the problem was solved by switching to operation modes with higher P_{indL} with high switching frequency in the vicinity of the voltage limit. A similar solution is proposed in [88] for a T-type inverter. Then, there was a new mode between each T mode. These additional modes would work in a band around the voltage limit, for instance, for the boundary between $T0$ and $T1^+$, $V_g - V_s = V_o$, the mode would operate between $V_g - V_s - V_{th} = V_o$ and $V_g - V_s + V_{th} = V_o$. The width of this voltage band would determine the minimum switching frequency of the inverter. This band is represented in the XY plot of Figure 4.17 b). The mode with lowest P_{indL} that exists for $V_o = V_g - V_s$ is $[111] \rightarrow [001] \rightarrow [010] \rightarrow [011]$. How the inductor waveform would look like in the band and its new limits is shown in Figure 4.17 a) This mode is referred to as T unnamed.

Figure 4.17: Example of solutions to the voltage limit between $T0$ and $T1^+$, a) former solution, b) another possible solution, c) a surface of the XYZ plot showing where the additional modes would be applied.

This solution leads to higher P_{indL} in the inductor in those regions, and, what is more important, implies that shifting from a mode to another through these boundaries changes the inductor current waveform suddenly. With this solution, the operation of the inverter would no longer be seamless, as it was described in Figure 4.13 b). Therefore, a different approach is preferred.

Another possible solution is to use a combination of T and Tra mode ($TTra$ mode) in these voltage regions. Those modes were not considered in the first place and are shown in Figure 2.13 b). The mode used in each voltage limit would be a combination of the modes used at both sides of the boundary. For instance, for the previous example, it would be to combine $T0$ with $T1^+$. The result is shown in Figure 4.17 c), referred to as $TTra^+$ unnamed.

This new mode has the advantage of low P_{indL} as it is the combination of two modes with minimum P_{indL} but requires an additional state. The additional state considerably increases the complexity of the control. This additional degree of freedom in these types of modes can be used to ensure that the shift to $T0$ and $T1^+$ is seamless, which is an improvement over the previous solution.

Unfortunately, there are points of the XYZ plot where this solution is not valid. Those are the points where voltage and current limits collide, involving T and Tra modes. This problem can be found in the limit between $Tra3^+$, $Tra2^+$, $Tra1^+$, $T0$, and $T1^+$, highlighted in the XYZ

cut in Figure 4.18 b). In this specific point, $I_g = I_o = -I_s$ and $V_o = V_g - V_s$; the input port should be directly connected to the series connection of the output and storage capacitor ports. In other words, the solution to this point would be to use the state $[+1 - 1]$ directly. This point is very interesting from a power processing standpoint, as there is no need for power conversion. Although, ironically, it is very problematic for the modulation and the control of the inverter because of the BCM operation.

Figure 4.18: Operation point between $Tra3^+$, $Tra2^+$, $Tra1^+$, $T0$ and $T1^+$ where voltage and current limits meet, a) waveforms in the different current limits, b) this operation point in the surface XYZ , c) discarded solution, d) former solution e) proposed solution.

A mode that could shift seamlessly to the other modes would have to be compatible with the four current limits $[+1 - 1] \rightarrow [0 - 1]$, $[+1 - 1] \rightarrow [-1 0]$, $[+1 - 1] \rightarrow [0 0]$ and $[+1 0] \rightarrow [+1 - 1]$. For such purpose, a mode with seven states would be required, $[+1 0] \rightarrow [+1 - 1] \rightarrow [0 0] \rightarrow [0 - 1] \rightarrow [-1 0] \rightarrow [-1 + 1] \rightarrow [0 + 1]$ shown in Figure 4.18 in the left. This solution is shown in Figure 4.18 c). A solution like this would be extremely hard to implement due to all the degrees of freedom. Moreover, ZVS would not be achievable, so this solution is discarded.

The former solution of replacing the modes in this point with the next with lower indirect power that could operate at this point would result in the use of T unnamed; the same mode presented for the limit between $T0$ and $T1^+$. The mode is shown again in Figure 4.17 d). Unfortunately, defining the limits of the operation of this additional mode would be complicated. What is worse, the modulation would not be seamless, as mentioned earlier.

An more straightforward solution could be to add states with an average current of zero between $[+1 - 1]$. The mode would be composed of three states, a state between $-I_{th}$ and I_{th} , then the state $[+1 - 1]$, and finally another state from I_{th} to $-I_{th}$. Controlling the value of I_{th} and the time $[+1 - 1]$ lasts, the port currents can be controlled. This solution is based on a TCM modulation rather than a BCM one. This idea is shown in Figure 4.18 e). As power is only stored and released in the inductor in the two states between I_{th} and $-I_{th}$, the indirect power is extremely low. This is the solution that is going to be applied and it is described in the following section. How seamless shifts between modes are obtained is explained too.

4.4 Proposed TCM modulation

In the previous section, it is explained how adding states between I_{th} and $-I_{th}$ can be used to achieve ZVS, reduce the high-frequency operation under light load conditions, and even to operate the inverter in the voltage limits where the frequency tends to zero. The rest of the chapter is dedicated to explaining the operation of the inverter when this modification is considered. How to select the states and value of I_{th} is also discussed. With this modification, the inductor current waveform can be regarded as TCM, and it is going to be referred to as TCM modulation to differentiate it from the BCM modulation explained in Section 4.1 and Chapter 2. The result is similar to the TCM modulation in [68].

As mentioned earlier, when a state is added between I_{th} and $-I_{th}$, its average current is zero. Therefore, the additional state used for i_L between I_{th} and $-I_{th}$ and the state used between $-I_{th}$ and I_{th} do not impact the limits of the nineteen operation modes described in Section 4.1.2. In other words, Figure 4.11 is left unchanged. Moreover, if I_{th} is well above the minimum current for ZVS, the dead time and variations of the current in the transitions between states can be neglected.

The proposed modulation aims to obtain ZVS in all transitions, as discussed in Chapter 3. Moreover, it is designed to obtain a seamless operation along the line cycle for the reasons explained in Section 4.1.4. The additional states are selected based on these two premises.

For smooth shifts between modes, all of them must use the same state to go from I_{th} to $-I_{th}$ and the same state to go from $-I_{th}$ to I_{th} . Since the same states must be used in all modes, but not all transitions can achieve ZVS as shown in Figure 3.2, the selection of the states is very limited. For the additional state used between $-I_{th}$ and I_{th} , the only state that always achieves ZVS transitions is [111]. [111] features ZVS transitions with $i_L > 0$ to any other state. Additionally, any other state can be switched to [111] with $i_L < 0$ with ZVS. Therefore, in the proposed modulation, the state [111] is applied from $i_L = -I_{th}$ to I_{th} the nineteen operation modes. For similar reasons, [000] is applied when i_L goes from I_{th} to $-I_{th}$. It features ZVS for transitions with positive and negative current regardless of the other state used. This solution is drawn in Figure 4.19, neglecting the time the ZVS transitions last or the variations of the inductor current in the transitions.

Figure 4.19: Added states between I_{th} and $-I_{th}$ for the TCM modulation, the transitions have been labeled as i , ii , iii , and iv for reference, also the time the two additional states last is included, T_{np} and T_{pn} respectively.

With this modification, seamless operation and ZVS in all transitions can be achieved, and the variations in switching frequency are reduced [87]. The times it takes for [111] to go from $-I_{th}$ to I_{th} and for [000] to go from I_{th} to $-I_{th}$ are named T_{pn} and T_{np} , respectively; these times are calculated as:

$$T_{np} = \frac{2I_{th}}{V_g - V_o} L \quad T_{pn} = \frac{-2I_{th}}{-V_g - V_o} L \quad (4.1)$$

The value for the threshold current, I_{th} , should be selected in such a way that ZVS is achieved in all modes. It also should be high enough for transitions times and current variations in the ZVS transitions to be negligible. Moreover, it should be high enough to limit the high-frequency operation to a reasonable value even under no-load. Finally, it should be high enough so that in the voltage limits between modes the switching frequency is limited to a reasonable minimum value too. The following subsections describe how I_{th} is determined for the previous considerations.

4.4.1 Threshold current to limit the minimum switching frequency

This subsection describes how the added states can improve the operation near voltage limits limiting the minimum switching frequency of the inverter. The goal is to obtain an appropriate value for I_{th} to ensure that the times the states last are below the resonant period of the inductor and the capacitors of the ports. For this purpose, the switching frequency is calculated as a function of I_{th} in the voltage frontiers in Figure 4.11, i.e., $V_g - V_s = V_o$ and $V_s = V_o$. The same results would be obtained for the limits $-V_g + V_s = V_o$ and $-V_s = V_o$. For this analysis, full power is considered, as it is when the times are longer. In this case, $V_g = 400$ V.

First, $V_g - V_s = V_o$ is analyzed. This voltage limit is bounded by two current limits, $I_g = I_o$ for positive output current and $I_s = I_o$ for negative. The inverter operates in the point described in Figure 4.18 when $I_g = I_o$. The frequency is low as the voltage of the state $[+1 - 1]$ is zero. On the other hand, for $I_s = I_o$, the waveform is a negative triangle formed by $[-1 + 1] \rightarrow [0 + 1]$, which is the negative part of $T0$ or $T1^+$, and the frequency is not that low as none of the voltages are zero. Therefore, the point where $V_g - V_s = V_o$ and $I_g = I_o$ is analyzed first as it is the worst case. The inductor current waveform is shown in Figure 4.20 a), with the additional $[111]$ and $[000]$ states.

Figure 4.20: Solution for the point in Figure 4.18 including the $[111]$ and $[000]$ states, a) inductor current waveform, b) different times as a function of I_{th} , c) times as I_o changes from $I_s = I_o$ to $I_g = I_o$ for $I_{th} = I_g = 2.5$ A and $V_g - V_s = V_o$ (along with the voltage limit between $T0$ and $T1^+$). b) and c) for $L = 80$ μ H, $V_g = 400$ V and $V_s = 340$ V

In this waveform, during T_{np} and T_{pn} , the average current in the inductor is zero, and, during $[101]$, the inductor current is $i_L(t) = I_{th}$. Then, the input current is directly given by:

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$$I_g = I_{th} \frac{T_{[101]}}{T_{np} + T_{[101]} + T_{pn}} \quad (4.2)$$

T can be plotted against I_{th} ; the results are shown in Figure 4.20 b) for $V_s = 340$ V and $I_g = 2.5$ A. The conclusion obtained from this plot is that I_{th} should be at least as high as I_g or the mode would not be valid in this point, regardless of the value of V_s or L .

The evolution of T and $T_{[101]}$ along the voltage limit is shown in Figure 4.20 c) to prove that the longest $T_{[101]}$ is found at $I_g = I_o$. Appendix C explains how these times are calculated.

The other frontier, $V_s = V_o$, is bounded only by $I_g = I_o$. At this specific point, the inductor current waveform is just a positive triangle with the states $[+1 \ 0] \rightarrow [+1 \ -1]$, which is the positive part of $T1^+$ and $T2^+$. In this case, the frequency is not low because the voltage of these states is not close to zero. However, as I_o is lower and gets away from this limit, the state $[0 \ +1]$ with negative current and $v_L = 0$ lasts longer, and a minimum value of I_{th} is required to avoid that the switching frequency tends to zero. The period as a function of I_o for different values I_{th} for the specific case of $V_s = 340$ V and $I_g = 2.5$ A is plotted in Figure 4.21 to clarify the operation of the inverter in this voltage limit. For a value of $I_{th} = 2.5$ A the time the state $[0 \ +1]$ last (that could be named $T_{[011]}$ in this analysis) rises as I_o goes below 2.5 A. With higher values of I_{th} this tendency is slowed down, meaning that the inverter can work with lower I_o in the frontier $V_s = V_o$. Nevertheless, this limit is not as important as the previous one because the inverter does not cross this limit at full power but for capacitive load, as shown in Figure 4.3, and when it does, I_o is almost as high as I_g . this implied that a low period is expected as shown in Figure 4.21.

Figure 4.21: Total period and time of the state $[011]$ as a function of I_o in the $V_s = V_o$ limit for different values of I_{th} , for $L = 80$ μ H, $V_g = 400$ V, $V_s = 340$ V and $I_g = 2.5$ A.

Therefore, the operation point where this inverter works with the lowest switching frequency is found at $V_g - V_s = V_o$ and $I_g = I_o$. Combining Equation 4.2 with Equation 4.1, the switching frequency in that point is given by:

$$f_{sw}|_{V_g - V_s = V_o, I_g = I_o} = \frac{1}{2I_{th}L} \frac{I_{th} - I_g}{I_{th}} \frac{V_g^2 - V_o^2}{2V_g} \quad (4.3)$$

It should be noted that this is only the minimum frequency when I_{th} is close to I_g . For larger values of I_{th} , the minimum frequency is found near the point of maximum output power, as in a conventional Full-Bridge operated in BCM. Equation 4.3 is minimum when $V_o \approx V_g$, but this voltage is never reached since $V_o = V_g - V_s$ in this point. Since the minimum value for $V_s \approx 295$ V,

the worst case can be considered at $V_o \approx 105$ V. For instance, for $I_{th} = 3.5$ A and $V_o = 105$ V, the switching frequency according to Equation 4.3 is $f_{sw} \approx 95.6$ kHz.

To conclude this discussion, I_{th} can be used to set the minimum switching frequency of the inverter. This value should be selected based on the resonant frequency of the inductor and capacitors in the ports. In the state $[+1 - 1]$, the input, storage, and output capacitor are in series with the inductor. The values used for the implementation described in Chapter 7 can be used to estimate the value of the resonant frequency. Those values are $C_s = 90$ μ F, $C_g = 10$ μ F and $C_o = 10$ μ F. The resonant frequency is given by $f_r = 1/(2\pi\sqrt{L(C_g||C_s||C_o)}) \approx 8.2$ kHz. Then, it is reasonable to set the minimum switching frequency at least five to ten times below this value.

As mentioned before, if I_{th} is large enough, the minimum switching frequency is not reached near $V_g - V_s = V_o$ and $I_g = I_o$. Figure 4.22 is included to show how I_{th} shapes the switching frequency along the line cycle for 1 kVA resistive load. As I_{th} increases, the switching frequency in the frontier between $T0$ and $T1$ (positive or negative) increases. On the other hand, the frequency decreases with I_{th} in $Tra4$. Therefore, large values of I_{th} can penalize the minimum switching frequency too. This plot is obtained calculating the times that each state lasts according to the analysis in Appendix C. It is observed that I_{th} limits the range of the switching frequency in the inverter.

Figure 4.22: Switching frequency along the line cycle for different values of I_{th} , for 1 kVA resistive load and $L = 80$ μ H.

Nevertheless, before the value of I_{th} is set, it is convenient to study the effects on the maximum switching frequency and ZVS too. From this section, it is concluded that the minimum value for I_{th} is I_g to ensure that the operation modes are defined in the point $V_g - V_s = V_o$ and $I_g = I_o$ and the point $-V_g + V_s = V_o$ and $-I_g = I_o$.

4.4.2 Threshold current and high-frequency operation

In this subsection, how I_{th} affects the maximum switching frequency is discussed. Under no-load, and neglecting the effect of the output capacitor, all the states last zero but for the additional

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[111] and [000] states, that last T_{np} and T_{pn} respectively. In this case, the operation of the inverter consists on the states [111] and [000] switching between I_{th} and $-I_{th}$ only. The operation is shown in Figure 4.23 in different points of the line cycle.

Figure 4.23: TCM operation of the inverter in different points of the line cycle without load and neglecting the capacitive load caused by the output capacitor.

Without load the frequency is limited by how long these states last. According to Equation 4.1, the switching frequency is given by:

$$f_{sw}|_{no\ load} = \frac{1}{T_{np} + T_{pn}} = \frac{1}{2I_{th} \cdot L} \frac{V_g^2 - V_o^2}{2V_g} \quad (4.4)$$

The maximum is obtained at $V_o = 0$, as it can be identified in Figure 4.23 at $\omega \cdot t = 0$ and $\omega \cdot t = \pi$. Therefore, the maximum frequency with this TCM modulation is given by:

$$f_{sw\ max} = \frac{V_g}{4I_{th} \cdot L} \quad (4.5)$$

From this equation, it is concluded that the maximum frequency can be limited through the selection of I_{th} . For instance, for $V_g = 450$ V (which is the voltage under no-load from $V_g = 450$ V– $20 \Omega \cdot I_g$), $L = 80$ μ H and $I_{th} = 2.5$ A, this maximum frequency would be 562.5 kHz. If I_{th} is increased to 3.5 A the maximum frequency would be reduced to ≈ 400 kHz. This maximum frequency should be limited to ensure that switching losses do not go too high or because of control restrictions.

4.4.3 Effects of the threshold current on ZVS transitions

In this section, the threshold current that ensures ZVS transition is found. It is also discussed how the transition time and the current after the ZVS transitions are affected by I_{th} .

First, the transitions considering $I_{th} = 2.5$ A are analyzed, as it is the minimum value from the limitation imposed by the voltage limits described in Section 4.4.1. For this purpose, the transitions shown in Figure 4.19 are analyzed using the *Matlab* scrip explained in the previous chapter. Due to the symmetry of the operation, transitions *iii* and *iv* are reciprocal to the transitions *i* and *ii* along the line cycle, so only the latter are described. In the *i* transitions, the last state of any mode is switched to [111] with $i_L(0) = -I_{th}$, while in the transition *ii* the state [111] gives way to the first state used in the mode, and the transition begins with $i_L(0) = I_{th}$. The input for the scrip is the operation mode and port voltages along the line cycle. With that information, the transition time and the value of the current after the transition are calculated. These values are calculated as

in Appendix A. For resistive load and 1 kVA, the current after the i and ii transition are depicted in Figure 4.24. For $I_{th} = 2.5$ A, all the transitions feature ZVS.

Figure 4.24: Evolution of the current waveform in the transitions i and ii for $I_{th} = 2.5$ A along the line cycle. The values $i_L(0)$, $i_L(T_{tr})$, and also $i_{L\ pk}$ are shown, and, to ease the interpretation of the plot, zooms of some transitions are included too. The arrows represent how the inductor current changes in the transitions and the gray area represents the part of the current where [111] is used. In the bottom, the evolution of the transition time for the transitions i and ii is shown.

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Since transition ii is easier to understand, it is discussed first. This transitions is represented in the top part of Figure 4.24 (the part with positive inductor current). There is no transition in almost the whole first half of the line cycle. The reason is that the first state in the modes $T1^+$, $Tra3^+$, and $Tra4^+$ is $[111]$. Therefore, there is no transition from the additional state $[111]$ to this one, as they are the same. In the other part of the line cycle, there are two different transitions. For the modes $T0$ and $T1^-$ the transition is $[111 \rightarrow 101]$ while for $Tra3^-$ and $Tra4^-$ the transition is $[111 \rightarrow 000]$, the one described in detail in Chapter 3. In both cases, as $v_L(0) > 0$ and $v_L(T_{tr}) < 0$, the current in the transition reaches its maximum, and then the inductor current decreases again.

For the transitions labeled as i , in the part of the plot where the inductor current is negative, there are four different transitions. The transition in the modes $Tra4^+$ and $Tra3^+$ is $[000 \rightarrow 111]$. For $T1^+$ and $T0$, the transition is $[011 \rightarrow 111]$. In $T1^-$ it is $[010 \rightarrow 111]$. Finally, it is $[110 \rightarrow 111]$ in $Tra3^-$ and $Tra4^-$. Only in the transition $[000 \rightarrow 111]$ $v_L(0) < 0 < v_L(T_{tr})$ and there is a negative current peak in the transition. In the other transitions $v_L(T_{tr}) > v_L(0) > 0$, which means that $i_L(T_{tr})$ is above $-I_{th}$. In fact, near $\omega \cdot t = 3\pi/2$, $i_L(T_{tr})$ approaches zero. A value slightly lower for I_{th} would lead to incomplete ZVS at this point in the line cycle because the current in the inductor would reach zero before the transition is over.

Moreover, it can be observed that $i_L(T_{tr})$ does not evolve continuously along the line cycle; there are abrupt changes in this plot. Those changes happen in the shifts between some modes, the largest one between $Tra3^+$ and $T1^+$. This step in $i_L(T_{tr})$ can impact the control of the inverter. Moreover, neglecting the difference between the current at the start and end of the transition is not valid. At $\omega \cdot t = 3\pi/2$, this difference is almost 2 A. The fact that the transitions are not negligible is a problem not only to the description of the inverter but also for the control implementation. As it is going to be described in Chapter 5, the control times are calculated assuming $i_L(0) = i_L(T_{tr})$.

Also, the evolution of the transition time along the line cycle for the transitions i and ii is shown in the bottom of Figure 4.24. It can be observed that T_{tr} is highly variable and has abrupt changes, which again is unsatisfactory from the control standpoint. For control purposes, T_{tr} is assumed zero.

The dead time has to be selected above T_{tr} to ensure soft-switching, and, to ease the implementation, the selected dead time is constant along the line cycle. Nearly 300 ns are required for $I_{th} = 2.5$ A. It cannot be shorter, or incomplete ZVS would be achieved in some transitions. This value is troublesome when considering the operation at $\omega \cdot t = 3\pi/2$. If it is slightly higher, the inductor current will reach zero in the dead time, and, at that time, the ZVS process will be reversed. The already discharged parasitic capacitances would start to be charged again while the inductor current rises above zero until the dead time is over, and the result would be incomplete ZVS too. Therefore, it is risky to set the value of I_{th} at 2.5 A, because the transitions are hardly negligible in this case, and because it is easy to lose ZVS. A higher value of I_{th} is desired. The analysis has been repeated for $I_{th} = 3.5$ A, and the results are shown in Figure 4.25.

From this plot, it is clear that the difference between $i_L(0)$ and $i_L(T_{tr})$ is reduced compared to the results for $I_{th} = 2.5$ A. Moreover, the steps in $i_L(T_{tr})$ between modes are considerably reduced too. More importantly, $i_L(T_{tr})$ is not as close to zero at $\omega \cdot t = 3\pi/2$ as before, but it is round 2.5 A. This implies a margin for the selection of the dead-time as it is less likely to lose ZVS if the

Figure 4.25: ZVS transitions for $I_{th} = 2.5$ A and $I_{th} = 3.5$ A. $i_L(0)$, $i_L(T_{tr})$, and T_{tr} for the transitions i and ii are shown.

dead time is selected slightly longer than the transition time. Also, the transition time is shorter and less variable, and 150 ns or 200 ns seems as safe value for the dead time when $I_{th} = 3.5$ A is considered.

The same calculations have been repeated for $PF = 0.7$ capacitive and inductive load, and under no load. In the three cases, $I_{th} = 3.5$ A and a dead time of 150 ns are enough for ZVS. However, to allow some margin for tolerances and delays, a value of 200 ns for the dead time is selected. If a larger value for I_{th} were used, $i_L(T_{tr})$ would be closer to I_{th} , and the dead-time would be decreased even more. Unfortunately, a higher I_{th} has negative implications, as discussed in the following subsection.

The minimum current for the transition is calculated for every possible transition and every possible voltage for the three ports in Appendix A, concluding that $I_{th} = 3.5$ A is enough in all conditions. In the worst case, the minimum initial current is as high as 2.6 A with the devices used for the prototype. This worst-case current is reached in the i transition [$110 \rightarrow 111$] when $V_g = 450$ V.

With this value of I_{th} , the transitions with " $i_L \neq 0$ " that lacked ZVS discussed in Section 4.2.1 (the transition [$101 \rightarrow 001$] in Figure 4.14), are no longer a problem. The reason is that with the

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TCM modification of the modulation, these transitions always take place at values above I_{th} (or below $-I_{th}$), meaning that the current is high enough for ZVS.

4.4.4 Negative impacts of the threshold current and discussion

Changing the modulation from BCM to TCM also has disadvantages. First, as I_{th} increases, so does T_{np} and T_{pn} , meaning that the inverter dedicates a considerable amount of the switching cycle to move power back and forth in the added states [111] and [000]. Therefore, higher I_{th} implies additional indirect power in the inductor, and higher rms and peak currents, ultimately leading to higher losses and volume. In general, this is the price to pay when TCM is applied in any converter, as discussed back in Section 2.1.3.

Another disadvantage associated with the additional states [111] and [000] is that the six switches are turned on and off once per switching cycle. That was not the case with the BCM modulation, where there were some modes where only two pairs of switches were switched per cycle. For instance, in $Tra4^+$, q^+ was always on. On the other hand, in the modes $T0$, $T1$, $T2$, $T3$, and $Th2$ (positive or negative), all devices were switched once, so the TCM modulation does not modify the number of devices switched.

Finally, it is noteworthy that due to the additional states, the control is more complex in TCM than with the BCM modulation.

To conclude this analysis, a value of 3.5 A for the threshold current seems reasonable, as it ensures ZVS in all transitions, avoids the low-frequency problems associated with the voltage limits between modes, and sets the maximum switching frequency at 400 kHz. Nevertheless, it is interesting to discuss how different parameters affect the selection of I_{th} , especially how the inductance value is a critical parameter in the inverter design and performance due to the switching frequency and ZVS constraints previously discussed. The goal is to extend the description in this analysis to other power levels and device selection. Because of the negative impact that I_{th} has in the operation of the inverter, it is desirable to keep it as low as possible.

From the equations for ZVS discussed in Chapter 3, $i_{L\ min}(0)$ (and then I_{th}) is ultimately proportional to $\sqrt{C_{oss}/L}$. Therefore, the selection of the inductance value and the used devices impacts the threshold value when it is limited by ZVS constraints. The constraint is not related to the currents in the ports. However, if the total C_{oss} is increased so does I_{th} .

The inductance value is related to the switching frequency through Equation 4.3 for the minimum value when it is reached in the voltage limits. Also, Equation 4.5 shows how the inductance value is related to the maximum switching frequency. These effects are not related to C_{oss} directly. The maximum frequency is inversely proportional to the inductance. Therefore, for a lower maximum switching frequency, the value of L should be increased. A different alternative to lower the maximum switching frequency could be to increase I_{th} beyond the value set by ZVS or minimum frequency, but this is not recommended, as mentioned earlier. This value is not a function of the nominal load as it is calculated for the no-load condition.

Finally, the relation of the parameters to the minimum frequency is more subtle. In the case of $V_g - V_s = V_o$ and $I_g = I_o$, the inductance is only related to how long the times T_{np} and T_{pn} last when I_{th} is held constant. For a given L , the minimum switching frequency is proportional

to $(I_{th} - I_g)/I_{th}^2$. As mentioned before, the first limitation is that $I_{th} > I_g$. Therefore, due to the operation is this point with the proposed TCM modulation, designs for higher power levels (higher I_g) require a higher value of I_{th} . Also, it should be noted that as I_{th} increases, a point is reached where the minimum switching frequency decreases instead. In other words, at $I_{th} = 2 \cdot I_g$, $f_{sw \min}$ stops increasing.

It is interesting to see how I_{th} could modify the actual design of the inverter. For the inverter, for 1 kVA nominal power, $L = 80 \mu\text{H}$, the C_{oss} of two *GS66516T* GaN devices in parallel, and I_{th} set at 3.5 A are used. Increasing the inductance value beyond 80 μH can slightly help to reduce the maximum switching frequency, but the minimum frequency would not change much if I_{th} is not varied. Increasing L implies that less $i_{L \min}(0)$ is required for ZVS. Unfortunately, I_{th} cannot be decreased as it is already close to I_g (2.5 A), so it is not advantageous. Moreover, increasing the value of L for the same power level implies higher energy in the inductor, probably leading to higher volume. Therefore, increasing the inductance trying to lower I_{th} does not seem a reasonable approach to follow.

On the other hand, decreasing the inductance leads to a smaller inductor size and increases the minimum frequency if I_{th} is held at 3.5 A. Unfortunately, the maximum switching frequency rises quickly. The current for ZVS increases too, although at a lower rate as it goes with the square root of the inductance. Therefore, with a lower value of L , the value of I_{th} would have to be increased, and so the rms and peak inductor current would increase.

Therefore, the value of the inductance is appropriate from the point of view of the I_{th} selection. A similar value for I_{th} for ZVS and minimum switching frequency constrains is obtained. However, the optimum value of I_{th} has to be obtained through careful optimization accounting for the volume and losses of all devices.

This value would change for different nominal I_g and C_{oss} . It is also interesting to analyze the scalability of this inverter in terms of output power. If the input current increases, I_{th} should be increased too. Then, depending on the value of C_{oss} , the inductor could be set, so ZVS is achieved with the value used for I_{th} . Even if ideal switching devices without C_{oss} were used, and no current was required for ZVS, I_{th} would not be reduced with the proposed solution. As a result, the value of I_{th} can be relatively high, as it is the case of the solution proposed, where $I_{th} = 3.5$ A in an inverter with an input current of 2.5 A.

4.4.5 Inductor current along the line cycle

The last part of this section is dedicated to explain how the TCM modulation with constant I_{th} shapes the current in the inductor along the line cycle. In this section, the transitions for ZVS are neglected too. Figures 4.26 to 4.29 show the inductor current waveform along the line cycle for $I_{th} = 3.5$ A and different loads, the same loads considered for Figures 4.2 to 4.5, respectively. Therefore, the sequence of modes along the line cycle is the same as in those plots. In Figures 4.26 to 4.29, the switching period has been enlarged twenty times, to depict the operation modes clearly. In these plots, it can be observed how I_o , I_s , and I_g are obtained through the modulation of i_L , and how the frequency changes along the line cycle. For this representation, the voltages and current

4.4. Proposed TCM modulation

in the ports are assumed constant during the switching cycle. For this reason, the current in the ports looks fragmented.

Figure 4.26: Representation of the modulation for 1 kVA resistive load and $I_{th} = 3.5$ A.

Figure 4.27: Representation for 1 kVA $PF = 0.7$ capacitive loads and $I_{th} = 3.5$ A.

In Figure 4.26, the inductor current waveform changes smoothly from a switching cycle to the next, even when the modes are shifted, proving that the modulation is seamless. The limits between modes are added as vertical lines as, otherwise, it would be hard to distinguish the different modes. In Figure 4.27 an abrupt change in the shape of the inductor current waveform seems to appear in $Tra3^+$, but this is because one out of twenty switching cycles is represented as the period is enlarged. In the real waveform, the evolution of the shape of the current waveform does not change sharply. Also, the frequency at that point is very low; the reason is that that operation point is close to $V_g - V_s = V_o$ and $I_g = -I_s = I_o$, discussed in Figure 4.20. Finally, as the load in Figure 4.29 is very low, it can be observed how the switching frequency is given by I_{th} mainly.

 Figure 4.28: Representation for 1 kVA $PF = 0.7$ inductive load and $I_{th} = 3.5$ A.

 Figure 4.29: Representation for 250 VA resistive load and $I_{th} = 3.5$ A.

To obtain these waveforms, the time each state lasts in different modes depends on the voltage and current in the three ports. A detailed analysis of how those times are calculated is given in Appendix C.

To highlight the effect that I_{th} has on the shape of the inductor current along the line cycle, Figure 4.30 shows the shape of i_L for different values of I_{th} and 1 kVA resistive load. In these waveforms, the switching period is not scaled, and, instead of showing the inductor current as a black line (that would cover the whole waveform), only the current in the transitions are marked. Said differently, the value of the current between different states is shown in gray. Those are the values I_{th} and $-I_{th}$, and the two peaks of the Tra^p , Tra^n , and T modes in Figure 2.11. The bottom plot for $I_{th} = 3.5$ A is the same plot shown in Figure 4.26 to clarify the idea. As before, the vertical lines represent the limits of the modes, and the green and purple shades represent the input current and storage capacitor current, respectively.

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Figure 4.30: Representation of the modulation for 1 kVA resistive load with $I_{th} = 1.5$ A, $I_{th} = 2.5$ A and $I_{th} = 3.5$ A respectively, highlighting the inductor current in the transitions between states.

Leaving aside the fact that in certain parts of the line cycle $I_{th} = 1.5$ A is not enough for ZVS and that there is no solution for the voltage limits, this plot shows how the peak current in the inductor is affected by I_{th} . The peak inductor current is reached in $Tra4^+$ and $Tra4^-$ slightly sooner than the point where P_o reaches the maximum, with a value around 13 A for $I_{th} = 3.5$ A. With lower values of I_{th} , this peak is reduced. In fact, for $I_{th} = 1.5$ A the value would be around 11.5 A. Therefore, I_{th} negatively impacts the rms and peak value of the inductor current as mentioned before. Also, the behavior in the limits between $T0$ and $T1^+$ and $T0$ and $T1^-$ get worse with a lower I_{th} . With $I_{th} = 1.5$ A, besides the low-frequency operation in these points, the peak current rises considerably, proving that the inverter cannot work for low values of I_{th} with the proposed modulation.

4.5 Justification of the selected modulation

The inverter and its modulation are designed to minimize the indirect power in the inductor. The combination of operation modes selected is the one featuring minimum P_{indL} in this inverter while allowing for ZVS transitions [16]. Nevertheless, it could be argued that this metric may not lead to the smallest and most efficient inductor design, and a different combination of operation modes may be better. In other words, different metrics could have been used. One can try to select the modes so the switching frequency is minimized for a given inductance, as a modulation with a lower f_{sw}/L would allow for a reduction of the inductance value for a given f_{sw} . One could try to minimize the peak energy in the inductor, aiming to minimize its size. This is equivalent to minimizing the peak current in the inductor. Perhaps minimizing the rms current in the inductor is a better metric to select the operation modes, as it also reduces the rms in switching devices since switching losses are already low because of the ZVS transitions. None of these metrics alone can provide the correct answer; the best modulation should come from optimization and comparison for each possible operation mode in each specific point. Although it should be noted that the previous metrics will contribute to some extent to the volume and losses in the inductor.

To highlight that P_{indL} is a reasonable metric for the selection of the modulation in this inverter, Figure 4.31 shows P_{indL} together with other possible metrics along the line cycle, for 1 kVA resistive load, $L = 80 \mu\text{H}$ and $I_{th} = 3.5 \text{ A}$. In the figure, all possible modes with ZVS are included, not only the nineteen used in the modulation (seven for resistive load). In this figure, the switching frequency, peak inductor current, and rms current are shown.

The first thing to notice from Figure 4.31 a) is that the selected modulation is not the one featuring the minimum P_{indL} once I_{th} is considered. There are modes with slightly lower P_{indL} than $T0$, $T1^+$, and $T1^-$. Nevertheless, the operation modes shown in Figure 5.6 are preferred, as seamless operation between modes is achieved and the difference in P_{indL} is not appreciable.

P_{indL} for the BCM modulation is also shown in this figure to show the negative impact of setting $I_{th} = 3.5 \text{ A}$. The amount of power that the inductor processes when the TCM modulation is applied considerably increase compared to the BCM modulation where $I_{th} = 0$.

Figure 4.31 b) shows the switching frequency along the line cycle for the selected and discarded modes. The switching frequency with this modulation is practically above the switching frequency that any different modulation would have. This is precisely the opposite of what is desired. It implies that other modulations could achieve similar switching frequencies with a lower value of L . Nevertheless, these modulations would feature higher inductor current, as shown in Figure 4.31 c) and d), so it would not be the optimum. It is concluded that selecting the modulation based on the switching frequency in this inverter would not be reasonable.

As shown in Figure 4.31 c), the selected operation modes feature the minimum peak current, $\max(|i_L|)$, possible. Therefore, the energy requirements in the inductor are minimum if this sequence of modes is used. Also, this modulation features the minimum rms current in the inductor, as shown in Figure 4.31 d). The conclusion is that, in this case, the operation modes with lower indirect power coincide with those with lower rms and peak inductor current. This discussion proves that P_{indL} is a good metric to compare and select the operation modes in this inverter.

4.5. Justification of the selected modulation

Figure 4.31: Evolution of various parameters that could have been used to optimize the inductor along the line cycle, for 1 kVA resistive load with $I_{th} = 3.5$ A and $L = 80$ μ H, not only for the selected modes but for all possible operation modes, a) P_{indL} , including the value for BCM modulation, c) switching frequency, b) absolute value of peak current in the inductor, d) rms of the inductor current.

4.6 Conclusion

In this chapter, the BCM modulation that minimizes P_{indL} while ensuring ZVS transitions has been introduced. The limits of each operation mode and the seamless shifts have been discussed. With this modulation, the inductor current can be controlled to ensure a constant input current and a sinewave output current for the different loads specified for the LBC competition. The use of P_{indL} as a metric to select the modulation has been justified.

Then, how to solve some practical issues is explained. The proposed solution is to use a TCM modulation where two additional states ([111] and [000]) are switched between the threshold currents (I_{th} and $-I_{th}$). It has been proven that setting I_{th} at 3.5 A is a good tradeoff between switching frequency and ZVS and the increase in rms and peak current in the inductor. With this value of I_{th} , all the transitions perform ZVS; even the transitions the last state of an operation mode to the first state of a different one. Moreover, the inductor current waveform with the TCM modulation also evolves seamlessly from a switching cycle to the next.

Throughout this chapter, the values of $L = 80 \mu\text{H}$ and the C_{oss} showed in Figure 3.7 have been used. Therefore, this value for I_{th} is only valid for the selected inductance and switching devices. Since the value of I_{th} is affected by different parameters when it is defined for minimum switching frequency, maximum switching frequency, or ZVS, normalization is not an effective method to generalize the results. The same analysis could be repeated if the selection of the devices is changed.

The contributions of this chapter to the research line are the introduction of the modes $Tra1$, $Tra2$, and $T2$ used for inductive and capacitive loads, and the modes $T3$ and $Th2$ for low storage capacitor voltage (both positive and negative modes). These modes have been introduced to achieve seamless modulation all along the line cycle. The second contribution is the unified TCM modulation and the analysis of the effects of I_{th} .

Control

In the previous chapter, the modulation for the inductor was discussed, showing the shape of the inductor current waveform along the line cycle to obtain a sinewave output current and constant input current. In this chapter, how to design a controller capable of realizing such modulation is discussed. The control is divided into various control loops and the inversion-based control, or *plant inversion*. In general, in three-port single-stage converters, the control is complicated because the control loops are cross-coupled [59]. The plant inversion is used to decouple the control variables from the modulation, enabling the use of regular control loops.

First, the control requirements of single-phase inverters with energy buffering are briefly reviewed, highlighting the challenges associated with single-stage power conversion. Then, the complete control structure and how the control loops are implemented for this inverter is shortly reviewed, based on the work in [40], [73], and [74]. Only a brief review is provided, as this is not a contribution of this work. Later, it is covered how the inversion-based control works, its implementation for the TCM modulation is the contribution of the chapter. Calculating the time each state lasts in the different operation modes is required for the inversion-based control and it is discussed in detail. The ideas discussed here are validated through simulation in *Gecko Circuit*.

5.1 Control implementation

This section reviews the design of the complete control structure and the control loops in this inverter to obtain a sinewave output voltage while ensuring constant power in the input port. First, the control of single-phase inverters is reviewed, then the decoupling networks for the control of single-stage inverters are discussed. Later, the control structure of this inverter and the different control loops are briefly explained.

5.1.1 Control loops for single-phase inverters with power decoupling

Before the implementation of the control in this inverter is discussed, the control loops typically employed in single-phase inverters with energy buffering are reviewed. According to the specifications of the LBC, reviewed in Section 1.3, the output voltage has to be 240 V rms at 60 Hz, and the input current has to be maintained nearly constant (a maximum of 20 % ripple).

A conventional solution to regulate the output voltage is to use a PI regulator. A proportional resonant (PR) controller can be used to improve the gain at 60 Hz [63].

On the other hand, the control of the input port depends on the type of architecture used. The different types of architectures were introduced in Section 1.5.1. For inverters with a bulky

input capacitor, there is no need to control the input current as the input capacitor is designed to meet the input current ripple specification. For two-stage architectures, the inverter controls the output voltage and the DC-DC stage is in charge of keeping the input current constant, regardless if the DC-DC stage is cascaded with the inverter or if it is an active filter. Nevertheless, the input current cannot be controlled directly for two reasons: how to determine the reference for the input current and how to ensure that the voltage in the storage capacitor is kept within the selected range.

For this reason, the input current reference is usually set based on the storage capacitor voltage. In [53] the storage capacitor voltage is controlled to follow a constant reference, and the loop is closed at 10 Hz to allow the 120 Hz voltage swing in the storage capacitor. This solution is also used in [45], where a slow PI loop controls the average value of V_s while allowing the voltage swing. The problem of this solution is the low bandwidth of the loop, resulting in a slow response of the average V_s under load steps, which may imply an oversized storage element.

A notch filter could be used to remove the 120 Hz component from the V_s measurement to improve the transient response. This technique is applied in [50], [51], [63] and [75]. With this solution, the bandwidth of the loop does not affect the 120 Hz component of V_s .

Another option to improve the dynamic response is to measure P_o and use this information together with the V_s loop to generate the reference for the input current. This solution is used in [5], as P_o changes with the load step, the effects in V_s are considerably attenuated. A similar solution is used in [12] and [43], where an *automatic-power-decoupling* control is proposed. Therefore, the voltage in the capacitor can be used to set the current reference for the DC-DC stage, although the controller should be designed to account for load steps.

To conclude, the control of two-stage solutions must ensure that the output voltage follows the reference and that the storage capacitor voltage is in the desired range while maintaining constant input power. The output and storage capacitor voltage loops are used to control the current of the ports, the inductor current directly, the duty cycle, or any other control variable of the power stages.

5.1.1.1 Decoupling techniques for single-stage inverters

This is also valid in single-stage three-ports inverters, but in this case, the control variables of the two voltage loops may be coupled through the power stage. However, the power stage couples the variables that are used to control V_s and V_o , and, as a result, conventional loops cannot be used directly.

Different techniques can be applied to decouple the control loops and enable the use of conventional controllers. These solutions are referred to as *decoupling networks*. In [89], the decoupling network consists of the inverse matrix of $G(s)$, where $G(s)$ is the matrix of the small signal transfer function of the plant. Adding this decoupling network after the regulators makes the transfer function from the regulator to the output to be $G(s) \cdot G^{-1}(s) = I$; the identity matrix. Therefore, the coupling of $G(s)$ is removed through the decoupling network, and conventional loops can be used. In [48] and [56], intermediate variables are used as control variables. Instead of controlling the duty cycle directly, two variables, each one associated with one loop, are used. Then,

5.1. Control implementation

these variables are related to the duty cycles through equations. As the intermediate variables are only a function of one of the loops each, the control is decoupled. A similar solution is also used in [51] and [75], in this case, applied to a single-stage rectifier. A technique called *feedback linearization* is proposed in [12] to decouple the control loops. In [59], the solution is also to include a network that behaves as $G^{-1}(s)$ for a DC-DC application involving a PV panel, a battery, and the load. In this case, the converter can work in different operation modes, and a different decoupling network is used for each case. A similar concept is applied to this inverter, called plant-inversion or inversion-based control, and it is going to be described in Section 5.2.

5.1.2 Control scheme in this inverter

The challenges the design of the controller for this inverter faces are explained in the previous section. As in any three-port inverter (single-stage or two-stage), not only the output voltage has to be controlled, but also the input current. It has to be controlled while keeping V_s in the desired range even after a load step. Also, the control loops are coupled because of the single power stage used, and decoupling networks are required. This section briefly discusses the general structure for the control of the inverter, how the different parts are related, and how the control loops are implemented. This section is not detailed because is not a part of the author's work but it is included for completeness. For a complete description of the control loops and advanced consideration please refer to [40], [73], [74], and to the Ph.D. dissertation of Regina Ramos to be presented in 2021.

The control scheme for the inverter is divided into two main parts: the control loops and the inversion-based control. In Figure 5.1 the complete control structure is shown.

Figure 5.1: Control scheme showing the loops in red, the inversion-based control and modulator in green, and the power stage and additional circuitry in yellow.

Every switching cycle, the output, storage capacitor, and input voltages are measured. The input and output currents are measured too. With this information, the regulator for the output voltage loop, $R_{V_o}(s)$, generates the reference for I_o , and the regulator of the storage capacitor loop, $R_{V_s}(s)$, sets the reference for I_g to keep the average V_s at the desired value. The reference current for I_g also includes the information of the active power of the output, added to speed up the response of the storage capacitor voltage loop after load steps. Then the inner current regulators, $R_{I_g}(s)$ and $R_{I_o}(s)$, correct the error between the references and the measured values for I_g and I_o . The outputs of these loops are the target I_g and I_o that should be obtained through the modulation of the inductor current in that switching cycle. For this purpose, the inversion-based control and

the modulator generate the adequate switching pattern for the six transistors to obtain the desired I_g and I_o .

The transfer function of the inversion and the power stage leads ideally to $I_g^{Real} = I_g^{Target}$ and $I_o^{Real} = I_o^{Target}$ because the modulation applied to the power stage creates the desired current waveform in the inductor, which is translated in the desired I_g and I_o . This concept is discussed in detail in Section 5.2.

The following subsections describe the control loops. For the design of the current loops, it is assumed that the plant inversion is ideal, this is, $I_g^{Real} = I_g^{Target}$ and $I_o^{Real} = I_o^{Target}$. The current loops are designed so $I_g^{Real} = I_g^{Target}$ and $I_o^{Real} = I_o^{Target}$ for any frequency. For the design of the voltage loops, the current loops are assumed to work ideally. Therefore, together with the assumption of an ideal inversion-based control, it is assumed that $I_g^{Ref} = I_g^{Real}$ and $I_g^{Ref} = I_g^{Real}$. It is also assumed that the voltage measurements are ideal ($H(s) = 1$), then $V_g^{Real} = V_g^{Meas}$ and $V_o^{Real} = V_o^{Meas}$. Furthermore, the delay caused by the controller is neglected. Those variables are represented in the scheme of Figure 5.1 to clarify the idea.

5.1.2.1 PI storage capacitor voltage loop

The goal of this loop is to ensure that the $\overline{V_s}$ is kept in the desired value (340 V) while allowing the voltage to swing for power decoupling. As mentioned before, an option to ensure that the storage capacitor voltage is kept within the desired DC value maintaining the input current nearly constant is to set the bandwidth of the storage capacitor loop well below $2\omega_{line}$.

$R(s) \cdot G(s)$ has to be designed as high as possible below the bandwidth to minimize the steady state error. For this reason, a PI regulator is selected. It is designed for bandwidth of 12 Hz, ten times below $2\omega_{line}$, and with enough phase margin [74].

5.1.2.2 Active power estimation

Since the capacitor voltage loop has very limited bandwidth (12 Hz), the input current takes a long time to change after a load step. When that happens, the storage capacitor may be overcharged and clamped to V_g with the body diodes of d^+ and d^- , or discharged to unreasonable values below $V_g/2$ where the capacitor current and inductor rms current increase considerably.

An active output power loop is included to reduce this effect, which adds its output to I_g^{Ref} , as shown in Figure 5.1. This active power estimation block makes the input current reference proportional to the output power. The input current reference has to be defined as $I_g = \overline{P_o}/V_g$ to make $P_g = \overline{P_o}$. Obtaining V_g for this equation is not a problem as it is measured once per switching cycle, however, obtaining $\overline{P_o}$ is more complicated as it varies at twice line frequency. To estimate the output power for linear loads, $\alpha\beta$ or dq theory to single-phase inverters can be applied [40], [74]. Conceptually, the average output power can be obtained by adding the output power a quarter cycle before and the actual P_o :

$$\overline{P_o}(t) = \frac{P_o(\omega_{line} \cdot t) + P_o(\omega_{line} \cdot t - \frac{\pi}{2})}{2} \quad (5.1)$$

5.2. Inversion based control

The value for I_g calculated as $\overline{P_o}/V_g$ through Equation 5.1 is added to the output of the V_s loop to generate the reference for the input current. This additional feedforward adjusts the input current within a quarter cycle in the event of a load step, significantly improving the dynamic response of the V_s loop [74].

5.1.2.3 Proportional resonant output voltage loop

The output voltage loop is designed to ensure that V_o follows the 240 V rms 60 Hz reference. Since the reference is a sinewave at 60 Hz, a PI regulator is not enough in this case as it would give a finite gain at line frequency. A resonant controller tuned at the line frequency is used to improve the gain.

Moreover, to improve the DC gain, a proportional controller is used. Therefore, a proportional resonant (PR) regulator to control V_o is used in this inverter [73]. The output of the PR regulator is the reference for the output current.

5.1.2.4 PI current loops

Current loops are added to the control scheme to ensure that I_g^{Real} and I_o^{Real} follow closely I_g^{Ref} and I_o^{Ref} respectively [40]. Therefore, the goal is to achieve loops with unity gain.

Unlike the voltage of the ports that are practically constant along the line cycle, the input and output currents evolve with the shape of the inductor current waveform along the switching cycle. Therefore, these currents contain harmonics at the switching frequency. A low pass is set at around $\omega_f = 2\pi \cdot 100$ Hz to measure the average input and output current while avoiding the switching frequency components. Therefore, in this case, the transfer function of the feedback is $H(s) = 1/(1 + s/\omega_f)$.

As $G(s) = 1$ since ideal plant-inversion is assumed, to obtain a closed loop gain of 1 the regulator is designed with the transfer function $R(s) = 1/(1 - H(s)) = \omega_f/s + 1$ to compensate for the effects of the low pass filter. Because of the fast response (infinite in theory) of the current loops, the assumptions $I_g^{Ref} = I_g^{Real}$ and $I_o^{Ref} = I_o^{Real}$ used in the design of the voltage loops are valid. However, for this scheme to work, the inversion-based control has to ensure that $I_g^{Real} = I_g^{Target}$ and $I_o^{Real} = I_o^{Target}$.

5.2 Inversion based control

As described earlier, a decoupling network is required to ensure that I_g and I_o are equal to the target values, regardless of what the control variables are. In this inverter, there is an additional degree of complexity for the decoupling network compared to other single-stage inverters: there are nineteen different operation modes with different relations between the control variables and I_g and I_o .

To shape the inductor current in each mode, the time each state lasts together with current detection for the levels I_{th} and $-I_{th}$, is required (following the representation in Figure 5.1). The task of the inversion-based control is to calculate the time each state lasts and the operation mode used. With this information and the detectors for the levels $i_L = I_{th}$ and $i_L = -I_{th}$, the

modulator generates the driving signal for the six transistors, shaping the inductor current. If the inversion-based control is accurate, the values for I_g^{Real} and I_o^{Real} in the switching cycle would match the input values of the inversion-based control, I_g^{Target} , and I_o^{Target} . The contribution of this section is the equations and implementation of the plant-inversion and modulator for the TCM operation of the inverter. For BCM modulation, this work can be found in [40].

The first part of this section explains how the TCM modulation is implemented. Then, a considerable part of the chapter is dedicated to describing how the times the states last are calculated.

5.2.1 TCM modulation and control of the time each state lasts

The inductor current for the TCM modulation proposed in the previous chapter is determined by a few factors: the sequence of switching states, which is the operation mode, the voltage applied to the inductor in each state, associated with the voltage in the three ports, the time the different states last, and the value of I_{th} and L . With this information, $i_L(t)$ is unambiguously defined.

The parameters that are controlled in this inverter are the operation mode and the times the states last. Other variables could have been used, such as the peak currents of the inductor waveform, or the duty cycles, phase-shifts, and switching frequency of the six switches. Yet, the most direct approach is to control the times directly from I_g^{Target} and I_o^{Target} [74].

The control based on the times each state lasts in this inverter is a more complex version of the on-time control commonly used in BCM PFC applications to obtain unity power factor. This type of control is sometimes referred to as *variable on-time control*, or merely *on-time control* [79]. In those cases, the time the magnetization state lasts is controlled (and kept nearly constant along the line cycle), and the demagnetization state lasts until $i_L = 0$ when the zero-current detection triggers. The on-time control should not be interpreted as duty cycle control with variable frequency since the demagnetization time does not end at a predefined time [79]. Since the inductor current waveform is estimated to generate the driving signals, the control could be considered a kind of predictive current control [90]. This TCM modulation and control can also be applied to DC-DC converters [91].

However, at least the times of two of the states have to be controlled as there are two control variables in this inverter. Also, the current detection does not trigger at $i_L = 0$ but at $i_L = I_{th}$ and $i_L = -I_{th}$. The equations that define i_L are more complex as a result.

5.2.1.1 Unified representation for all modes

To describe the relation of the inductor current and the time each state lasts in different operation modes, the waveform for the T , Tra^p , and Tra^n modes in Figure 2.11 and the additional states shown in Figure 4.19 can be combined into the waveform shown in Figure 5.2.

With this representation, in Tra^p modes $T_4 = T_5 = T_6 = 0$, in Tra^n modes $T_1 = T_2 = T_3 = 0$ and $T_2 = T_5 = 0$ in T modes. In this work, T_1 to T_6 ($\mathbf{T}_{1-6}$) are termed *control times*. $\mathbf{I}_{1-6}$ are the current in the different states. It should be clarified one more time that I_1 to I_6 refers to the average current of each state along the total switching cycle, not the time each state lasts. $\mathbf{m}_{1-6}$ represents the slope of the current in each state, v_L/L . The advantage of such representation is that

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Figure 5.2: Generic waveform for the inversion-based control. Valid for Tra^p , Tra^n , and T modes with TCM modulation and showing the names of the variables used.

it is valid both for T and Tra modes, and it is helpful to avoid repetition in the implementation of the plant-inversion.

A fundamental property of this modulation is that at the beginning of the switching cycle $i_L = -I_{th}$, a constant value, as shown in Figure 5.2. Therefore, the inductor current is not a state-variable, implying that I_L is not a function of I_L of the previous cycle and simplifying the control structure. This is generally a property of converters operated in BCM.

5.2.1.2 Equations for the plant-inversion

As mentioned before, the goal of the inversion is to relate the target input and output current with the control times for any given mode. The complete analysis of how these variables are related is included in Appendix C, not to extend this chapter. Only the results are reviewed in this section. This analysis is based on the previous work of Regina Ramos developed for the BCM modulation, it is explained in Appendix B with a general nomenclature. To obtain this relationship, first, the current in each state is obtained, and then they are related to the control times.

The process described Section 2.2.2 can be used to relate the current in the state with the current in the ports. In other words, Equations 2.15 for Tra modes and 2.23 for T modes are valid. Only the number of the state should be updated to match Figure 5.2. These equations are obtained again in Appendix C, discussing why I_{th} does not change the results and why this step is required to obtain the control times.

Once I_1 to I_6 are obtained as a function of I_g , I_s and I_o , the relation between I_{1-6} , m_{1-6} , and T_{1-6} is given by Equation C.3, repeated here to clarify the problem:

$$\begin{aligned} I_1 &= \frac{T_1}{T} \frac{2I_{th} + m_1 \cdot T_1}{2} & I_2 &= \frac{T_2}{T} \frac{2I_{th} + m_1 \cdot T_1 - m_3 \cdot T_3}{2} & I_3 &= \frac{T_3}{T} \frac{2I_{th} - m_3 \cdot T_3}{2} \\ I_4 &= \frac{T_4}{T} \frac{-2I_{th} + m_4 \cdot T_4}{2} & I_5 &= \frac{T_5}{T} \frac{-2I_{th} + m_4 \cdot T_4 - m_6 \cdot T_6}{2} & I_6 &= \frac{T_6}{T} \frac{-2I_{th} - m_6 \cdot T_6}{2} \end{aligned} \quad (5.2)$$

Where T is the sum of T_{np} , T_{pn} , and the control times. T_{np} and T_{pn} can be obtained directly from Equation 4.1. Unfortunately, from this relation it is hard to obtain the control times, the reason is that the system of equations is nonlinear and that all the control times appear in all the equations in the term T . When BCM is considered, an analytical solution can be obtained, as described in Appendix B [40]. Unfortunately, it is no longer possible when I_{th} is considered. To

obtain $\mathbf{T}_{1-6}$ an iterative process based on a fixed-point iteration is proposed in Appendix C. This iterative process is:

$$\begin{cases} T_1^{[n+1]} = 2 \cdot I_1 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} + m_1 \cdot T_1^{[n]}} \\ T_2^{[n+1]} = 2 \cdot I_2 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} + m_1 \cdot T_1^{[n]} - m_3 \cdot T_3^{[n]}} \\ T_3^{[n+1]} = 2 \cdot I_3 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} - m_3 \cdot T_3^{[n]}} \\ T_4^{[n+1]} = 2 \cdot I_4 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} + m_4 \cdot T_4^{[n]}} \\ T_5^{[n+1]} = 2 \cdot I_5 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} + m_4 \cdot T_4^{[n]} - m_6 \cdot T_6^{[n]}} \\ T_6^{[n+1]} = 2 \cdot I_6 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} - m_6 \cdot T_6^{[n]}} \end{cases} \quad (5.3)$$

$\mathbf{T}_{1-6}^{[n]}$ converges to the solution after a few iterations, as demonstrated in Appendix C. To clarify the concept, Figure 5.3 shows $\mathbf{T}_{1-6}$ solving Equation 5.3 with a hundred iterations after $\mathbf{I}_{1-6}$ are calculated with Equations B.8, B.8, and B.11, for 1 kVA resistive load, $L = 80 \mu\text{H}$, and $I_{th} = 3.5 \text{ A}$.

Figure 5.3: Evolution of the control times along the line cycle, 1 kVA resistive load, $L = 80 \mu\text{H}$ and $I_{th} = 3.5 \text{ A}$.

Some jumps are observed in the control times in some shifts between modes. For instance, in the boundary between $Tra3^+$ and $T1^+$ or $T1^+$ and $T0$. The reason is that control times are not associated with defined switching states in terms of $[dhq]$ or $[g \ s]$, they are associated with the position of the state in the sequence.

Figures 4.26 to 4.29 were obtained using a hundred iterations and starting from $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$ for every switching cycle too. Solving a large number of iterations is not a problem for a *Matlab* script. Unfortunately, implementing such iterative process in a controller that solves these equations in real-time is challenging. Each iteration takes some computing time, and a hundred iterations may be unreasonable as it could take longer to calculate the control times than the switching period itself. Also, lowering the number of iterations is not a good solution either as it reduces the accuracy, leading to errors in the inversion-based control.

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To overcome this problem and ensure high accuracy with a low number of iterations, a solution is to choose the initial iteration point, $\mathbf{T}_{1-6}^{[0]}$, already close to the solution, as illustrated in the next subsection.

5.2.1.3 Control times and applied times

To reduce the number of iterations in Equation 5.3 for a given accuracy, $\mathbf{T}_{1-6}^{[0]}$ should be selected close to the final solution. For this purpose, the value of T_1 to T_6 from the previous switching cycle can be used as $\mathbf{T}_{1-6}^{[0]}$, as control times barely change from a switching cycle to the next. This is commonly applied for implicit integration of ordinary differential equations where the initial iterate is derived from the solution at the previous time step [92]. Unfortunately, this solution is not applicable all along the line cycle; there are abrupt changes in the control times in the shift between some modes, as explained before. For instance, this is not a good solution for the shift from $Tra3^+$ to $T1^+$ in Figure 5.3, because $T_3 = 0$ in $Tra3^+$ but it is around $3 \mu s$ in $T1^+$. Therefore, setting $T_3^{[0]} = 0$ to calculate the control times in the first cycle of $T1^+$ hardly reduces the number of iterations required. The appropriate value for $T_3^{[0]}$ in $T1^+$ at this point would be the value of T_2 in the last cycle of $Tra3^+$. The reason is that the state [101] is labeled as 3 in $T1^+$ but as 2 in $Tra3^+$. In other words, the times evolve smoothly, just not according to the definition of $\mathbf{T}_{1-6}$ used in Figure 5.2. For this reason, a different waveform to represent the operation modes is introduced. In this representation, times are defined so a continuous evolution from a switching cycle to the next is achieved, even in the shift between modes.

Figure 5.4 shows this general representation valid for all modes. In this case, the states are associated with the $[dhq]$ or $[g \ s]$ sequence. This waveform results from the combination of the added states for ZVS shown in Figure 4.19 with the diagram of the transitions achieving ZVS depending on the direction of the current in the inductor from Figure 3.2. The waveform is divided into ten states, the auxiliary states [111] and [000], and the other states labeled from a to h .

Figure 5.4: Generic waveform, including I_{th} with states labeled according to the $[g \ s]$ nomenclature.

The times T_a to T_h are termed *applied times*, to differentiate them from the control times described before ($\mathbf{T}_{1-6}$ in Figure 5.4). As before, for any given operation mode, most of the times

last zero. Also, there are three possible states for the cases b , c , f , and h , which of the three states is used in each case is selected depending on the mode. A solution where a single variable is used to represent three different states is preferred. For instance, T_b is used for the states $[0 \ 0]$, $[+1 \ -1]$ or $[0 \ +1]$ with positive current. The reason is that these three states are never used together in a mode. As it is going to be detailed later, the waveform in Figure 5.4 is used to determine the gate signal for the six switches based on the operation mode and applied times.

Since the modulation is seamless, $\mathbf{T}_{a-h}$ change continuously along the line cycle. This evolution is depicted in Figure 5.5 for the same port variables used in Figure 5.3. Unlike $\mathbf{T}_{1-6}$ in Figure 5.3, in this case, $\mathbf{T}_{a-h}$ is continuous even in the shift of modes. This plot validates the concept of seamless modulation and shows that the changes in $\mathbf{T}_{a-h}$ from a cycle to the next one are small, proving useful to use the calculated times in the previous cycle as the starting point for the iteration of the following one.

Figure 5.5: Evolution of the applied times along the line cycle, 1 kVA resistive load, $L = 80 \mu\text{H}$, and $I_{th} = 3.5 \text{ A}$.

These times have not been calculated, instead, the values of $\mathbf{T}_{1-6}$ from Figure 5.3 have been assigned to $\mathbf{T}_{a-h}$ for every mode. An iteration for $\mathbf{T}_{a-h}$ as Equation 5.3 for $\mathbf{T}_{1-6}$ is not proposed. The reason is that the equations that would be required to relate the current in the ports to the applied times would much more complex if the representation in Figure 5.4 is considered.

Figure 5.6 clarifies how the control times and applied times are assigned in different modes. This figure includes the nineteen operation modes, represented with the states $[111]$ and $[000]$ between I_{th} and $-I_{th}$, and with their states labeled according to the $[dhq]$ and $[g \ s]$ nomenclature. The figure summarizes the work presented in Chapter 4, and it is a more detailed description of the work presented in [87].

To conclude this section, the advantage of using the times $\mathbf{T}_{a-h}$ is that the evolution is continuous along the line cycle. Therefore, the value of the previous cycle can be used as the initial point for the iteration process used to calculate $\mathbf{T}_{a-h}$ in the following switching cycle. Thus, improving accuracy and/or reducing the computational cost of the iteration. This one of the contributions of this work, and the main reason why a seamless modulation is required to

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Figure 5.6: Inductor current waveform for the nineteen operation modes with TCM modulation, including the control and applied times, using the $[dq]$ and $[g-s]$ nomenclature for the different states.

control the inverter. In the following section, how the iteration is implemented including how $T_{1-6}^{[0]}$ is defined as the value of the previous cycle is discussed.

5.2.2 Implementation of the inversion-based control

In this section, the operation of the *inversion-based control and mode selector* block in Figure 5.1 is described. The goal of this block is to translate the target input and output current into the operation mode and applied times used in the modulator to generate the driving signals for the

transistors. The tasks of this part of the controller are mainly to select the operation mode, to obtain the current in each switching state, and to calculate the applied times. A flowchart representing the different steps in this process is shown in Figure 5.7. This process is repeated every switching cycle, and, besides I_g^{Target} and I_o^{Target} , it requires the measured voltages in the three ports and the applied times of the previous switching cycle. Each step of the inversion-based control is detailed below, labeled as in Figure 5.7:

Figure 5.7: Different stages of the inversion-based control.

- **1) Storage capacitor current:** The target I_s is required to decide which mode to apply and to calculate the current of the different states in Tra modes. I_s is obtained through the power balance of the three ports as:

$$I_s^{Target} = \frac{V_o^{Meas} \cdot I_o^{Target} - V_g^{Meas} \cdot I_g^{Target}}{V_s^{Meas}} \quad (5.4)$$

- **2) Mode selector:** With the target currents and the measured voltages in the three ports, the operation point can be identified; this can be interpreted as finding the point of the XYZ plots from Section 4.1.3. The operation mode that should be applied is identified. Therefore, by checking the voltage limits of the modes given in Table 4.3 and the current limits in Table 4.4, which of the nineteen operation modes has to be used is determined. Once the mode is determined, so is the sequence of switching states, in other words, the parameters g_{1-6} and s_{1-6} or g_{a-h} and s_{a-h} are obtained.
- **3) Inductor current slope:** With the operation mode, the voltage applied to the inductor in each state can be calculated using $v_L = g \cdot V_g^{Meas} + s \cdot V_s^{Meas} - V_o^{Meas}$ with the values g_{1-6} and s_{1-6} obtained before. The slope of the inductor current in each switching state, m_{1-6} , is calculated by dividing the voltage applied over the inductance value. As described in Appendix C, m_2 and m_5 are not required for the following calculations.
- **4) Previous time assignation:** In this step, the appropriate values for $T_{1-6}^{[0]}$ for the iteration process are defined. For this purpose, the applied times of the previous cycle are used, T_{a-h}^{prev} . The values of T_a to T_h of the previous switching cycle are assigned to T_1 to T_6

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for the selected mode to set the initial values for the iteration ($\mathbf{T}_{1-6}^{[0]}$). The applied times are assigned to the control time using the relationships for the times in Figure 5.6.

- **5) State current calculation:** For the iteration used to calculate $\mathbf{T}_{1-6}$, the current in the states is required, $\mathbf{I}_{1-6}$. The currents are obtained based on the parameters $\mathbf{g}_{1-6}$ and $\mathbf{s}_{1-6}$ for *Tra* modes according to Equation B.8, and based on $\mathbf{g}_{1-6}$, $\mathbf{s}_{1-6}$, and $\mathbf{m}_{1-6}$ for *T* modes according to Equation B.12. This process is detailed in Appendix B for BCM operation, although it is valid for TCM operation too.
- **6) Iteration for the time calculation:** With the slopes, $\mathbf{m}_{1-6}$, the currents, $\mathbf{I}_{1-6}$ and the previous times, $\mathbf{T}_{1-6}^{[0]}$, the control times, $\mathbf{T}_{1-6}$, can be calculated using the iteration process of Equation 5.3. The value of I_{th} is needed for the iteration. T_{np} and T_{pn} are calculated through Equation 4.1, since T_{np} and T_{pn} are required to obtain the total period, $T^{[n]}$. As $\mathbf{T}_{1-6}^{[0]}$ are already close to $\mathbf{T}_{1-6}$, high accuracy is obtained even with few iterations.
- **7) Time assignation:** The last part of the process is to obtain $\mathbf{T}_{a-h}$, as it is required for the modulator. In this step, T_1 to T_6 are assigned to T_a to T_h based on the relation between applied and control times in Figure 5.6.

With this process, the relation cycle by cycle of the target I_g and I_o with $\mathbf{T}_{a-h}$ and the operation mode is obtained. Then, when the operation mode and the applied times are used to generate the signal for the six switches, i_L in the power stage has the expected shape. As a result, the average input and output currents are equal to I_g^{Target} and I_o^{Target} if the error introduced by the iteration process is neglected. The limitations of this concept are described later in Section 5.4. The great advantage of the plant-inversion is that the current loops are decoupled for all operation modes [74]. In other words, the control variables I_g^{Target} and I_o^{Target} are independent of the selected mode and operation point.

5.2.2.1 Iterative method with a single step

As shown before, $\mathbf{T}_{a-h}$ changes slightly from a switching cycle and the next one along the line cycle. This property can be used to reduce the number of iterations required to get an accurate solution for $\mathbf{T}_{1-6}$.

The iteration process in Equation 5.3 requires six divisions per step. Hence, it is a time-consuming process for the FPGA implementation, further detailed in Appendix D. Therefore, it is important to use the minimum number of steps possible. To minimize the time it takes for the iteration, a single step is used to solve the iteration process. Equation 5.3, when a single step is used becomes:

$$\begin{cases}
T_1 = 2 \cdot I_1 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{2I_{th} + m_1 \cdot T_1^{Prev}} \\
T_2 = 2 \cdot I_2 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{2I_{th} + m_1 \cdot T_1^{Prev} - m_3 \cdot T_3^{Prev}} \\
T_3 = 2 \cdot I_3 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{2I_{th} - m_3 \cdot T_3^{Prev}} \\
T_4 = 2 \cdot I_4 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{-2I_{th} + m_4 \cdot T_4^{Prev}} \\
T_5 = 2 \cdot I_5 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{-2I_{th} + m_4 \cdot T_4^{Prev} - m_6 \cdot T_6^{Prev}} \\
T_6 = 2 \cdot I_6 \frac{T_{np} + T_1^{Prev} + T_2^{Prev} + T_3^{Prev} + T_{pn} + T_4^{Prev} + T_5^{Prev} + T_6^{Prev}}{-2I_{th} - m_6 \cdot T_6^{Prev}}
\end{cases} \quad (5.5)$$

Where T_{1-6}^{Prev} are not the values of $\mathbf{T}_{1-6}$ of the previous cycle directly, but the values they would have had according to $\mathbf{T}_{a-h}$ of the previous cycle, as described before. This section is dedicated to proving that the accuracy is not significantly penalized when a single step for the fixed-point iteration is used.

A *Matlab* script has been implemented to validate this idea and check the error caused by using a single iteration. This iteration leads to the waveform of Figure 5.8 a) for the evolution of the total period, T , when different time distances between a cycle and the next one are chosen. The thick gray line represents the period obtained with the iteration process from Equation 5.3 setting $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$ with a hundred steps, and it is considered as the solution to the problem. Then, the lines with circles represent the period calculated using a single iteration and setting $\mathbf{T}_{1-6}^{[0]}$ as the values calculated a specific time before. In this case, these times are 1 ms, 500 μ s, and 100 μ s. It is observed that good accuracy is obtained when the value of $\mathbf{T}_{1-6}$ 100 μ s ago is used as $\mathbf{T}_{1-6}^{[0]}$. However, if this time between calculations is large, T gets far from the ideal value, and a considerable delay-like effect appears. This is a consequence of the control times depending on the previous values, and because the control times do not reach the final value. This plot is added to highlight that a single step iteration is only accurate when the time between calculations is high. Then, for switching frequencies higher than 10 kHz (100 μ s), the results are accurate.

The actual T calculated based on the values of $\mathbf{T}_{1-6}$ from the previous cycle considering the actual variable switching frequency of the inverter is shown in Figure 5.8 b). The waveform obtained using a hundred iterations is also shown for reference. These two waves are nearly equal. The relative error of the period obtained with a single iteration based on the previous step as compared to the ideal T , $(T|_{100 \text{ steps}} - T|_{\text{previous cycle}})/T|_{100 \text{ steps}}$, is shown in Figure 5.8 c). The error is more significant when the derivative of T with respect to time changes. The reason is this delay-like effect of using the cycle of the previous cycle as the initial point for the iteration. The conclusion is that the error in the total period is well below 5 %, so it is acceptable. The iteration of a single step based on the previous values is one of the contributions of this work, valid only because the times evolve smoothly from a switching cycle to the next.

5.2.3 Current detection and driving signals

The last part of the control is the modulator and dead time generator, shown in Figure 5.1. It is the state machine that generates the driving signal for the switches based on the times each state should last and the operation mode. Besides $\mathbf{T}_{a-h}$ and the operation mode, in this stage, it is also

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Figure 5.8: Fixed-point iteration based on the previous step for 1 kVA resistive load, a) for a determined time distance between a cycle and the next, b) for the real variable switching frequency of the inverter, c) error compared to the solution when a hundred steps are used.

required to know when the inductor current crosses the values I_{th} and $-I_{th}$. For this purpose, a current detector is implemented. The outputs of the current detector are two digital signals that change as i_L goes through a threshold.

The inductor current is measured to know when $i_L = I_{th}$ and when it is equal to $-I_{th}$ to ensure the correct operation of the additional states, [111] and [000]. Fortunately, i_L does not have

to be sampled; the current can be directly compared with the thresholds I_{th} and $-I_{th}$ to obtain the digital signals. These digital signals are called D^+ , D^- , and are implemented, as shown in Figure 5.9. D^+ is high when $i_L < I_{th}$ and low otherwise, and D^- is high when $i_L < -I_{th}$.

Figure 5.9: Digital signals for the detection of the current level. The current waveform does not correspond to any particular operation mode.

With this current detector, over-current (OVC) events can also be detected; it avoids the inductor current to get close to the saturation value of the core. For this design, OVC is set to $I_{ovc} = 18.5$ A, positive or negative. The digital signal that warns the FPGA in the case of OVC is also named OVC , and it is shown in Figure 5.9. How OVC protection is implemented is discussed in Section 5.2.4 and Appendix D.

T_{a-h} and the operation mode are obtained as discussed in the previous section. With this information and the digital signals D^+ and D^- , the driving signal for the six switches along the switching cycle can be generated. A general representation for the sequence of states valid for all modes along the switching cycle was represented in Figure 5.2, and it shows when each state begins. Yet, to clarify the concept, Figure 5.10 shows the state machine proposed to generate the driving signals. The first state is [111] starting with $i_L = -I_{th}$, which is equivalent to have a falling edge on D^- . [111] ends with the falling edge of D^+ . Then [111] is maintained for T_a . The second state is either [101] or [011] depending on the mode, and it lasts T_b ([110] is not used in any of the nineteen modes during T_b). The operation during T_c is similar. Then, after T_d , i_L should be equal to I_{th} again. At this point, [000] is applied until there is a rising edge in D^- . Then the rest of the states are applied with different states for T_f and T_g depending on the mode. After T_h , i_L should be equal to I_{th} and the new switching cycle begins.

As an additional protection to guarantee ZVS, the detectors are used to switch in case the current enters the band $-I_{th}$ to I_{th} before expected. D^+ is used after states two, three, and four if for any reason the current falls below I_{th} , and D^- is used after states seven, eight, and nine in case it goes above $-I_{th}$. When this happens, the modulation directly switches to [000] or [111], respectively, to ensure ZVS transitions in abnormal circumstances.

To avoid a false trigger of this protection, the detection right after the beginning of the states is disabled. This feature is similar to a *leading-edge blanking*. It waits for a time, T_{leb} , before reading D^+ from the change from state two, three, or four. The same is implemented for D^- in states seven, eight, and nine.

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Figure 5.10: State machine used to generate the driving signals as a function of the detection signals, the operation mode, and the applied times. *dhq* nomenclature is used to define the state of the six switches.

As a matter of fact, T_d and T_h are not required for the modulator because the state does not change after T_d or T_h . In other words, $[000]$ starts after T_c and ends when T_e ends, and $[111]$ lasts from the moment T_g is over to the point where T_a ends. Nevertheless, these values are calculated as they are used to obtain $T_{1-6}^{[0]}$ for the plant inversion. The state machine divided in ten steps is useful for synchronization with other processes, as it is detailed in Appendix D.

As mentioned in Section 4.4.3, for $I_{th} = 3.5$ A, a dead time around 200 ns should be used to ensure ZVS transitions. This dead-time is applied every time a state gives way to the following one. For the first 200 ns of each switching state, the devices that are going to be turned on are left open; it is only after the first 200 ns of the time each switching state last that the devices are closed. Even if a state lasts less than 200 ns, the 200 ns dead time is maintained. This implementation assumes the dead time as a part of the starting switching state. Regina Ramos implemented the dead-time generator, and it is further described in her thesis.

With this last detail, the structure of the complete control scheme in Figure 5.1 is covered, from the control loops to the modulator, including the plant-inversion.

5.2.4 Other aspects of the operation of the inverter

In this section, the start-up of the inverter and implementation of the protections are described.

Start-up sequence

The storage capacitor is precharged to 340 V before the output voltage is generated to avoid extremely high current in the storage capacitor upon start-up. This precharge is done at a slow pace, to avoid high inductor current, thus it can be considered as a soft-start. The soft-start is also going to be described in the dissertation of Regina Ramos.

Over-current protection

In the event of over-current detection, when there is a falling edge of the *OVC* signal, the six switching devices are opened to avoid the inductor current to keep rising. This condition is reset as soon as the inductor current is between I_{th} and $-I_{th}$ again. If OVC takes place with positive current ($D^+ = 0$), the cycle is resumed from the fifth state with [000] as soon as there is a rising edge in D^+ . On the other hand, if $D^- = 1$ when OVC triggers, the operation is resumed with the first state after the falling edge in D^- . This implementation avoids hard switching after the OVC condition. However, if OVC is reached several times, it may affect the leakage current because it generates a step in the CM voltage; this is further discussed in Section 6.3.1.1.

5.3 Validation through simulation

A simulation has been developed in *Gecko Circuit*, based on the simulation developed by Regina Ramos used in [40] to validate the proposed inversion-based control based on a single iteration. *Gecko Circuit* is selected as it allows to program digital blocks, which is a mandatory feature to implement this control. Since this simulation is only intended for the control, many aspects of the real implementation are neglected: the input voltage is considered constant, the switching devices are simulated without C_{oss} , and the delay between the detection signal and the gate signal is neglected. In Chapter 7, a simulation including these aspects is presented. Details on the implementation of the controller with variable switching and sampling frequency are given in [73].

The circuit used for the simulation is shown in Figure 5.11 a). For 1 kVA resistive load, the simulation results are shown in Figure 5.11 b). On the plot on top, the voltages of the three ports are represented, showing that the output voltage is a perfect sinewave, and showing how the storage capacitor swings around 340 V. In the bottom plot, the instantaneous current of the three ports is represented, similarly to what was shown in Figure 4.26. However, these plots are not identical for a few reasons: the gain of the loops is not infinite, the plant inversion introduces some error because of the single iteration used, and, more importantly, because of the load introduced by the output capacitor, set to 10 pF in this simulation. Further discussion on the effect of C_o are given in Chapter 7.

To prove the validity of the control loops, the evolution of the measured, target, and reference currents and voltages of the ports are shown in Figure 5.12 a). The different variables are labeled as in the general diagram in Figure 5.1. The input current is nearly constant and the output voltage follows the reference perfectly, which are the two objectives of this controller, proving that the control developed by Regina Ramos and described in [40] and [73] work as intended.

5.3. Validation through simulation

Figure 5.11: Simulation to validate the control using $10 \mu\text{F}$ for C_o , $L = 80 \mu\text{H}$ and $I_{th} = 3.5 \text{ A}$, a) power stage, b) port voltages and currents for 1 kVA resistive load.

Figure 5.12: Results of the simulation, a) variables of the control loops, b) evolution of the applied times, each unit is equivalent to 10 ns .

Also, to validate the inversion-based control implemented with a single iteration, Figure 5.12 b) shows the evolution of the applied times along the line cycle. As explained in the previous section and shown in Figure 5.5, T_{a-f} changes continuously from a switching cycle to the next one. If the switching period in this figure is compared with the one in Figure 5.8, the shape is slightly different. As before, the main reason is that C_o increases the load and makes it more capacitive. Yet, as the measured and target input and output current are very similar in Figure 5.12 a), it is proven that a single iteration is accurate enough.

With this simulation, the steady state operation of the inverter has been validated, showing that the sophisticated control required to modulate the inductor current works.

5.4 Limitations of this control scheme

Although the control has been validated through simulations, the real operation of the inverter may be different when the real prototype is considered. In this section, different issues and nonidealities are discussed, describing to what extent they interfere with the operation of the inverter.

Mismatches in the inversion-based control

The control of the inverter has been designed assuming that the transfer function of the power stage times the transfer function of the plant inversion is equal to one. Said differently, $I_g^{Target} = I_g^{Real}$ and $I_o^{Target} = I_o^{Real}$ are assumed. This is not always the case, as there are some discrepancies between the model for the inductor current waveform and the actual waveform.

Some of these effects have been described already, like the fact that ZVS transitions are not accounted for in the inversion. This effect is minimized if I_{th} is set large enough compared with $i_{L\ min}(0)$ as discussed in Section 4.4.3.

Other source of error is the mismatch between the values for I_{th} and L stored in the FPGA and the actual values of the prototype. Therefore, the values defined in the FPGA should be as close as possible to the ones measured in the prototype.

Finally, the plant-inversion is based on the measured voltages; the differences between the measured values and real ones can generate mismatches between the real and modeled inductor current waveform too. It should be noted that this error has a different impact depending on the operation mode. These errors can cause small steps on T_{a-h} when the mode changes.

Another source of error is the assumption that the voltage applied to the inductor during a switching state is constant. This assumption is not valid if the inverter operates at very low frequency, as described in Section 4.3.2. Moreover, the output voltage ripple can generate a difference between the measured voltage and the actual average voltage because voltages are measured close to the beginning of the switching cycle (see Appendix D). Therefore, the ripple in the ports negatively impacts the control accuracy. The effect can be reduced if C_o and C_g are designed to ensure low ripple.

Fortunately, if all these mismatches are small, the current loops can correct them, as mentioned in [40]. Overall, the inversion-based control is a powerful method to simplify the control design in this inverter, but care has to be taken to ensure that the modeled inductor current waveform matches the real one.

Delay from the measurement to the calculations

In Section 5.1.2, the effects of the delay introduced by the controller were neglected for the design of the loops. Unfortunately, the applied times calculated in a switching cycle are used in the following switching cycle. As a result, there is a cycle delay (or two switching cycles for $f_{sw} > 200$ kHz) in the inversion-based control, as mentioned in the implementation of the FPGA code in Appendix D.

This nonideality of the plant-inversion is also corrected by the current loops, and details explaining how this delay affects the design of the loops are given in the Ph.D. dissertation of Regina Ramos.

5.4. Limitations of this control scheme

Delays in the detection signals

One of the main sources of error in the operation and control of the inverter is caused by the delay from the inductor current detection to the driver's gate voltage. This delay is caused by the current detector circuitry, the time it takes to read the digital signals in the FPGA, the time the modulator takes to generate the gate signals, and finally, the delay in the gate driver. This delay has been measured to be around 100 ns in the prototype described in Chapter 7. Delays are a common problem of topologies employing detection of the inductor current, such as digital peak current mode controllers or TCM controllers. A similar problem is reported in [88]. Delays are especially problematic when the detection level is used for ZVS or when high-frequency operation is used. Delays are also a problem in the inverter operated in TCM described [68], where the measured delay is between 20 ns and 50 ns, but the switching frequency is high.

The effects of this 100 ns delay are important in this inverter, to clarify the impact of the delay in the current detection, Figure 5.13 a) shows the waveform for $Tra4^+$ for the same T_a , T_b , and T_c when the delay is present and when it is neglected. This plot represents the difference between the real waveform and the modeled one (because the delay is not considered in the plant-inversion). The current detection is displaced from the theoretical value, and, what is worst, not in the same magnitude for the positive and negative thresholds. For instance, when $V_o = 340$ V, $V_g = 400$ V, $L = 80$ μ H and $I_{th} = 3.5$ A, if a delay of 100 ns is considered, the state [111] for ZVS end at $i_L = 3.575$ A instead of 3.5 A, which is not much of a problem. However, the state [000] ends at -4.425 A instead of -3.5 A; the error has a substantial impact in the inductor current. The lower I_{th} , the larger the discrepancies between the real and effective threshold current since the variations due to the delay are proportional to the slope of the current and the delay time.

Figure 5.13: Effect of the delays in detection of the inductor current waveform in $Tra4^+$, a) effect of the delay for the detectors set and I_{th} and $-I_{th}$, b) a possible solution for $I_{th\ eff} = 0$ to use a zero-current detector.

An important property of the proposed state machine for the driving signals (Figure 5.10) is that the state [000] starts as soon as T_c is over, even if i_L has not reached I_{th} yet. This feature makes the modulation more immune to losing ZVS in the transitions marked as *i* and *iii* in Figure 4.19 because the transitions never take place at a current below the threshold. For this reason all the applied times are used in the modulator, which is different from the solution in [40] where only two control times were calculated for each mode.

If this delay is nearly constant, a possible solution to this problem would be to account for this delay in the signal generation [93], [88]. The idea is to use a threshold level below I_{th} , and then wait a certain time, that, together with the delay, causes the transition to happen precisely at $i_L = I_{th}$. This additional time, namely T_{ext} , should be calculated based on V_g and V_o and L , the target I_{th} and the detection delay T_{delay} (100 ns in this case), through the following equations:

$$I_{th} = I_{th\ eff} + \frac{V_g - V_o}{L} (T_{ext}^+ + T_{delay}) ; \quad -I_{th} = -I_{th\ eff} + \frac{-V_g - V_o}{L} (T_{ext}^- + T_{delay}) \quad (5.6)$$

Where $I_{th\ eff}$ is the actual value where the threshold for D^+ and D^- is set. With a solution like this, $I_{th\ eff}$ could be set to zero, so a single signal (D^0) would be required for the modulator, instead of D^+ and D^- . A single detection can slightly simplify the circuitry of the inverter. The inverter would rely only on the correct timing to obtain the appropriate current values for ZVS. This concept is shown in Figure 5.13 b) to clarify this idea.

To implement this concept, the modulator should be modified and a few more calculations would be required. This solution has been validated in the simulation, however, since the current detector circuitry explained in Section 7.2.2 should be modified, this concept is not experimentally validated. Fortunately, although the effect of the delay is far from negligible, the current loops overcome this issue by adjusting the target I_g and I_o along the line cycle. However, this delay also increases the rms and peak current in the inductor because the effective value of I_{th} and $-I_{th}$ is increased.

Other sources of error

There may be other effects associated with the interaction of the control with the modulation and real parameters of the inverter not discussed here. Only those observed in prototype and simulation have been described. Fortunately, none of these issues make the control to malfunction. Electrical simulations accounting for these effects are presented in Chapter 7.

The fact that the modulation is seamless also makes the control more robust. Since the modulation is seamless, the difference between the target and real currents due to these errors barely changes from a cycle to the next. Because of the slow dynamics of the error, the loops can correct it.

5.5 Conclusion

This chapter has described how the control for this inverter is designed and implemented. The different parts of the controller have been explained, detailing the plant-inversion implemented with a single-step iteration. As it achieves good accuracy without excessive complexity, it can be implemented in real-time. These concepts have been validated in simulation. Finally, some problems arising from this intricate control design have been discussed.

Leakage current filter

PV arrays exhibit a relatively large parasitic capacitance from the positive and negative terminals to ground. In nonisolated inverters, a Common Mode (CM) voltage appears between the input port and output port, which generates undesirable leakage current through the parasitic capacitance when the output is grounded. A CM filter is required to reduce the leakage current. This chapter details the generation of leakage current in this topology and describes the design considerations for the filter to meet the specifications of the LBC.

The parasitic capacitance affects inverters differently depending on the topology and modulation used. Notably, filtering the leakage current is more difficult in the analyzed inverter than in other topologies. This chapter also discusses how the design decisions impact the design of the filter. The last part of the chapter is dedicated to the design of the filter and the validation through simulation.

It should be noted that this is not the CM EMI filter of the topology. The CM part of the EMI filter is intended to reduce the CM noise in the output port of the inverter. Limits are defined at different frequencies, and for values above 150 kHz. The leakage current filter, on the other hand, is intended to reduce the CM current through the parasitic capacitance. The harmonic content is not specified, and low frequency is also limited. The limit states that the current through the parasitic capacitance in the input has to be below 50 mA rms. For this reason, the design of the leakage current filter differs from the design of the CM EMI filter.

6.1 Leakage current in inverters for PV applications

In this section, how the leakage current is generated in different topologies is discussed.

The parasitic capacitance between PV arrays and ground depends on the physical structure of the array and weather conditions, [94], [95], [96], it is highly variable [97], and it even changes with frequency [98]. The parasitic capacitance of the panel is sometimes referred to as stray capacitance [99]. This capacitance is modeled as a capacitor from the positive terminal to ground, termed C_{cm+} in this chapter, and a capacitor from the negative terminal to ground, C_{cm-} . The analysis can be simplified considering a single capacitance, $C_{cm} = C_{cm+} + C_{cm-}$, since both C_{cm+} and C_{cm-} are effectively in parallel.

As discussed in the specifications of the LBC in Section 1.3, a capacitance around 120 nF should be considered between the input and ground to model the parasitic capacitances found in PV panels. The capacitance is considered equally split between the positive and negative terminals. For testing purposes, a power supply in series with a resistor to supply the inverter is specified

instead of that of a PV array. The power supply also introduces a capacitance to ground, so the behavior is similar to a PV panel.

For leakage current to flow through C_{cm} , the inverter must be grounded. Otherwise, there would be no return path for this current as C_{cm} would be floating. According to the specifications from Section 1.3, the chassis of the inverter and one of the terminals of the output must be grounded. Ground can be connected either to the midpoint of the load or to one of its terminals. The possible grounding configurations of the system were shown in Figure 1.5.

Since the output is grounded, C_{cm} is effectively connected between the input and the output of the inverter, as shown in Figure 6.1. As a result, the CM voltage between the input and the output ports, v_{cm} , is directly applied to the capacitance. This CM voltage is determined by the topology, modulation, and voltage levels [25], [94], but it is not a problem when isolated topologies are used, due to the galvanic isolation.

Figure 6.1: Parasitic capacitance of the PV panel when the output of the inverter is grounded; leakage current, i_{lk} , is generated due to the CM voltage.

In nonisolated inverters where the output is grounded, due to the CM voltage applied to the parasitic capacitance, certain current flows through the inverter and the parasitic capacitance as shown in Figure 6.1. This current is sometimes called leakage current, ground current or common-mode current in the literature [25], [97]. In this work, this leakage current, i_{lk} , is defined as the current through C_{cm} . Therefore, the amplitude and frequency spectrum of v_{cm} determine i_{lk} .

This leakage current impairs the system for several reasons: it increases the conducted and the radiated EMI, it increases the distortion in the grid current and system losses, it increases the noise level in the installation and disrupts the operation of the ground-fault protection, leading to unsafe working conditions [28], [94], [95], [97], [98]. For these reasons, a maximum level for i_{lk} is established by regulations and standards. In the LBC specifications, the maximum i_{lk} is set to 50 mA: neither the DC value nor the rms AC value can be above this limit. Moreover, this current, if significant, can disrupt the operation of the inverter.

6.1.1 Leakage current issues in conventional inverters

Before discussing how to suppress the leakage current in this inverter specifically, how other participants of the LBC tackled this problem is briefly reviewed, following the review from

6.1. Leakage current in inverters for PV applications

Section 1.6. After this review, the critical differences between this topology and more common solutions are clarified.

When the LBC specifications were first published, i_{lk} was specified to be below 5 mA rms. i_{lk} becomes a major issue under such strict restriction, and topologies or modulations with a very low v_{cm} were a must. Therefore, most of the LBC participants considered this specification as a premise for the selection of the topology and modulation. Conversely, the topology analyzed in this study has a higher v_{cm} generation which must be addressed.

Depending on the topology and modulation, different shapes of v_{cm} are obtained, leading to different amplitude and frequency components. v_{cm} can be either a DC voltage, contain line-frequency components (low-frequency), switching frequency components (high-frequency), or a superposition of the previous three. Figure 6.2 shows different v_{cm} waveforms for common nonisolated inverters.

Figure 6.2: Common-mode voltage for different topologies and modulations, a) input grounded, b) DC value, c) line-frequency harmonics, d) voltage step, e) high switching-frequency harmonics, f) all combined.

There are some topologies where C_{cm} is effectively shorted. Those are architectures with a terminal of the output is connected to a terminal of the input [25]. This is a feature of the inverters proposed in [53], [54] or [96]. In this case, no CM voltage is present, as shown in Figure 6.2 a).

There are also architectures where the CM voltage is constant, as shown in Figure 6.2 b). This is the case of a Full-Bridge inverter (Figure 1.3 a)) with bipolar modulation and ground connected to the midpoint of the load ideally. It is also the case of the *two buck converters* (Figure 1.3 b)) when modulated to keep v_{cm} fixed. This architecture was used by the *Fraunhofer IISB* team [64] and the *!verter* team to comply with the initial 5 mA rms specification [68]. Other interesting families of inverters featuring constant CM voltage are the HERIC, H5, H6, and related topologies [25]. These inverters feature lower voltage applied to the inductor as in Full-Bridges with unipolar modulation, but without v_{cm} generation [99], [100]. Finally, other architectures that feature constant v_{cm} , this time regardless of the modulation, are the Half-Bridge or Neutral-Point Clamped inverters [96], [99], although these structures could not be used for the LBC since $V_g > 2 \cdot V_{o \max}$. In this and the previous case, as v_{cm} is constant, there is no leakage current theoretically.

There are also architectures where v_{cm} changes at low frequency along the line cycle or, in other words, at f_{line} and its harmonics. This is the case of inverters with 4-switch unfold as in Figure 1.3 d), which has a v_{cm} shown in Figure 6.2 c). The *UIUC Pillawa Group* used this configuration, with ground connected to the midpoint of the load [67]. In this case, there is a low-frequency leakage current, but, as the impedance of C_{cm} is high at low frequencies, and i_{lk} is usually below the specified limits.

There are converters where there are steps in v_{cm} twice per cycle, as shown in Figure 6.2 d). A converter with this CM voltage is the buck converter with 2-switch unfolded (Figure 1.3 c)) [1], [24]. Comparisons on CM voltage for Full-Bridge structures and the Buck plus 2-switches unfolded can be found in [24], [28], and [30]. As before, the frequency content of the waveform are the harmonics of f_{line} , but in this case, i_{lk} becomes a large spike if not filtered.

In the previous cases, the only high-frequency components in v_{cm} are the harmonics of f_{line} , with decreasing amplitude as the frequency increases. However, there are also topologies with switching frequency components in v_{cm} , as shown in Figure 6.2 e). The Full-Bridge with unipolar modulation with ground connected to the midpoint of the load has this v_{cm} . It is also the case of topologies used by the winners, *CE+T* [61], and *Schneider Electric Team* [18]. Both modulations are designed to have a constant average CM voltage along the line cycle, but with switching frequency components in v_{cm} . In [98], the leakage current of unipolar and bipolar modulations of the Full-Bridge are compared, separating the high and low-frequency components too.

Due to the low impedance of C_{cm} at switching frequency, i_{lk} would have an inadmissible amplitude if v_{cm} changes at switching frequency. Therefore, in these cases, a filter is mandatory to ensure that the harmonic content at switching frequency is not applied to the parasitic capacitor but to the filter. For this purpose, CM chokes are used. The choke, together with C_{cm} or any additional CM capacitor (C_y), forms a low pass filter for the voltage between the input and output ports [101]. Typically, the resonant frequency of the filter is set below one-tenth of the switching frequency to limit i_{lk} and avoid the need to damp the resonance of the filter [28]. For this reason, both *CE+T* and *Schneider Electric Team* had to include large filters because of the switching frequency components of the CM voltage [18].

Finally, there are inverters with both switching frequency and line frequency and their harmonics in v_{cm} , as shown in Figure 6.2 f). The inverter studied in this work is submitted to such v_{cm} . Unlike the previous case where the average v_{cm} is constant along the line cycle, the presence of low-frequency components implies, in this case, that the filter has to be designed carefully to avoid resonances. Additionally, the resonant frequency of the filter has to be set below the switching frequency.

In the literature, the leakage current is addressed either by filtering, by designing topologies that do not generate i_{lk} inherently, or by applying modulations without switching frequency components in v_{cm} if possible [98]. There are shapes for v_{cm} not included in Figure 6.2, but this short review provides an idea of the problem when it comes to the design of the filter to comply with the 50 mA rms specification for this inverter which is described next.

6.2 Leakage current in this inverter

The inverter and modulation were designed aiming to minimize the indirect power in the inductor, not to reduce the CM voltage. As a result, the leakage current should be mitigated through the proper design of a filter.

The inverter is shown in Figure 6.3 including the parasitic capacitances between input and ground, the possible connections for ground in the output port, and omitting the line transformer

6.2. Leakage current in this inverter

that was shown in Figure 1.5. In this circuit, the model for the input port and the input capacitor, C_g , is included, as it is important to determine the leakage current path.

Figure 6.3: Inverter including the PV parasitic capacitance, with the impedance of the ground connection, and the possible options for grounding the output port.

In this plot, Z_{gnd} represents the impedance of the ground path between the PV array and the output port or, for the tests, the ground impedance of the input power supply. This impedance depends on the setup or installation of the inverter and might help to limit the leakage current. However, as Z_{gnd} is not specified for the contest. This impedance, if resistive, can be helpful to mitigate resonances in the filter, so it is typically beneficial. Neglecting this impedance implies a larger portion of the CM voltage applied to C_{cm} , which is the worst-case scenario. $Z_{gnd} = 0$ is considered for the rest of the analysis. Therefore, the parasitic capacitor directly connects the input and output ports.

In Figure 6.4, a simplified version of the circuit from Figure 6.3 is shown, where Z_{gnd} has been removed. Also, $C_{cm} = C_{cm+} + C_{cm-} \approx 120$ nF has been placed in the negative terminal of the input source (the leakage current is independent of the terminal used). In this figure, ground is connected to the midpoint of the load, although it could have been placed on either side of the load as well. This is the preferred position for ground to minimize i_{lk} , which is discussed in Section 6.2.2. The voltage of the PV capacitance, v_{cm} , is defined from ground (the midpoint of the load) to the negative input terminal. As a result, this voltage is positive. Other noteworthy voltages that are required for the analysis are v_q and v_{dh} , which are the voltage across q^+ and across d^- plus h^- respectively. With this definition $v_{dh} - v_q = v_L + V_o$, independently of the parasitic capacitance.

Figure 6.4 also shows the path the leakage current takes. At switching frequency and above, the impedance of C_g , C_s , and C_o can be neglected compared to the impedance of L , Z_{load} , or R_{in} . Therefore, the leakage current flows mostly through the q switches. From q^+ , i_{lk} directly returns to C_{cm} , whereas it goes through C_g and then returns to C_{cm} for q^- . It flows through one or the other, depending on which one is closed. The effect that the inductor position has in the leakage current and the filter design are discussed in Section 6.2.3.

Figure 6.4: Equivalent circuit showing the leakage current, including the names of the variables used in the analysis.

If left unfiltered, the voltage in q^+ would be directly applied to C_{cm} , and, since the q branch switches at switching frequency, the leakage current that would appear would be unreasonably high. Considering a constant dv/dt in the q branch along the 200 ns dead time, the current required to charge 120 nF at 450 V would be 270 A, this value shows how unreasonable the peak could be. ZVS would be lost, conduction and switching losses would increase drastically, and the operation of the inverter would be disrupted. Accordingly, this inverter cannot operate without a filter, not only to comply with specifications but to ensure its proper operation.

6.2.1 Filter for the leakage current

When a CM choke is added in the path of the leakage current, the CM voltage between input and output is no longer directly applied to the parasitic capacitance, but to the inductance of the choke in series with the parasitic capacitance. This added impedance reduces the magnitude of the leakage current, leaving the operation of the inverter unaltered. If the magnetizing inductance of the choke, L_{cm} , is high enough, the leakage current at switching frequency can be reduced, and the specifications met. At the same time, as i_{lk} is in the range of tens to hundreds of milliamps, it does not affect the modulation and control described in Chapters 4 and 5, nor in the currents of the input and output ports.

The CM equivalent circuit for the inverter, once the choke is added, is shown in Figure 6.5, neglecting the leakage inductance of the CM choke. The equivalent model has been obtained following the procedure described in [101] but neglecting the parasitic capacitances to ground of semiconductors. L_{cm} and C_{cm} form a low pass filter for $v_q + V_o/2$. Therefore, the equivalent circuit for the leakage current can be easily obtained given v_q . The choke can be placed in the input or output of the inverter as described later in Section 6.2.4 and shown in Figure 6.12.

The voltage in the q branch is a function of the operation mode and the control times that were calculated in Chapter 4. This voltage along the line cycle, together with $V_o/2$, is shown in Figure 6.6 for 1 kVA resistive load, $I_{th} = 3.5$ A and $L = 80$ μ H. The switching period has been enlarged twenty times in the figure for better readability. The voltage applied to the filter formed by L_{cm} and C_{cm} is $v_q + V_o/2$ when ground is placed in the midpoint of the load. The average voltage in the q branch along a switching cycle is termed V_q , following the nomenclature used in

6.2. Leakage current in this inverter

Figure 6.5: Equivalent CM circuit for the leakage current, here $i_{lk} = i_{cm}$.

this work. In this analysis, the *low-frequency* components of the CM voltage are given by $V_q + V_o/2$, whereas the *high-frequency* components are defined as $v_q - V_q$. To clarify the concept, these values are also shown in Figure 6.6.

Figure 6.6: CM voltage evolution along the line cycle for 1 kVA resistive load, $L = 80 \mu\text{H}$ and $I_{th} = 3.5 \text{ A}$ enlarging the switching period twenty times.

The choke is designed to block the high-frequency components, $v_q - V_q$, while allowing the low frequency, $V_q + V_o/2$, to pass through. Accordingly, the goal is to make v_{cm} equal to $V_{cm} = V_q + V_o/2$. Therefore, the resonant frequency of the filter should be above f_{line} but below f_{sw} to limit i_{lk} and avoid extremely high values of inductance.

There are two important properties of this CM voltage, V_{cm} , shown in black in Figure 6.6. First, it continuously evolves along the line cycle because the modulation applied is seamless, as discussed in Section 4.1.4. Second, V_{cm} has not only components at DC and f_{line} but also contains the odd harmonics of f_{line} . Note the limits between $T1^-$ and $T0$, and $T0$ and $T1^+$; the sharp corners imply that the spectrum of V_{cm} reaches high-frequencies too. Nevertheless, the low-frequency components in C_{cm} are not a problem: for 120 nF, the rms current is $I_{lk} \approx 6.4 \text{ mA rms}$, far below the limit specified for the LBC. The conclusion from this plot is that the harmonic content of the CM voltage is very rich; it contains the line frequency and its odd harmonics and the switching frequency and its harmonics too.

Before the design of the choke is covered, it is worth discussing three design considerations that affect the filter: the selection of the ground placement in the output port, the position of the main inductor and the output between the q and dh branches, and the place for the choke, as it can be placed in the input side or the output side.

6.2.2 Selection of the ground connection

Different waveforms for V_{cm} are obtained depending on how the inverter is grounded. Ground can be connected either to the terminals or the midpoint of the output, as shown in Figure 6.3. This analysis only considers the low-frequency component of the CM voltage as the high-frequency ones do not depend on this connection.

If ground is connected between the inductor and the load, the voltage in the PV parasitic capacitance would be $V_q + V_o$, which is simply $V_{cm} = V_{dh}$. If ground is connected to the other terminal of the output, the voltage would directly be $V_{cm} = V_q$. Finally, if ground is in the middle point, as in Figure 6.4, the voltage is $V_q + V_o/2$, which is equal to $V_{cm} = (V_{dh} + V_q)/2$. It should be noted that these voltages do not depend on the position of the inductor or the common-mode choke, as their average voltage in a switching cycle is zero.

Since V_{cm} depends on the ground connection, so does the low-frequency leakage current, I_{lk} . Figure 6.7 shows V_{cm} and I_{lk} for the three options along the line cycle. The leakage current associated with V_q , V_{dh} , and $(V_q + V_{dh})/2$ is 9.3 mA rms, 7.4 mA rms, and 6.4 mA rms, respectively. Therefore, I_{lk} is not a problem regardless of the grounding configuration since it is well below the specified 50 mA rms when 120 nF are considered. For resistive load, the largest peak and rms leakage current is obtained if ground is connected to the q leg side, so this solution is avoided. Connecting ground to the midpoint reduces the rms current while connecting it between the inductor and the output (dq side) leads to a lower peak. In Figure 6.8 the spectrum of V_{cm} is shown at full-load and no-load conditions. The only difference in the CM voltage of the three possible configurations is the output voltage component (60 Hz). As load decreases, the connection to the midpoints is preferable, because under no-load $(V_q + V_{dh})/2 = V_g/2$, which is constant and leads to $I_{lk} = 0$, making this configuration preferable.

Although the best position for ground is the midpoint of the output port, the current would not be considerably increased if ground is connected between the inductor and the load. For the prototype, to avoid the use of a line-frequency transformer to have the terminal for the midpoint of the load available, ground is connected between the inductor and the output port. However, for the rest of the analysis, the midpoint is considered for its reduced I_{lk} .

The conclusions drawn from this section are that the position of ground only affects the low-frequency components of the CM voltage and that I_{lk} is below the specified limit regardless of the selection of ground. As a result, only the high-frequency components of the CM voltage must be filtered.

6.2. Leakage current in this inverter

Figure 6.7: V_{cm} and I_{lk} for the three ground configurations at full power for $C_{cm} = 120$ nF.

6.2.3 Selection of the inductor position

The place of the main inductor, L , determines the leakage current path. Three possible scenarios are considered here: the inductor connected to the dh branch, as considered so far, the inductor connected between the q branch and the load and the dh side, and a coupled inductor with both primary and secondary having the same inductance value with the load in the middle. Figure 6.9 shows the three possible scenarios. For this comparison, it is assumed that the choke is designed so that the voltage applied to the parasitic capacitance is $v_{cm} = (V_{dh} + V_q)/2$, and L_{cm} blocked the high frequency.

As the voltage applied to the inductor in the different switching states does not change with its position, the analysis for the modulation and control in Chapters 4 and 5 remain valid for the cases in Figure 6.9 b) and c) too, as long as the leakage current is low enough compared to i_L . The inductor position affects the high-frequency voltage applied to the choke. In a), this voltage is $v_q - V_q$, as it was shown in Figure 6.6. In b), the voltage applied to the magnetizing inductance of the choke is $v_{dh} - V_{dh}$. Finally, the case where the inductor is split, the voltage is $(v_q - V_q + v_{dh} - V_{dh})/2$. These voltages are shown in Figure 6.10.

As a metric to compare these solutions, the volts-second in the choke can be obtained, as it determines the saturation value of L_{cm} and the CM current through the choke. The volt-seconds are defined as the integral of the voltage applied to the choke. Although, as the voltage in a

Figure 6.8: Spectrum of V_{cm} and I_{lk} , a) V_{cm} at full load, resistive, b) V_{cm} without load, c) I_{lk} for the voltage on top, d) I_{lk} for the voltage on top.

switching cycle is zero due to volt-second balance precisely (as it is assumed that V_{cm} is not blocked), the volt-seconds of the absolute value of the voltage are used instead [102]:

$$VS_{L_{cm}} = \int_0^T |v_{L_{cm}}(t)| dt \quad (6.1)$$

The evolution of the volts-second along the line cycle is shown in the bottom part of Figure 6.10, which gives an idea of the evolution of the high-frequency CM current flowing through the inductor along the line cycle, i_{cm} . This plot reveals that placing the inductor between the dh branch and the load and splitting the inductor in two (Figure 6.9 a) and c) respectively) are preferred to the solution where the inductor is connected to the q branch (Figure 6.9 b)). The lowest i_{cm} peak will be obtained if the inductor is split.

Nevertheless, although splitting the inductor is slightly better than placing it on the dh side, the latter option is selected. The reason is that i_{cm} affects the current for ZVS, and the dh position always helps ZVS rather than disturb it. As shown in Figure 6.10 a), the position of the inductor and the value of L_{cm} determines the waveform of the CM current at high frequency. The current has to be considerably high to disrupt the operation of the inverter in terms of affecting the control or modulation, so this is not technically a problem. Nevertheless, even low values of CM current can modify the current available for ZVS, and ZVS could be lost if this effect is disregarded. This is only the case if i_{cm} is high.

For this discussion, it is assumed that the high-frequency components in i_{cm} are considerably higher than the low-frequency ones, so the latter can be neglected. This assumption is reasonable if L_{cm} is not very high, which is precisely when the CM current can be problematic for ZVS.

6.2. Leakage current in this inverter

Figure 6.9: Different inductor placement of the main inductor: a) to the dh side, b) to the q side, c) coupled and split.

When the inductor is placed in the dh branch (Figure 6.9 a)) the voltage applied to L_{cm} is rectangular, so the shape of i_{cm} is triangular and centered in zero. The magnetic flux of the choke is represented in Figure 6.11 a) along the switching cycle to give an idea of the magnitude of that current. This plot shows the relationship between inductance and leakage current: for $L_{cm} = 100 \mu\text{H}$ the peak current would be around 4.5 A, for 1 mH around 0.45 A. The peak CM current is directly related to the volt-second plot of Figure 6.10, as expected.

While q^+ is closed, i_{cm} goes from positive to negative. Due to the triangular shape of i_{cm} , when q^+ is opened, this current is negative and, since the current in the q branch is equal to $i_L - i_{cm}$, it helps to charge the capacitance of q^+ and discharging q^- . Therefore, this current increases the available current for ZVS, thus helping in the process. In the other transition, when q^- is opened, the value of the current is positive, which is also beneficial for ZVS. This concept is represented in Figure 6.11 b) for the inductor in the dh side and the mode $Tra4^+$, near $\omega \cdot t = \pi/2$.

For this reason, it is advised to place the main inductor on the dh side if the value of L_{cm} is not large enough to make i_{cm} negligible as compared to i_L , as represented so far in this work. It should be noted that if large values of L_{cm} are used, this effect is negligible. It would be reasonable to think that this is never the case, as the maximum leakage current is 50 mA rms because of the specification. However, when C_y is used, the current in the choke can be above i_{lk} . The use of C_y is discussed in Section 6.3.

Moreover, an advantage of having a single inductor is that it is easier to measure the current. If the inductor is split, different measurements of the inductor current will be obtained depending on which inductor is measured.

A solution that has not been described here, commonly employed in Full-Bridge inverter, is to split the inductor without coupling them. This configuration is beneficial as the inductance adds impedance to the leakage current path, thus helping to reduce its value. However, this solution

Figure 6.10: CM voltage applied to the choke for 1 kVA resistive load enlarging the switching period twenty times; in the bottom, the volt-seconds of each of the voltage waveforms are included.

Figure 6.11: a) a representation of i_{cm} for different values of the magnetizing inductance of the choke, $i_{cm} \cdot L$. Enlarging the switching period twenty times, b) effect of i_{cm} in the ZVS of the q branch when the inductor is placed in the dh branch.

is not considered for this inverter because if the inductor is split but not coupled, the voltage applied to the inductor will change. Hence, it will no longer be true that $v_L + V_o = v_{dh} - v_q$ unless $L_{cm} \gg L$, implying that the shape of the operation modes will be different, and the proposed inversion-based control will not be applicable.

6.2. Leakage current in this inverter

6.2.4 Selection of the choke place

The last design consideration is the placement of the choke in the topology. It can be placed either between the input port and the inverter or between the output port and the inverter. The circuit with the output or input choke is shown in Figure 6.12 a) and b), respectively.

Figure 6.12: Rearranged topology, including the CM choke: a) in the output port, b) in the input port.

Both solutions have the same effect regarding the leakage current, as L_{cm} is always in the path of the leakage current, and, in both cases, the voltage applied is the same. However, these solutions lead to different sizes for the choke. Since the rms input current is lower than the output rms current, it is better to use an input choke. Therefore, the choke to limit i_{lk} is placed on the input side. An additional choke may be required in the output to comply EMI standards.

6.3 Leakage current filter design

This section describes the design of the leakage current filter considering that ground is connected to the midpoint, the inductor is connected between the dh branch and the load, and the filter is placed in the input side of the inverter.

As shown in Figure 6.11 a), high values of inductance are needed to obtain a reasonable attenuation of the leakage current. If a single choke is used, as shown in Figure 6.12 b), around 2.5 mH would be required to keep the high-frequency i_{lk} at 50 mA rms.

With such design, only values of $L_{cm} > 2.5$ mH would be valid. However, this may not be the optimum value for the choke, as further discussed in Section 6.3.2. A capacitor in parallel with C_{cm} can be added to allow for lower values of L_{cm} or further decrease the leakage current. This CM capacitor is termed C_y , and the equivalent CM circuit including it is shown in Figure 6.13 a). With this added capacitance, only a fraction of the choke current flows through the parasitic capacitance: $i_{lk} = i_{cm} \cdot C_{cm} / (C_{cm} + C_y)$, effectively reducing i_{lk} for a given value of L_{cm} . Therefore, C_y adds a degree of freedom in the choke design because L_{cm} is not directly bonded to the i_{lk} constrain. As a counterpart, C_y leads to higher reactive power in the inverter, as this capacitance is charged and discharged along the line cycle as V_{cm} changes [68]. If the value of the current in C_y is significant, the low-frequency CM current through the choke, I_{cm} , might negatively affect the ZVS transitions. Basically, for $C_y \gg C_{cm}$, increasing C_y can be used to decrease L_{cm} , at the expense of higher I_{cm} . An optimization would be required to find the optimum values for C_y and L_{cm} .

Figure 6.13: Equivalent CM circuit of the filter, a) including C_y , b) with an additional $R_b C_b$ network to damp the resonances.

Another important advantage of using $C_y \gg C_{cm}$ is that C_y can be used to tune the resonant frequency of the filter. Due to the high variability of C_{cm} in PV panels under different weather conditions, the resonant frequency of the filter may vary too much if C_y is not used [26].

6.3.1 Damping undesired resonances

A disadvantage of this inverter compared to common structures is that it contains the odd harmonics of f_{line} , as shown in Figure 6.8. Therefore, in this inverter, some harmonic components fall near the resonant circuit formed by L_{cm} , C_{cm} , and C_y . Additionally, at those frequencies, the impedance of the CM filter is very low, resulting in high current even at low voltage. At those frequencies, the volt-seconds in the inductor can be high, saturating the choke [102]. The resonant frequency of the CM filter is given by:

6.3. Leakage current filter design

$$\omega_r = \frac{1}{2\pi\sqrt{L_{cm} \cdot (C_y + C_{cm})}} \quad (6.2)$$

If the filter is designed correctly, its resonant frequency would be much lower than f_{sw} , so the resonances can be analyzed considering only the low-frequency spectrum of the CM voltage, V_{cm} (Figure 6.8). All parasitic resistances damp this resonance along the path. Unfortunately, in designs aiming for very high efficiency, those are minimized. Therefore, a damping network should be added to the filter.

There are a few well-known networks that can be used to damp resonances, usually applied to differential mode (DM) filters, but the concept is the same for CM filters. These solutions are based on RL or RC damping networks [103]. The solution based on an additional RL branch in parallel with L_{cm} has an important drawback; the high-frequency attenuation is degraded [103], which is not admissible in this design. The solution based on a damping R in parallel with L , both in series with L_{cm} , is not convenient as the additional inductance has to have a value larger than L_{cm} , which is not desired either.

Therefore, only the RC damping network is considered in this work. This solution adds a resistor in series with a capacitor in parallel with C_y . The drawback of this solution is that the additional capacitor is in the same range of values as C_y . This solution incurs in increased reactive power, although the volume is not a problem. This is the solution used, although it is not ideal. The CM circuit, including this damping network, is included in Figure 6.13 b). This solution is commonly employed in the literature for CM EMI filter designs.

With this additional R_b and C_b network, the impedance at high frequency is dominated by L_{cm} , and the high-frequency current flows through C_{cm} and C_y . At low frequency, the impedance is given by $C_y + C_{cm} + C_b$. This total capacitance means higher reactive power of the filter. Therefore, its value should be minimized, without compromising the performance of the main capacitance of the filter, $C_{cm} + C_y$. At the resonant frequency, the impedance of this extra network must have a resistive behavior to damp the resonances, which implies that C_b has to be in the order of magnitude of $C_y + C_{cm}$. Once C_b is selected, according to [103], the value of R_b that maximizes the impedance is given by:

$$R_b = \sqrt{\frac{L_{cm}}{2} \cdot \frac{(2 \cdot C_{cm} + 2 \cdot C_y + C_b) \cdot (4 \cdot C_{cm} + 4 \cdot C_y + 3 \cdot C_b)}{(4 \cdot C_{cm} + 4 \cdot C_y + C_b) \cdot C_b^2}} \quad (6.3)$$

Both C_b and R_b negatively impact the inverter operation, due to the additional reactive power and the additional resistive losses, respectively. Figure 6.14 shows the power stage with the leakage filter included. C_y and the $C_b R_b$ branch are split between both the positive and negative rail of the input.

6.3.1.1 Importance of the continuous modulation

Resonances mostly appear when there is a shift between $T0$ and $T1$ modes because the evolution of V_{cm} sharply changes, as shown in Figure 6.7. In these shifts, the voltage in C_{cm} does not perfectly match V_{cm} due to the low-pass filter effect of L_{cm} . Furthermore, even with a damping network,

Figure 6.14: Selected leakage filter included in the topology.

I_{cm} might show a resonant behavior and deviate from its expected low value. This resonance is further discussed in Section 6.3.3. These resonances, if high enough, can lead to saturation of the choke besides increasing the leakage current. Therefore, it is essential to have a damping network with high impedance at ω_r and modulations with a smooth V_{cm} .

As a result, it is important for V_{cm} not to change abruptly. This is why a seamless modulation is important for the filter design. If instead of the proposed modulation a different one where the duty cycle in the q switches changed suddenly is used, these resonances would be much more significant. Even with proper damping, the CM current could take unreasonable values. A representation of this issue is shown in Figure 6.15, where the seamless modulation is compared with a modulation with a step in V_q . Right after the step, the voltage applied to the CM choke would take some time to return to zero. The choke would have to be oversized to withstand these conditions.

 Figure 6.15: Evolution of the leakage current, a) with seamless evolution of V_q , b) effect of a step on V_q assuming enough damping.

6.3.2 Selected values for the filter

In this section, the values used for the filter of Figure 6.14 are discussed based on the previous analysis. The optimization to minimize volume and losses is not provided as it is out of the scope of the thesis.

6.3. Leakage current filter design

For the value of the magnetizing inductance of the choke, considering a core without gap, the inductance and maximum CM current below saturation are given by:

$$L_{cm} = \frac{n^2 \cdot A_e \cdot \mu_o \cdot \mu_r}{l_e} \quad (6.4)$$

$$i_{cm \text{ sat}} = \frac{A_e \cdot B_{sat} \cdot n}{L} = \frac{B_{sat} \cdot l_e}{n \cdot \mu_o \cdot \mu_r} \quad (6.5)$$

Where n is the number of turns in one of the two windings, A_e is the effective area of the core, l_e the effective length, B_{sat} the magnetic flux density saturation of the material, μ_o the vacuum permeability and μ_r the relative permeability of the material.

As the volt-seconds are fixed by the operation of the inverter, increasing L_{cm} decreases i_{cm} proportionally, from Figure 6.11 a), which lowers the maximum CM current. Therefore, large values of L_{cm} are preferred as they soften the requirements for saturation current [28]. However, this is true only up to a certain value, as I_{lk} is fixed and given by $C_{cm} + C_y + C_b$. Increasing L_{cm} is only advantageous provided that the high-frequency i_{cm} is dominant compared to the low-frequency current. Otherwise, the saturation would be determined mostly by I_{cm} . Regardless of the cause for maximum CM current, $i_{cm \text{ max}}$, the goal is to design a choke with high L_{cm} where $i_{cm \text{ max}} < i_{cm \text{ sat}}$ while having low losses and volume.

First, for a given A_e and l_e , from Equations 6.4 and 6.5, it is clear that materials with large values of μ_r and B_{sat} are preferred. For this reason, nanocrystalline cores are recommended for those applications [28]. In this case, the material *VITROPERM 500 F* has been selected [104]. This material has also been used in the design of the choke of the *Inverter* and *Schneider* teams [68], [18].

The core *T60006 – L2045 – V101* from *Vacuumschmelze* has reasonable values of A_e and l_e for this application, as it allows for designs with a relatively low number of turns [105]. This core with $n = 13$ has a magnetizing inductance around 2.5 mH at 100 kHz, which is the minimum required if C_y is not included. This number of turns lead to a saturation current around 450 mA at 100 kHz. According to Figure 6.11 a), i_{cm} would peak at 180 mA for this inductance, so the saturation of 450 mA is reasonable as it provides a margin for the saturation of the core due to leakage inductance and DM current [106], and a margin for the value of I_{cm} and the resonance.

The resonance for $L_{cm} = 2.5$ mH and $C_{cm} = 120$ nF would fall around 9 kHz, which is reasonable as it falls below the switching frequency. Nevertheless, as mentioned before, to further reduce i_{lk} and ensure that the resonant frequency does not vary much, a $C_y > C_{cm}$ is recommended. For such purposes, $C_y = 300$ nF is selected. With such values, the resonant frequency would fall at around 5 kHz instead. However, at this resonant frequency, the inductance is higher due to the core material selected, and the resonant frequency falls around 4.3 kHz, where the inductance value is near 3.3 mH. For the damping network, a large value of C_b would provide good damping, yet it is preferred to minimize the reactive power and I_{cm} , so the value is set to $C_b = 520$ nF. For this value, the optimum resistance is $R_b = 110 \Omega$, according to Equation 6.3.

These values have been selected after trying several combinations of chokes and capacitors in a *Matlab* script and simulation. The resulting design is good enough as it complies specifications

with some margin. However, if the target is to minimize volume and losses, a multi-objective optimization would be required. It should be noted that the design of this filter is different from the CM EMI filter design, as mentioned at the beginning of the chapter. The target is not to provide a given attenuation for a given frequency, but to keep $i_{lk} < 50$ mA rms. Usually, for EMI filter design, the target is to find the appropriate value of L_{cm} that provides the desired attenuation.

With this design, the resulting i_{cm} and i_{lk} are shown in Figure 6.16. Here, i_{cm} is approximated as the sum of the high-frequency component as if the high frequency were only applied to L_{cm} and the low-frequency as if the voltage in $C_{cm} + C_y + C_b$ were $(V_{dh} + V_q)/2$, neglecting the resonance. This is a rough approximation but useful to get an idea of the waveform expected in the prototype. Figure 6.16 shows that i_{cm} always switches between positive and negative values in a switching cycle, implying that ZVS is not negatively affected. With the selected values of C_y and C_b , the low frequency current is almost negligible, $I_{cm\ rms} \approx 52$ mA rms with a maximum value of 253 mA. Since this current is low, the effect on the port voltages can be neglected, and the modulation is barely affected by the filter.

Figure 6.16: CM current and leakage current with the proposed designs, showing the average current in each switching cycle, and the superposition of the average current with the triangular shape at switching frequency, for $L_{cm} = 2.5$ mH and $C_{cm} + C_y + C_b = 960$ nF.

6.3.3 Validation through simulation

This filter has been included in the simulation in *Gecko Circuit* described in Section 5.3, to validate its effectiveness. Figure 6.17 a) shows the filter added to the topology. The inductance has been modeled with an additional L_{lk} of 10 μ H and winding resistance of 150 m Ω , according to the measurements of the implemented choke at 100 kHz.

Figure 6.17 b) shows the voltage applied to the CM choke and the voltage of the parasitic capacitor for 1 kVA resistive load. The results are similar to Figure 6.6 but for the sharp corners in V_{cm} that are smoothed by the choke. The current waveforms are shown in Figure 6.17 c). Again the results are similar to the expected waveforms from in Figure 6.16, slightly different for the loading effects of C_o . The simulated i_{lk} has a value of 23 mA rms and it is expected to be lower when Z_{gnd} is considered, so the 50 mA rms specification is met. For the current in the choke, the

6.3. Leakage current filter design

Figure 6.17: a) circuit added to simulate the behavior of the leakage current filter, b) voltage applied to the choke and V_{cm} along the line cycle, c) leakage current and CM current through the choke along the line cycle.

peak reaches 350 mA, so there is some margin until saturation is reached. Finally, it is appreciated that the oscillations are quickly damped, thanks to $C_b R_b$. Additionally, the estimated losses in R_b are below 100 mW.

Simulation for capacitive, inductive ($PF = 0.7$), and light load (250 VA) have also been performed, and the results are similar in all cases. For capacitive and inductive load, sometimes I_{cm} is larger than the high-frequency component, which implies that i_{cm} is positive in a few switching cycles. Consequently, the current for ZVS is below the threshold a few cycles, yet it is not a problem as the difference is below 100 mA. Also, it is observed that there is more ringing when the load is capacitive. For light load, the CM current is considerably reduced as the switching frequency is higher.

Finally, it has also been simulated the case where ground is placed in the positive terminal of the load instead of the midpoint, because this is the configuration that is going to be used in the prototype. In this case, i_{lk} barely increases. The only difference is that I_{cm} is steeper near $\pi/2$ and $3\pi/2$. The simulation validates the design under different conditions.

6.4 Leakage current filter and CM EMI filter design

Before the chapter is concluded, this section discusses a few aspects of the design of the CM EMI filter and the effects of the leakage current filter on reducing the conducted noise.

The normative *FCC Part 15 B for unintentional radiators* [17] is one of the specifications of the LBC, as mentioned in Section 1.3. This normative sets a limit in the radiated and conducted emission, and, for the latter, it limits the noise in the output, as shown in Figure 1.1. The noise is measured from both output terminals to ground with a 50 $\mu\text{H}/50\ \Omega$ LISN network, this was represented in Figure 1.5. The complete system is shown in Figure 6.18 to clarify the idea.

Figure 6.18: Inverter including the leakage filter, the DM and CM EMI filter, and the LISN. The parasitic capacitances of the power stage are also shown. Unfortunately, it is hard to decrease i_{cm} with a CM EMI filter.

The problem of this solution is that i_{cm} flows through the LISN, which is considerably higher than i_{lk} as shown in Figure 6.16. Due to the high impedance of the inductance in the LISN, this current is diverted to the RC network, which is turned to CM noise. Increasing the CM inductance of the EMI filter would not help much as it is in series with L_{cm} of the leakage current filter unless its value is much higher than L_{cm} . Therefore, a considerably high value of magnetizing inductance on the CM EMI filter would be required to reduce i_{cm} , probably with a prohibitive volume.

A different solution is proposed to address this issue. The idea is to refer the leakage current filter to the output of the inverter rather than to earth, as shown in Figure 6.19. This solution was proposed by the winners of the competition, *CE+T*, in [61]. This scheme decreases the CM noise considerably, as it confines i_{cm} inside the inverter, so it does not flow through the EMI filter or the LISN but through the additional path, [1]. This additional path can be connected to either side of the output, although the best scenario is to connect it to the middle point of the output capacitor to minimize the low-frequency components of the CM current in the choke. This idea has been validated in simulation by adding the LISN model to the simulation of the previous section, without EMI filter. Both configurations have been tested: connecting the leakage current to ground as in Figure 6.18, and to the additional node as in Figure 6.19. The latter shows much lower CM noise, yet, in both cases, CM filters are required to meet specifications.

This solution can be regarded as having a two-stage CM filter. It should be noted that the $C_b R_b$ should be tuned again as C_{cm} is no longer a part of the leakage current filter.

6.5. Interleaving

Figure 6.19: Solution with the leakage current filter referred to the negative output of the inverter.

Finally, if the leakage filter is referred to the midpoint of the capacitor, connecting this point to ground may be beneficial. The leakage current would be confined to the inverter because of the and the impedance of the LISN and the EMI filter. But this is only valid if ground is set to the midpoint of the load. Since ground is connected to one of the terminal of the load in the prototype, this solution is not discussed in detail. It should be noted that this is the preferred configuration, as in simulation it shows almost negligible CM noise (separating the noise in CM and DM following [107]), no CM filter beside the leakage current filter would be required.

Please note that this is far from sufficient for the design of the EMI filter, in the simulation ideal switching transition are considered and the parasitic effects of passive elements is not considered. The CM filter should limit the current caused not only by C_{cm} , but also by any additional capacitance from the inverter to the chassis. This capacitance depends on the physical structure of the inverter. The design should account for these parasitic and the parasitic behavior of components at high frequency; effects that are very important when it comes to a good high-frequency attenuation. The design of the EMI filter is beyond the scope of this dissertation, but it was important to clarify that the design of the leakage current filter can be independent of the EMI filter design.

6.5 Interleaving

The analysis and the design of the prototype in this work considered a nominal power of 1 kVA. However, the specifications for the LBC stated a nominal power of 2 kVA. The initial idea for this project was to interleave two 1 kVA stages. Interleaving could significantly reduce the value of C_o which would reduce the reactive power and could reduce the CM and DM noise compared to a single 2 kVA stage. Unfortunately, interleaving in this topology is far from straightforward.

As in a Full-Bridges with a single inductor, power stages cannot be interleaved directly. In this topology, the reason is that the three ports are switching with respect to each other. For instance, if two power stages were interleaved, q^+ from one stage and q^- from the other may be turned on at the same time, shorting the input.

6.6. Conclusion

Further research on this topic is out of the scope of this work, but it is important since interleaving may help to obtain an optimized inverter. A single stage has been used for the experimental results presented in the following chapter.

6.6 Conclusion

In this chapter, a comprehensive view of the critical design considerations regarding the leakage current for nonisolated PV inverters is provided, highlighting the differences and additional challenges that the inverter studied in this work represents, compared to more conventional structures. It is shown how the selection of the ground connection only affects the low-frequency components CM current, concluding that the inverter can meet the 50 mA rms specified in the competition. It is also concluded that this inverter is not suitable for PV specifications requiring lower leakage current, such as 5 mA rms [1]. Perhaps this inverter may be better suited for fuel-cells applications. Because of the small ground capacitance, the filter could be omitted or removed [26]. It has also been discussed how the position of the main inductor influences the volt-seconds of the choke. The choke is placed in the input side of the inverter to reduce winding losses. The proposed leakage current filter includes a damping network to avoid the oscillatory behavior of the CM current, caused by the harmonic content of the CM voltage near the resonant frequency. A design for the filter has been proposed and validated through simulation.

Experimental validation

In this chapter, the concepts examined in the previous chapters are validated. First, through a simulation, including ZVS transitions, the operation of the leakage current filter, and the modulation and control altogether. Then, the prototype is described, highlighting the different circuitry and the device selection, followed by the description of the setup and equipment used to test it. Different tests are performed to show the correct operation of the inverter and validate the multimode modulation explained in this dissertation.

7.1 Simulation of the complete system

In this section, the results obtained from a simulation intended to represent the real behavior of the inverter are discussed. Figure 7.1 shows the schematic of the circuit in the simulator *Gecko Circuits*, which is a complete version of what has been discussed in Sections 3.3.3, 5.3 and 6.3.3.

Figure 7.1: Circuit used for simulation, including the power stage, control, and leakage current filter. In blue, the electric part, and, in green, the control and measurement.

For this simulation, switching devices are modeled as *on* and *off* resistances and the voltage drop of the body diode only. R_{ds} is selected to match the value two *GS66516T* from *GaN Systems* in parallel. To model the nonlinear C_{oss} accurately, the data-points of Figure 3.7 are used. The values used for the inductor, capacitors, and leakage current filter are listed in Table 7.1, described in the following section. The choke is modeled with 10 μH of leakage inductance and 150 $\text{m}\Omega$ for the winding resistance according to the measurements of the implemented choke. For C_s , the model accounts for the variations in capacitance due to voltage, as ceramic X6S material exhibits a significant drop on capacitance at nominal voltage. This aspect is discussed in the following section. A parasitic capacitance is included to model the parasitic capacitance from the PV panel to ground, with a value of 213 nF as it is the measured value for the input source used for the test, different from the 120 nF specified in Section 7.3. Ground is connected between the load and the inductor to model the setup in the prototype. Note that this is different from what was described in the previous chapter. Also, the capacitors of the leakage current filter are connected to the positive terminal of the output of the inverter.

The main code implemented as a *Java* block, calculating the operation mode and applied times based on the references generated by the loops and measurements every switching cycle, following the description in Chapter 5. To model the switching cycle delay in the FPGA due to the time it takes for the whole processes to be computed, the measured V_g , V_s , V_o , I_g , and I_o of the previous cycle are used for the calculation of the actual switching cycle. There is an additional *Java* block used to generate the dead times and mathematical blocks to implement the current detection and over-current protection. A 100 ns delay is added to the detection signals to account for delays from the detection to the gate signal. The delay negatively affects the operation of the inverter. Finally, there are voltmeters, ammeters, and scopes to monitor different variables of the circuit.

Figure 7.2 shows the port voltages and currents for 1 kVA $PF = 1$, $PF = 0.7$ capacitive, $PF = 0.7$ inductive, and 250 VA $PF = 1$ loads, respectively. In the four cases, the output voltage is a perfect sinewave, and the input current and voltage are nearly constant. However, these waveforms are different from those shown in Figure 4.26 to 4.29 when the modulation was introduced. There are two main reasons for these differences, besides the fact that the references are not followed exactly because of the loops.

First, the effect of the output capacitor is not negligible. It was not considered when the modulation was described in Chapter 4 as it was not fundamental to understand the operation of the inverter, and it would have added complexity without improving the quality of the explanation. The capacitor increases the apparent power, and makes the power factor slightly capacitive [68]. For $C_o = 10 \mu\text{F}$, the added reactive power is 217 VA. At full power, implies an apparent power around 1023 VA. However, for capacitive load with $PF = 0.7$, the total reactive power becomes 924 VA, so the apparent power is 1164 VA, increasing the current in the inductor and the voltage swing in the storage capacitor as shown in Figure 7.2 b). This is also the reason why the apparent power in inductive load is decreased, and why at light load the behavior is mostly capacitive. Without load, the inverter moves charge from C_s to C_o back and forth, demanding only the input current required to compensate losses.

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Figure 7.2: Results of the simulation, a) for 1 kVA restive load, b) 1 kVA $PF = 0.7$ capacitive load, c) 1 kVA $PF = 0.7$ inductive load, d) 250 VA resistive load.

The second reason for the differences with the description in Chapter 4 is the delay from the detection to gate signals. This delay increased the effective threshold current depending on the slope of the inductor current, as shown in Figure 5.13 a). As a result, the negative current in $Tra4^+$ is well below $-I_{th} = -3.5$ A. The delay causes a small ripple in I_g and I_o , and increase the rms and peak inductor current as described in Section 5.4. The effect of the delay is also discussed in [68]. In [68], the threshold current is set to 2 A, but the actual current is between 4 A and 6 A depending on the operation point, because of the delay and the resonance of L and C_{oss} in the ZVS transition.

A zoom of the operation in the mode $Tra4^+$ at $\pi/2$ for 1 kVA resistive load is shown in Figure 7.2 b). It is easy to identify here the difference between $-I_{th}$ and the actual value of the current in the $[000 \rightarrow 111]$ transitions. The operation at $\omega \cdot t = 0$ is shown in Figure 7.2 a), operating in $T0$. In this case, the difference between $-I_{th}$ and the actual current in the transition is not that high because the slope of the inductor current in $[000]$ is lower as compared with the slope in $Tra4^+$. In these figures, the gate signals and detection signals (D^+ and D^-) are also included.

To validate that the leakage current is not modified when the nonidealities are considered, Figure 7.4 a) shows the CM voltage and current in the choke and the parasitic capacitor along the

Figure 7.3: Zoom of the waveform for 1 kVA resistive load, a) near $\omega \cdot t = 0$, b) near $\omega \cdot t = \pi/2$.

line cycle for 1 kVA resistive load. It should be noted that ground is not connected in the middle point of the load as in Figure 6.17, which increases I_{cm} . The voltage and current in the choke and in the parasitic capacitance from the input to ground are not changed considerably and i_{lk} is equal to 36 mA rms. Therefore, the specifications are expected to be met, although the model is simplistic: it does not include parasitic capacitances in the choke nor Z_{gnd} . As a result, real waveforms may differ.

Figure 7.4: Validation of the leakage current filter for 1 kVA resistive load, a) CM voltage and current in the parasitic capacitance and the choke, b) effects of the CM current in the current of the q leg.

To validate that the CM current does not affect the operation of the inverter, a zoom of the operation at $\pi/2$ is shown in Figure 7.4 b). In this figure, the inductor current is shown together with the difference between the inductor current and the choke current; this is the current that flows through the q branch. Since the CM current is very small compared to i_L , the current in the q switches is barely modified when the choke is introduced, so the current for ZVS is not affected.

The evolution of the values for the loops is depicted in Figure 7.5 a) with variables named as in Figure 5.1 to show that the control is not influenced much by delays, ZVS transitions, or the

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leakage current filter. The output voltage follows the reference perfectly, and the average storage capacitor voltage is 340 V with the expected swing because of the low bandwidth of the loop. As for the currents, the measured values do not follow the references closely. This is caused mostly by the delay from the current detection to the gate signals. It implies large discrepancies between the current modeled for the plant-inversion and the real inductor current waveform. Nevertheless, the voltage loops adjust the current references, so this is not a problem.

Figure 7.5: Validation of the control for 1 kVA resistive load, a) control loops, b) applied times and operation mode, each unit of the applied times corresponds to 10 ns.

The evolution of the control times and the operation modes is shown in Figure 7.5 b). The applied times evolve continuously and are slightly different from those shown in Figure 5.12 when the simulation was ideal. The range of the switching frequency with this load is 29 kHz to 141 kHz. The sequence of operation modes remains unchanged. Although, as the load is slightly capacitive, the sectors where the modes are used have changed compared to the ideal operation from Figure 4.2.

Finally, to validate the ZVS transition, a zoom of the operation near $\pi/2$ is included in Figure 7.6 a). In this plot, the voltage across the transistors d^+ , h^+ and q^+ , the current in the inductor, and the current through the parasitic capacitances of the MOSFETs are shown. In the plot $i_{cq} = i_{C_{q+}} - i_{C_{q-}}$, and the same for i_{cd} and i_{ch} . The different voltages withstood by each device can be observed. ZVS is always achieved in the whole line cycle. Figure 7.6 b) shows a magnification for the $[000 \rightarrow 111]$ transitions of the previous plot. Full ZVS is achieved as the drain-source voltages of the three switching devices are discharged relatively slowly in less than 200 ns. Note that the current is well below $-I_{th}$ because of the delay and the resonance of the inductor with the parasitic capacitors in the transition.

It is concluded that the inverter works as intended even when parasitics and adverse effects are considered, validating the concepts described from Chapters 3 to 6. Further accuracy would require an estimation of parasitic capacitances and inductances of the prototype. Therefore, it is preferred to validate the real operation in the prototype directly.

Figure 7.6: Validation of the ZVS transitions for 1 kVA resistive load, a) zoom near $\omega \cdot t = \pi/2$, b) further zoom of the [000 → 111] transition.

7.2 Proof-of-concept prototype design

In this section, the proof-of-concept prototype of the inverter is described. Besides the power stage and leakage current filter, the prototype requires additional circuitry like the FPGA, an auxiliary supply, the circuits to measure voltages and currents, the current detection, or the drivers. Figure 7.7 shows the schematic of the inverter, including these additional parts.

Figure 7.7: Schematic of the prototype showing the main components and circuitry used, here C_b , C_y , and R_b represent the value of the components instead of their equivalent CM values.

The following subsection describes the component selection for the power stage and leakage current filter. The additional circuitry is briefly described in Section 7.2.2.

7.2.1 Device selection

The value for the main inductor is selected based on an optimization developed in the early stage of the project considering the BCM modulation in specific points. Further optimization would be required accounting for the TCM modulation explained in Chapter 4 to achieve higher efficiency

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and power density. A list of the components used for the power stage and leakage current filter and its values is included in Table 7.1.

Component	Value	Description
Inductor	80 μ H	2 $\times$ RM10 , 3C95 , $n = 21$, Litz wire: 200 strands, 1.1 mm diameter
Storage capacitor	90 μ F	216 $\times$ 2.2 μ F 450 V X6S, [108]
Input capacitor	12 μ F	<i>CeraLink</i> SP500 20 μ F 500 V [109]
Output capacitor	10 μ F	PP film 250 V rms, C4ATFBW5100A3FJ [110]
MOSFETs	—	2 $\times$ GS66516T 650 V 60 A, [86]
CM choke	2.5 mH	Vitroperm 500 F , T60006-L2045-V101, [105] $n = 13$, solid wire, 1.5 mm diameter
C_y	150 nF each	100 nF + 47 nF , 450 V C0G
C_b and R_b	270 nF and 270 Ω each	2 $\times$ 100 nF + 22 nF, 450 V C0G

Table 7.1: Description of the components used for the 1 kVA power stage and leakage current filter.

Two GaN devices in parallel are selected as it helps to reduce R_{ds} and to spread the heat generated. Nonetheless, more devices in parallel, aside from increasing the price, would increase C_{oss} , which in turn would increase the value of I_{th} .

Two 40 μ H inductors are used in series to minimize the total height. The saturation current is set around 18 A. This value is close to the maximum observed in simulation, and it is selected to minimize the volume of the inductors. With this inductor and the C_{oss} of the devices selected, I_{th} is set at 3.5 A as described in Chapter 4.

Class II ceramic capacitors are selected for C_s because they feature an energy density similar to electrolytic capacitors, but a much higher current capability. This effect is important when high voltage swing is allowed [65], [111]. The device C5750X6S2W225K250KA from *TDK* has been selected because it shows the best power density in the market, according to [41] and [68]. Unfortunately, X6S capacitors show a significant capacitance drop with applied voltage, meaning that the capacitance at nominal voltage is much lower than the specified [111]. For instance, the capacitance of a C5750X6S2W225K250KA capacitor is just 20 % of the nominal value at 400 V (2.2 μ F), therefore 440 nF only [108]. For this reason, to obtain a capacitance near 90 μ F for C_s , 216 capacitors in parallel have to be used.

For the input, *CeraLink* technology is employed to avoid using many ceramic capacitors. The selected capacitor shows a higher value of capacitance at 400 V, which makes it ideal for this application. Nevertheless, higher power density can be obtained if ceramic capacitors are used instead. The value of C_g is selected to obtain a reasonably low voltage ripple at switching frequency and to ensure that the inductor does not resonate with C_g when the switching frequency is low. Twice-line frequency is not a concern for the design of the input capacitors as the difference between the input and output power is buffered by the storage capacitor.

For the design of the output capacitor, a relatively low value should be used as C_o increases the reactive power of the inverter, as mentioned in the previous section and in [65]. Still, the capacitance has to be large enough to filter the switching frequency components of i_L . A reasonable value is 10 μ F, which filters well the ripple and adds around 220 VA of reactive power, as discussed in

Section 7.1. Unfortunately, the ceramic technology used for C_s or C_g is not well suited for the design of C_o . Due to the nonlinear capacitance of Class II capacitors, the value is lower precisely when higher capacitance is needed. Also, the current in C_o would not be sinusoidal, and the output power would contain harmonics at frequencies higher than $2 \cdot f_{line}$. This current can disturb the operation of the active power loop described in Section 5.1.2.2 because of how $\overline{P_o}$ is calculated. Moreover, ceramic capacitors are designed for DC applications; AC voltage is not among the specifications in general. As mentioned in [18], the maximum DC voltage determines the maximum peak to peak voltage when an AC waveform is considered in these types of capacitors. For 240 V rms, the ceramic capacitor should be rated at 680 V. For these reasons, a film capacitor has been selected. This solution is bulky, and it can be modified in the future to increase power density. To reduce the volume, ceramic capacitors could be placed in series, increasing the withstood voltage and reducing the variations of capacitance compared to using a single ceramic capacitor [18]. Another alternative could be to use C0G ceramic capacitors. These capacitors show a very stable capacitance, although they feature lower capacitance per unit of volume compared with X6S capacitors. The problem is that many capacitors would have to be used in parallel due to the low capacitance values of the commercially-available capacitors of this type.

For C_b and C_y C0G capacitors are used to reduce the volume and avoid variations in the capacitance with the applied voltage. As for R_b , it has been slightly adjusted, its final value is 270 Ω each, instead of the theoretical 220 Ω , as it damped the resonance in the choke faster. Finally, the choke design proposed in Chapter 6 is used. It is wound manually trying to keep the turns and winding as far as possible from each other to minimize the parasitic capacitance and leakage inductance following the recommendations in [112].

7.2.2 Auxiliary circuitry

In this section, the additional circuitry required to operate and control the power stage is described briefly. The author has also contributed to the design of the additional circuitry, but specific detail and the complete schematic are a part of the dissertation of Edwin Peredo to be presented the following years.

The gate drivers are designed following the recommendations of the manufacturer [113]. The driver used is the *Si8275*, from a family of isolated drivers with high CM dv/dt immunity. The drivers for d^- and q^- are supplied through one of the outputs of the isolated supply. The other MOSFETs are supplied with bootstraps, as shown in Figure 7.7.

For the detection of the current to generate the signals D^+ , D^- , and OVC , a shunt resistor is connected in series with the inductor. The voltage in the shunt is amplified and compared with fixed voltages in such a way that the outputs of the comparators change at $i_L = I_{th}$, $i_L = -I_{th}$, or $i_L = \pm I_{ovc}$ following Figure 5.9. These signals go directly to the FPGA. Isolation is not required since the ground for the FPGA and the ground for the detection circuitry is the same; the node between the load and the inductor, as shown in Figure 7.7. This is important to avoid isolators and reduce the delay between the generation of the signals and the detection in the FPGA, which is already an important issue.

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Measurements of voltages and currents are required for the control loops and inversion-based control. For the voltages, voltage dividers referred to the control ground are used. Then, a differential amplifier is used to remove the CM component from the measurement. These signals go to the ADCs in the FPGA. For the current measurements, hall-effect sensors from *Allegro MicroSystems* are used as isolation is intrinsically provided. To get rid of the switching frequency component of the current, a low pass filter is added before the signal goes to the ADCs.

To supply the auxiliary circuitry in the inverter, a Flyback supplied from the input port is used to generate four independent outputs: 5 V for the FPGA, the detectors, and the control side of the drivers. 15 V and -15 V for the voltage sensors. Finally, 10 V for the drivers, this last one referred to the source of d^- and h^- .

As described in Chapter 5, the FPGA selected for this work is an *Artix-7* from *Xilinx* [114]. A module from *Trenz Electronic* integrating the FPGA is used to interface the FPGA with the inverter [115]. A *USB-JTAG programming Cable* from *Xilinx* is used to connect the FPGA and the PC.

Finally, there are slide switches, a LED, and the connectors. The different parts listed above are shown in Figure 7.8. This is a picture of a former prototype designed in such a way that all parts were accessible, so it is useful to show the different circuitry. For the new prototype, a few modifications are made, the design is modified to increase the power density, and to include the bootstrap, auxiliary supply, and leakage current filter. The description of the final inverter will be included in the dissertation from Edwin Peredo, as he developed the schematics and PCBs.

Figure 7.8: On the left, a picture of the former prototype, with the different circuitry highlighted. In the right, the passive components used in the prototype used for the tests.

7.2.3 PCB design

For the PCB design, care has been taken to minimize switching loops for the power stage. Switching devices and the decoupling capacitor are set in both top and bottom layers to minimize the area, leaving the auxiliary circuitry and drivers to the sides of the board. A small heatsink is added to

each GaN transistor since *top-cooled* devices are used. Although the drivers are relatively far from the transistors as shown in Figure 7.8, traces are arranged to minimize the gate driver loop. A large plane connected to the node between the inductor and the load is set below the auxiliary circuitry because the FPGA is referred to this node. This plane and sensitive traces are routed far from the power stage to avoid coupling. Finally, as there is no chassis in this prototype, a connection to earth ground is not provided.

Even with the considerations above, lack of ZVS can generate severe issues and disrupt the operation of the inverter. Noise is coupled to the current detector. Therefore, ZVS is not only desired to reduce EMI and losses but to ensure safe operation of the prototype.

This board was developed with *Altium* by Noemí Nogal, the contribution of the author was the design of parts of the schematics and the supervision of the layout design.

To give an estimate of the volume of this inverter, the sum of the volumes of each component in Figure 7.8 can be obtained. For the PCB, the thickness of the heatsinks, the PCB itself, and the FPGA are considered. As for the other components, its rectangular enclosure is provided. Additionally, the Flyback board has to be considered, although it is not depicted. A list of the estimation of volume is given in Table 7.2. Nevertheless, this volume is not an accurate representation of the total volume that a compact design could have. On one hand, the dimensions of the main PCB can be easily reduced, and most of the volume considered is actually air. Since most of this volume comes from the main PCB, a large margin of improvement is still available. On the other hand, the size of different components should not be considered as the total volume because in the integration process it is impossible to fill all the space with components. With this approximate volume, the power density of this prototype (designed for 1 kW) is roughly 2 kW/dm³, or 33 W/in³, below the target value for the competition, 50 W/in³. Nevertheless, it should be noted that this prototype is designed to validate the operation of the modulation and control of the inverter rather than to achieve very high power density.

Part	Dimensions	Box volume
Main PCB	161.2 mm · 141.4 mm · (2.3+4.8+8) mm	344.2 cm ³
Flyback PCB	73.9 mm · 40.4 mm · (1.1+10.4) mm	34.3 cm ³
Inductor	2 × 24.7 mm · 24.7 mm · 18.7 mm	22.8 cm ³
Storage capacitor	216 × 5.7 mm · 5 mm · 2.5 mm	15.4 cm ³
Input capacitor	33 mm · 22 mm · 11.5 mm	8.3 cm ³
Output capacitor	41.5 mm · 20 mm · 40 mm	33.2 cm ³
CM choke	43.1 mm · 43.1 mm · 18.5 mm	34.4 cm ³
Total volume		492.6 cm³

Table 7.2: Volume occupied by the different components in the prototype, as the cubic enclosure.

7.3 Setup to test the inverter

In this section, the setup used for different tests is discussed. Besides regular operation where the inverter is connected between the input and output, DC-DC tests are also performed to validate the open loop operation of the inverter. In these cases, a third port is required for C_s . Figure 7.9

7.3. Setup to test the inverter

shows the equipment that has been used for the tests, and Figure 7.10 shows how the different instruments are connected. The equipment is described below:

Figure 7.9: Picture of the setup and equipment used to test the inverter.

Figure 7.10: Connection of the inverter with the different equipment.

- A computer is used to program the FPGA and to read internal variables. The software used is *Vivado* 2016.2 and *ChipScope* 64-bit, respectively, as described in Appendix D.
- The DC-source N8762A from *Agilent Technologies* is used to supply the input power. This supply has 213 nF between its terminals and ground, which is close to the specified in the LBC, 120 nF.
- In series with the input source, a 20 Ω resistor is used to model the behavior of a PV panel, so the input voltage ranges from 400 V to 450 V depending on the load.

- A resistive load is directly connected to the output port of the inverter. Banks of passive resistors from the company *Paliba* are used.
- For DC-DC test where C_s alone cannot be used as the third port, an additional source, PS1000-30 from *APS*, or an electronic load, *Chroma* 63204, are connected in parallel to C_s .
- Also, for tests where the input voltage is increased from zero, the Flyback is supplied through an auxiliary supply, *BK Precision* 1762.
- To obtain the power losses and other measurements, a *Yokogawa* WT1800 power analyzer is employed.
- Further measurements are taken with multimeters *Fluke* 8808A for auxiliary voltages.
- Finally, the oscilloscope RTE 1104 from *Rohde&Schwarz* has been used to test internal voltages and currents, with differential probes RT-ZD01 and current probes RT-ZC20B.

It is important to account for the parasitic capacitances to ground of the different equipment used, not to induce ground currents inadvertently. This is especially important when using the DC source or DC load instead of the storage capacitor for DC-DC tests, as they present high values of capacitance from their terminals to earth ground. For this reason, an additional CM choke is required as shown in Figure 7.10, preferable with very high inductance. Otherwise, the voltage applied to that parasitic capacitance would change at switching frequency, inducing large currents that can disrupt the operation of the inverter.

Another important aspect of the setup is the connection of the USB to the PC for debugging purposes; it connects earth ground to the control ground of the inverter. In other words, out^+ of in Figure 7.10 is connected to ground. Hence, tests with the USB connected to the PC are only possible if ground is actuality connected to out^+ in the load, but not to the midpoint or the other terminal, and only if there is no EMI filter or LISN. Nevertheless, even with this configuration, the communication between the FPGA and USB is only reliable up to certain voltage levels, at a higher input voltage, the noise disrupts communications.

Finally, another important consideration is the connection of the Flyback converter. It should be connected to the input port. However, for tests where the input voltage is increased from zero, a separate supply is used as the input for the Flyback. This supply, with the negative terminal connected to in^- , is necessary as the Flyback can only work for input voltages above 30 V.

7.4 Experimental results

In this section, the results obtained with this setup and the prototype are presented. A variety of tests have been performed to validate different aspects discussed in the thesis. The author conducted the tests with the help of Edwin Peredo. These test include the operation of the inverter as three-port DC-DC converter in different operation points, tests to validate the ZVS transitions, the operation of the inverter under different resistive loads, and the validation of the leakage current filter.

7.4. Experimental results

7.4.1 Open loop DC-DC tests

First, the results of the open loops tests are discussed. These DC-DC tests were realized in the former prototype, and do not include leakage current filter because the output is not grounded, I_{th} is set to 2.5 A, and a large input capacitor is used, yet this is enough to validate the correct operation of the inverter. These results, presented in [87], are discussed here in detail. In these tests, the only inputs for the FPGA are the detection signals D^+ and D^- to know when i_L crosses I_{th} and $-I_{th}$. The applied times, T_{a-h} , and the operation mode are defined manually. Besides showing the correct operation of the power stage, the goal is also to measure the losses in different points of the line cycle and to check what is the effect of the threshold current in the efficiency. For this purpose, the inverter has been tested in the equivalent conditions for the DC-AC operation at $\omega \cdot t = 0$, $\omega \cdot t = \pi/4$, $\omega \cdot t = \pi/2$ and $\omega \cdot t = 3\pi/4$ for resistive load and 1 kVA, neglecting the load added by the output capacitor. As the nominal load is considered, the input voltage is held at 400 V, and no input resistor is added. The storage capacitor port is configured as a source for $\omega \cdot t = 0$, with a value of 340 V. To represent the operation at $\omega \cdot t = \pi/2$, the storage capacitor port is configured as a load with $V_s = 340$ V too. Meanwhile, for $\omega \cdot t = \pi/4$ and $\omega \cdot t = 3\pi/4$ the storage capacitor is fixed to 380 V and 295 V respectively, although it does not provide or store any power. The operation mode and applied times are calculated so the desired current flows in each port and in such a way that for $R_{load} = 57.2 \Omega$, V_o takes the value 0 V, 240 V, 340 V and 240 V for the four points respectively. The measured waveforms for each one of these points are shown in Figure 7.11, including the current and voltage in the inductor and the voltage in one of the switches, d^- .

In Figure 7.11 a), the operation mode is $T0$, symmetrical since the applied times for the positive and negative part of i_L are equal. The mode in Figure 7.11 c) is $Tra4^+$, and, since $V_s = V_o$, the slope of the state $[0 \ +1]$ is zero. Both waveforms in Figure 7.11 b) and d) are the same but for v_{d+} , because these operation points are in the frontier between $Tra4^+$ and $Tra3^+$ ($I_s = 0$), and the storage capacitor is not used since the sequence is $[+1 \ 0] \rightarrow [0 \ 0]$. The difference in magnitude and switching frequency in i_L for the different points can be observed. These results validate the correct operation of the power stage.

In DC-DC operation, it is possible to adjust I_{th} to the specific value required for every operation point and to remove the states $[111]$ and $[000]$ for ZVS if they are not required for ZVS. In this case, the states $Tra3^+$ and $Tra4^+$ do not require the state $[000]$, as $[001]$ is directly switched to $[111]$ with negative current. On the other hand, $T0$ requires both $[111]$ and $[000]$ as it is the only way to obtain ZVS, so the only difference compared to Figure 7.11 a) is the lower threshold level.

These results show how much the shape of i_L is affected by I_{th} and the addition of the states $[111]$ and $[000]$. The results with nearly the optimum I_{th} , set to $i_{L \ min}(0)$, for each operation point as before are shown in Figure 7.12.

In the four cases, the rms and peak value of the current is reduced compared to the results in Figure 7.11, underlining the downsides of the proposed TCM modulation. Nevertheless, the waveforms in Figure 7.12 are valid only for specific points. This solution is not applicable along the line cycle for DC-AC operation because of the high and low switching frequency limitations, the fact that I_{th} should be dynamically adjusted, the control would have to be modified, and because

Figure 7.11: Results of the DC-DC tests for $I_{th} = 2.5$ A, for the equivalent operation of the inverter at $\omega \cdot t = 0$, $\omega \cdot t = \pi/4$, $\omega \cdot t = \pi/2$ and $\omega \cdot t = 3\pi/4$ respectively. The scale in the plots is 200 V/div, 4 A/div and 4 μ s/div.

the modulation would no longer be seamless as discussed in Chapter 4. The measured losses of the power stage for the waveforms in Figure 7.11 and 7.12 are listed in Table 7.3 to quantify the drawbacks of the TCM modulation. These solutions are referred to as fixed I_{th} and dynamic I_{th} , respectively.

ωt [rad]	V_g [V]	V_s [V]	V_o [V]	P_g [kW]	P_s [kW]	P_o [kW]	losses $I_{th\ fix}$ [W]	losses $I_{th\ dyn}$ [W]
0	400	340	0	1	-1	0	12.34	6.84
$\pi/4$	400	380	240	1	0	1	15.15	10.01
$\pi/2$	400	340	340	1	1	2	17.67	12.02
$3\pi/4$	400	295	240	1	0	1	15.73	10.20

Table 7.3: Losses of the power stage for the DC-DC tests, the voltage and power of the measured points change slightly from what is listed here as it is hard to adjust the applied times accurately.

The results show that the losses of the power stage are very low thanks to the use of GaN devices and the fact that the modulation is designed to minimize P_{indL} , and it shows how I_{th} increases the losses considerably. The average losses of these four points are 9.8 W when I_{th} is adjusted for each point and the additional states removed if not required, but 15.2 W for $I_{th} = 2.5$ A and with the states [111] and [000], a 50 % increase. To give a sense of scale, using these average losses to calculate the efficiency of the power stage, that would mean $\eta|_{I_{th\ dyn}} \approx 99.02$ % and $\eta|_{I_{th\ fix}} \approx 98.48$ %. It should be noted that this does not represent the actual efficiency of the power stage, it is just a figure of merit obtained from the losses of the DC-DC test.

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Figure 7.12: Results of the DC-DC tests for the optimum threshold current in each case and without the additional states for ZVS if not required, for the equivalent operation of the inverter at $\omega \cdot t = 0$, $\omega \cdot t = \pi/4$, $\omega \cdot t = \pi/2$ and $\omega \cdot t = 3\pi/4$ respectively. All plots use 200 V/div, 4 A/div, and 4 μ s/div as in the previous picture.

7.4.2 Closed loop ZVS tests

In Figures 7.11 and 7.12 v_{d-} is shown, no ringing is observed in the transitions because of the low dv/dt due to the ZVS operation. Additionally, a test has been developed to validate the ZVS transitions in the latest prototype. For this test, the code of the FPGA is modified to ensure that the storage capacitor is at 300 V while the output is kept at 0 V. The input voltage is set at 400 V. Therefore, v_q^- , v_h^- , and v_d^- reach 400 V, 300 V, and 100 V respectively, and the evolution of the voltage in the transition is easily observed. Moreover, as the power is zero, the inductor current only switches the states [111] and [000] between I_{th} and $-I_{th}$ mostly. For this test, I_{th} is already set to 3.5 A, and the external connections for the storage capacitor ports are removed as the inverter is working on closed loop. Figure 7.13 a) show the inductor current and the voltage across q^- , h^- and d^- . A zoom of the [111 $\rightarrow$ 000] transition with positive current in the inductor is shown in Figure 7.13 b). The voltages in the nodes change slowly during the transitions after all devices are turned off, and it takes a different time to discharge the different capacitances as discussed in Chapter 3. All complementary devices are turned on after the 200 ns dead-time with ZVS, although a lower time is required for the three switches to reach $V_{ds} = 0$, $T_{tr} \approx 127$ ns in this test.

This transition can also be analyzed with the *Matlab* script described in Chapter 3. For $i_L(0) = 4$ A for the transition (which is the result of setting I_{th} at 3.5 A and considering a delay of 100 ns) $T_{tr} \approx 110$ ns, close to the measured value.

Figure 7.13: Validation of the ZVS transition with all switches involved, a) waveform of a test with $V_g = 400$ V, designed to keep V_s at 300 V and V_o at 0 V b) zoom of the transition [111 $\rightarrow$ 000] with an inductor current slightly above I_{th} . 100 V/div is used for the voltages.

7.4.3 Closed loop DC-AC tests

Once the correct operation of the power stage and ZVS are validated, the DC-AC operation with the loops closed is tested. The setup used is the one shown in Figure 7.10 with ground connected to the positive terminal of the load, and cs^+ and cs^- floating. To ensure safe operation of the inverter, the output voltage reference is defined to be proportional to V_g , until V_g reaches its nominal value of 400 V, where the amplitude of the output voltage reference is 340 V. Therefore, problems can be identified at lower voltages, where the safety of the inverter is not at stake. These tests have been performed, including the leakage current filter and with I_{th} set to 3.5 A. The dead time is set to 200 ns and T_{leb} to 500 ns, more information about T_{leb} is provided in Section 5.2.3.

Figure 7.14 shows the results for 1 kVA resistive load. In this figure, the sinusoidal output voltage and current are observed, also the 120 Hz voltage in V_s , buffering the difference between the input and output current, and the constant input current. The effects of the 100 ns delay are visible in the i_L waveform; the effective I_{th} and $-I_{th}$ are above 3.5 A and -3.5 A. Also, the input current contains some ripple still. The measured DC current is $2.4425 \text{ A} \pm 2 \text{ mA}$ while the rms value is $2.446 \pm 2 \text{ mA}$ showing that the ripple is small. If all the ripple is assumed to be caused by the 120 Hz component, it would correspond to an amplitude of the component of 235 mA, which leads to a ripple right below the 20 % specified for the competition.

A zoom of the plot in Figure 7.14 in different instants of time are shown in Figure 7.15 to clarify how the operation of the inverter varies along the line cycle. This plot shows the shape of i_L for different operation modes and applied times long the line cycle. The evolution of the applied times is continuous, as the difference between i_L in a switching cycle and the next in all the figures is very small. Furthermore, the last zoom corresponds to the shift between modes $T1^-$ and $T0$, where T_e , T_g , T_h last zero.

This test has also been repeated for 750 VA, 500 VA, 250 VA, and without load. The results are shown in Figure 7.16. The maximum input voltage is reached without load, in Figure 7.16 a), when the input current is nearly zero. Although the output current is zero, the average inductor current supplies the current needed for the output capacitor to have a sinewave voltage, so a little current is required, and the load seen from the inductor is purely capacitive. A small voltage ripple

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Figure 7.14: Main waveforms of the inverter along the line cycle for 1 kVA resistive load, the scales are 200 V/div for V_g , V_s , V_o , and $v_L - V_o$, 5 A/div for I_{in} , I_{out} and i_L , and 2 ms/div.

in C_s buffers the reactive power caused by C_o . The shape of i_L is mainly determined by I_{th} and the 100 ns delay, as applied times are short. As the load increases, in Figure 7.16 b) to d), the input voltage decreases, the swing in V_s increases, and the inductor current increases because applied times are longer.

These tests prove the operation of the inverter under different resistive load. Unfortunately, under capacitive load, the leakage current choke was reaching saturation, and it was unsafe to reach nominal voltage. Only partial results at the highest input voltage reached are presented, shown in Figure 7.17.

With capacitive loads, a voltage distortion is observed in the shift from $Tra2$ to $Tra3$, positive and negative, near the point where $V_g - V_s = V_o$ described in Section 4.3.2. Also, in this specific test, V_s was reaching V_g because of how the reference for V_o is generated, this problem is likely to disappear when nominal input voltage is reached. This distortion correspond to the operation at very low frequency, measured to be below 30 kHz.

As for inductive load, there was no inductance available in the lab to perform the test and it was only tested with a load far above the specified only in low voltage. As a result, the operation has been only validated experimentally with resistive loads so far.

The efficiency of the power stage in these tests has been measured with the *Yokogawa* power analyzer once the temperature in the different devices reached a steady value. The measured losses for the different tests are shown in Figure 7.18 a). The power losses however, change slightly from a cycle to the following one because the bandwidth of the storage capacitor loops is very low. For this reason error bands are added. These error bands do not include the tolerance in the measurements in the power analyzer. Losses are in the 15 W to 20 W range regardless of the load, where the minimum is near half the nominal power. The reason for this is that, at low power, the switching frequency is much higher, and, although ZVS is obtained, losses in the C_{oss} and magnetic components are high. These losses do not include the consumption of the Flyback, which is measured to be below 3 W in the worst case. The efficiency accounting for the power stage and consumption of the Flyback for the different tests is shown in Figure 7.18 b), reaching 97.8 % at

Figure 7.15: Zoom of the main waveforms of the inverter along the line cycle for 1 kVA resistive load in steps of 1 ms considering 0 ms the point in time where $V_o = 0$. The scale is 200 V/div, 5 A/div, and 5 μ s/div. The corresponding mode of each zoom is also included.

full power, well above the minimum specified (95 %). Moreover, the THD in the output voltage is measured to be below 1 % in all the tests.

It should be noted that a discussion on losses distribution is out of the scope of this work. Moreover, the distribution of the losses cannot be measured in this setup. Nevertheless, the temperature in different devices was measured. For an ambient temperature of 25 °C, the leakage

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Figure 7.16: Main waveforms of the inverter along the line cycle for different resistive load, a) no-load, b) 250 VA, c) 500 VA, d) 750 VA. The scales are 200 V/div, 5 A/div and 2 ms/div.

current choke reached 70 °C without load, the maximum measured in the different tests. The inductor and MOSFETs temperatures are maximum in the 1 kVA test, where the inductor temperature only increases to 61 °C and in the GaN devices to 78 °C, with higher temperature in the q switches. The temperature in the capacitors was much lower in all cases. No forced convection was used for the tests.

7.4.4 Validation of the leakage current filter

The leakage current filter ensures that low current flows in the parasitic C_{cm} of the input supply, connected between the input and output ports, as described in Chapter 6. Also, thanks to the leakage current filter, the large CM current spikes that would disrupt the operation of the converter are avoided. The measurements of the variables related with the filter obtained in the previous test are shown in Figure 7.19, under no-load, and for 1 kVA resistive load.

The waveforms for V_{cm} shown here resemble those obtained in the simulation in Figure 7.4 a) and follow from the theoretical analysis described in Chapter 6. The CM current is measured as the difference between the input current sourced from the positive terminal and the currents sunk by the negative terminal at the output of the choke. It has a low resolution because of how it is measured. To have a better understanding of the shape of i_{cm} , a zoom for the 1 kVA test is shown in Figure 7.20 a) and b), showing the waveforms near $\omega \cdot t = 0$ and $\omega \cdot t = \pi/2$, respectively.

Figure 7.17: Operation of the inverter with capacitive load, with $V_{in} \approx 375 \text{ V}$ instead of 450 V due to the saturation in the core, a distortion in the output voltage can be observed. The scale is 200 V/div for the voltages, 5 A/div for i_L , and 2 ms/div in a) and $82 \mu\text{s/div}$ in b).

Figure 7.18: Measurements for the different loads used, a) losses in the power stage b) total efficiency, including the consumption of the auxiliary supply.

Here, the shape of i_{cm} in the switching cycle can be observed. During the transitions the current is distorted since the choke is not ideal.

In Figure 7.19, the resonance in the shifts of modes near $V_o = 0$ is identifiable. In the transition between $T0$ and $T1$, the derivative of V_{cm} with respect to time changes, and, as a result, a resonance is observed. Although the damping network helps to damp this resonance, at full load, it is not enough to prevent the core from saturation, leading to spikes in the current. A zoom of the resonance is shown in Figure 7.20 c). These spikes, if larger, can impair the operation of the inverter and it is the reason why capacitive load was not successfully tested. This experiment shows that the design of the choke in this specific converter is very constrained due to the rich harmonic content of V_{cm} .

Although the goal is to keep the leakage current below 50 mA rms , this value is not shown in the previous pictures. The reason is that it contains noise generated by the input power supply. This noise is larger than the expected current waveform, making it impossible to distinguish the leakage current generated from the inverter from the one generated by the input power supply. In fact, this leakage current is present even when the inverter is turned off. The measured waveforms with the input power supply turned on and off are shown in Figure 7.20 to clarify the nature of this issue. In both tests the prototype is turned off, but the leakage current has an amplitude of 50 mA already. As a result, with the power supply available for the test, representative measurements of

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Figure 7.19: Waveforms of the leakage current filter, including the voltage applied to the choke, v_{Lcm} , and the voltage applied to the C_y capacitors, V_{cm} . The difference between the current in both windings of the choke is also measured, and termed i_{cm} , a) without load, b) for 1 kVA resistive load. The scale is 200 V/div for the voltages, 500 mA/div for i_{cm} , and 2 ms/div.

the leakage current cannot be obtained. Nevertheless, it is clear that the leakage current filter can decrease this current substantially since the voltage applied to the capacitor is just V_{cm} because the high frequency components are filtered.

In future designs of the inverter, the filter design should be slightly modified, and a less thigh design with a margin for saturation should be provided. The conclusion is that filtering the CM voltage is possible thanks to the proposed modulation, which enables the converter to operate with ground referred to the load when C_{cm} is present.

7.4.4.1 Effects of abrupt changes in the modulation

Throughout this thesis, it has been emphasized how a continuous evolution of the applied times along the line cycle was one of the main goals of the proposed modulation, and how it affected the design of the leakage current filter. During the tests, a problem associated with the code made the inverter to skip some pulses and work only switching between I_{th} and $-I_{th}$ for a few cycles. Although the problem is fixed, the waveforms obtained during this test are helpful in visualizing the problem of abrupt changes. A zoom of the problem found in an earlier test is shown in Figure 7.21, where the input voltage reached is only 350 V as the problem prevented the operation at higher voltages.

Due to the abrupt change in the modulation, V_q changes suddenly, and after just a few cycles, the average voltage applied to the choke in a few cycles is enough to saturate the core, and a large spike in the CM current occurs. As a result, the operation of the leakage current filter is only reliable if V_q changes only slightly from a cycle to the next one, proving that a continuous evolution of the variables is almost mandatory in this topology.

Figure 7.20: Zoom of the waveforms of the leakage current filter for 1 kVA resistive load, a) near $\omega \cdot t = 0$, b) near $\omega \cdot t = \pi/4$, c) in the resonance. The scale is 200 V/div for the voltages, 500 mA/div for i_{cm} , and 5 μ s/div in a) and b) and 98 μ s/div in c). d) Zoom of the actual leakage current, the i_{lk} measured during operation gives results far from ideal because most of the noise is generated by the input power supply, the scales are 20 mA/div and 400 ns/div.

7.5 Conclusion

In this chapter, the operation of the inverter has been validated both in simulation and through a proof-of-concept prototype. The simulation, design of the prototype, and setup used for the tests have been described. Load steps to validate the control loops or the soft-start are not included in this work as they are not part of the contributions, they can be found in the dissertation of Regina Ramos. Unfortunately, the operation under capacitive load and inductive load has not been tested.

The operation of the power stage has been validated through DC-DC tests, where the inverter interfaced not only the input and output ports but an additional supply or load (representing the storage capacitor). These tests have been useful to briefly discuss the effects of I_{th} , showing how I_{th} penalizes the efficiency, but showing how it is useful to obtain ZVS and reduce the variations in switching frequency.

The results of the DC-AC operation have proven that the storage capacitor can handle the differences between input and output power and have validated the control loops, the inversion-based control, and the correct operation in the different operation modes. Finally, the operation of the leakage filter has also been validated.

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Figure 7.21: Example of abrupt change in the operation of the inverter due to an error in the FPGA code, the CM current saturates only after a few skipped cycles. The scale is 200 V/div, 4 A/div and 10 μ s/div.

As a summary, this chapter shows that this single-stage inverter achieves promising values of efficiency. Thanks to the proposed modulation, the inverter has been able to operate at nominal input voltage, nominal power, and with the output port grounded for the first time.

Conclusions and future work

In the previous chapter, the operation of the inverter was validated; the inverter successfully achieved almost constant input current while controlling the output sinewave with the proposed TCM modulation. In this chapter, a reflection on this work is provided. The specific contributions of this dissertation are highlighted. Future work is discussed, as this project is not over yet, and there are still some open questions and improvements to be made.

As a brief summary, the inverter studied in this work as the following advantages and disadvantages:

- The inverter is designed to integrate the active filter within the inverter, therefore achieving sinusoidal output voltage and constant input current in a single stage, with few components and a small storage capacitor.
- The main advantage of the topology and modulation is that the power processed in the inductor is reduced by taking advantage of the integration. The storage capacitor is used as a flying capacitor in some sectors of the line cycle.
- Moreover, the modulation uses the inductor current to perform ZVS transitions in all devices, regardless of the operation mode used, the instant of the line cycle, or the load.
- Unfortunately, the control is very complex, not only because the power stage is used to control two variables, but also because the modulation is divided into several operation modes, and these modes are composed of several switching states. The control requires a decoupling network to avoid cross-coupling between the control loops and make them independent of the mode selected.
- A drawback of the considered topology is that a large filter has to be used to limit the leakage current.

8.1 Contributions to the research line

In this section, the contributions of the dissertation are summarized. The bulk of the thesis was dedicated to the analysis and implementation of the modulation of this inverter; from the high-level description to the small details. Since the modulation is based on an *ideal* modulation that was not implementable, first, the state of the project prior to the work of the author is reviewed.

It should be clarified one more time that this project was a collaborative effort and many of the discussed aspects were proposed before this Ph.D. thesis started. As mentioned in the first

chapter, this research line started in 2014 when the LBC was launched. Prof. José A. Cobos led the *CEI@UPM* team that participated in the competition. He proposed the indirect power as a high-level metric to compare architectures, concluding that a single-stage was the optimum solution from the power processing standpoint [70].

The topology he proposed integrates the active filter in the inverter, and to reduce the inductor volume and losses through this integration by means of minimizing the indirect power. This topology is attractive as it requires few components for the power stage, and because a single inductor can control the power between the three ports [16].

The operation of the inverter was divided into multiple operation modes along the line cycle. Ideally, the inverter operated in BCM with variable switching frequency, and modes were classified depending on the type of waveform as triangular or trapezoidal modes [39]. José A. Cobos, Regina Ramos, and Iñigo Zubitur investigated most of the operation modes that are used now.

For ZVS transition, the BCM modulation was slightly modified, and a threshold current was defined. Additional states were added to some modes to ensure ZVS in most transitions before this work. However, none of the proposed solutions paid attention to the importance of having a seamless the modulation.

The digital control of the inverter was mostly developed by Regina Ramos. Together with Jesús A. Oliver, she proposed the solution that is currently being used [40], [73], [74]. The control is divided into four loops and the active power decoupling, and the outputs of the loops are the target current in the input and output ports. To decouple the control variables and be able to use control loops, she proposed a decoupling network. This decoupling network, namely plant-inversion, calculated the times required to generate the i_L that would have the desired values of I_g and I_o . A remarkable property of this solution is that operation modes did not affect the control of the inverter. Analytic equations were used to obtain the control times for triangular and trapezoidal modes based on the shape that i_L should have. The drawback of the implementation of the plant-inversion was that it was designed considering BCM modulation even when the applied modulation was slightly different. In other words, for the control it was assumed that the threshold current could be neglected, but, unfortunately, this was not the case. As a result, the operation of the inverter was affected.

For the control of the inverter, an FPGA was selected. The program used for the digital control of the inverter was developed by Ángel de Castro and Alberto Sánchez in accordance with the implementation of the control.

The contributions of this thesis to the research line are:

1. **The first contribution of this dissertation was to analyze P_{indL} systematically for all possible operation modes of the inverter.** With this analysis, the operation modes $T2$, $T3$, $Tra1$, $Tra2$, and $Th2$ (positive and negative) were found and added to the already existing $T0$, $T1$, $Tra3$, $Tra4$, and $Th1$ (positive and negative again), forming the set of nineteen modes currently in use. The new modes ensured minimum indirect power in the inductor in abnormal V_s conditions and when capacitive or inductive loads were used. Additionally, it ensured that there were no voltages or currents in the ports for which a mode did not exist.

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Once these modes were defined, an interesting property emerged. The boundary of a mode always coincided with the boundary of other modes. This is not a general property of all modulations, but it is specific to the BCM modulation with minimum P_{indL} described in this work. It implied that the evolution of the shape of i_L from a switching cycle to the next changed only slightly, even when a different mode was used. **Obtaining a seamless modulation was among the goals of the analysis of the modulation.**

2. **A second contribution of this work is an in-depth analysis of the ZVS transitions and to find the optimum current for ZVS.** With this analysis, a safe value for I_{th} and the required dead time was set. This analysis can be extended to other topologies and modulations.
3. **The most important contribution of this work was to redefine the TCM modulation of the inverter in such a way that all modes used the states [111] and [000] for ZVS.** This solution was selected as it maintained the seamlessness of the modulation. Moreover, the problems that the BCM modulation had regarding the considerable variations in the switching frequency were also solved. The effects that the threshold current had in the modulation have been studied in detail. The proposed TCM solution enabled full ZVS operation in all conditions and constrained the switching frequency to a reasonable range, which allowed the inverter to operate correctly.

This TCM modulation is not the only possible solution to the previously mentioned issues, as discussed along Section 4.2. Other solutions may have a lower impact on efficiency, but it is most likely that the complexity of the modulation is increased as different solutions should be used for each problem, namely ZVS and low and high switching frequency. The difficulty also lies in the fact that a seamless modulation should be achieved, or a different inversion-based control would have to be proposed. In other words, without a seamless modulation, the calculation of T_{a-h} based on the previous cycle may lead to inaccurate results, and perhaps a different method to obtain T_{a-h} should be proposed. Moreover, if the modulation has abrupt changes, the design of the leakage current filter may have to be redesigned. It should be noted that this TCM modulation is the only solution that has been successfully validated, and, in the author's opinion, the seamless operation along the line cycle was the main reason for the success.

4. Regarding the control of the inverter, **the plant-inversion was redefined to account for the effects of I_{th} in the shape of i_L to ensure a correct operation.** For this purpose, the set of equations that determine the time each state lasts is calculated through a fixed-point iteration. Moreover, as the modulation of the inverter is seamless, the previous switching cycle can be used to set the initial point of the fixed-point iteration. As the initial value is already close to the solution, a single step can be used, greatly simplifying the implementation in the FPGA.
5. One of the main disadvantages of the architecture is the large CM voltage between the input and output ports, which generates leakage current in the parasitic capacitance of PV

panels. **In this dissertation, the leakage current in this topology and the design considerations for the leakage current filter are also discussed.** Nevertheless, further optimization of the different components in the filter is required, with a detailed analysis of the resonances to avoid saturation of the choke. Also, a setup where the leakage current can be properly measured is also required to confirm all the presented analysis.

A large portion of the author's time was dedicated to the validation of these previous contributions. For this purpose, beside all the theoretical analysis and the development of simulations, a hardware prototype was employed. The FPGA code had to be extensively modified to implement for the proposed TCM solution. All the operation modes were redefined to be able to generate the driving signals with a single state machine and to give a single definition for the applied times. Another modification was to add all the calculations related to the proposed plant-inversion with the fixed-point iteration. Useful functionality that allowed for low voltage tests was added. The FPGA implementation is detailed in Appendix D. The author has also collaborated in the development of the PCBs and auxiliary circuitry of the proof-of-concept prototype. Although earlier versions of the prototype were already developed when the Ph.D. begun several modifications have been made since 2015. As for the tests, the author had been in charge of the of the setup and measurements of the inverter, lately with the help of Edwin Peredo. These tests, led to the successful validation of the operation of the inverter at nominal voltage and nominal power.

This dissertation has proven that the proposed modulation can be used to control the output voltage while balancing the input and output power, can keep the switching frequency in a reasonable range, can obtains ZVS in all transitions, and allows for a *conventional* design of the leakage current filter.

8.2 Future work

Overall, this dissertation has detailed the operation of this single-stage inverter with TCM modulation. Nevertheless, several aspects have been omitted in this work, either because it is not fundamental to the operation of the inverter or because it is a part of other Ph.D. candidates' work. The implementation of the control loops and the earlier modulation of the inverter will be described in detail in the thesis of Regina Ramos, and the implementation of the latest prototype and the optimization of magnetic components will be covered in the dissertation of Edwin Peredo.

In this section, the most remarkable future lines are described. First, the future lines of the concepts described in the dissertation are provided, followed by the future work regarding the project in general.

Future improvements on the modulation studied in this work could comprise:

- **Triangular positive and negative modes.** Returning to the discussion of the optimum BCM modulation given in Chapter 2, the operation modes have been constrained to Tra^p , Tra^n , and T modes. This is how the modulation was first conceived in [16]. Anyhow, different types of modes could be proposed, namely, *triangular positive* and *triangular negative* modes, T^p and T^n for short, respectively. T^p is composed of two triangles with positive current as

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it was shown in Figure 2.13 d), and T^n is composed of two triangles with negative current. General aspects of these modes are provided in [82].

To determine if these modes are worth the study, all these possible modes with ZVS in the transitions with $i_L \neq 0$ can be included in the P_{indL} plot of Figure 4.1 described back in Chapter 4. The results for BCM modulation ($I_{th} = 0$) are shown in Figure 8.1. There are T^p and T^n modes that feature lower P_{indL} than the ones currently being used.

Figure 8.1: P_{indL} including T^p and T^n modes for 1 kVA resistive load, for BCM modulation.

Figure 8.2 shows the additional T^p and T^n modes with minimum P_{indL} from the previous plot, and those with minimum P_{indL} for capacitive and inductive loads. $Tp3$ and $Tp4$ could be applied in resistive load while $Tp2$ and $Tp1$ would be required for capacitive and inductive loads only. These modes feature lower indirect power in the inductor compared with Tra modes. It should be noted that the modes cannot replaced directly the trapezoidal modes, and it would lead to different frontiers between modes.

Figure 8.2: T^p and T^n modes in BCM featuring minimum P_{indL} .

Unfortunately, with the proposed inversion-based control and TCM modulation, these modes cannot be implemented. They cannot be represented with the general waveform of Figure 5.4 and ZVS would require four additional states rather than the two used right now. How to implement ZVS in these modes with seamless transitions to T modes remains an open question. It is concluded that these modes are promising, but further study is required.

- Rectifier operation modes.** As the inverter is made with MOSFETs, it can work as a rectifier in theory. For such purpose, not only different control loops would be required, but a different set of operation modes would be needed too. The modulation described in this work is only defined for $I_g > 0$, but the modulation for $I_g < 0$ could be defined as well. The result would be a very similar set of modes with similar boundaries. The modulation with minimum P_{indL} can be obtained by swapping the current direction in the existing modes and reversing the time direction, in other words, advancing from right to left. For instance, the equivalent rectifier mode complementary to $Tra4^+$ would have negative current and the sequence $[001] \rightarrow [011] \rightarrow [111]$. This mode is shown in Figure 8.3 to clarify this concept. The rest of the modes are not depicted as it is just to do a mirror in the horizontal and vertical axis in each mode shown in Figure 4.7.

Figure 8.3: $Tra4^+$ and its complementary mode for rectifier operation, voltage and current limits are included. States are labeled according to the $[dhq]$ nomenclature.

These modes have not been tested as it is out of the scope of the work, but it should be noted that the architecture is not limited to DC-AC conversion.

- Variable threshold current.** P_{indL} increases in the proposed TCM modulation with respect to BCM. In the previous chapter, Table 7.3 also showed that the efficiency dropped when this solution is applied. These drawbacks are expected since the proposed solution consists of adding the states $[111]$ and $[000]$ during $-I_{th} < i_L < I_{th}$, having an average current of zero but increasing the total rms current. More importantly, these states use a fraction of the switching cycle, which leaves less time for actual power processing. This solution was proposed as it tackles several problems of the BCM modulation at once, namely, the lack of ZVS transitions when $i_L = 0$, the minimum frequency tending to zero, the maximum frequency tending to infinity and it maintains the seamless operation. Therefore, this TCM modulation was a relatively simple modification to the BCM modulation that allowed the inverter to work.

Nevertheless, if these problems are overcome with alternative solutions, a dynamically adjusted value of I_{th} would be preferred, using the appropriate value in each specific point of the line cycle, similar to what is proposed in [93]. The problem associated with low switching frequency only happens in specific conditions; there are other points of the line cycle where a lower I_{th} is enough to guarantee ZVS. Also, the high-frequency operation is only a problem at light load, I_{th} could be increased in these special conditions only. It should be clarified that this modification would affect only the threshold level, the additional states $[111]$ and $[000]$ should be maintained to ensure seamless modulation. Therefore, this modification does

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not correspond to the waveforms shown in Figure 7.12, where the states [111] and [000] were removed, and I_{th} was set near $i_{L\ min}(0)$. Also, to ensure seamless modulation, I_{th} should change smoothly from a switching cycle to the next one.

This solution presents several challenges, starting with how to modify I_{th} dynamically, some of the calculations in the FPGA would have to be modified. A solution like this would be exciting if the current required for ZVS is low as the result of a higher value of L or switching devices having lower C_{oss} . In general, this solution would obtain a nearly optimum current shape, but it would require a complete redefinition of the inversion-based control since the equations described in Chapter 5 are not valid.

- **Experimental validation of the delay compensation.** As mentioned in Chapter 5, the main source of error for the inversion-based control is the large delay from the detection of i_L to the response of the gate driver. Fortunately, the solution is relatively simple for constant delays as described in Section 5.4. The compensation could be easily implemented in the FPGA and the current detection circuitry could be simplified, as described in Equation 5.6 and Figure 5.13. However, due to time constraints, this aspect has only been validated in simulation.

Regarding the overall project, the prototype used in this dissertation cannot meet the LBC specifications listed in Section 1.3. As a result, there are more general aspects that need to be addressed:

- **EMI filter.** A crucial part of the design of the final prototype is the design of the DM and CM EMI filters to meet the standard *FCC Part 15 B for unintentional radiators*. In this dissertation, a few comments regarding the interaction of the EMI filter with the leakage current filter are provided. Nevertheless, further study is required to analyze the influence that it can have in the control of the inverter, and the additional volume it will use. The design should account for the parasitic capacitances from different points to chassis of the final inverter.
- **Interleaving.** As mentioned in Chapter 6, one of the earlier ideas was to use two stages of 1 kVA interleaved to reach the 2 kVA specified for the competition. Nevertheless, this idea presents several issues that should be overcome and further analysis on this topic is required. Otherwise, to comply with the specification, the power stage should be redesigned to handle 2 kVA instead.
- **Soft-start, protections and load steps.** To comply with the specifications of the contest, which was the initial goal of the research line, it is required to perform more test and modify the code in the FPGA. All tests so far have been performed increasing the input voltage from zero to the nominal value slowly. However, the inverter should be able to be connected to the input voltage directly. For such purpose the soft-start function and initialization of the control loops should be tested. Moreover, the specification also lists a set of protections and load steps that the converter should withstand. These issues associated with the control of the inverter are not a part of this dissertation and but should be implemented and validated.

- **Optimization and integration.** The prototype used in this thesis was designed to validate the proposed modulation, it has been designed to be handy rather than compact. However, the main goal of this research line was to obtain an inverter with extremely high power density.

Therefore, a last task that should be performed before the research line is over would be to optimize the inverter and build a compact prototype. The optimization should minimize volume while ensuring an efficiency above 95 %. This optimization is very important as it may conclude that $L = 80 \mu\text{H}$ is not the optimum value, and better designs are achievable.

This would allow a fair comparison with the state-of-the-art inverters. But it will not be until this optimum design is found, the EMI filter included, and a compact inverter is built that the comparison with other architectures will be possible and fair.

So far, a very promising prototype achieving very high efficiency has been built. Since this is prototype is not compactly designed, low power density is achieved. Once these last tasks are completed and this concept is turned into a version closer to a product, it will be possible to quantify how good this topology and modulation are for future single-phase inverters for PV applications and whether there are other application or power level where it performs better.

It is important to continue with the research in this specific topology, and, in general, the research in the field of single-stage inverters. These architectures are a promising alternative to two-stage solutions, often reducing the number of components and leading to higher efficiency and power density. In turn, this will support the deployment of more PV systems, helping to drive the energy generation worldwide towards a more renewable and greener scenario.

Minimum current for ZVS in TCM

In Chapter 4, the TCM modulation with the additional states [111] and [000] is described. This appendix is dedicated to obtain the minimum current for ZVS transitions. Only the transitions from the different states to [111] and [000], or from [111] and [000] to the other states are analyzed. The equations and the methodology described in Chapter 3 are used to calculate $i_{L \min}(0)$ based on the nonlinear C_{oss} of the switching devices and the voltage of the three ports [81].

For the analysis, the results for 1 kVA resistive load are discussed first. Then the analysis is extended to the complete operation range for the different operation modes. Only the transitions from any state to [111] with negative current, and from [111] to any other state with positive current are studied. These are the transition labeled as i and ii in Figure 4.19. The results are similar for the transitions from [000] with negative current and to [000] with positive current.

A.1 Minimum current along the line cycle

For resistive load, the operation modes used along the line cycle are $T0$, $T1$, $Tra3$, and $Tra4$ positive and negative. There are different states involved in the transitions with negative current in the inductor in the line cycle, labeled as i Figure 4.19. Those are: $[000 \rightarrow 111]$ for $Tra3^+$ and $Tra4^+$, $[110 \rightarrow 111]$ for $Tra3^-$ and $Tra4^-$, $[011 \rightarrow 111]$ for $T0$ and $T1^+$ and $[010 \rightarrow 111]$ for $T1^-$. These transitions can be analyzed given the voltage in the ports and the value of L and C_{oss} . The minimum current in the inductor before and after the transitions can be calculated following the steps in Figure 3.9. The obtained $i_{L \min}(0)$ and $i_{L \min}(T_{tr})$ are shown in Figure A.1 along the line cycle. In this figure, the shaded area marks when the additional [111] state is applied. The arrows show the time direction, in other words, how is the evolution of the inductor current in the transition.

Figure A.1: Minimum current for ZVS in the transitions from different states to [111] with negative current along the line cycle, for 1 kVA, $L = 80 \mu\text{H}$, and the C_{oss} of two *GS66516T* in parallel per switch.

There are two types of ZVS transitions in this figure, those beginning with $i_L = 0$ and those ending with $i_L = 0$. The former case is represented in the top-right of Figure A.1, it is the case

of the modes $Tra3^+$ and $Tra4^+$. In this case, $v_L(T_{tr}) > 0 > v_L(0)$, therefore, the minimum peak current, $i_{L \min pk}$, is reached before the transition is over. Once $i_{L \min}(T_{tr})$ is reached and ZVS is achieved, the state [111] starts. The latter case, for the other modes, ends with $i_L(T_{tr}) = 0$ because $v_L(T_{tr}) < v_L(0) < 0$. This one is depicted in the bottom-right corner of Figure A.1. A certain current in the inductor is required before the transition to guarantee ZVS. The conclusion obtained from this analysis is that the minimum value at which the transition has to start is slightly above -2.5 A, a value reached at $3\pi/2$ for this load.

For the transition from [111] to any other state, labeled as ii in Figure 4.19, the values of $i_{L \min}(0)$ and $i_{L \min}(T_{tr})$ are shown in Figure A.2 along the line cycle.

Figure A.2: Minimum current for ZVS in the transitions from [111] with positive current, for 1 kVA, $L = 80 \mu\text{H}$, and the C_{oss} of two *GS66516T* in parallel per switch.

There are three types of transitions in this case. The first one is trivial; it is the case of $T1^+$, $Tra3^+$, and $Tra4^+$, where there is no transition because the state after [111] for ZVS is still [111]. The second type of transition is depicted in the top-right part of Figure A.2. The transition starts with $i_L = 0$, then the peak current is reached, and it ends with a certain positive value of $i_L(T_{tr})$. This is the case of the transition $[111 \rightarrow 000]$ for the modes $Tra3^-$ and $Tra4^-$. The process to obtain $i_{L \min}(T_{tr})$ is detailed and exemplified in Section 3.3.2. Finally, there are transitions where the initial and final voltage is positive, and have the shape shown in the bottom-right of Figure A.2. These transitions start with $i_L(0) = 0$ and end with a certain positive inductor current, which is the case of the transitions $[111 \rightarrow 101]$ in modes $T0$ and $T1^-$. From this plot, it is clear that ZVS is always achieved in the ii transitions even when the transition starts with $i_L(0) = 0$.

It is important to note that if the minimum current for ZVS were applied for the modulation, the transitions would start and end with very different values of current in the inductor in different parts of the line cycle. The continuity of the modulation would be compromised and the accuracy of the equations to calculate the time each state last described in Chapter 5 would be inaccurate. Keep in mind that $I_g = 2.5$ for nominal conditions and the variations of current in the transitions are in this range. Therefore, the transitions are far from negligible.

It is also important to clarify that these results are only valid for 1 kVA resistive load, different plots would be obtained for other loads and power factors. Then, an analysis of all the possible operation points is required to obtain the worst-case current for ZVS in all conditions.

A.2 Analysis in the operation range of each mode

In this section, the transitions are analyzed for each mode and the different voltages in the ports. With this analysis, the *worst-case* minimum current ($\max(i_{L \min})$) can be obtained. For this analysis, V_s from 250 V to 400 V is considered, as it is the range where the storage capacitor port

A.2. Analysis in the operation range of each mode

is intended to operate, with some margin. The operation modes $T3$ and $Th2$ are not included in this analysis as they are only applied if V_s is below $V_g/2$. The output voltage is considered in the range -350 V to 350 V. Finally, to avoid a third variable, all the analysis is done assuming V_g constant, with the values 400 V or 450 V as they are the maximum and minimum values for the input voltage. For this analysis, first, the transitions are identified, then the range of V_o where the modes are applied is obtained, and, finally, the minimum current for ZVS is calculated. In other words, $i_{L \min}(0)$ and $i_{L \min}(T_{tr})$ are obtained for the defined V_o range, for V_s between 250 V and 400 V and $V_g = 400$ V and 450 V.

First, the transition from any mode to $[111]$, labeled as i in Figure 4.19 is studied. Identifying the states involved in the transition i is just a matter of finding the last state of each mode in Figure 4.7. In Tra^p modes, this transition is $[000 \rightarrow 111]$ because the last state is the additional $[000]$ for ZVS. In $Tra1^-$, $Tra2^-$, $T2^+$, and $Th1^+$ there is no i transition as the last state is $[111]$ already. These transitions, together with the voltage limits of the modes, are summarized in Table A.1.

Mode	Transition	Voltage limits
$Th1^+$	No transition	$V_g > V_o > V_s$
$Tra4^+$	$[000 \rightarrow 111]$	$V_g > V_o > 0$
$Tra3^+$	$[000 \rightarrow 111]$	$V_g > V_o > 0$
$Tra2^+$	$[000 \rightarrow 111]$	$V_g - V_s > V_o > -V_g$
$Tra1^+$	$[000 \rightarrow 111]$	$V_g - V_s > V_o > -V_g$
$T2^+$	No transition	$V_g > V_o > V_s$
$T1^+$	$[011 \rightarrow 111]$	$V_s > V_o > V_g - V_s$
$T0$	$[011 \rightarrow 111]$	$V_g - V_s > V_o > -V_g + V_s$
$T1^-$	$[010 \rightarrow 111]$	$V_g - V_s > V_o > -V_s$
$T2^-$	$[010 \rightarrow 111]$	$-V_s > V_o > -V_g$
$Tra1^-$	No transition	$V_g > V_o > -V_g + V_s$
$Tra2^-$	No transition	$V_g > V_o > -V_g + V_s$
$Tra3^-$	$[110 \rightarrow 111]$	$0 > V_o > -V_g$
$Tra4^-$	$[110 \rightarrow 111]$	$0 > V_o > -V_g$
$Th1^-$	$[100 \rightarrow 111]$	$-V_s > V_o > -V_g$

Table A.1: Transition i depending on the mode and the voltage limits of the modes.

There are only four possible types of transition i , which are shown later in the first and second columns in Table A.1. Then, $i_{L \min}(0)$ and $i_{L \min}(T_{tr})$ can be obtained for different values of V_g , V_s , and V_o for each one of the transitions.

The current in the transition $[110 \rightarrow 111]$ is plotted against V_o for the two values of V_g in Figure A.3. V_s is not shown as this specific transition is not a function of V_s . The range of V_o is set from -350 V to 0 V as these transitions happen only if $-V_g < V_o < 0$. In the worst case, for $V_g = 450$ V and $V_o = -350$ V the transition has to start with ≈ -2.6 A.

This transition is plotted for different V_s and V_o for $V_g = 400$ V only in Figure A.4 a). It does not depend on V_s , as mentioned before, but it is helpful to understand the following plots. The other four transitions are shown in Figure A.4 b) to e), as a function of V_o and V_s and for $V_g = 400$ V too. In these graphs the minimum of $i_{L \min}(0)$ or $i_{L \min}(T_{tr})$ is plotted, termed $i_{L \text{ ZVS}}$:

$$i_{L \text{ ZVS}} = \min(i_{L \min}(T_{tr}); i_{L \min}(0)) \quad (\text{A.1})$$

Because one of the two values is always zero, only the minimum of the two is of interest for the analysis. The area shaded in blue represents the part where $i_{L \text{ ZVS}} = i_{L \min}(0)$ and the area shaded in yellow represent the values of V_o and V_s where $i_{L \text{ ZVS}} = i_{L \min}(T_{tr})$. Therefore, Figures A.4 a), c) and d) represent $i_{L \min}(0)$, while in Figure A.4 b) and e) both $i_{L \min}(0)$ and

Figure A.3: Minimum current for ZVS in the first transition for $[110 \rightarrow 111]$, for $L = 80 \mu\text{H}$ and the C_{oss} of two *GS66516T* in parallel per switch. $i_{L \min}(T_{tr})$ is not shown because it is 0.

$i_{L \min}(T_{tr})$ are represented together. For instance, in the transition $[000 \rightarrow 111]$ (Figure A.4 e)) the regions with negative V_o mostly represent $i_{L \min}(0)$ as $i_{L \min}(T_{tr}) = 0$. While, for positive values of V_o , $i_{L \min}(T_{tr})$ is represented and $i_{L \min}(0) = 0$. The gray area is outside the operation range where the transition takes place.

This analysis has been repeated for $V_g = 450 \text{ V}$. The results, together with the results in Figure A.4, are used to obtain the worst case current for ZVS for the different i transitions. Those results are summarized in Table A.2.

Transition	Voltage limits		$-i_{L \min}(0)$		$-i_{L \min}(T_{tr})$	
			$V_g=400 \text{ V}$	$V_g=450 \text{ V}$	$V_g=400 \text{ V}$	$V_g=450 \text{ V}$
$[110 \rightarrow 111]$	0	$> V_o > -V_g$	2.5 A	2.6 A	—	—
$[011 \rightarrow 111]$	V_s	$> V_o > -V_g + V_s$	1.0 A	1.2 A	1.4 A	1.5 A
$[010 \rightarrow 111]$	$V_g - V_s$	$> V_o > -V_g$	2.5 A	2.2 A	—	0.1 A
$[000 \rightarrow 111]$	V_g	$> V_o > -V_g$	2.1 A	2.2 A	2.5 A	2.3 A
$[100 \rightarrow 111]$	$-V_s$	$> V_o > -V_g$	1.8 A	1.9 A	—	—

Table A.2: Worst-case current for ZVS in the transition i , for $L = 80 \mu\text{H}$ and the C_{oss} of two *GS66516T* in parallel per switch.

The minimum among the worst-case points is $i_{L \min}(0) \approx -2.6 \text{ A}$, reached in the transition $[110 \rightarrow 111]$ shown in Figure A.3. It should be noted that sometimes transitions with $V_g = 400 \text{ V}$ require less current than transitions with $V_g = 450 \text{ V}$. For this reason, both cases of V_g are considered.

The same analysis is repeated for the transition labeled as ii in Figure 4.19. Those are the transitions with positive current starting with $[111]$. This time, to avoid repetition, only the final results are included. The possible transitions and range of voltage where they are applied are found in the first and second columns of Table A.3. The other columns show the maximum values of $i_{L \min}(0)$ and $i_{L \min}(T_{tr})$ for $V_g = 400 \text{ V}$ and $V_g = 450 \text{ V}$.

For this transition, the worst initial current is 2.1 A, obtained in the $Tra1^-$ mode when $V_o = V_s$ and $V_g = 450 \text{ V}$. The most restrictive transition not in terms of ZVS but accuracy is $[111 \rightarrow 101]$, where the current reach 3.3 A for $i_L(0) = 0$, which is the largest increment of current during the transition in this inverter.

Since transitions iii and iv in Figure 4.19 are symmetric to those presented already, there is no need to obtain their values, the transition iii gives the same results as transition i but for positive current, and the iv the same result as in ii but with negative current.

Figure A.4: Minimum current for ZVS in the i transition as a function of V_s and V_o for $V_g = 400$ V, again for $L = 80$ μ H and the C_{oss} of two *GS66516T* in parallel per switch.

A.3 Conclusion

To conclude this appendix, the minimum value for I_{th} for the TCM modulation proposed in Chapter 4 has to be set to 2.6 A to ensure ZVS transitions in the worst-case scenario. Moreover, 2.6 A is just the lower limits, a larger value is recommended to allow for tolerances in the inductor and the capacitances, or to account for delays from the detection. A larger value is also recommended to improve the accuracy of the inversion-based control from Chapter 5 since it implies a lower difference between $i_L(0)$ and $i_L(T_{tr})$.

Transition	Voltage limits	$i_{L \min}(0)$		$i_{L \min}(T_{tr})$	
		$V_g=400$ V	$V_g=450$ V	$V_g=400$ V	$V_g=450$ V
[111 $\rightarrow$ 101]	$V_g - V_s > V_o > -V_s$	—	—	3.3 A	3.4 A
[111 $\rightarrow$ 100]	$-V_s > V_o > -V_g$	—	—	2.5 A	2.6 A
[111 $\rightarrow$ 000]	$V_s > V_o > -V_g$	1.9 A	2.1 A	2.5 A	2.3 A
[111 $\rightarrow$ 010]	$-V_s > V_o > -V_g$	—	—	1.9 A	1.9 A

Table A.3: Worst-case current for ZVS in the transition ii , for $L = 80$ μ H and the C_{oss} of two *GS66516T* in parallel per switch.

Control times for BCM modulation

In this appendix, the relationship between the times each state lasts and the currents and voltages in the ports is obtained for BCM modulation. The analysis is a generalization of the work of Regina Ramos for each specific type of mode [40]. With BCM modulation, the operation modes start and end with $i_L = 0$ ($I_{th} = 0$). For the analysis, the following assumptions are considered:

- The inverter is assumed lossless, therefore, the sum of the power in the three ports is zero, $P_g + P_s + P_o = 0$. As a result, the storage capacitor current is given by:

$$I_s = \frac{V_o}{V_s} I_o - \frac{V_g}{V_s} I_g \quad (\text{B.1})$$

- The transitions between states are not considered: the dead time is neglected and the change in i_L along transitions is neglected too.
- It is assumed that the voltage in the ports is constant along the switching cycle, as in [90]. The resonance between the inductor and the input, output, and storage capacitor is not considered. This is valid if the switching frequency is much higher than the resonant frequency.

B.1 General representation valid for all modes

This appendix also introduces a representation for the inductor current waveform valid for all modes. This representation makes the analysis general so there is no need to obtain the relationships for each one of the nineteen modes separately. This concept was already introduced in Section 2.2.2, where T , Tra^p , and Tra^n modes are represented according to the shapes regardless of the specific mode used (see Figure 2.11). The result of combining these three waveforms in a single one is shown in Figure B.1 a). The waveform is divided into six states. The time each one lasts is T_1 to T_6 , or simply $\mathbf{T_{1-6}}$. As discussed in Chapter 5, $\mathbf{T_{1-6}}$ is referred to as *control times*. $\mathbf{I_{1-6}}$ is the average current of each one of the six states divided over the complete switching cycle. In other words, these currents are the shaded area in gray of each state, which represents the charge over the switching cycle, T . The slopes of the inductor current in the different states are termed $\mathbf{m_{1-6}}$, which are the voltages applied to the inductor over the inductance value. And, finally, i_{12} , i_{23} , i_{45} , and i_{56} are the instantaneous values of the current in the transitions between states. With this nomenclature, I_1 , I_2 , and I_3 are always positive and I_4 , I_5 , and I_6 negative. Also, m_1 and m_6 are always positive and m_3 and m_4 negative, m_2 and m_5 can be positive or negative. Accordingly, the shape of a Tra^p , Tra^n , and T modes is represented in Figure B.1 b), c) and d), respectively. Note that in T modes, the second and fifth states are skipped.

There are certain relations between the currents, the slopes, and the times that are useful to obtain $\mathbf{T_{1-6}}$ as a function of the port variables. First, from the fact that $i_L = 0$ at the beginning of the switching cycle and between the third and fourth states, the following equations associated with the BCM operation are always valid:

Figure B.1: Representation of the inductor current waveform valid for all modes, divided into six states, and showing the variables used in the analysis, a) complete waveform, b) waveform when T_3 , T_4 , and T_6 are zero, c) waveform when $T_1 = T_2 = T_3 = 0$, c) when $T_2 = T_5 = 0$.

$$m_1 \cdot T_1 + m_2 \cdot T_2 + m_3 \cdot T_3 = 0 \quad m_4 \cdot T_4 + m_5 \cdot T_5 + m_6 \cdot T_6 = 0 \quad (\text{B.2})$$

The current in the transitions between states are given by:

$$\begin{aligned} i_{12} &= m_1 \cdot T_1 = -m_2 \cdot T_2 - m_3 \cdot T_3 & i_{23} &= m_1 \cdot T_1 + m_2 \cdot T_2 = -m_3 \cdot T_3 \\ i_{45} &= m_4 \cdot T_4 = -m_5 \cdot T_5 + m_6 \cdot T_6 & i_{56} &= m_4 \cdot T_4 + m_5 \cdot T_5 = -m_6 \cdot T_6 \end{aligned} \quad (\text{B.3})$$

There are two possible definitions because of the relations in Equation B.2. The solutions that do not require m_2 and m_5 are used because T modes do not have m_2 and m_5 , this is:

$$i_{12} = m_1 \cdot T_1 \quad i_{23} = -m_3 \cdot T_3 \quad i_{45} = m_4 \cdot T_4 \quad i_{56} = -m_6 \cdot T_6 \quad (\text{B.4})$$

With the current in the transitions, the average current in the states can be calculated as:

$$I_1 = \frac{T_1}{T} \frac{i_{12}}{2} \quad I_2 = \frac{T_2}{T} \frac{i_{12} + i_{23}}{2} \quad I_3 = \frac{T_3}{T} \frac{i_{23}}{2} \quad I_4 = \frac{T_4}{T} \frac{i_{45}}{2} \quad I_5 = \frac{T_5}{T} \frac{i_{45} + i_{56}}{2} \quad I_6 = \frac{T_6}{T} \frac{i_{56}}{2} \quad (\text{B.5})$$

Where $T = T_1 + T_2 + T_3 + T_4 + T_5 + T_6$.

B.1.1 Relation with the voltages and currents in the three ports

Equations B.2, B.4, and B.5 relate the variables of the waveform shown in Figure B.1 a). The second part of this analysis is to relate the variables of the six states with the voltages and currents in the ports, to calculate T_{1-6} . Recalling from Chapter 2, states were defined according to the $[g \ s]$ nomenclature. Depending on how the ports are connected to the inductor, g and s take

B.1. General representation valid for all modes

the values -1 , 0 , or 1 for each state. Therefore, for each mode, there is a different combination of $\mathbf{g}_{1-6}$ and $\mathbf{s}_{1-6}$. The voltage in the ports directly related to the slope of each state through Equation 2.11 as:

$$\mathbf{m}_{1-6} = \frac{1}{L} (\mathbf{g}_{1-6} \cdot V_g + \mathbf{s}_{1-6} \cdot V_s - V_o) \quad (\text{B.6})$$

The matrix that relates $\mathbf{I}_{1-6}$ with the current in the three ports is:

$$\begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} = \begin{bmatrix} g_1 & g_2 & g_3 & g_4 & g_5 & g_6 \\ s_1 & s_2 & s_3 & s_4 & s_5 & s_6 \\ 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \\ I_5 \\ I_6 \end{bmatrix} \quad (\text{B.7})$$

Unfortunately, there is no inverse for this matrix, meaning that $\mathbf{I}_{1-6}$ cannot be calculated as a function of I_g , I_s , or I_o directly. Therefore, to associate the current in the states and the current in the ports T , Tra^p , and Tra^n modes must be studied separately, as done in Section 2.2.2.

Current in trapezoidal modes

The relation between the currents in the three ports and the current in the three states for Tra^p modes was obtained in Section 2.2.2.1 based on Equation 2.14. It consists of obtaining the inverse matrix of Equation B.7 once states four, five, and six are eliminated. The inverse is repeated here for completeness:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \frac{\begin{bmatrix} s_2 - s_3 & g_3 - g_2 & g_2 \cdot s_3 - g_3 \cdot s_2 \\ s_3 - s_1 & g_1 - g_3 & g_3 \cdot s_1 - g_1 \cdot s_3 \\ s_1 - s_2 & g_2 - g_1 & g_1 \cdot s_2 - g_2 \cdot s_1 \end{bmatrix}}{g_1 \cdot s_2 + g_2 \cdot s_3 + g_3 \cdot s_1 - g_3 \cdot s_2 - g_2 \cdot s_1 - g_1 \cdot s_3} \cdot \begin{bmatrix} I_g \\ I_s \\ I_o \end{bmatrix} \quad (\text{B.8})$$

A similar result is obtained for Tra^n modes. The solution for Tra^n modes is obtained by replacing states one to three in Equation B.8 with states four to six. The specific solution of this equation for the four Tra^p modes and the four Tra^n modes as a function of I_g , I_s , and I_o is included in Chapter 5 in Table D.1.

Current in triangular modes

For T modes, the inverse matrix was obtained in Chapter 2. Here it is clarified using the new nomenclature for the states. In T modes, $i_{12} = i_{23}$, labeled i_{13} in Figure B.1 d). Also, $i_{45} = i_{56}$, labeled i_{46} . Since I_1 and I_3 are calculated using i_{13} in Equation B.5, and I_4 and I_6 use i_{46} , the following relationships are obtained:

$$\frac{I_1}{T_1} = \frac{I_3}{T_3} \quad \frac{I_4}{T_4} = \frac{I_6}{T_6} \quad (\text{B.9})$$

Moreover, since the second and fifth states are not used, Equation B.2 becomes $m_1 \cdot T_1 + m_3 \cdot T_3 = 0$ and $m_4 \cdot T_4 + m_6 \cdot T_6 = 0$. Combined with Equation B.9, an important relation between the currents and the slopes in T modes is obtained:

$$\frac{I_1}{m_1} = -\frac{I_3}{m_3} \quad \frac{I_4}{m_4} = -\frac{I_6}{m_6} \quad (\text{B.10})$$

In Figure B.1 b), I_{13} is defined as $I_1 + I_3$ and $I_{46} = I_4 + I_6$. These values are used as it simplifies the relation with the port currents. As for the times, $T_{13} = T_1 + T_3$ and $T_{46} = T_4 + T_6$. With these definitions, the following relations are obtained:

$$\begin{aligned} I_{13} &= I_1 \left(1 - \frac{m_1}{m_3}\right) = I_3 \left(1 - \frac{m_3}{m_1}\right) & I_{46} &= I_4 \left(1 - \frac{m_4}{m_6}\right) = I_6 \left(1 - \frac{m_6}{m_4}\right) \\ T_{13} &= T_1 \left(1 - \frac{m_1}{m_3}\right) = T_3 \left(1 - \frac{m_3}{m_1}\right) & T_{46} &= T_4 \left(1 - \frac{m_4}{m_6}\right) = T_6 \left(1 - \frac{m_6}{m_4}\right) \end{aligned} \quad (\text{B.11})$$

To obtain the relation between the current in the ports and the current in the states, Equation B.7 without the second and fifth states (this is, the former Equation 2.18) cannot be directly used as it is not a square matrix. The solution is to solve for I_{13} and I_{46} and remove I_s to obtain a $2 \cdot 2$ matrix, as done in Section 2.2.2.2. The inverse of this matrix is given by:

$$\begin{bmatrix} I_{13} \\ I_{46} \end{bmatrix} = \frac{\begin{bmatrix} (m_6 - m_4) \cdot (m_3 - m_1) & -(m_6 \cdot g_4 - m_4 \cdot g_6) \cdot (m_3 - m_1) \\ -(m_6 - m_4) \cdot (m_3 - m_1) & (m_3 \cdot g_1 - m_1 \cdot g_3) \cdot (m_6 - m_4) \end{bmatrix}}{\begin{bmatrix} (m_3 \cdot g_1 - m_1 \cdot g_3) \cdot (m_6 - m_4) & -(m_6 \cdot g_4 - m_4 \cdot g_6) \cdot (m_3 - m_1) \end{bmatrix}} \cdot \begin{bmatrix} I_g \\ I_o \end{bmatrix} \quad (\text{B.12})$$

This equation, together with the relation between I_{13} and I_1 and I_3 , and the relation between I_{46} and I_4 and I_6 from Equation B.11 is used to obtain the state currents as a function of the currents and voltages in the ports. The results for the operation modes considered in this work are summarized in Table D.1.

B.2 General solution for the control times

According to the previous discussion, $\mathbf{I}_{1-6}$ and $\mathbf{m}_{1-6}$ are related to the port currents and voltages through equations that do not involve $\mathbf{T}_{1-6}$. Once $\mathbf{I}_{1-6}$ and $\mathbf{m}_{1-6}$ are defined depending on the type of mode, the last part of the analysis is to obtain $\mathbf{T}_{1-6}$ as a function of $\mathbf{m}_{1-6}$ and $\mathbf{I}_{1-6}$. The advantage of this procedure is that in this last step $\mathbf{g}_{1-6}$ and $\mathbf{s}_{1-6}$ are not required.

Elaborating Equation B.5, the following relation only involving $\mathbf{I}_{1-6}$ and $\mathbf{m}_{1-6}$ is obtained:

$$\begin{cases} I_1 = \frac{T_1}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{m_1 \cdot T_1}{2} \\ I_2 = \frac{T_2}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{m_1 \cdot T_1 - m_3 \cdot T_3}{2} \\ I_3 = \frac{T_3}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{-m_3 \cdot T_3}{2} \\ I_4 = \frac{T_4}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{m_4 \cdot T_4}{2} \\ I_5 = \frac{T_5}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{m_4 \cdot T_4 - m_6 \cdot T_6}{2} \\ I_6 = \frac{T_6}{T_1+T_2+T_3+T_4+T_5+T_6} \frac{-m_6 \cdot T_6}{2} \end{cases} \quad (\text{B.13})$$

As this system of equations is nonlinear, obtaining an analytic solution for $\mathbf{T}_{1-6}$ is not straightforward. This equation also helps to understand the effects of changing from BCM modulation to TCM modulation discussed in the following appendix.

Only four equations are required to obtain an analytic solution since T_2 and T_5 can be obtained from the relation with the other times using Equation B.2. Moreover, Equation B.2 could be used to remove T_2 and T_5 from the denominators in Equation B.13. However, it is more convenient to use the following relations obtained from Equation B.13 as they do not depend on m_2 and m_5 :

$$I_2 = I_1 \frac{T_2}{T_1} + I_3 \frac{T_2}{T_3} \quad I_5 = I_4 \frac{T_5}{T_4} + I_6 \frac{T_5}{T_6} \quad (\text{B.14})$$

Removing T_2 and T_5 and using the previous equation, the problem to solve can be stated as:

$$\begin{cases} m_1 \cdot T_1^2 = +2 \cdot I_1 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 + T_4 + \frac{I_5 \cdot T_4 \cdot T_6}{I_4 \cdot T_6 + I_6 \cdot T_4} + T_6 \right) \\ m_3 \cdot T_3^2 = -2 \cdot I_3 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 + T_4 + \frac{I_5 \cdot T_4 \cdot T_6}{I_4 \cdot T_6 + I_6 \cdot T_4} + T_6 \right) \\ m_4 \cdot T_4^2 = +2 \cdot I_4 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 + T_4 + \frac{I_5 \cdot T_4 \cdot T_6}{I_4 \cdot T_6 + I_6 \cdot T_4} + T_6 \right) \\ m_6 \cdot T_6^2 = -2 \cdot I_6 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 + T_4 + \frac{I_5 \cdot T_4 \cdot T_6}{I_4 \cdot T_6 + I_6 \cdot T_4} + T_6 \right) \end{cases} \quad (\text{B.15})$$

B.3. Conclusion

From this equation, the following relationships are obtained:

$$\frac{T_1}{T_3} = \sqrt{-\frac{I_1}{I_3} \frac{m_3}{m_1}} \quad \frac{T_4}{T_6} = \sqrt{-\frac{I_4}{I_6} \frac{m_6}{m_4}} \quad (\text{B.16})$$

With these relations, Equation B.15 can be turned into a system of two equations. Nevertheless, the obtain the solution is complicated. This is not difficult when applied to T or Tra modes separately, as done in [40]. The results are repeated below for completeness.

Specific solution for trapezoidal modes

For Tra^p modes, since I_4 , I_5 and I_6 are equal to 0, Equation B.15 becomes:

$$\begin{cases} m_1 \cdot T_1^2 = +2 \cdot I_1 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 \right) \\ m_3 \cdot T_3^2 = -2 \cdot I_3 \left(T_1 + \frac{I_2 \cdot T_1 \cdot T_3}{I_1 \cdot T_3 + I_3 \cdot T_1} + T_3 \right) \end{cases} \quad (\text{B.17})$$

T_1 and T_3 are easy obtained using the relation in Equation B.16, in this case leading to:

$$\begin{aligned} T_1 &= 2 \sqrt{\frac{I_1}{m_1}} \left(\sqrt{\frac{I_1}{m_1}} + \sqrt{\frac{I_3}{-m_3}} + \frac{I_2}{\sqrt{-m_3 I_3 + \sqrt{m_1 I_1}}} \right) \\ T_3 &= 2 \sqrt{\frac{I_3}{-m_3}} \left(\sqrt{\frac{I_1}{m_1}} + \sqrt{\frac{I_3}{-m_3}} + \frac{I_2}{\sqrt{-m_3 I_3 + \sqrt{m_1 I_1}}} \right) \end{aligned} \quad (\text{B.18})$$

T_2 is then obtained through $T_2 = I_2 / (I_1/T_1 + I_3/T_3)$. A similar solution is obtained for Tra^n modes. This equation has been implemented in *Matlab* to obtain the frequency of the BCM modulation in Figure 4.15.

Specific solution for triangular modes

Equation B.15 for T modes can be simplified using I_{13} in the first equation and I_{46} in the third, resulting in:

$$\begin{cases} \frac{m_1 \cdot m_3}{m_3 - m_1} T_{13}^2 = 2 \cdot I_{13} (T_{13} + T_{46}) \\ \frac{m_4 \cdot m_6}{m_6 - m_4} T_{46}^2 = 2 \cdot I_{46} (T_{13} + T_{46}) \end{cases} \quad (\text{B.19})$$

For the control times, rearranging from Equation B.19, and after a few steps, the following equations are obtained:

$$\begin{aligned} T_{13} &= 2 \cdot I_{13} \left(\frac{m_3 - m_1}{m_1 \cdot m_3} + \sqrt{\frac{I_{46}}{I_{13}} \frac{m_3 - m_1}{m_1 \cdot m_3} \frac{m_6 - m_4}{m_4 \cdot m_6}} \right) \\ T_{46} &= 2 \cdot I_{46} \left(\frac{m_6 - m_4}{m_4 \cdot m_6} - \sqrt{\frac{I_{13}}{I_{46}} \frac{m_3 - m_1}{m_1 \cdot m_3} \frac{m_6 - m_4}{m_4 \cdot m_6}} \right) \end{aligned} \quad (\text{B.20})$$

T_{1-6} is obtained using Equation B.11. Equation B.20 has been used to draw Figure 4.15, together with the equation for Tra modes.

B.3 Conclusion

This appendix is included to show how times are calculated when BCM modulation is used, based on [40]. The analysis shows that it is convenient to obtain the slopes and current in the states as a function of the ports voltages and currents and $\mathbf{g}_{1-6}$ and $\mathbf{s}_{1-6}$ first, and then to relate $\mathbf{I}_{1-6}$ and $\mathbf{m}_{1-6}$ with $\mathbf{T}_{1-6}$. Moreover, this appendix has shown that it is complex to obtain analytic solutions to the equations to obtain $\mathbf{T}_{1-6}$. In both T and Tra modes, the analytic solution requires fractions and square roots, this is not a problem for a *Matlab* script, but it is a severe complication when considering the implementation in an FPGA discussed in Appendix D. For such purposes, numeric methods are more feasible.

Control times for TCM modulation

The goal of this appendix is to obtain the relationship between the voltage and current in the three ports and the control times, $\mathbf{T}_{1-6}$, for the TCM modulation. It is the same analysis described in the previous appendix, but for $I_{th} \neq 0$, which is a more detailed version of the explanation in [87]. The same assumptions as in the previous appendix are used: lossless inverter, ZVS transitions neglected, and constant voltage in the port in the switching cycle. Additionally, the delay from the detection event to the switching event discussed in Section 5.4 is not considered.

As in Appendix B, first, the current and slopes for the different states are related to the voltages and current in the ports. With this information, the control times can be related to the slopes and currents of each state later. It could be possible to obtain equations for $\mathbf{T}_{1-6}$ for every single operation mode or type of mode, however, it is more useful to solve the problem generally. Figure C.1 a) shows the inductor current waveform valid for all modes, including the states [111] and [000] between I_{th} and $-I_{th}$ for ZVS. This waveform represents the modulation with the proposed modification for ZVS described in Section 4.4. As in Figure B.1, states are numbered from one to six, and the same variables are used. The additional states last T_{np} and T_{pn} , as shown in Figure 4.19, and their values are given by Equation 4.1. With this representation, Tra^p modes have the shape shown in Figure C.1 b) and T modes the shape of Figure C.1 c).

The equations that relate the different values of the waveform are slightly different when I_{th} is considered, although some equations of the previous appendix, when $I_{th} = 0$, remain valid. For instance, Equation B.2 is still valid because the inductor current has the same value at the beginning of state 1 and the end of state 3. Also, the current at the beginning of state 4 is equal to the current at the end of state 6.

However, the current in the transitions are different, when I_{th} is considered they are given by:

$$i_{12} = I_{th} + m_1 \cdot T_1 \quad i_{23} = I_{th} - m_3 \cdot T_3 \quad i_{45} = -I_{th} + m_4 \cdot T_4 \quad i_{56} = -I_{th} - m_6 \cdot T_6 \quad (C.1)$$

Also, the current in the different states is different because of the effect of I_{th} :

$$\begin{aligned} I_1 &= \frac{T_1}{T} \frac{I_{th} + i_{12}}{2} & I_2 &= \frac{T_2}{T} \frac{i_{12} + i_{23}}{2} & I_3 &= \frac{T_3}{T} \frac{I_{th} + i_{23}}{2} \\ I_4 &= \frac{T_4}{T} \frac{-I_{th} + i_{45}}{2} & I_5 &= \frac{T_5}{T} \frac{i_{45} + i_{56}}{2} & I_6 &= \frac{T_6}{T} \frac{-I_{th} + i_{56}}{2} \end{aligned} \quad (C.2)$$

Where T is now equal to $T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6$, T_{pn} is given by $2 \cdot I_{th} \cdot L / (V_g - V_o)$ and $T_{np} = 2 \cdot I_{th} \cdot L / (V_g + V_o)$ from Equation 4.1. The relation of the slopes and current in the different states with the variables in the three ports given in the previous appendix remain valid even when I_{th} is considered. Equation B.6 gives the slopes, and the matrix in Equation B.7 gives the current in each state. This matrix is valid since the current in the states added for ZVS is between $-I_{th}$ and I_{th} . Therefore, these states do not contribute to the net current of the ports, as discussed in Section 4.4. As a consequence, Table D.1 is also valid when I_{th} is considered.

Therefore, $\mathbf{m}_{1-6}$ and $\mathbf{I}_{1-6}$ can be calculated from V_g , V_s , V_o , I_g , I_s , and I_o . Again, the last step, and the complicated one, is to relate the slopes and currents with the control times, $\mathbf{T}_{1-6}$. Using the values in Equations C.1 in Equation C.2, the problem to solve can be stated as:

Figure C.1: Generic representation for the inductor current waveform valid for all modes when I_{th} is considered, a) complete representation, b) representation for Tra^p modes ($T_4 = T_5 = T_6 = 0$), c) for T modes ($T_2 = T_5 = 0$).

$$\begin{cases} I_1 = \frac{T_1}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{2I_{th}+m_1 \cdot T_1}{2} \\ I_2 = \frac{T_2}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{2I_{th}+m_1 \cdot T_1 - m_3 \cdot T_3}{2} \\ I_3 = \frac{T_3}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{2I_{th}-m_3 \cdot T_3}{2} \\ I_4 = \frac{T_4}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{-2I_{th}+m_4 \cdot T_4}{2} \\ I_5 = \frac{T_5}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{-2I_{th}+m_4 \cdot T_4 - m_6 \cdot T_6}{2} \\ I_6 = \frac{T_6}{T_{np}+T_1+T_2+T_3+T_{pn}+T_4+T_5+T_6} \frac{-2I_{th}-m_6 \cdot T_6}{2} \end{cases} \quad (C.3)$$

Although it is similar to Equation B.13, it is more complex because of the terms I_{th} , T_{np} and T_{pn} . The problem is that analytically solving this system of equations is not feasible. To begin with, the relations of Equation B.14 and B.16 are no longer valid. Even when the problem is restricted to different types of modes, the problem is still complex. For instance, for Tra^p modes, using the relation $m_1 \cdot T_1 + m_2 \cdot T_2 + m_3 \cdot T_3 = 0$ (Equation B.2) to remove T_2 leads to:

$$\begin{cases} I_1 = \frac{T_1}{T_{np}+T_1 \left(1 - \frac{m_1}{m_2}\right) + T_3 \left(1 - \frac{m_3}{m_2}\right) + T_{pn}} \frac{2I_{th}+m_1 \cdot T_1}{2} \\ I_3 = \frac{T_3}{T_{np}+T_1 \left(1 - \frac{m_1}{m_2}\right) + T_3 \left(1 - \frac{m_3}{m_2}\right) + T_{pn}} \frac{2I_{th}-m_3 \cdot T_3}{2} \end{cases} \quad (C.4)$$

When T modes are considered Equation C.3 becomes:

C.1. Iterative methods

$$\begin{cases} I_{13} = \frac{T_{13}}{T_{np}+T_{13}+T_{pn}+T_{46}} \frac{2I_{th}+T_{13} \frac{m_1 \cdot m_3}{m_3-m_1}}{2} \\ I_{46} = \frac{T_{46}}{T_{np}+T_{13}+T_{pn}+T_{46}} \frac{-2I_{th}+T_{46} \frac{m_4 \cdot m_6}{m_6-m_4}}{2} \end{cases} \quad (C.5)$$

In both systems of equations, obtaining the control time analytically is complicated and not practical. Numerical methods should be used instead.

C.1 Iterative methods

Numerical methods can be used to solve Equation C.3. It is preferred to solve Equation C.3 instead of Equations C.4 and C.5 separately to simplify the implementation. Another advantage of solving Equation C.3 is that the error (always present when numerical approaches are used) would be independent of the mode selected. The goal is then to solve a system of six nonlinear equations, where all the equations have the form:

$$I_i = \frac{T_i}{T} \frac{i_{i-1,i} + i_{i,i+1}}{2} \quad (C.6)$$

For $i \in [1, 6]$, and where $i_{i-1,i}$ and $i_{i,i+1}$ are the inductor currents before and after the state i respectively, which are either the threshold currents or given in Equation C.1 ($i_{0,1} = I_{th}$, $i_{1,2} = i_{12}$, $i_{2,3} = i_{23}$ and so on). Note that T , $i_{i-1,i}$ and $i_{i,i+1}$ are a function of T_i . Many iterative processes can be used to solve nonlinear systems of equations [92]. In this section, the iterative methods that have been considered are briefly discussed.

C.1.1 Newton's method

Newton's method is generally used when it comes to this type of problem [92], [116]. The equation that has to be solved is defined as $\mathbf{f}(\mathbf{T}_{1-6}) = \mathbf{0}$, obtained by making Equations C.3 equal to 0. $\mathbf{f}(\mathbf{T}_{1-6})$ is composed of six equations with six variables, namely $f_1(T_{1-6})$ to $f_6(T_{1-6})$. The Newton's method to calculate $\mathbf{T}_{1-6}^{[n+1]}$ from $\mathbf{T}_{1-6}^{[n]}$ is defined as:

$$\mathbf{T}_{1-6}^{[n+1]} = \mathbf{T}_{1-6}^{[n]} - \mathbf{J}(\mathbf{f})|_{\mathbf{T}_{1-6}^{[n]}}^{-1} \cdot \mathbf{f}|_{\mathbf{T}_{1-6}^{[n]}} \quad (C.7)$$

Where $[n]$ is the iteration number and $\mathbf{J}(\mathbf{f})$ is the Jacobian matrix, a $6 \cdot 6$ matrix where each element is defined as $J_{ij} = \partial f_i / \partial T_j$. A possible way to define the function for the iteration comes directly from Equation C.6, as:

$$f_i(\mathbf{T}_{1-6}) = \frac{T_i}{T} \frac{i_{i-1,i} + i_{i,i+1}}{2} - I_i = 0 \quad (C.8)$$

However, with this definition, the Jacobian matrix is complex as the partial derivatives require a lot of operations on their own; for instance, $\partial f_1 / \partial T_1$ is:

$$\frac{\partial f_1}{\partial T_1} = \frac{\frac{m_1}{2} T_1^2 + (T_{np} + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6) (m_1 \cdot T_1 + I_{th})}{(T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6)^2} \quad (C.9)$$

Obtaining in real-time the inverse of a matrix like this is very complex. Therefore, a different method should be considered.

There are several iteration methods based on Newton's method. The *gradient descent method* is not advised as it requires the Jacobian matrix as well. Other methods that could be used are the *Broyden's method*, the *Chord method*, *Regula Falsi*, yet, a very straightforward one is the *Fixed-point* method, so it is the one considered in this work [92]. Further study of these methods is

beyond the scope of this work, as the objective is to find a practical and straightforward solution for Equation C.3.

C.1.2 Fixed-point iteration

The goal of fixed-point methods is to solve $\mathbf{T}_{1-6} = \mathbf{g}(\mathbf{T}_{1-6})$ through a series of iterations, $\mathbf{T}_{1-6}^{[n+1]} = \mathbf{g}(\mathbf{T}_{1-6}^{[n]})$ [92]. $\mathbf{T}_{1-6}^{[0]}$ is the initial point from which the iteration is started. Nevertheless, the complexity of the problem lies in the fact that there are infinite ways Equation 5.2 can be expressed as $\mathbf{T}_{1-6} = \mathbf{g}(\mathbf{T}_{1-6})$, and convergence depends on the method selected and the initial values. Only $\mathbf{g}(\mathbf{T}_{1-6})$ requiring simple equations and without square roots are considered. In Equation C.6, T_i appears in three different places, in the denominator as a part of T , in the numerator independently, or in the current $i_{i-1,i}$ or $i_{i,i+1}$. Three equations for $\mathbf{T}_{1-6} = \mathbf{g}(\mathbf{T}_{1-6})$ are obtained solving for each of the T_i described above:

- **a**: solving for T_i in the denominator, $\mathbf{g}(\mathbf{T}_{1-6})$ would take the form:

$$\begin{aligned} T_1 &= \frac{T_1}{I_1} \frac{2 \cdot I_{th} + m_1 \cdot T_1}{2} - (T_{np} + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6) \\ T_2 &= \frac{T_2}{I_2} \frac{2 \cdot I_{th} + m_1 \cdot T_1 - m_3 \cdot T_3}{2} - (T_{np} + T_1 + T_3 + T_{pn} + T_4 + T_5 + T_6) \\ T_3 &= \dots \quad T_4 = \dots \quad T_5 = \dots \quad T_6 = \dots \end{aligned} \quad (C.10)$$

- **b**: if the equation is solved for T_i in the numerator, the resulting equations are:

$$\begin{aligned} T_1 &= 2 \cdot I_1 \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{2 \cdot I_{th} + m_1 \cdot T_1} \\ T_2 &= 2 \cdot I_2 \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{2 \cdot I_{th} + m_1 \cdot T_1 - m_3 \cdot T_3} \\ T_3 &= \dots \quad T_4 = \dots \quad T_5 = \dots \quad T_6 = \dots \end{aligned} \quad (C.11)$$

- **c**: finally, solving for the times that appear in $i_{i-1,i}$ and $i_{i,i+1}$ leads to:

$$\begin{aligned} T_1 &= \frac{2 \cdot I_1}{m_1} \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{T_3} - \frac{2 \cdot I_{th}}{m_1} \\ T_3 &= -\frac{2 \cdot I_3}{m_3} \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{T_3} + \frac{2 \cdot I_{th}}{m_3} \\ T_4 &= \dots \quad T_6 = \dots \end{aligned} \quad (C.12)$$

However, in this last case T_2 and T_5 cannot be directly obtained as they are not a part of $i_{i-1,i}$ and $i_{i,i+1}$. Then, T_2 and T_5 would have to be obtained after the iteration process.

This last case is less attractive as it requires an extra step to obtain T_2 and T_5 . There are more options to write $\mathbf{g}(\mathbf{T}_{1-6})$, yet, for simplicity, options **a** and **b** are analyzed first. To determine which is the best method to apply some practical considerations should be taken into account. The iteration should work when one of the calculated times tends to zero. For instance, for iterations starting with $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$, in **a** the first iteration would lead to negative values for the times while in **b** it leads to positive ones, so **b** seems a better solution. The iteration should also be valid when one of the average currents in a state (I_i) is zero. In case **a** the denominator of the iteration is 0, and although the state lasts zero, the result is a 0/0 situation that may be troubling when it comes to the implementation. In case **b** when $I_i = 0$, $T_i = 0$, which is what should happen. Finally, as I_{th} gets closer to zero in the case **a**, the iteration simply approximates the behavior for the BCM modulation. In **b**, as I_{th} is in the denominator, it can cause problems when the slopes or times approach 0, as the iteration would have a division over a very small number. After this discussion, it seems that the iteration **b** is the best option as long as I_{th} does not get close to zero.

C.2 Selected fixed-point iteration

The iteration process that is going to be solved is $T_i = 2 \cdot I_i \cdot T / (i_{i-1,i} + i_{i,i+1})$, which, as a function of T_i , is:

$$\begin{cases} T_1^{[n+1]} = g_1(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_1 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} + m_1 \cdot T_1^{[n]}} \\ T_2^{[n+1]} = g_2(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_2 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} + m_1 \cdot T_1^{[n]} - m_3 \cdot T_3^{[n]}} \\ T_3^{[n+1]} = g_3(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_3 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{2I_{th} - m_3 \cdot T_3^{[n]}} \\ T_4^{[n+1]} = g_4(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_4 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} + m_4 \cdot T_4^{[n]}} \\ T_5^{[n+1]} = g_5(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_5 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} + m_4 \cdot T_4^{[n]} - m_6 \cdot T_6^{[n]}} \\ T_6^{[n+1]} = g_6(\mathbf{T}_{1-6}^{[n]}) = 2 \cdot I_6 \frac{T_{np} + T_1^{[n]} + T_2^{[n]} + T_3^{[n]} + T_{pn} + T_4^{[n]} + T_5^{[n]} + T_6^{[n]}}{-2I_{th} - m_6 \cdot T_6^{[n]}} \end{cases} \quad (C.13)$$

The advantage of this method is that it is relatively simple, requiring a single division per equation and step. A drawback is that it is not valid for the BCM modulation.

The convergence of this specific method should be studied to determine when this method is valid and when it is not. To find if an iterative process converges, the *Banach Fixed-Point Theorem* should be applied [117]. This theorem states that the method converges if the function $\mathbf{g}(\mathbf{T}_{1-6}) : \mathbb{R}^n \rightarrow \mathbb{R}^n$ is a contraction, which means that it is continuous, and the value of its Jacobian matrix norm is below one. Any norm can be used to check convergence, but it is convenient to use the ∞ -norm or 1-norm as described in [116] for simplicity. Their values for the 6×6 Jacobian matrix are given by

$$\|J\|_\infty = \max_{(i=1\dots 6)} \left(\sum_{j=1}^6 |J_{ij}| \right) \quad \|J\|_1 = \max_{(j=1\dots 6)} \left(\sum_{i=1}^6 |J_{ij}| \right) \quad (C.14)$$

The iteration only converges ($\|J\| < 1$) for some values of $\mathbf{T}_{1-6}$, for a given $\mathbf{I}_{1-6}$. As stated in [116], it is a difficult problem to determine the set of initial points ($\mathbf{T}_{1-6}^{[0]}$ in this case) that end up converging to the solution. This problem is especially challenging because different iterations are defined for different operation points; this is, the iteration is different for different $\mathbf{I}_{1-6}$, $\mathbf{m}_{1-6}$, or T_{np} and T_{pn} . Since the function $\mathbf{g}(\mathbf{T}_{1-6})$ defined in Equation C.13 is continuous for $\mathbf{T}_{1-6} > \mathbf{0}$, determining the convergence consists in obtaining the norm of the Jacobian matrix of $\mathbf{g}(\mathbf{T}_{1-6})$. The matrix has thirty six values, given by $J_{ij} = \partial g_i / \partial T_j$ for $i, j \in [1, 6]$. Most of these derivatives are similar since the equations are similar. There are three "types" of derivatives, and an example for each is given below:

$$\begin{aligned} J_{11} &= \frac{\partial g_1(T_{1-6})}{\partial T_1} = \frac{2 \cdot I_1}{2 \cdot I_{th} + m_1 \cdot T_1} \left(1 - m_1 \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{2 \cdot I_{th} + m_1 \cdot T_1} \right) \\ J_{12} &= \frac{\partial g_1(T_{1-6})}{\partial T_2} = \frac{2 \cdot I_1}{2 \cdot I_{th} + m_1 \cdot T_1} \\ J_{21} &= \frac{\partial g_2(T_{1-6})}{\partial T_1} = \frac{2 \cdot I_2}{2 \cdot I_{th} + m_1 \cdot T_1 - m_3 \cdot T_3} \left(1 - m_1 \frac{T_{np} + T_1 + T_2 + T_3 + T_{pn} + T_4 + T_5 + T_6}{2 \cdot I_{th} + m_1 \cdot T_1 - m_3 \cdot T_3} \right) \end{aligned} \quad (C.15)$$

Therefore, obtaining the sums of the rows or the columns to obtain $\|J\|_\infty$ or $\|J\|_1$ would lead to very long equations from which no meaningful information is obtained. It is concluded that analyzing the convergence theoretically is not possible, basically because the iteration uses parameters that can take very distinct values. In other words, because $\mathbf{I}_{1-6}$ and $\mathbf{m}_{1-6}$ can be different depending on the operation point considered. Therefore, it is not practical to try to prove the convergence mathematically, and it has to be validated empirically by testing the iteration in different cases. To prove the convergence of the method, a *Matlab* script has been implemented. The script performs the iteration in Equation C.13 for the selected values of I_{th} , $\mathbf{I}_{1-6}$, and $\mathbf{m}_{1-6}$, setting $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$ as the initial point. The author was not able to find any operation point where

the iteration did not converge, although a systematic approach should be used if further validation is needed, or if any problem is found with this method.

The evolution of the switching period along the line cycle for a different number of iterations (1 to 10) is included in Figure C.2 a) for 1 kVA resistive load, $L = 80 \mu\text{H}$, and $I_{th} = 3.5 \text{ A}$ to illustrate the validation. The darker lines represent T calculated with a higher number of iterations. For this plot, first, $\mathbf{m}_{1-6}$ and $\mathbf{I}_{1-6}$ are obtained through Equations B.6, B.8, and B.11 given the voltages and currents of the three ports. How the period changes with each iteration is shown in Figure C.2 b) for two specific points of the line cycle. It is observed how the process converges towards the solution. From the ninth to the tenth iteration the increment of the calculated switching period is $T^{[10]} - T^{[9]} < 10 \text{ ns}$ at $\omega \cdot t = \pi/2$ for $T^{[10]} = 29.97 \mu\text{s}$ and of 11 ns for $T^{[10]} = 8.434 \mu\text{s}$ at $\omega \cdot t = \pi$. It proves that this iteration converges rapidly, so it is valid even when a small number of iterations is used.

Figure C.2: Switching period for 1 kVA resistive load, $L = 80 \mu\text{H}$, $I_{th} = 3.5 \text{ A}$ and $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$ for each point of the line cycle, calculated for an increasing number of iterations, a) along the line cycle, from light gray to black as the number of iterations is increased, b) iterations for the operation points at $\omega \cdot t = \pi/2$ and $\omega \cdot t = \pi$, showing how the method converges to the solution.

The same plot has been obtained for a power of 100 VA to 1 kVA in 100 VA steps, for $\cos \phi \in [-0.795, 0.795]$ in steps of 0.3975 and $I_{th} \in [0.5; 6] \text{ A}$ in steps of 0.5 A to validate the convergence in every condition. In all those cases, the iteration method tends toward the solution.

C.3 Conclusion

In this appendix, a numerical method to obtain the control times as a function of the port values is proposed. This method is valid to calculate $\mathbf{T}_{1-6}$ when the TCM modulation described in Section 4.4 is used. The solution is obtained through a fixed-point iteration, that tends towards the solution for $I_{th} > 0$ and starting with $\mathbf{T}_{1-6}^{[0]} = \mathbf{0}$ after a few steps. The convergence has been validated testing the iteration for all possible scenarios where this inverter operates. This iteration method has been used to plot Figure 4.22 and Figures 4.26 to 4.30 and it is required for the control of the inverter described in the following appendix.

FPGA implementation

This appendix is dedicated the VHDL implementation details of the controller in an FPGA. The FPGA selected for this purpose is an *Artix-7* FPGA from *Xilinx* [114]. An FPGA has been selected for its capability to run multiple tasks at once, without requiring interruptions. Paralleling multiple tasks is important given the complexity of the control and the fact that the loops and plant-inversion have to be calculated in a switching cycle. Further discussion on possible implementations on different devices such as DSPs or microcontrollers is out of the scope of this work.

The implementation of the control in VHDL is challenging. The goal is to decrease the total computational cost (hardware requirements) and minimize the time required to make all calculations. For this reason, it is convenient to minimize the number of operations and make them as simple as possible. It is also important to correctly select the resolution of the different variables.

The contributions of this work to the FPGA implementation are the modifications to include the additional modes *Tra1*, *Tra2*, *T2*, *T3* and *Th2* (positive and negative) to the mode selector, the implementation of the inversion-based control based on a single iteration, the redefinition of the modulator applicable to all operation modes, a few protections, and improvements for the sequence of processes. The main body of the code was created by Ángel de Castro and Alberto Sánchez through a collaboration contract between Universidad Autónoma de Madrid and Universidad Politécnica de Madrid for this project.

D.1 Code structure

The software *Vivado* is used for the implementation of the code. In this section, how the code is implemented is described.

As the calculations required in this control are complex, float numbers are not recommended since operating with them consumes too much hardware and time. Instead, fixed-point variables (*sfixed*) are used [118]. With it, each variable is defined with a certain number of bits for the integer part and a different number of bits for the decimal part. The advantages of the *sfixed* numerical notation are described in [119]. Please note that fixed-point notation and the previously mentioned fixed-point iteration are two completely separated subjects.

Before the processes are described, all variables, constant or additional blocks have to be defined. For the implementation, some constants are required; the value of the dead-time, the current threshold, the value of the inductance, or the values for the references for the loops are examples of such constants.

Then the signals are defined, some are *integers*, *boolean* or *logic vectors*, but most of them are *sfixed* variables. For instance, the variables to calculate loops, the variables involved in the inversion-based control, or the measured voltages and currents are fixed-point variables. The number of bits used for the different variables has to be carefully defined. For this purpose, the maximum value and accuracy of all variables for a correct operation is required, which is challenging to set. It is not the goal of this section to explain in detail how the length of all variables is set as it is not required to understand the implementation of the code.

After the variables are defined, some blocks are added. These blocks perform narrowly-defined tasks. For instance, they read the ADCs, store the value of P_o for the active power estimation in a memory block, generate a sinewave for V_o^{Ref} , or perform divisions.

Then, all processes are defined in the bulk of the code. All processes are run in parallel unless something else is specified. These processes control all the aspects of the inverter: the loops, the modulator, how variables are measured, protections, and so on.

In the following paragraphs, the implementation of the different processes is briefly described, to show the different features and functions of the code.

Inverter working state

The first thing that the code must define is the working state of the inverter. This does not refer to the switching states or the operation modes. Depending on the situation, the inverter may be in the following working states:

- **Normal state:** The inverter operates as described in this work, with the loops closed and the inversion-based control.
- **Over-current state:** After OVC is detected, all switches are opened until the current returns to the safe value, as explained in Section 5.2.4.
- **Soft-start state:** This state is used to precharge the storage capacitor to V_s^{ref} before the inverter starts its regular operation, as described in Section 5.2.4. Loops are not closed yet.
- **Idle state:** the inverter does not switch, and loops and the inversion-based control are not calculated before a manual switch is turned on and the input voltage is not high enough.

ADC measurements

The selected FPGA integrates ADCs with 12-bits [120], used to read V_g , V_s , V_o , I_g , and I_o . The time it takes to read the ADCs is long, and the reading process is not parallelizable. The ADCs are read in pairs, and two measurements take between 960 ns and 1170 ns to be performed. As a result, this is the most time-consuming task.

Sensors are calibrated by adjusting two parameters in the FPGA, namely, offset and gain of each measure to avoid errors in the measurements due to tolerances. This calibration is done a single time before the inverter is tested for the first time. For this purpose, the values read in the FPGA are displayed on the computer. How to read this information is discussed later when the *Chipscope* function is described.

Memory for P_o

As mentioned when the loops were described in Section 5.1.2.2, for the input current reference, the output power is estimated by adding the output power and output power a quarter line cycle before. For that purpose, the value of P_o has to be stored and read from a memory block. This block is precompiled, and it is not compatible with the simulator included in the *Vivado* software, which implies that the simulations for the code do not include the active power estimation.

Sinewave reference

A unit sinewave at 60 Hz is required to generate V_o^{Ref} . For this purpose, a precompiled block is used. Unfortunately, it cannot be used in simulation as before. A different process with the same functionality is implemented for the simulation.

Control loops

The control loops are not run in parallel as the output of the voltage loops is the input of the current loops; the sequence of process is described later.

D.1. Code structure

The proportional resonant loop for the output voltage has been implemented using the delta transform as described in [73]. For the storage capacitor loop, a PI regulator has been implemented with a bandwidth of 12 Hz, described in Section 5.1.2. For the output power estimation, the average value of P_o stored previously is divided by V_g^{Meas} . A division block is used, so this process takes a considerable amount of time compared with the time required to compute the other loops. Finally, both I_g and I_o loops are implemented following the description in Section 5.1.2. The outputs of the loops are the target current used in the inversion-based control.

Inversion-based control

This part of the code follows the flowchart for the plant-inversion shown in Figure 5.7. First I_s is obtained, which is time-consuming as a division has to be performed. Then, the mode selector is implemented as nested *if* clauses, comparing the measured voltages and the target currents to determine the mode applied, Table 4.3 and Table 4.4 described the operation region of each mode. For the slopes, the voltage in different switching states is divided over the inductance value. Since the inductance value is a parameter stored in the FPGA, it is not a variable, the division can be implemented as a multiplication. Moreover, since the slopes m_1 and m_6 are always positive and m_3 and m_4 always negative, the values $-m_3$ and $-m_4$ can be used in the equations. With this implementation all values are positive [74]. Technically, first, the slopes for the eight switching states are calculated; then, the slopes are only assigned to $\mathbf{m}_{1-6}$ once the mode is known. For the iterative process of a single step, the previous values for $\mathbf{T}_{a-h}$ are assigned to $\mathbf{T}_{1-6}^{[0]}$ for the selected mode.

As explained in Section 5.2, Equations B.8 and B.12 are solved to obtain $\mathbf{I}_{1-6}$. However, this would require several operations. The equations required for each mode are directly defined in the FPGA to simplify the calculations. The nineteen equations that relate the port currents with $\mathbf{I}_{1-6}$ are listed in Table D.1. The current in the states can be defined as positive for the FPGA implementation, as I_4 , I_5 , and I_6 are always negative [74]. For T modes, a division is always required, so this process takes some time to be computed.

Then, the control times are calculated using a single iteration (see Equation 5.5). In this step, divisions are required too. Note that the six control times in Equation 5.5 are calculated at the same time, decreasing the amount of time required but demanding more hardware capabilities. Finally, the values of $\mathbf{T}_{1-6}$ are associated with $\mathbf{T}_{a-h}$. Applied and control times are integer variables, where each unit is equivalent to 10 ns, the clock period.

Current detection and OVC protection

As shown in Figure 5.9, the circuit that generates digital signals based on the inductor current level is used to detect the current. It also contains some logic to detect whether the over-current condition is reached with positive or negative current. As an additional level of protection, $D^+ = 0$ while $D^- = 1$ implies that there is a problem with the detection. In this case the inverter shuts down.

Modulator

A state machine with ten states is implemented as described in Figure 5.10 to generate the signals that drive the MOSFET. As an additional safety measure, if a state lasts more than a maximum time, named T_{sat} , it is switched to the following state. T_{sat} ensures that the state ends in case of a problem with the control times or the current detection. For the *leading edge blanking* described in Section 5.2.3 too, T_{leb} is set to 500 ns.

The dead-time and the gate signals during the transitions are generated in a separate process, following the description in Section 5.2.3.

Mode	I_1	I_2	I_3	
$Tra4^+$	I_g	I_s	$-I_g - I_s + I_o$	
$Tra3^+$	$I_g + I_s$	$-I_s$	$-I_g + I_o$	
$Tra2^+$	$-I_s$	$I_g + 2I_s + I_o$	$-I_g - I_s$	
$Tra1^+$	$I_g + I_s + I_o$	$-I_g - 2I_s - I_o$	$I_s + I_o$	
		$\begin{cases} I_1 \\ I_3 \end{cases}$	$\begin{cases} I_4 \\ I_6 \end{cases}$	
$Th2^+$	$\frac{I_s+I_o}{2V_g-V_s-V_o}$	$\begin{cases} -V_s+V_o \\ V_g-V_o \end{cases}$	$\frac{-I_g-I_s+I_o}{2V_g-V_s-V_o}$	$\begin{cases} V_g-V_s-V_o \\ V_s+V_o \end{cases}$
$Th1^+$	$\frac{-I_g+I_o}{V_g-V_o}$	$\begin{cases} -V_s+V_o \\ V_g-V_o \end{cases}$	$\frac{-I_g-I_s+I_o}{V_g-V_o}$	$\begin{cases} V_g-V_o \\ -V_g+V_s+V_o \end{cases}$
$T3^+$	$\frac{-I_g-I_s+I_o}{2V_g-V_s-V_o}$	$\begin{cases} V_s+V_o \\ V_g-V_s-V_o \end{cases}$	$\frac{I_s+I_o}{2V_g-V_s-V_o}$	$\begin{cases} V_g-V_o \\ V_s-V_o \end{cases}$
$T2^+$	$\frac{-I_g-I_s+I_o}{V_g-V_o}$	$\begin{cases} -V_g+V_s+V_o \\ V_g-V_o \end{cases}$	$\frac{-I_g+I_o}{V_g-V_o}$	$\begin{cases} V_g-V_o \\ -V_s+V_o \end{cases}$
$T1^+$	$\frac{-I_s+I_o}{V_g+V_s-V_o}$	$\begin{cases} -V_g+V_s+V_o \\ V_g-V_o \end{cases}$	$\frac{-I_g+I_o}{V_g+V_s-V_o}$	$\begin{cases} V_s-V_o \\ V_g-V_s+V_o \end{cases}$
$T0$	$\frac{-I_s+I_o}{2V_g}$	$\begin{cases} V_s+V_o \\ V_g-V_s-V_o \end{cases}$	$\frac{I_s+I_o}{2V_g}$	$\begin{cases} V_s-V_o \\ V_g-V_s+V_o \end{cases}$
$T1^-$	$\frac{-I_g-I_o}{-V_g-V_s-V_o}$	$\begin{cases} V_s+V_o \\ V_g-V_s-V_o \end{cases}$	$\frac{-I_s-I_o}{-V_g-V_s-V_o}$	$\begin{cases} -V_g+V_s-V_o \\ V_g+V_o \end{cases}$
$T2^-$	$\frac{-I_g-I_o}{-V_g-V_o}$	$\begin{cases} V_g+V_o \\ -V_s-V_o \end{cases}$	$\frac{-I_g-I_s-I_o}{-V_g-V_o}$	$\begin{cases} -V_g+V_s-V_o \\ V_g+V_o \end{cases}$
$T3^-$	$\frac{I_s-I_o}{-2V_g+V_s-V_o}$	$\begin{cases} V_g+V_o \\ -V_s-V_o \end{cases}$	$\frac{-I_g-I_s-I_o}{-2V_g+V_s-V_o}$	$\begin{cases} -V_g+V_s-V_o \\ -V_s+V_o \end{cases}$
$Th1^-$	$\frac{-I_g-I_s-I_o}{-V_g-V_o}$	$\begin{cases} V_g+V_o \\ -V_g+V_s-V_o \end{cases}$	$\frac{-I_g-I_o}{-V_g-V_o}$	$\begin{cases} -V_s-V_o \\ V_g+V_o \end{cases}$
$Th2^-$	$\frac{-I_g-I_s-I_o}{-2V_g+V_s-V_o}$	$\begin{cases} V_g-V_s+V_o \\ V_s-V_o \end{cases}$	$\frac{I_s-I_o}{-2V_g+V_s-V_o}$	$\begin{cases} -V_g-V_o \\ V_s+V_o \end{cases}$
	I_4	I_5	I_6	
$Tra1^-$	$-I_g - I_s + I_o$	$I_g + 2I_s - I_o$	$-I_s + I_o$	
$Tra2^-$	I_s	$-I_g - 2I_s + I_o$	$I_g + I_s$	
$Tra3^-$	$-I_g - I_s$	I_s	$I_g + I_o$	
$Tra4^-$	$-I_g$	$-I_s$	$I_g + I_s + I_o$	

 Table D.1: Equations to obtain I_{1-6} directly for each operation mode.

ChipScope

For debugging purposes and calibrating the ADC measurements, the FPGA can send some variables back to the computer where they are displayed in real-time with the software *Chip Scope Pro*. This

D.1. Code structure

software is used to obtain the values read by the ADCs, the operation mode, and the operation state of the inverter (normal state, OCV state, soft-start state or idle state), plus some other variables useful for debugging. A *USB-JTAG programming Cable* from *Xilinx* is used to connect the FPGA to the computer; also required to program the FPGA.

Switching period counter and other counters

For the correct operation of the inverter, a few counters are required. A counter is used to calculate the total switching period that is required for the implementation of the control loops. There is also a counter used to synchronize the different processes as discuss next.

D.1.1 Synchronization of processes

As the FPGA runs many processes simultaneously, synchronization is important as certain processes should run before others. For instance, T_1 cannot be calculated before m_1 is updated. For this purpose, processes are synchronized to the begging of the switching cycle. A flag indicates that the new switching cycle has begun and the calculations of the previous cycle are done. A diagram showing the sequence of process and the time each process takes is shown in Figure D.1. Since the number and nature of the mathematical operations are known, the number of clock cycles each process takes to compute all calculation can be estimated.

Figure D.1: Sequence of the processes for the control, showing the processes that depend on previous processes and the estimated time it takes for each one, on top, the processed associated with the ADCs, in the middle the processes associated with the loops, and in the bottom, the processes related to the plant-inversion.

After the flag, the code begins by updating the mode and times used in the modulator for this switching cycle. It also reads the ADCs in pairs. There are five variables read in the following sequence: first V_o and V_s , followed by I_g and I_o , and finally V_g only. It takes around 1 μ s to read each pair of variables.

Once V_o and V_s are read, the reading process for I_g and I_o begins. Also, the equations used in the V_s and V_o loops are calculated. This takes 80 ns and 140 ns, respectively, which is much faster than the time it takes for the currents to be measured. Unfortunately, for the active power estimation, the V_g measured in the previous cycle is used, but, since V_g barely changes, this is not a problem.

After the currents are read, the current loops are calculated and the process to read V_g begins. The loops are calculated in 100 ns, much faster than the time it takes for the ADCs to read.

The part of the code for the inversion-based control is processed once V_g is read and the current loops are calculated, following the sequence described in Section 5.2. First, I_s^{Ref} and the slopes of the eight possible states are calculated, then the operation mode is determined, followed by the assignation of $\mathbf{m}_{1-6}$ and $\mathbf{T}_{1-6}^{[0]}$. When this is ready, $\mathbf{I}_{1-6}$ is obtained, followed by the single iteration for $\mathbf{T}_{1-6}$. Finally, $\mathbf{T}_{a-h}$ is assigned for the next switching cycle. The time each of these processes last is shown in Figure D.1. The problem is that each division takes around 400 ns. Therefore, the inversion-based control takes a total of 1600 ns to be completed.

Therefore, the complete process takes around 5 μ s from the beginning of the switching cycle. There is a flag indicating that the calculations are over, reset once the new cycle begins. If the flag is not reset when a new switching cycle starts, the calculations are not restarted, and the same mode and applied times are used in the following switching cycle. Therefore, only if the total switching period is above 5 μ s, the calculations are restarted at the beginning of the new cycle. Otherwise, the calculations are restarted after two cycles. In other words, for high-frequency operation ($200 \text{ kHz} < f_{sw} < 400 \text{ kHz}$), the calculations are only updated every two switching cycles.

In general, this control introduces a switching cycle delay. Although, for high-frequency operation, the introduced delay is two switching cycles. At any rate, the maximum delay introduced by the digital control is reached when the switching frequency is minimum. It should be noted that with this solution, the maximum switching frequency is not limited by the controller, which is an advantage over the previous implementation of the VHDL code. The goal of the sequence is to calculate everything as fast as possible, but a cycle delay is the best that can be achieved with this FPGA and the actual code.

D.1.1.1 Coding for debugging purposes

For debugging and testing purposes, it is convenient to be able to disable or enable different parts of the code or to add additional functionality. For this purpose, some *generic variables* (generics) are defined. Those variables are not a part of the FPGA program but are used to select which parts of the code is actually coded. Some generics enable or disable the different loops or additional protections. Other generic allows the inverter to operate in a predefined mode with predefined values for $\mathbf{T}_{a-h}$. The most important generic enables low input voltage operation. This feature has been very important as it is used to test the inverter at safe voltages first, and check temperature and ZVS as the input voltage is increased. When this generic is enabled, the output and storage capacitor references are proportional to the input voltage until the nominal value of $V_g = 400 \text{ V}$ is reached, point where V_o^{Ref} and V_s^{Ref} reach their nominal value too.

One of the contributions to the code is this additional flexibility, which has been of great help in the debugging process of the inverter and for the final tests.

D.2 Simulation of the code in *Vivado*

A simulation created by Ángel de Castro and Alberto Sánchez has been used to debug the code. It models the ideal behavior of the power stage, solving the state variables at clock frequency, similar to the work in [118] and [119].

For this purpose, the integrated simulator in *Vivado* can be used. Unfortunately, precompiled blocks cannot be simulated here, implying that neither the output power estimation loop nor the time the ADCs take to measure is included. For the simulations, the ADCs are read at the beginning of the switching cycle. Other software, such as *ModelSim*, should be used to model these blocks [39].

Figure D.2 shows some of the variables that can be extracted from the simulation. In this plot, the evolution of the inductor current waveform is shown, together with the voltage and current in the three ports and the evolution of the control times. The results are like the ones obtained in the simulation of Section 5.3, proving that the modifications in the FPGA code work as intended.

Figure D.2: Results of the simulation in *Vivado*, for 1 kVA resistive load, $L = 80 \mu\text{H}$ and $I_{th} = 3.5 \text{ A}$.

Also, a zoom of this plot is included in Figure D.3 for the mode $T0$. In this plot, the shape of the inductor current in a switching cycle is shown. The signals of the current detection, the driving signals and number of the switching state according to the state machine in Figure 5.10 are also included in the figure.

Figure D.3: Zoom of the simulation in *Vivado* showing D^+ , D^- , and OVC , the inductor current waveform, the driving signals, and the number of the switching state.

The simulator has been essential while coding, as it helped to find errors and to set the correct timing for the inversion process. With these results, it is shown that the control of the inverter, although complex, can be implemented.

D.3 Conclusion

This appendix has briefly covered the implementation of the VHDL code for the FPGA, the different processes and their synchronization has been explained. The main objective for the code is to accurately calculate the applied times for each switching cycle as fast as possible. With the proposed synchronization for the processes, it takes around 5 μ s to complete the calculations, which imply just a switching cycle delay for switching frequencies below 200 kHz.

The results obtained in simulation validate the correct operation of the code, which has been used to test the inverter in Chapter 7.

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