

# The impact of silicon feedstock on the PV module cost

G. del Coso<sup>a,\*</sup>, C. del Cañizo<sup>a</sup>, W.C. Sinke<sup>b</sup>

<sup>a</sup> Instituto de Energía Solar—Universidad Politécnica de Madrid, ETSI Telecomunicación, Ciudad Universitaria, 28040 Madrid, Spain

<sup>b</sup> ECN Solar Energy, POB 1, NL-1755 ZG Petten, The Netherlands

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## ABSTRACT

The impact of the use of new (solar grade) silicon feedstock materials on the manufacturing cost of wafer-based crystalline silicon photovoltaic modules is analyzed considering effects of material cost, efficiency of utilisation, and quality. Calculations based on data provided by European industry partners are presented for a baseline manufacturing technology and for four advanced wafer silicon technologies which may be ready for industrial implementation in the near future. Iso-cost curves show the technology parameter combinations that yield a constant total module cost for varying feedstock cost, silicon utilisation, and cell efficiency. A large variation of feedstock cost for different production processes, from near semiconductor grade Si (30 €/kg) to upgraded metallurgical grade Si (10 €/kg), changes the cost of crystalline silicon modules by 11% for present module technologies or by 7% for advanced technologies, if the cell efficiency can be maintained. However, this cost advantage is completely lost if cell efficiency is reduced, due to quality degradation, by an absolute 1.7% for present module technology or by an absolute 1.3% for advanced technologies.

## 1. Introduction

The photovoltaic (PV) industry and research institutions are working on solar grade silicon (SoG-Si) feedstock alternatives, aiming at reduction of the energy consumption and the cost in the production processes [1–3]. Both aims are related since an important cost driver of the SoG-Si processes is the energy cost. It is important, nevertheless, to analyze the entire manufacturing chain, from the feedstock to the PV module, considering the fact that the influence on module cost is related to cost, utilisation, and quality of the SoG-Si feedstock material [4,5].

In this paper, we analyze the effect of the following variables on the total module cost (for the calculations assumed to be independent): the feedstock cost, the yield of the feedstock production process, the material loss in ingot growing, the wafer thickness and the kerf loss (hereafter the sum of the wafer thickness and the kerf loss will be referred to as 'slicing pitch'), and the cell efficiency. With the exception of the slicing pitch they have been chosen because Si feedstock can have a clear impact on them. The slicing pitch is important as a parameter because it partly determines the silicon utilisation. Effects of variations in yield caused by alternative Si feedstock are not discussed in this paper to reduce the number of variables to handle, thus, the yields of every process except feedstock production are considered as constant in this work.

The assessment described in this work has been carried out within *CrystalClear*, a European Integrated Project carried out in the 6th Framework Programme. *CrystalClear* gathers expertise from 9 industries, 3 universities, and 4 research centres, aiming at "research, development, and integration of innovative manufacturing technologies that allow solar modules to be produced at a cost of 1€ per watt-peak in next generation plants".

The impact of feedstock features on module cost is assessed, analyzing a c-Si reference technology, referred to as "Basepower", and four alternative advanced technologies, now in the R&D stage, which aim to realise the manufacturing cost target of 1 €/watt-peak (Wp). These technologies are implemented in large-scale manufacturing plants (500 MWp/a–1 GWp/a) that can be operational in 2011 and beyond. Although it has been proposed to adapt (optimize) the solar cell processing to the available material (see for example Ref. [6]), the approach of *CrystalClear* has been to develop a roadmap detailing next generation technologies which allow broad classes of feedstock to be used [7].

Cost modelling has been carried out using information on the cost structure of the PV technology that was provided by industry partners in the *CrystalClear* project. Data concerned direct manufacturing costs and covered silicon crystallisation, wafering, cell fabrication, and module assembly. Note that we always refer to cost and not price. This will help to make the analysis independent of external and temporary factors influencing PV price, such as the recent shortage of high-purity silicon.

It should be noted that the impact of Si feedstock on the generation cost of solar electricity is determined not only by the

\* Corresponding author: Tel.: +34 91 543 35 49; fax: +34 91 544 63 41.  
E-mail address: gdelcoso@ies-def.upm.es (G. del Coso).

influence on the module cost, but also on other aspects such as Balance-of-System (BoS) cost, performance ratio, global solar irradiation, etc.

## 2. Cost calculations

### 2.1. Cost modelling

The impact of new silicon feedstock materials on the module cost is quantified by describing the new materials in terms of cost (€/kg) and quality (relative cell efficiency, ratio of the cell efficiency with a new material, and the cell efficiency achieved with the conventional material). The impact of silicon utilisation is also analyzed, considering that the amount of silicon feedstock consumed to produce one watt-peak (Wp) of module power is determined by the expression<sup>1</sup>

$$\frac{\text{kg}}{\text{Wp}} = \frac{d_{\text{Si}}(w_t + k)}{\eta G_{\text{ce}}} \frac{1}{f_{\text{ig}} \prod_j Y_j} \quad (1)$$

where  $d_{\text{Si}}$  is solid silicon density expressed in  $\text{kg m}^{-3}$ ,  $w_t$  wafer thickness expressed in m,  $k$  the kerf loss expressed in m,  $\eta$  the cell efficiency, and  $G_{\text{ce}}$  the solar irradiance under standard conditions ( $1000 \text{ W m}^{-2}$ ).  $Y_j$  is the yield of technological step  $j$ , covering the whole value chain, from SoG-Si feedstock production ( $Y_f$ ) to module assembly ( $Y_i$  for ingot growth,  $Y_w$  for wafering,  $Y_c$  for cell processing, and  $Y_m$  for module assembly). The ingot-growth fraction,  $f_{\text{ig}}$ , stands for the ratio of silicon output to silicon input in the ingot growth, considering material losses and recycling. Silicon utilisation therefore depends on the losses in ingot growth (that take into account the recycling), the slicing pitch, the cell efficiency, and the yield of every technological step.

Considering a certain technology, for example any of those presented in Section 2.2, alternative Si feedstock and efficiency of utilisation will impact on its module total cost (in terms of €/Wp) according to the following expression:

$$C_{\text{total}} = A \frac{1}{(f_{\text{ig}})_{\text{rel}} (Y_f)_{\text{rel}}} \frac{(w_t + k)_{\text{rel}}}{\eta_{\text{rel}}} \frac{\text{€}}{\text{kg}} + B \frac{1}{(f_{\text{ig}})_{\text{rel}}} \frac{(w_t + k)_{\text{rel}}}{\eta_{\text{rel}}} + C \frac{(w_t + k)_{\text{rel}}}{\eta_{\text{rel}}} + D \frac{1}{\eta_{\text{rel}}} \quad (2)$$

in which the subscript *rel* stands for relative ratio (compared to the parameter that describes the considered technology) and the constants A, B, C, and D are derived from the considered technology as follows:

$$A = \frac{\text{kg}}{\text{Wp}}, \quad B = C_i, \quad C = C_w, \quad D = C_c + C_m$$

By  $C_i$ ,  $C_w$ ,  $C_c$ , and  $C_m$  we mean the fully integrated processing cost (in terms of €/Wp) of ingot growth, wafering, cell processing, and module assembly, respectively. It means that the cost  $C_i$  also includes the yield losses in the subsequent technological steps. For instance, as it can be seen in Fig. 1, the fully integrated cost of ingot growth includes the accumulated yield losses during ingot growing, wafering, cell processing, and module assembly. To produce an ingot has a certain cost (€/Wp), and this cost increases if the power produced per ingot diminishes not only because ingots are (partly) out of specifications, but also because wafers are broken, cells are wrongly processed or modules are out of specifications.

<sup>1</sup> Silicon consumption is expressed in the international system base units,  $\text{kg Wp}^{-1}$ , although in the PV industry this figure is commonly expressed in  $\text{g Wp}^{-1}$ .

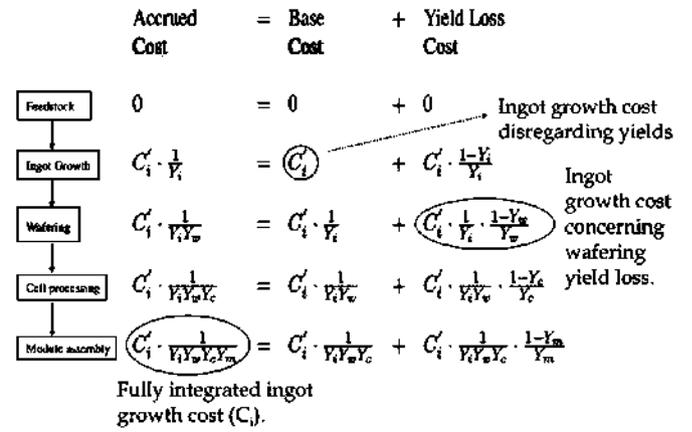


Fig. 1. Explanation of the “fully integrated cost” concept, using silicon growth as an example. Throughout the production chain the yield losses ( $Y_j$ ) are accumulated and therefore the ingot growth cost increases.  $C_i$  is the cost for the ingot growth process disregarding any yield loss.

A useful concept to help in the analysis of the influence of the variables in Eq. (2) on the total cost is the “sensitivity”. The sensitivity of a quantity  $Q$  to changes in a parameter  $P$  is defined as follows:

$$S_P^Q = \frac{\partial Q/Q}{\partial P/P} \quad (3)$$

The sensitivities for the main parameters involved in the cost calculations are determined by the following expressions:

$$\begin{aligned} S_{\eta}^{C_{\text{total}}} &= -1 \\ S_{C_{Fm}}^{C_{\text{total}}} &= 1 - \frac{C_i + C_w + C_c + C_m}{C_{\text{total}}} \\ S_{Y_f}^{C_{\text{total}}} &= -1 + \frac{C_i + C_w + C_c + C_m}{C_{\text{total}}} \\ S_{f_{\text{ig}}}^{C_{\text{total}}} &= -1 + \frac{C_w + C_c + C_m}{C_{\text{total}}} \\ S_{w_t + k}^{C_{\text{total}}} &= 1 - \frac{C_c + C_m}{C_{\text{total}}} \end{aligned} \quad (4)$$

$C_{Fm}$  is the feedstock cost expressed in €/kg.

### 2.2. Cost data from CrystalClear

The technologies described in the CrystalClear roadmap have been defined and characterised in terms of the different feedstock material classes used, the device architectures, the potentials for cost reduction, and corresponding development risk profiles, as explained in Refs. [5,8,9]. Their characteristics are defined for large-scale industrial production, in the range 500–1000 MWp/a, which benefits from economy-of-scale savings, a high level of automation and integration of the different steps in the PV value chain. They are briefly described here as follows:

- **Basepower:** Basepower is conceived as a “standard” crystalline silicon technology implemented in a large-scale integrated plant that has the property that if it is being built today, it would be operative in 2011. It is based on cast multicrystalline silicon, solar grade (SoG-Si) feedstock, ingot-growth fraction 93.0%, wafer thickness 180  $\mu\text{m}$ , kerf loss 170  $\mu\text{m}$ , wafer size  $156 \times 156 \text{ mm}^2$ , conventional P-AI cell technology with front and rear electrodes, encapsulated cell efficiency 15.8%, front-to-rear interconnection, and standard lamination. Silicon utilisation for Basepower is 6.5 g/Wp.

**Table 1**  
Parameters for the cost calculations regarding the influence of feedstock cost, efficiency of silicon utilisation, and cell efficiency.

	$A (\times 10^3)$	$B$	$C$	$D$	Total cost (€/Wp)
Basepower	6.5	0.068	0.125	0.822	1.15
Multistar	4.5	0.046	0.088	0.779	1.00
MultistarR	4.4	0.045	0.086	0.844	1.07
Superslice	3.9	0.102	0.077	0.737	1.03
SuperslicE	4.0	0.104	0.078	0.830	1.13

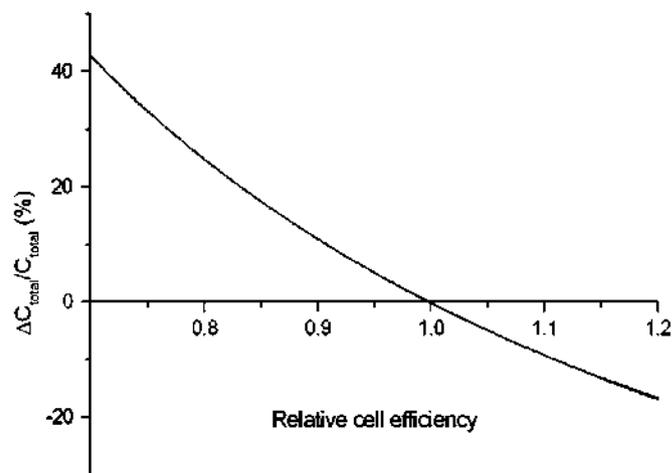
- **Multistar:** This is based on cast multicrystalline silicon, solar grade (SoG-Si) feedstock, ingot-growth fraction 95.8%, wafer thickness 120  $\mu\text{m}$ , kerf loss 140  $\mu\text{m}$ , wafer size 156  $\times$  156  $\text{mm}^2$ , front and rear electrodes, encapsulated cell efficiency 16.7%, front-to-rear interconnection, standard lamination, and is frameless. Silicon utilisation is 4.5 g/Wp.
- **MultistarR:** This is based on cast multicrystalline silicon, solar grade (SoG-Si) feedstock, ingot-growth fraction 95.8%, wafer thickness 120  $\mu\text{m}$ , kerf loss 140  $\mu\text{m}$ , wafer size 156  $\times$  156  $\text{mm}^2$ , metallization wrap-through [10], encapsulated cell efficiency 17.0%, all-rear interconnection, integrated conductive pattern, standard lamination, and is frameless. Silicon utilisation is 4.4 g/Wp.
- **Superslice:** This is based on Cz monocrystalline silicon, near semiconductor grade (Near SeG-Si) feedstock, ingot-growth fraction 95.8%, wafer thickness 120  $\mu\text{m}$ , kerf loss 140  $\mu\text{m}$ , wafer size 125  $\times$  125  $\text{mm}^2$ , rear side passivated with  $\text{SiO}_x$  and  $\text{SiN}_x$ , encapsulated cell efficiency 18.7%, front-to-rear interconnection, standard lamination, and is frameless. Silicon utilisation is 3.9 g/Wp.
- **SuperslicE:** This is based on Cz monocrystalline silicon, near semiconductor grade (Near SeG-Si) feedstock, ingot-growth fraction 95.8%, wafer thickness 120  $\mu\text{m}$ , kerf loss 140  $\mu\text{m}$ , wafer size 125  $\times$  125  $\text{mm}^2$ , emitter wrap-through, encapsulated cell efficiency 18.5%, all-rear interconnection, integrated conductive pattern, standard lamination, and is frameless. Silicon utilisation is 4.0 g/Wp.

The CrystalClear roadmap includes two other technologies (one based on thin ribbon material and the other on thin Si film epitaxially grown on a low-cost substrate). They have not been treated here for reasons of simplicity and conciseness.

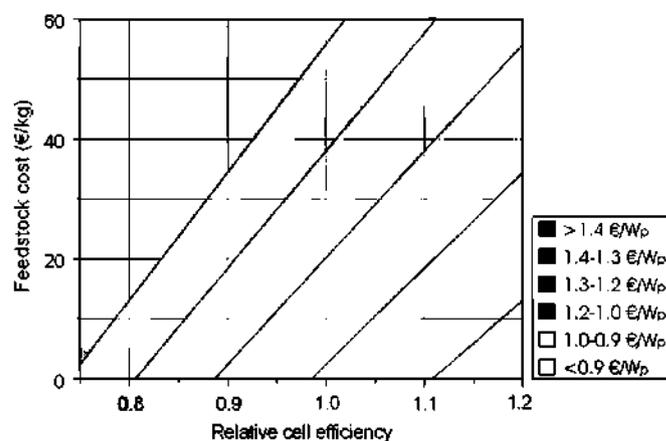
Data on production costs, provided by industry partners, have been averaged and divided in the following categories: equipment (with 10 years for depreciation), labour, materials, yield losses, and fixed costs. Energy and maintenance costs are included in the equipment category, and consumables in materials. The cost distribution is applied to the different technology steps considered: ingot growth, wafering, cell processing, and module assembly. Estimations on cost savings due to large-scale production have been included in the calculations. An aggregated figure, in €/kg, is assumed for silicon feedstock cost and the feedstock process yield is assumed to be 1, since development of feedstock production processes is outside the scope of CrystalClear. For cost breakdown of each CrystalClear technology we can consult in Ref. [9]. Table 1 summarizes, for the five CrystalClear technologies considered in this work, the parameters that describe each of them in terms of Eq. (2).

### 3. Impact of feedstock cost, silicon utilisation, and cell efficiency

The impact on total module cost of the variables can be analyzed by modifying a certain one while the others remain



**Fig. 2.** Module cost savings regarding relative cell efficiency for Basepower technology.



**Fig. 3.** Iso-cost curves for Basepower technology regarding cell efficiency and feedstock cost.

constant. For instance, in Fig. 2 the Basepower module cost dependence on cell efficiency is presented, which shows that a cell efficiency reduction from 15.8% to 14.2% (reduction by 10% in relative values) increases the module cost by 11%. A similar figure showing the variation in total cost vs feedstock cost can be drawn; if so, it would show that if the feedstock cost were 0 €/kg, the module cost would decrease by 11%.

Nevertheless, an alternative feedstock might change the cell efficiency, the feedstock yield, or the ingot-growth fraction ( $f_{ig}$ ). Thus, analysis of the impact on module cost regarding a combination of variables is recommended. Iso-cost curves, showing variable combinations for which the total module cost is constant, can be deduced from the cost calculations. Regarding Basepower technology, the iso-cost curves are presented in Fig. 3 (for feedstock cost vs relative efficiency), Fig. 4 (for feedstock cost vs relative fraction of Si used in ingot growth), and Fig. 5 (for feedstock cost vs feedstock process yield). The iso-cost curve for feedstock cost vs relative slicing pitch is presented in Fig. 6, analyzing the importance of slicing pitch as a cost driver of module cost.

From the iso-cost curves and their slopes some conclusions can be drawn. In Fig. 3, the steeper lines show that the technology is relatively insensitive to feedstock cost increases. Coming from the situation of 20 €/kg and relative efficiency 1, if the feedstock cost

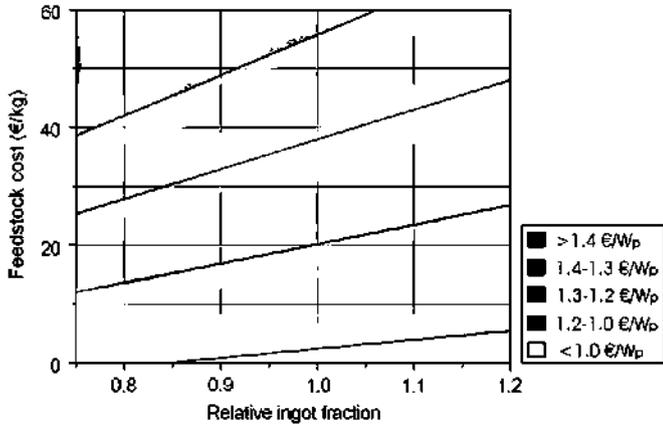


Fig. 4. Iso-cost curves for Basepower technology regarding fraction of Si used in ingot growth ( $f_{ig}$ ) and feedstock cost.

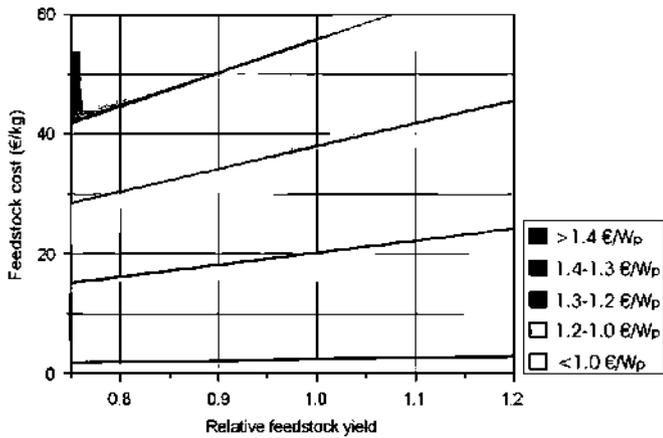


Fig. 5. Iso-cost curves for Basepower technology regarding feedstock process yield and feedstock cost.

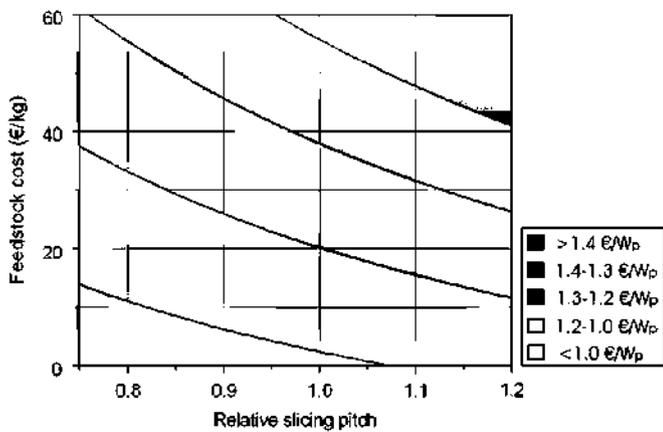


Fig. 6. Iso-cost curves for Basepower technology regarding slicing pitch and feedstock cost.

increases to 30 €/kg (50% up), increasing efficiency by 6% neutralises the cost increase and the module cost remains constant. Likewise, if the efficiency decreases by 10%, the feedstock cost should decrease to 2 €/kg (90% down) to keep the module cost constant.

Table 2

Sensitivity factors to changes in total module cost of feedstock cost, slicing pitch, cell efficiency, ratio of output silicon to input silicon in ingot growth process and feedstock process yield.

	$S_{f_{ig}}^{total}$	$S_{W_{f_{ig}}}^{total}$	$S_{\eta}^{total}$	$S_{f_g}^{total}$	$S_{Y_f}^{total}$
Basepower	0.11	0.28	-1	-0.17	-0.11
Multistar	0.09	0.22	-1	-0.14	-0.09
MultistarR	0.08	0.21	-1	-0.12	-0.08
Superslice	0.11	0.29	-1	-0.21	-0.11
SuperslicE	0.11	0.27	-1	-0.20	-0.11

Concerning ingot growth step, the fraction of the incoming silicon that is crystallised into usable silicon might vary when using different feedstock material. The effect of the combination of feedstock cost and ingot-growth fraction,  $f_{ig}$ , is shown in Fig. 4. Coming from the situation of 20 €/kg and relative ingot fraction 1, if the feedstock cost decreases to 10 €/kg (50% down), the ingot-growth fraction could be relaxed a relative 31% yielding constant module cost.

In the iso-cost curve presented in Fig. 5 the module remains constant for constant ratio of feedstock cost to feedstock yield, as expected from Eq. [2]. Thus, coming from the situation of 20 €/kg and a relative feedstock production yield 1, if the feedstock cost decreases to 10 €/kg (50% down) the feedstock yield could be relaxed a relative 50% yielding constant module cost.

Similar reasoning can be applied to iso-cost curves presented in Fig. 6, where cell efficiency and feedstock yield are kept constant, and slicing pitch and feedstock cost are modified. From the starting situation of 20 €/kg and relative slicing pitch 1, if the feedstock cost increases to 30 €/kg (50% up), reducing the slicing pitch by a relative 16% neutralises the cost increase and the module cost remains constant. Likewise, if the slicing pitch increases by 10%, the feedstock cost should decrease to 15 €/kg (25% down) to keep the module cost constant.

Similar iso-cost curves can be drawn and analyzed for the rest of the technologies. It turns out that SuperslicE is the least sensitive technology to feedstock cost increases, followed by Superslice, MultistarR, Multistar, and finally, Basepower. The technologies with higher ratio of total cost (€/Wp) to silicon utilisation (kg/Wp) are less sensitive to feedstock variations since it means that the feedstock processing cost weight in the total cost is lower.

Sensitivity factors, detailed in Table 2, also provide valuable information. It can be seen that for any of the five technologies analyzed the highest sensitivity (in absolute value) is for the efficiency, followed by the slicing pitch, the ingot-growth fraction, and finally, the feedstock cost and feedstock yield. The efficiency sensitivity is more than ten times the feedstock cost sensitivity, the slicing pitch sensitivity is 3 times the feedstock cost sensitivity, and the ingot-growth fraction sensitivity is 1.5-2 times the feedstock cost sensitivity in all cases analyzed. The sensitivity factors show the importance of every parameter as mathematical independent variable, but it has to be understood that the difficulty of varying the slicing pitch or the feedstock cost by, for instance, 10% is completely different from varying the cell efficiency, the ingot-growth fraction, or the process yields by 10%.

#### 4. New feedstock sources

In the past, the PV industry consumed semiconductor grade silicon, characterized by high quality and high production cost. Currently, the industry demands specific silicon (solar grade silicon) for solar applications, with the required quality and

**Table 3**

Maximum relative variation of efficiency, feedstock yield or ingot-growth fraction allowed for UMG-Si feedstock (10 €/kg) to be more cost effective than near SeG-Si feedstock (30 €/kg).

	Relative efficiency (%)	Relative feedstock yield (%)	Relative ingot-growth fraction (%)
Basepower	-10.8	-66.7	-49.5
Multistar	-8.5	-66.7	-49.5
Multistar	-7.9	-66.7	-49.5
Superslice	-7.5	-66.7	-35.6
SupersliceE	-7.0	-66.7	-35.6

lowest production cost. The uncertain trade-off between quality and cost acceptable for the industry is the scope of this section.

A simple classification of SoG-Si sources distinguishes two main approaches: "chlorosilane routes" [11], which are supposed to yield silicon relatively similar to conventional polysilicon for semiconductor applications, and "metallurgical routes" [12], with a bigger potential for cost reduction, but a larger uncertainty regarding the impact on cell efficiency and the silicon utilisation [13].

In this work two limits have been estimated for feedstock manufacturing cost: the upper limit is 30 €/kg corresponding to near-semiconductor grade silicon (Near SeG-Si), and the lower limit is 10 €/kg [13] corresponding to upgraded metallurgical grade silicon (UMG-Si). Since near SeG-Si quality is very good, its utilisation as feedstock material in every technology considered is supposed to yield a relative efficiency of 1, a relative feedstock yield of 1, and a relative ingot-growth fraction of 1. Since the cost of UMG-Si is lower, the use of this material could be more cost effective on the module level despite the reduction of feedstock quality or efficiency of silicon utilisation. This UMG-Si cost advantage can be lost under unfavourable combinations of efficiency, feedstock yield, and ingot-growth fraction during module manufacturing. Therefore, the maximum variation of efficiency, feedstock yield or ingot-growth fraction allowed for UMG-Si feedstock (10 €/kg) to be more cost effective than with near SeG-Si feedstock (30 €/kg) is detailed in Table 3.

Then, regarding Basepower technology and absolute values, coming from the situation of near SeG-Si utilisation and an encapsulated cell efficiency of 15.8%, a feedstock yield 1 and an ingot-growth fraction 93.0%, the cost advantage of UMG-Si will be lost if the encapsulated cell efficiency is less than 14.1%, the feedstock yield is less than 33% or the ingot-growth fraction is less than 50%.

The feedstock yield and ingot-growth fraction variations do not introduce strong limitations for UMG-Si users, according to Table 3, since the minimum values acceptable are probably not difficult to reach. On the other hand, the UMG-Si users must be careful with the cell efficiency, avoiding reductions further than 1.7% (absolute) by means of, for instance, bulk quality enhancement or defect engineering [6].

## 5. Conclusions

Using data provided by industry partners in the framework of the CrystalClear project, the influence of silicon utilisation, cell efficiency, and feedstock cost on the module cost has been calculated. The calculations are made for five manufacturing technologies. The first relates to baseline manufacturing technology, ready for

production in 2011. The last four relate to advanced wafer silicon technologies.

The authors conclude that if the cell efficiency can be maintained, a large variation of feedstock cost for different feedstock production processes, from near SeG-Si to UMG-Si, changes the cost of c-Si modules between 11% and 7%. The greatest change is for baseline technology and the lowest is for advanced technologies. However, the cost advantage of low-cost feedstock utilisation is completely lost if cell efficiency is reduced, due to quality degradation, by an absolute 1.7% for baseline module technology or by an absolute 1.3% for advanced technologies.

Finally, it is concluded that the variations of feedstock yield and variations of ingot-growth fraction only weakly affect low-cost feedstock users since the minimum values accepted are well within reach.

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