UNIVERSIDAD POLITÉCNICA DE MADRID
Escuela Técnica Superior de Telecomunicación

Design of Ultra-Low Power and Area Circuits for Cell-Size Microsystems

DOCTORAL THESIS

Submitted for the degree of Doctor by:

Javier de Mena Pacheco
Máster Universitario en Ingeniería de Sistemas Electrónicos

Madrid, 2024

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Doctoral Degree in Electronic Systems Engineering

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D O C T O R A L T H E S I S

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Under the supervision of:
Dr. María Luisa López Vallejo

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A mis abuelos, que me quisieron con locura y que, desde donde estén, se sentirían orgullosos de aquel niño que creció entre los paisajes y rincones de Extremadura.

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Abstract

The concept of smart dust emerged in the early 21st century to enable large-scale distributed sensing and computation. Progress was hindered for years due to the slow development of key technologies like nanotechnology, microelectronics and wireless communication.

Recent advancements in technology have continually pushed the limits of what is possible in computing, sensing, and communication, leading to a resurgence of interest in autonomous microsystems. A key frontier in this evolution is the development of cell-sized autonomous microsystems. Achieving microsystems smaller than 100 μm has the potential to revolutionize data collection. These tiny devices can be deployed in environments where traditional sensors are either impractical or impossible to use, unlocking numerous groundbreaking applications in fields such as medicine, environmental science, and industrial monitoring to cite a few.

In this context, this thesis aims to contribute to the development of cell-sized autonomous microsystems by focusing on the study and design of some necessary circuitry for these systems such as the power management and the communication subsystems. As a consequence, our contributions address the design of these two building blocks while facing the challenges imposed by the drastic miniaturization of these electronic particles.

The primary limitation of cell-size microsystems is the extremely constrained space available. This causes a drastic reduction in functionality, which, in some cases such as in this thesis, forces a fully analog circuit design.

Another severe limitation lies in the power supply for these microsystems. At such small scales, traditional battery systems are impractical. Therefore, energy-harvesting methods are required, but the amount of energy that can be collected at the cell-size is remarkably small, which raises the difficulty of design.

Regarding the energy management of the microsystem, this work describes two power management units (PMUs), each one of them targeting a different scenario. Both PMUs integrate a voltage reference and a voltage regulator with an extremely low area and power consumption.

In particular, the first design targets *in vitro* applications. The temperature stability of this scenario relaxes the constraints related to temperature variations, allowing us to focus more on parameters such as line regulation and power supply rejection. These parameters are crucial to mitigate the fluctuations coming from the power supply. Indeed, our first PMU proposal integrates a voltage reference that features the best line regulation reported in the literature.

The second PMU proposal focuses on environments with varying temperatures, requiring temperature compensation. It aims for low supply and temperature dependency while providing sufficient regulated power in a compact area and with minimal quiescent current draw. The existing literature has limited solutions for these challenges. Our second proposal implements a novel topology that incorporates the voltage reference in the feedback loop of the regulator. This optimizes area and power resources and also allows for temperature compensation through transistor sizing.

Regarding the communication interface, the analog voltage provided by the sensor of the microsystem must be digitized in order to be transmitted to the outside world. Time-domain digitization emerges as a lightweight digitization method to save significant area and power at the expense of sacrificing some accuracy and speed with respect to traditional ADCs. Consequently, we also present in this thesis a sub-nW voltage-controlled oscillator with a quasi-linear response to perform time-domain digitization.

Throughout this dissemination, we address the significant challenges of limited power and area in these designs and show a detailed discussion of the trade-offs involved and the solutions adopted.

Resumen

El concepto de *smart dust* surgió a principios del siglo XXI para habilitar la detección y computación distribuidas a gran escala. Su desarrollo fue limitado durante años debido a la falta de avances en nanotecnología, microelectrónica y comunicación inalámbrica. Sin embargo, los recientes progresos tecnológicos han renovado el interés en los microsistemas autónomos, destacando los dispositivos del tamaño de una célula, menores a 100 μm. Estos sistemas tienen el potencial de revolucionar la recolección de datos en campos como medicina, ciencia ambiental y monitoreo industrial, al operar en entornos donde los sensores tradicionales son imprácticos.

Esta tesis contribuye al desarrollo de microsistemas autónomos del tamaño de una célula mediante el diseño de circuitos esenciales, como los subsistemas de gestión de energía y comunicación. Estos diseños enfrentan los desafíos impuestos por la miniaturización extrema, que limita el espacio disponible y reduce la funcionalidad, obligando en muchos casos al uso de circuitos completamente analógicos.

Otra de las mayores limitaciones de estos microsistemas es el suministro energético. A escalas tan pequeñas, las baterías tradicionales son inviables, lo que hace necesaria la recolección de energía ambiental. Sin embargo, la cantidad de energía recolectable a esta escala es muy limitada, lo que incrementa la complejidad del diseño. Para abordar estos desafíos, este trabajo propone dos unidades de gestión de energía (PMUs), cada una orientada a un escenario específico, integrando una referencia de voltaje y un regulador con un consumo de área y potencia extremadamente bajo.

El primer diseño está destinado a aplicaciones *in vitro*, donde la estabilidad térmica del entorno permite centrarse en parámetros como la regulación de línea y el rechazo al ruido de la fuente de alimentación. Estos parámetros son esenciales para mitigar las fluctuaciones de la fuente de alimentación. La primera propuesta de PMU incluye una referencia de voltaje que presenta la mejor regulación de línea reportada en la literatura, lo que mejora significativamente el desempeño con fuentes débiles e inestables.

La segunda propuesta se centra en entornos con variaciones de temperatura, lo que requiere compensación térmica. En este caso, la PMU debe lograr una baja dependencia con respecto al voltaje de alimentación y la temperatura, al tiempo que proporciona suficiente potencia regulada en un área compacta y con un consumo mínimo. Este trabajo presenta una topología novedosa que integra la referencia de voltaje en el lazo de retroalimentación del regulador, optimizando los recursos de área y potencia. Además, esta configuración permite compensación térmica mediante el dimensionamiento de transistores, abordando así limitaciones no resueltas en la literatura.

En cuanto al subsistema de comunicación, el voltaje analógico de los elementos sensores del microsistema debe digitalizarse para ser transmitido al exterior. Dado que los ADCs tradicionales son poco viables debido a su elevado consumo de energía y área, se optó por la digitalización en el dominio del tiempo como alternativa ligera. Este método sacrifica algo de precisión y velocidad a cambio de ahorros significativos en energía y área. En este contexto,

la tesis propone un oscilador controlado por voltaje con un consumo inferior a 1 nW y una respuesta cuasi-lineal para realizar la digitalización en el dominio del tiempo.

A lo largo de esta disertación, se abordan los desafíos de potencia y área extremadamente limitadas en los diseños de estos microsistemas ultraminiaturizados. Además se presenta un análisis detallado de los sacrificios involucrados y se discuten las soluciones adoptadas para superar las restricciones impuestas por la miniaturización extrema.

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Abbreviations and Acronyms

ADC analog-to-digital converter.

BJT bipolar junction transistor.

CMOS complementary metal-oxide-semiconductor.

CTAT complementary to absolute temperature.

DRC design rules check.

EA error amplifier.

EHP electron-hole pair.

FOM figure of merit.

HDO high-dropout.

HVT high threshold voltage.

I/O input/output.

IoT internet of things.

LDO low-dropout.

LED light emitting diode.

LVS layout vs. schematic.

MEMS micro-electromechanical systems.

MIT Massachusetts Institute of Technology.

MOSFET metal-oxide-semiconductor field effect transistor.

MTL Microsystems Technology Laboratory.

PMU power management unit.

PSR power supply rejection.

PTAT proportional to absolute temperature.

PVT process, voltage and temperature.

RFID radio-frequency identification.

SCM self-cascode MOSFET.

STI Shallow trench isolation.

TC temperature coefficient.

UGF unity-gain frequency.

UPM Universidad Politécnica de Madrid.

UV ultraviolet.

VCO voltage-controlled oscillator.

WPE well proximity effect.

Chapter 1

Introduction

1.1 Context

In the last half-century, microelectronics has fueled incredible technological advancements that have given rise to devices like smartphones, laptops, and smart TVs. These products rely on semiconductor chips which have become increasingly cheaper and more powerful by reducing the size of electronic devices. However, even though Moore's law and Dennard's scaling have allowed for transistor scaling down to 2-nanometer sizes, improvements in semiconductor processing have mostly been used to increase the number of transistors on a chip exponentially. As a result, this trend has forced to keep the size of chips on the millimeter scale.

A research branch based on small circuits, known as *smart dust*, emerged 23 years ago [1] with the purpose of creating a sensor network system for monitoring the environment and machinery, primarily for military use. The system would consist of hundreds to thousands of sensor nodes, which would be completely autonomous and capable of sensing a particular parameter, processing the signal, and communicating it to the outside world. The key concept of this research lies in these systems being shrunk to the scale of a dust mote and below.

These tiny devices have the potential to unlock numerous breakthroughs due to their size advantages. These electronic particles can reach places currently inaccessible to conventional electronics, opening up new possibilities for various applications. Their small size would allow them to interact with individual biological cells, making it possible to locally measure basic physiological parameters such as temperature, pH or blood pressure. They could also circulate within the body to detect early stages of cancer. However, their applications are not limited to just biological use but also have many industrial applications enabling new ways of environmental monitoring. These tiny devices are small and light enough to potentially be carried by the wind [2] or embedded in everyday objects such as paint and thread to make fabric, which would be useful in creating large sensing networks on almost any surface.

However, only a small number of autonomous sensor nodes, based on silicon, have been developed with volumes of one cubic millimeter and below [3, 4]. These nodes have been designed for a wide range of applications, such as measuring temperature [4], sensing glucose [5], recording neural activity [6], [7], acquiring images [8], and authenticating banknotes [3].

The microsystems mentioned above were built using advanced complementary metal-oxide-semiconductor (CMOS) technology and have volumes as small as $200\times200\times100$ μm^3 [8]. However, these fully integrated microsystems are still much larger than biological cells, even though impressive progress has been made in miniaturization.

1.2 Thesis Motivation

The advancement of technology has continually pushed the boundaries of what is possible in the fields of computing, sensing, and communication. One of the most compelling frontiers in this evolution is the development of cell-size autonomous microsystems. Obtaining microsystems below 100 μm can be achieved by strongly reducing the complexity of the system, but this comes at the cost of having less functionality. However, this huge size reduction holds transformative potential across a wide array of applications:

- Revolutionizing Healthcare: In healthcare, cell-size autonomous microsystems can revolutionize the way we monitor and treat diseases. These tiny devices can be deployed within the human body to monitor physiological parameters at a cellular level, providing real-time data on a patient's health status. This capability can lead to early detection of diseases, continuous monitoring of chronic conditions, and personalized treatment plans. For example, in [9] an autonomous microsystem that can be implanted within the human eye was demonstrated. This microparticle targeted continuous intraocular pressure monitoring for glaucoma diagnosis and management. In another study, [5], a tiny electronic microparticle that can be injected painlessly into the skin was presented. This microsystem was used to monitor glucose levels *in vivo*, which is vital in diabetic patients. In the future, if micro- and nanotechnology keep progressing at the same pace, truly transformative advancements, such as automatic cancerous cell detection, seem possible, hence, highlighting the relevance of this research field.
- Industrial and Infrastructure Monitoring: Industrial and infrastructure monitoring can also benefit from the rise of autonomous microsystems. If the size of these particles is reduced to a cell-size scale, these microsystems can easily obtain enough energy from vibrations, temperature gradients, light, or electromagnetic fields to function. Such energy sources are very common in industrial environments making these devices very suitable for use in such scenarios. Cell-size autonomous microsystems can be embedded in structures to monitor stress, detect failures, and predict maintenance needs, thereby preventing catastrophic failures and extending the lifespan of critical infrastructure.
- Scientific Research: In biological research, cell-size autonomous microsystems can significantly advance *in vitro* and *in vivo* measurements by allowing precise and localized sensing. This could provide insights into cellular processes, enabling breakthroughs in our understanding of life at the microscopic level. For instance, in [4] a tiny microsystem to monitor cellular temperature was presented. Many diseases, such as cancer, are characterized by abnormal metabolism, leading to changes in cellular temperature. Consequently, [4] could be used to detect diseases at the cellular level. Another example of using these microsystems in research is given in [6], where a microparticle was demonstrated to record neural activity in living animals *in vivo* while causing minimal

tissue damage.

- Smart Farming: As the global population continues to grow, the demand for food quality and production efficiency is increasing. This research branch can enhance precision farming techniques by providing detailed data on soil conditions, crop health, and microclimatic variations. Cell-sized autonomous microsystems have recently appeared, [10], demonstrating high sensitivity to putrescine. This is an organic compound highly present in the plants' tissue and directly correlated to parasite infections. The detection of a reduction in the normal putrescine concentration level at an early stage can help farmers treat plants accordingly. Hence, the number of infections can be significantly diminished.

In general, the introduction of cell-size sensing nodes into previously inaccessible locations can lead to numerous advances in data collection and monitoring, ultimately contributing to a smarter, more connected world.

In this context, this thesis aims to contribute to this groundbreaking field of research by studying and designing the silicon circuits required in these cell-sized microsystems.

1.3 Autonomous Microsystems Requirements

Although this research branch was put on hold for a long time due to the low maturity at the time of basic pillars such as nanotechnology, microelectronics, and wireless communication, it has experienced a revival in recent years. Several autonomous microsystems have already been demonstrated. Despite their diverse applications, they share common requirements. For a general-purpose *smart dust* monitoring system, several building blocks are mandatory:

- A power supply is needed to power up the whole system, which can be either a harvester, a capacitor, or a battery.
- A sensor to measure a certain magnitude.
- A power management unit (PMU) in charge of starting up the circuit, generating the bias currents and voltages, delivering regulated power to the core to operate with precision, checking that everything is at the correct operating point, etc.
- A communication building block that integrates a transmitter, such as an antenna or an LED, and some kind of logic to convert the signal sensed by a sensor into the most convenient communication protocol. The topology of this subsystem depends very much on the type of application targeted.

As the name implies, the most obvious feature of these systems is their complete autonomy. This means that they have the ability to operate and communicate without relying on external power for a certain period of time. However, achieving this becomes a challenging task when the size of the system needs to be pushed beyond commercial standards. Conventional solutions such as using commercial batteries are no longer an option. Instead, energy harvesters, ultrasmall batteries [11], and supercapacitors [12] show up as the best way to address this issue.

A very elegant, as well as optimized energy harvesting option is radio-frequency identification (RFID) [9, 13, 14] where the same physical component, an antenna, is used to supply power to the system and to communicate with the outside world simultaneously. However, it is not currently feasible to reduce the area from approximately 0.5 mm^2 or lower the peak power consumption from a few mW when transmitting information, as demonstrated by the smallest integrated RF coil presented in the literature [9].

In the case of a thermal gradient is present in the application, such as industrial electronic devices, automobile engines or human body to ambient air for wearable devices [15], a silicon-based thermoelectric-generator becomes a serious option to consider. It can deliver around 10-100 $\mu W/cm^2$ [16], which may not be a very high-power density but can certainly cover applications that do not require high power or those that are not too constrained in area.

Another remarkable solution is solar cells, which have the best power density among the most common energy harvesters. As demonstrated in [17], photovoltaic cells can deliver 100-400 $\mu W/mm^2$, generating over 100 times more power than other transducers that rely on heat, motion, and radiation.

Other transducers based on motion convert mechanical energy into electrical energy. This is the case of piezoelectric harvesters which come with the downside of being very bulky for what is required in *smart dust*. Most of the fabricated devices are in the range of a few hundred of mm^3 [18], which leaves them clearly out of the cell-size microsystems scope.

Some microsystems have opted for an ultra-small battery approach, with the smallest reported battery being 1.69 x 1.1 x 0.15 mm^3 in size and having a capacity of approximately 10 μAh [11]. This battery was later used in [19]. While this approach produced good results, the battery's low power output meant that other energy harvesting sources were required as backups, leading to a complex power management and integration design.

In [12], a microsystem powered up by a capacitor was demonstrated for a 15-minute life target. The main focus of the design was to be able to measure under the huge and very stringent voltage variation range provided by the capacitor (1.8-0.3V). Due to this, the system was designed for the specific purpose of discriminating between two input values, and therefore the complexity and precision of the system were given up.

The power consumption of autonomous microsystems is restricted either by the small and limited power source used in energy harvesters or the targeted duration of operation for devices powered by a capacitor or an ultra-small battery. These systems are generally conceived to operate in the range of a few nW to μW. Because these power sources are very weak, they can collapse if the current demanded exceeds certain limits, causing a critical voltage drop that can shut down the system unintentionally. For this reason, it is important not only to keep the average consumption within affordable limits but also to monitor the peak power consumption carefully during the transients. Even if these peaks are not large enough to cause the system to collapse, they can cause variations in the supply voltage that can affect the precision with which the system operates, and this may or may not be permitted depending on the application. Considering all these points, one common requirement for all of these systems is to be able to operate over a wide voltage range to endow it with some robustness. As a consequence, other than the applications where high precision is not required

like [12], most of the systems developed employ a PMU to perform a power conversion from the output power generated by the power source to a very stable and robust voltage for the core electronics. Some of them are just a voltage or a current reference [6], at their simplest expression. In contrast, others are rather complex, like the one proposed in [19], where a battery and several harvesters coexist, requiring a dynamically adjustable DC-DC converter in charge of up-conversion during harvesting and down-conversion in the absence of harvesting conditions. At the same time, it must be able to supply regulated power over more than 1000× load variation range.

Of course, complexity comes with the trade-off of size. Most autonomous electronics today have macroscopic dimensions due to insufficient energy storage and integration challenges at the microscale. However, this macroscale reduces the range of applications that can be targeted. *In vivo* or *in vitro* applications, smart paints for multiple different surfaces, smart clothes, or sensing systems that blow in the wind are examples of what going beyond the size barrier in electronics could mean.

The reference volume for microsystems of this kind is the cubic millimeter, as established by [9],[19]. However, even a cubic millimeter is too large for certain applications, such as *in vivo* procedures like [6]. In such cases, tissue damage has been reported even with 80 μm-diameter electrodes.

Pushing the size limits to enable new functionalities may help to achieve important breakthroughs but as a counterpart, it brings more complexity to the communication task. Ideally, it is desired that the system can communicate wirelessly with the outside world but when you put together ultra-small size and ultra-low power consumption, this becomes a hard mission. Some fabricated systems [12] avoid facing this problem directly by communicating through probe tips directly placed on top of very small pads. RF is a feasible solution when the area is not too stringent [9]. However, for structures that aim scales in the order of 100 μm and beyond, it is very difficult to create efficient RF wireless communications, as the antenna size is small compared with typical wavelengths, leading to low directivity. Optical wireless communication is one of the most employed solutions [4, 6] since it scales the best on area and efficiency.

Last, we would like to mention that the implantation and passivation of these autonomous microsystems is a topic outside the scope of this thesis. The interface between devices fabricated in modern CMOS processes with biological systems is the focus of intense research, being a matter that requires careful engineering, especially when targeting *in vivo* scenarios. It brings to the table some concerns, such as the development of a long-lasting biocompatible coating [20] as well as the opacity and transparency for the areas that are sensitive to light.

1.4 Design Strategies

In order to satisfy the very stringent constraints of area and power consumption several well-known strategies were considered.

First of all, selecting the right technology is crucial. In comparison to bipolar junction transistor (BJT), a CMOS-only approach is a more power-efficient solution. This is because

BJTs require an additional current at the gate terminal, especially at low frequencies, which is not the case with CMOS. Moreover, CMOS transistors are smaller and require less area than BJTs because they have one less junction and a much better-developed fabrication process. Another key advantage of using MOS transistors is that they introduce less noise, which is a key factor to consider when designing low-power applications.

Using a deep sub-micron CMOS technology is a decision that benefits both area and power consumption. Smaller transistors result in a smaller footprint, and also reduce parasitic capacitances, which in turn reduces the amount of current needed to fulfill them. However, there are some drawbacks to consider from both transistor and system perspective.

From a device point of view, short-channel effects can occur. To cite a few, the output resistance can be greatly reduced due to a more significant channel length modulation effect. Additionally, drain-induced barrier lowering can reduce the threshold voltage as the drain-to-source voltage increases, further lowering the output impedance. Hot carriers are also an issue that process engineers frequently face.

In addition, some technologies offer specific design advantages that must be taken into account as well. For instance, FDSOI offers reduced parasitics and leakage, along with the potential for back-gate biasing. This feature is particularly beneficial in analog designs, where back-gate biasing can enhance parameters such as gain, power supply rejection (PSR), and bandwidth. It can also be used for trimming purposes or to reduce the width of devices while maintaining constant current levels.

However, in the context of *smart dust*, a large number of sensors must be manufactured and deployed where the application requires them. This leads us to prioritize the economic aspect more than other features. Economically speaking, the cost of manufacturing increases exponentially with smaller nodes and more complex processes.

In this thesis, we have chosen a 65 nm CMOS technology for the two tape-outs that support the contributions of this work. This technology provides a good trade-off between the price per mm^2, and the area and power reduction achieved with respect to larger nodes, and the second-order effects, which are not too severe for this technology given our design purposes.

Another important strategy for low-power and low-area applications is to resort to the use of a resistor-less design. Integrated resistors in conventional technologies have very low sheet resistance, which means that they require a lot of area if low currents are requested. Additionally, these integrated resistors lack accuracy and can introduce mismatch and variability issues into the design. However, following this guideline can increase the complexity of the design.

Working with ultra-low frequencies becomes another possible and interesting approach to reduce power consumption at the cost of reduced computational speed. Nevertheless, most *smart dust* systems have very low computational requirements. However, this becomes such a hard task when using deep sub-micron nodes because ultra-low frequencies require very large time constants, which would lead to large passive devices in a straightforward approach.

Finally, sub-threshold biasing is a commonly used technique in low-power designs. This technique allows working at extremely low currents, which is more current-efficient for

transconductance than the strong inversion region. Transconductance is a crucial parameter in analog designs, and the optimal performance is achieved at the edge of the weak inversion region. However, working with such low currents can result in increased sensitivity to process, voltage and temperature (PVT) variations.

1.5 Design Methodology

In this thesis, we adopted the full custom design flow shown in Fig 1.1 to enhance the robustness of the design process. All the circuit designs and simulations were performed using the professional IC design software Cadence Virtuoso IC 6.1.7.715.

The design flow in Fig. 1.1 is a process in which the designer must iterate within a stage or even return to the previous stages until the results are valid. For clarity, no return loops are shown in Fig. 1.1.

Once the system specifications are established, the design flow starts with the schematic entry stage. This stage involves extensive research to select a circuit topology whose features best fit the specifications. A functional simulation then follows to ensure the selected topology works properly and meets the specifications. It is necessary to remark that in our case all the simulation models used in this thesis follow the long-channel transistor equations. This approximation is valid for us because the channel lengths of the most sensitive devices in the circuit are significantly larger than the minimum channel length of the technology.

The initial sizing of the devices might be sufficient to meet all the requirements in the typical scenario. However, this does not guarantee that the circuit can operate if PVT variations occur.

As transistors get smaller and voltages decrease, the effect of variations becomes more pronounced. Hence, a variability-aware design stage is required.

Process variations can be categorized as inter-die or intra-die. The foundry provides models to simulate the circuit across both types of process variations. Corners simulations allow us to understand the effects of maximum inter-die variations, while Monte-Carlo simulations do the same with intra-die variations.

At this point, a sizing refinement is usually needed to improve the circuit performance across PVT and/or to maximize chip yield meeting the specifications. Therefore, a design centering (Fig. 1.2) is conducted, where certain over-performing specifications are normally sacrificed to ensure that the circuit will always meet all specifications regardless of PVT variations.

Once the sizing has concluded, the physical design begins. A schematic-driven approach is used initially to minimize errors and ease the subsequent verification. This approach allows the designer to pre-populate the layout with correctly sized devices and to identify the routing to be done, among other things. The layout is then completed manually. The physical design of the circuit can have a notable impact on the performance. Hence, layout theory should be studied within this stage to be aware of the most significant layout-dependent effects and the different approaches to mitigate them. Proper placement and interconnection must be performed so that the circuit behaves as closely as possible to the pre-layout simulations.

After the layout is complete, the design needs to be verified. The manufacturability is checked by the design rules check (DRC). On the other hand, the layout vs. schematic (LVS) ensures that the layout circuit matches the schematic netlist previously defined. Last, parasitics are extracted, and a post-layout simulation is run to check if there is any major deviation when accounting for the physical design effects. If so, further iterations must be done around the layout stage or even the sizing stage if required.

Once the complete system layout is ready and verified, the tape-out process starts. First, floor planning is required to optimize the available die area as well as to avoid undesired effects such as cross-talk or unbalanced jitter. Next, an appropriate input/output (I/O) ring is assembled to meet the needs of the chip. Last, during this phase it is convenient to communicate with the foundry to ask for any relevant information about the chip design, such as if some DRC rules can be intentionally ignored, as was the case with us.

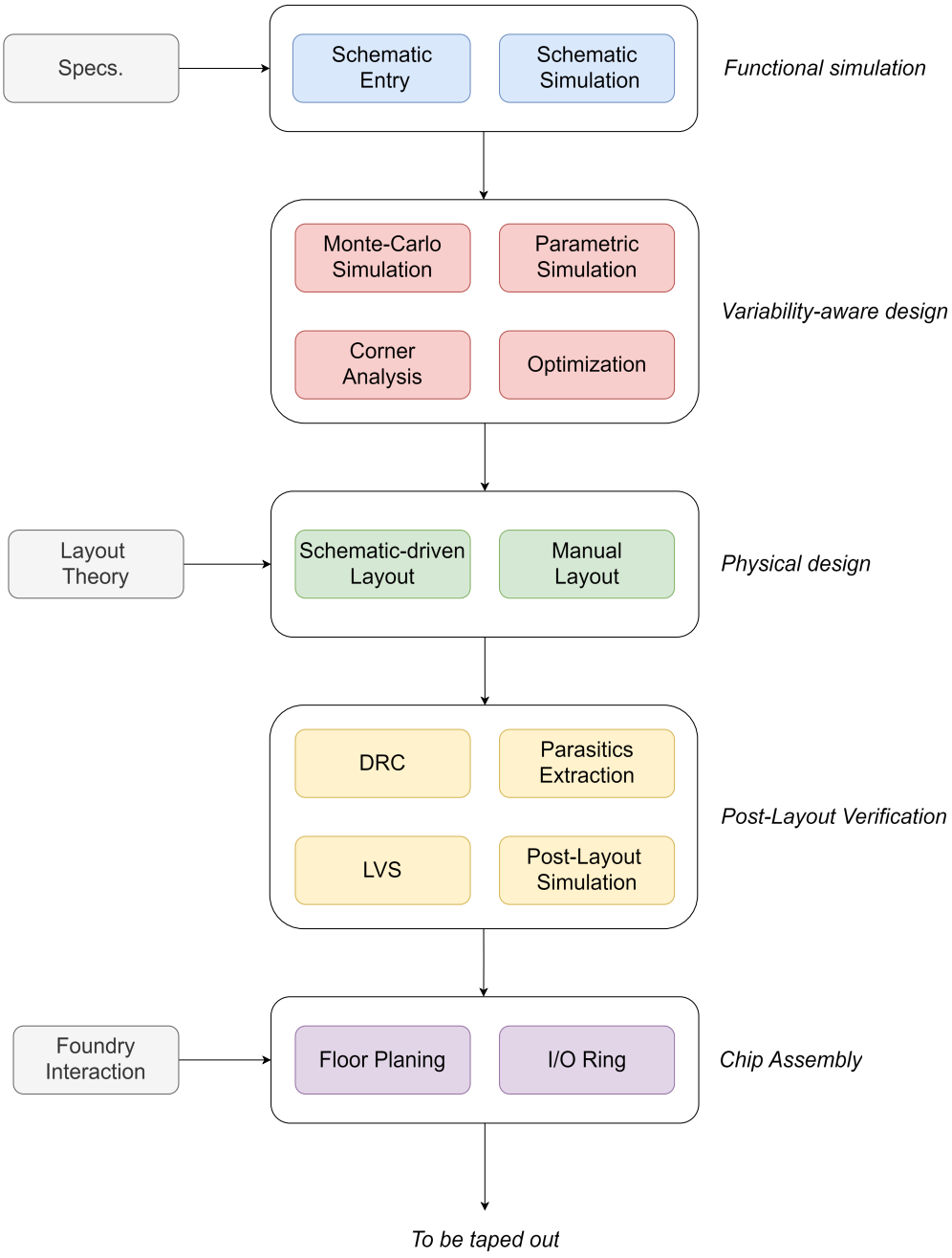

Figure 1.1: Full custom IC design flow.

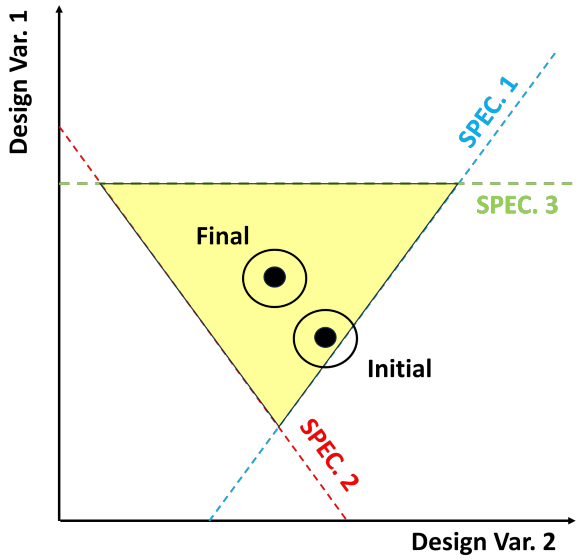

Figure 1.2: 2D representation of design centering.

1.6 Physical Design General Guidelines

Analog layouts are characterized by requiring strong device matching as well as different techniques to avoid layout effects that might degrade the circuit performance. These layout effects become more significant when using deep sub-micron technologies, such as the 65 nm CMOS technology used in this thesis.

To ensure a robust physical design and mitigate layout effects, the following guidelines have generally been followed in this work.

1.6.1 Device Implementation and Placement

- Minimum-size devices were avoided in the critical parts of the design since they might experience greater deviations during the fabrication process, consequently affecting the overall yield.
- When ratioed devices are required in a design, such as in a current mirror, using different transistor sizes would result in an uneven ratio due to the limited fabrication process precision. Instead, it is better to keep all sizes the same and unfold a device as many times as required to set the ratio. With this approach, process precision is no longer a limiting factor.
- In the case two transistors need to have a diffusion electrically connected, the transistors can be abutted so that they share the same physical diffusion. By this means parasitic capacitances and resistances are reduced and some area is saved.
- In general, the device placement in this work prioritizes minimizing the space occupied while maintaining functionality and manufacturability.
- All devices were put in the same orientation in the layout for better matching. Gradients in the fabrication process would affect unevenly devices with different orientations.
- In structures that needed to be critically matched, common centroid and interdigitation were applied. Symmetry with respect to an axis cancels the variations produced by linear gradient deviations of the fabrication process.
- It is known that the doping profiles near the well edges are not totally abrupt. Instead, there is a certain gradient in which the doping concentrations are not at their ideal levels. Consequently, if any transistor is placed in the neighboring of a well edge it can suffer a significant deviation of its threshold voltage. This is called the well proximity effect (WPE) and, in some cases, variations up to 50 mV from the nominal value have been observed [21]. To minimize this effect, implementing transistors close to a well edge was avoided when possible. At the same time, those transistors that required matched V_{th} were placed equidistantly to the surrounding well edges.
- Shallow trench isolation (STI) is the most common method of isolating transistors in deep sub-micron technologies. The trenches are inserted in between active areas introducing mechanical stress as a side effect. This stress compresses the crystalline structure at the channel which reduces the carriers' mobility in NMOS transistors and

increases it in the PMOS transistors. This effect becomes more pronounced the shorter the distance from a device to a trench is and the smaller a device is [21]. If the size of the transistor cannot be modified, there are two techniques to minimize this effect. The length of the diffusion can be extended or a dummy device can be placed next to the active device. Both methods move the trench away from the channel. However, the first requires less extra area for the same effect, while the second adds a lower parasitic capacitance to the diffusion. The first method was implemented in this design when accurate or matched mobilities were required.

1.6.2 Routing

- Minimum-spaced and minimum-width wires were avoided as they make it difficult to reproduce of a given pattern, resulting in increased process inaccuracy.
- A reduced count of vias between metal layers may become a bottleneck to the current in some cases. This can eventually turn into a potential origin of failures. Every metal layer interconnection was carried out through multiple vias to mitigate any related issues.
- Polysilicon routing was avoided for medium and long-distance interconnects because its sheet resistance is much higher than the metal layers. Otherwise, the design could suffer from IR drop issues.
- Wide higher metal layers are used to distribute the power supply across the chip as they provide the lowest sheet resistance of all available layers.
- Symmetrical connections are made when possible, but especially in those structures that require higher matching.
- When the current density in a connection exceeds a certain limit the electrons can displace the atoms causing an increased resistance in the connection or even the total rupture of the wire. This effect is called electromigration and it can lead to unrecoverable errors at its worst. Hence, all the connections in this Thesis were made wide enough not to incur electromigration according to the foundry guidelines.

1.6.3 Reliability and Manufacturability

- When possible, small-feature patterns were avoided to improve the manufacturability.
- During the fabrication process, polysilicon, metals, and vias etching are usually done through plasma etching (such as *reactive ion etching*). This can result in a temporary charge accumulation in the conduction paths which may lead to a rise in the potential. The thin gate oxide can be damaged if the voltage on a path directly connected to the gate exceeds a certain limit. This is also known as the "Antenna effect" since the quantity of collected charge depends on the size of metal and polysilicon structures, which serve as an "antenna", connected to the gate. In this Thesis, the bridging technique was used to avoid gate damage in lighter cases. However, when the amount of metal area connected to a gate was too large to be solved with bridging, reverse-biased diodes were

connected to the power and ground rails to provide a harmless discharging path.

- In a similar manner, electrostatic discharge can break gate dielectrics due to an excessive accumulation of charge. For this reason, every device directly exposed to any interaction or with the outside world was protected with ESD diodes.
- The latch-up effect can manifest when transient voltage differences appear at the substrate. If these voltage spikes are large enough, parasitic bipolar transistors, formed between NMOS, PMOS and n-wells, can unleash a positive loop that may bring the circuit to an unrecoverable failure. To prevent this from happening, all NMOS and PMOS are laid apart and enclosed by their respective guard rings. Additionally, some noisy devices directly connected to an I/O pad, which are prone to trigger the latch-up, were surrounded by their own guard ring.
- The chemical-mechanical polishing of metal layers can result in "dishing". This may increase the connections' resistance and cause possible issues in ulterior lithography and etching processes. Dummy patterns were included in the layout design to minimize this effect.

1.7 Objectives and Specifications

Our aim in this thesis is to contribute to the development of cell-size autonomous microsystems by studying and designing the most frequently needed circuitry within these systems.

A special case of autonomous microsystems is the *SynCell* [10], a tiny autonomous microsystem (50×50 μm^2) developed at MIT, that assembles, through heterogeneous integration [22], a variety of building blocks such as 2D material-based sensors, iron magnets for actuation, and GaN LEDs and solar cells for communications and energy harvesting. They were conceived to operate in *in vitro* applications and they will be described in detail in chapter 2.

Throughout this thesis, we collaborated in the design of the second generation of *SynCells* as a way to demonstrate sensing capabilities in the microscale. Unlike its predecessor, the second generation of *SynCells* has improved the functionality including a wireless communication interface and a tiny control. This is done in a CMOS *Si* chip that must achieve the following requirements:

- The *Si* chip must serve as the carrier for the energy harvester, the sensor, and the optical communication block.
- *SynCells* look for pushing size boundaries in electronic particles. Consequently, the *Si* chip cannot occupy more than the integration space required for the previously mentioned blocks (i.e., solar cell, sensor ...), which was restricted to 50×50 μm^2.
- The *Si* chip must be powered with a maximum of 100 nW coming from a solar cell.
- The main functionality of the chip is to convert the sensor's analog voltage into electrical pulses of variable period. Then these pulses drive an light emitting diode (LED) to transmit the information to the outside world. To facilitate the receiver task of capturing the light and decoding the information, the total pulse length needs to be on the order

of micro- to milliseconds.

- The *Si* chip is also responsible for delivering a PVT-stable voltage to the sensor to suppress potential sources of errors such as the fluctuation in the voltage provided by the solar cell.

Although the ultimate goal of the *Syncell* project, in which this thesis is emplaced, is to develop a complete microsystem aimed at in vitro measurements applications, this thesis focuses only on the design of the CMOS circuitry needed for the microsystem whose main building blocks as well as its main function will be detailed later in the document. The remaining parts of the microsystem (sensor, power supply, transmitter and heterogeneous integration) will be developed by the Microsystems Technology Laboratory (MTL) research group at Massachusetts Institute of Technology (MIT) as a result of the collaboration between MIT and Universidad Politécnica de Madrid (UPM).

1.8 Document Structure and Contributions

This thesis document is organized into six chapters:

- Chapter 1 has presented an overall explanation of the *Autonomous Microsystems* research branch, exposing its breakthrough potential, that motivated this thesis, and the general requirements of these microsystems.
- Chapter 2 gives a detailed description of the *SynCell* microsystem, in which context this thesis is mainly placed. This chapter describes each module that integrates the *Syncell* and the requirements and constraints they impose on this work.
- Chapter 3 presents the two different PMUs designed for cell-size autonomous microsystems.
- Chapter 4 presents the voltage-controlled oscillator (VCO) designed for the *SynCell* as a method to achieve a time-domain digitization with ultra-low area and power consumption.
- Chapter 5 shows the electrical global verification of the CMOS *Si* chip designed in this thesis for the *SynCell*.
- Chapter 6 ends this thesis document by drawing some conclusions and explaining the potential opportunities for future research following this thesis.

The work performed during this dissertation has resulted in the following contributions in the form of peer-reviewed publications:

[23] Javier de Mena Pacheco, Tomas Palacios, Marek Hempel, and Marisa Lopez Vallejo. A highly linear ultra-low-area-and-power CMOS voltage-controlled oscillator for autonomous microsystems. *Micromachines*, 15(10):1193, 2024.

[24] Javier de Mena Pacheco, Juan Manuel Carrillo, Palacios, Tomas and Marisa Lopez Vallejo. A highly power- and area-efficient PMU for cell-size autonomous microsystems. IEEE Transactions on Circuits and Systems I: Regular Papers, 2024.

[25] Javier De Mena Pacheco and Marisa Lopez-Vallejo. A 65nm current and voltage reference with improved line regulation for implantable biosensors. In 2021 XXXVI Conference on Design of Circuits and Integrated Systems (DCIS), pages 1–5. IEEE, 2021.

Chapter 2

SynCell Autonomous Microsystem

2.1 Introduction

Shrinking energy harvesting, communication, and sensing capabilities to sizes below 1 mm^3 has provided cell-size autonomous microsystems with disruptive potential. The development of these tiny devices can significantly transform how and where data can be collected.

When the concept of these autonomous sensing nodes was first introduced [1], the necessity for several low-matured cutting-edge technologies to converge, including nanotechnology, microelectronics, and wireless communication, forced this research branch to be put on hold.

With the continuous advances in these required technologies, *smart dust* has regained interest again as its feasibility has become real. Since the idea was presented, impressive advances have been reported and many autonomous microsystems have been achieved. In particular, the MTL at MIT has focused on the development of the *SynCell* [10]. The *SynCell* is an autonomous microsystem designed to showcase microscale sensing capabilities.

In this thesis, we collaborated with MIT in the design of the second generation of *SynCells* developing a cell-sized *Si* controller for the aforementioned microsystem.

2.2 *SynCell* Description

A special case of autonomous microsystems is the *SynCell*. This tiny autonomous microsystem developed at MIT integrates various components through heterogeneous integration [22], including 2D material-based sensors, iron magnets for actuation, micro-LEDs for optical communication, and solar cells for energy harvesting. They were initially intended for in *in vitro* applications (Fig. 2.1), such as localized chemical sensing.

In particular, the sensor assembled in the *SynCell* demonstrated high sensitivity to certain amines, such as putrescine. Putrescine is an organic compound present in all organisms [26]. In meat or fish, its concentration rises when decomposition starts, hence, becoming a natural bioindicator of food quality [27]. Additionally, putrescine can be indicative of cell proliferation and cell growth [28]. In this way, it is especially relevant in plants [29]. The

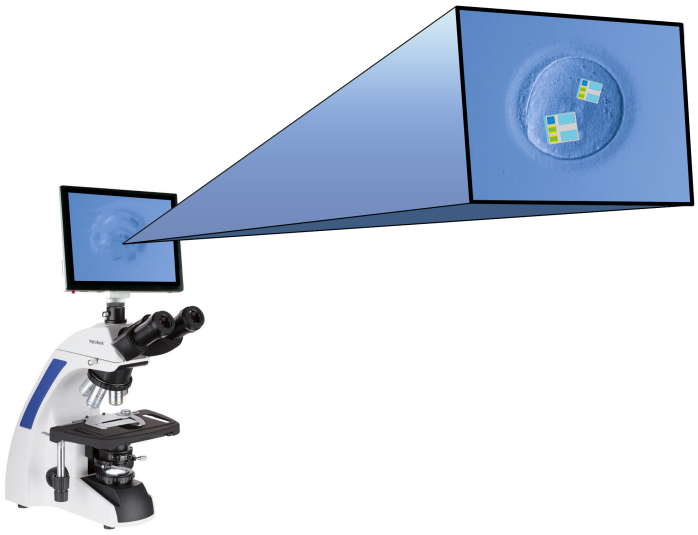

Figure 2.1: A potential use case example of the deployment of *SynCells* next to an ovum for invitro measurements.

absence of putrescine in plants is associated with an increase in both parasite and fungal populations. The application of putrescine and other polyamines can extend the shelf life of fruit by delaying the ripening process. Pre-harvest application of putrescine has been shown to increase plant resistance to high temperatures and drought. As a result, autonomous tracking of putrescine concentrations in a very localized manner shows plenty of beneficial use cases.

The first generation of *SynCells* [10] contained, in an area of 60x60 μm^2, iron magnets for magnetic placement, an MoS_2 sensor, and pads to extract the information. After the deployment of the *SynCell*, the chemical sensor changes its conductance according to putrescine concentration (in air or water). The slow recovery time of the sensor allows for passively storing the concentration. After sensing, these microparticles need to be retrieved, with the help of a magnet, to be electrically energized through the pads and lately extract the measured information. Once a supply voltage is provided to the microsystem through a probe station, the changed conductivity in the sensor is converted into an analog voltage, by means of a voltage divider. Eventually, this voltage becomes the readable signal that contains the target information.

The read-out interface of the first generation of *SynCells* constituted a clear limitation to their applications since they required to be recovered from the deployment place. In the second generation of *SynCells*, extended functionality was aimed at a reduced area of 50x50 μm^2. The pads were substituted by an LED, to allow for wireless optical communication, and solar cells, to provide power to the system. A silicon chip was included to regulate the power generated by the solar cells and drive the LED. In this way, the LED is blinked at a pace

proportional to the sensor's output voltage to transmit the information. Additionally, the silicon chip serves as the carrier for the rest of the system to be heterogeneously integrated on top of it. The main building blocks in the system are shown in Fig. 2.2.

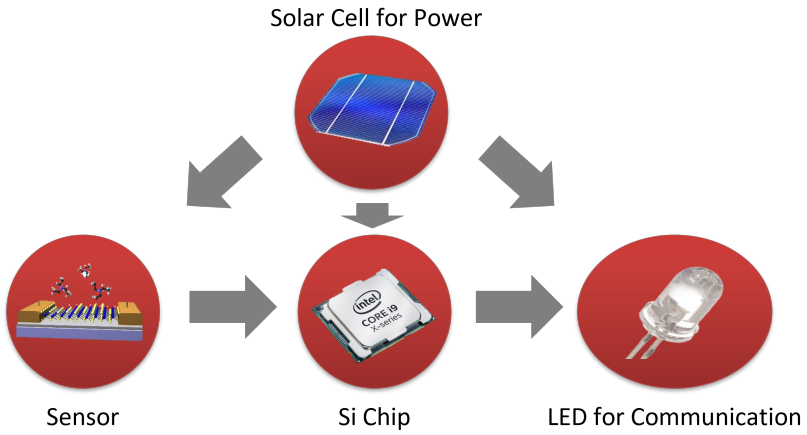

Figure 2.2: Building blocks of the second generation of *SynCells* (© Marek Hempel, MIT).

2.3 State of the Art

Prior to this thesis, several autonomous microsystems, that share similar characteristics to the second generation of *SynCells*, have been demonstrated. However, they all stayed over the 100 μm size barrier mainly due to the power constraint.

Different methods of energy harvesting have been utilized for the power source. However, the electric energy that can be stored or harvested in a microsystem thinner than a human hair ($\sim$100 μm) is severely limited. This has constituted one of the main constraints that have kept most of the published microsystems above the 100 μm barrier. Solar cells stand as the energy harvester that scales down in size with the best power efficiency ($\sim$ 20%). They have been used in numerous autonomous microsystems with very different applications, including *in vivo* scenarios using the incident light in a human eye [9] or the scattered light in a mouse brain [6]. More general-purpose applications have also utilized this energy source such as in the temperature sensor reported in [19]. Nevertheless, their sizes do not usually descend below 50x50 μm^2 as the generated power would become insufficient in many cases. Hence, resulting in a challenging design scenario when targeting ultra-small sizes.

At the same time, several microsystems have been published with optical communication blocks similar to the approach followed by the *SynCells*. For instance, the microsystem presented in [4] includes an LED that was used for optical communication. They made an impressive effort to reduce the power consumption of the whole system to just 16 nW, which meets perfectly the requirements to work with weak energy harvesters. However, to establish optical communication significantly higher peaks of power were required, hence a 100 pF capacitor was integrated on-chip to accumulate charge for burst transmission. Besides, the decision to add some complexity to the communication, such as bi-directionality, resulted in the need for a cortex-M0 processor. These two integrated blocks, the capacitor and the

processor, constituted their main limiting factor for further area reduction occupying a total of 360x400 μm^2.

A much more reduced system, that also uses an LED for optical communication, was described in [6]. In this case, this microsystem had a more relaxed power budget of 1 μW. Unidirectional communication was developed allowing for a compact area of 250x57 μm^2.

Such reported sizes still restrict the deployment of these tiny microsystems inside of, for example, microfluidics channels or blood vessels. At the same time, they are also larger than the biggest human cell (ovum, $\sim 100\mu m$), which may impede the possibility of single-cell interaction.

After analyzing the communication blocks in [4] and [6], we found that both microsystems use a charge pump with large capacitors to drive the LED. This approach came from the necessity of elevating the harvester's nominal voltage over the turn-on voltage of the LED while supplying enough current to make it emit light. Nevertheless, the large size of this building block became a bottleneck that kept these two systems away from being further reduced.

2.4 Objectives and Specifications

The second generation of *SynCells* is desired to show, within a cell-size scale, four core functionalities: energy harvesting, sensing, computation, and communication. The high-level description of what the microparticle is intended to do is as follows:

- Operate in air or liquid.
- Be integrated within an area of $50 \times 50\mu m^2$.
- Be powered by light (e.g. microscope, laser, or ambient light) using a solar cell.
- Measure chemical concentration using a 2D material chemiristor. In the first version of *SynCells* the sensor was sensitive to amines. However, any kind of sensor that changes its resistance can be valid as long as it satisfies the power and area constraints.
- Convert the sensor's voltage into electrical pulses variable period.
- Use electrical pulses to drive an LED to carry out optical communication.

2.5 Building Blocks Description

2.5.1 Power Supply

Luminous energy was selected as the power source for the target microsystem since solar cells have proven to perform with the best efficiency among micro-scale energy harvesters.

Solar Cells Operating Principle

At its simplest form, a solar cell is a PN junction. Similarly to every other PN junction, there is a large doping concentration difference between both regions that makes, due to the diffusion principle, the majority charge carriers flow into the opposite region. As a consequence of this process, the closest region to the junction gets depleted of carriers, thus ionizing the atoms present in that area (Fig. 2.3). As a result, a built-in electric field is generated across the junction. This built-in potential, E_{bi}, forces a drift current opposite to the diffusion current, which, in the steady state, compensate each other resulting in a zero net current state.

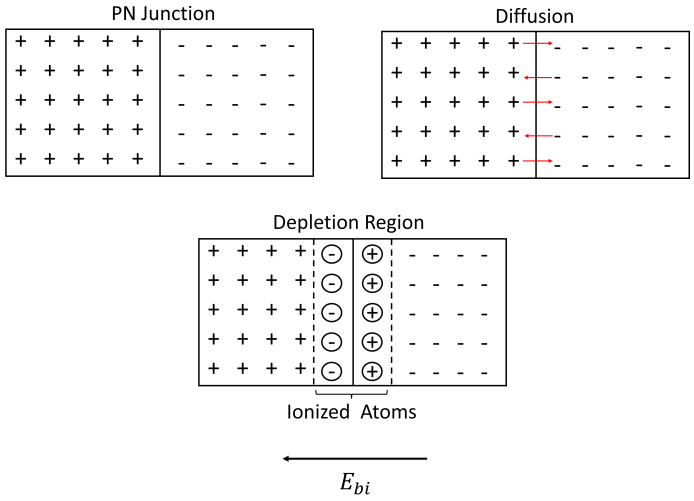

Figure 2.3: Depletion region formation in a PN junction.

The operating principle of a solar cell relies on the photoelectric effect to disrupt the equilibrium of the drift-diffusion current, thereby transforming incoming light into electrical energy. When light strikes a PN junction, covalent bonds with low energy break apart, creating electron-hole pair (EHP). The light provides enough energy for the valence electrons to break free from the atoms to a depth proportional to the wavelength of the incoming light. Short wavelengths are quickly absorbed (a few micrometers), while longer wavelengths penetrate deep into the cell substrate (hundreds of micrometers).

The minority charge carriers produced on each side of the junction, along with the ones formed in the depletion region, move towards the opposite side as shown in Fig. 2.4. Specifically, only the minority charge carriers generated within the average diffusion length from the depletion region reach the other side and add to the photoelectric current (I_{ph}). The remaining minority charge carriers recombine with the majority charge carriers before they can contribute.

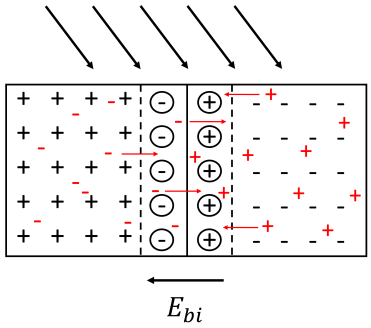

Figure 2.4: Creation of the photogenerated current in a PN junction.

Solar Cells Decisions and Power Budget

The power specifications of the systems were set based on the measurement results of previous fabricated test solar cells.

At first, we attempted to utilize silicon solar cells in the microsystem by integrating PN junctions directly within the same silicon die as the CMOS controller. A single silicon solar cell usually generates around 0.45V in open circuit (no load is connected). To raise the voltage up to a workable value the idea was to stack several solar cells connected in series.

The silicon die substrate, if it is P_{sub}, is typically biased to the most negative available voltage. As a result, none of the physical structures for photodiodes that use the substrate as a terminal can be used, because the voltage at this terminal is already fixed and cannot be changed. In the 65 nm CMOS technology chosen, the only remaining option is the n-well/P^+ diodes, where the n-well serves as the negative terminal and the P^+ as the positive terminal.

A chain of several in-series connected$n$-well/P^+ photodiodes was fabricated in a CMOS chip for evaluation purposes with a scheme similar to Fig. 2.5. Unexpectedly, we found that the voltage did not increase from the first stage on, hence the voltage remained at 0.45 V through the whole chain. This occurs because of a parasitic diode between the n-well region of the second device and the P substrate. The shallow layers allow for the light to reach the substrate and activate the parasitic photodiode easily. As the substrate has a very low doping concentration, the parasitic photodiode is stronger than the actual solar cell for the same given area, and it draws the whole current generated in the previous stage ($I_{b2} \geq I_{a1}$). This prevented the voltage from rising.

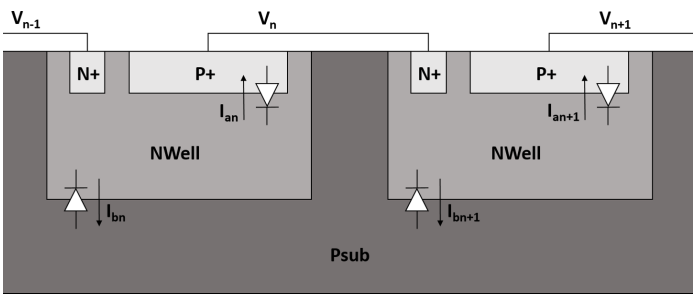

Figure 2.5: Chain of *Si* solar cells connected in series.

A solution to this issue was proposed in [30] and requires increasing the area of the n^{th} stage to make the photogenerated current I_{an} stronger than the losses through the parasitic diode of the $n+1^{th}$ stage (I_{bn+1}). It was also demonstrated in [30] that one stage has to be at least 8 times larger than the following one for the solar cell to reach the correct voltage as is shown in Fig. 2.6.

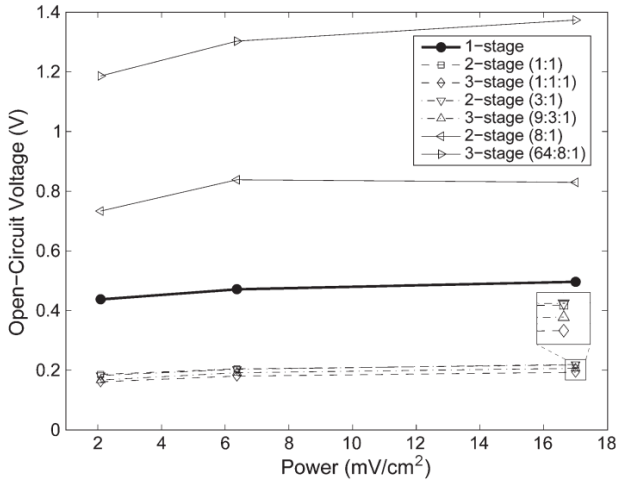

Figure 2.6: Measured open-circuit voltage for different implementations reported in [30].

This issue makes silicon solar cells, integrated within the same die, very inefficient in terms of area and power. Hence this option was eventually discarded. Instead, GaN solar cells in separate substrates arose as the chosen solution. At the cost of requiring a custom fabrication process and subsequent laborious integration, GaN solar cells have a higher open-circuit voltage, which allows to power up easily the majority of low-power CMOS technologies.

A 23×35 μm^2 GaN solar cell was patterned and fabricated at MTL and later characterized with ultraviolet (UV) radiation. Fig. 2.7 shows the experimental results. An open-circuit voltage of around 2.5 V was found along with a short-circuit current of approximately 5.5 μA. [1]

In order for the microsystem to be able to feed on less-energetic light spectrums, such as white light, the measured current under UV radiation, shown in Fig. 2.7, was downscaled 4 times. As a result, a constrained power budget of just 1.2 μA was available to power up the LED, the sensor and the Si controller.

2.5.2 Sensor

The chemical sensor is made of 2D materials such as graphene or MoS_2. Both of them can work as chemiristors, which means they change resistance based on their environment. This chemiresistive behavior is based on the doping of 2D materials from molecules adsorbed on the 2D material surface.

[1] The short-circuit current is the current obtained from the solar cell when the voltage across the solar cell is zero (i.e. when the solar cell is short-circuited).

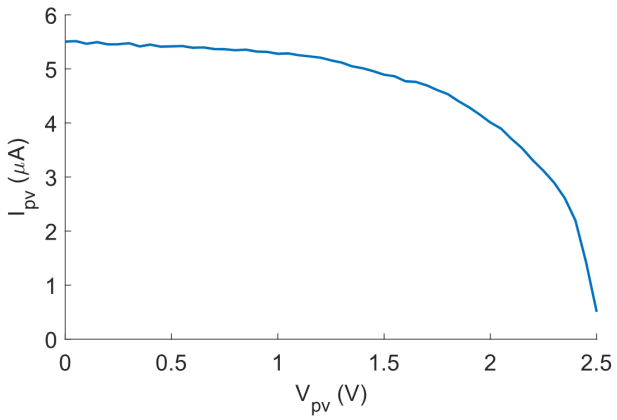

Figure 2.7: Measured I_{pv} vs. V_{pv} of the fabricated GaN solar cell.

MoS_2 was prioritized over graphene since, for the same area, resistances between five to six orders of magnitude higher can be achieved. This choice contributes to limiting the overall power consumption of the system while keeping the area of the system low. The sensor will be integrated on top of the silicon chip occupying an area of 10x25 μm^2.

The resistivity variation is converted into an analog voltage through a voltage divider configuration. Two MoS_2 resistors will be placed in series, one of them open to chemical exposure acting as a variable resistor R_{var} and the other one passivated with a polymer coating acting as a reference resistance R_{ref}. This way, the initial voltage signal is self-calibrated and does not suffer from batch-to-batch inaccuracy due to MoS_2 resistance variation. In particular, the 10x25 μm^2 dedicated for the sensor will be distributed between both MoS_2 devices in a proportion such that the initial R_{var} value is ∼11 times larger than R_{ref}. This would generate a voltage of ∼0.9 V_{dd} in the voltage divider. Assuming a resistance reduction of about 100× after maximum chemical exposure, R_{var} would drop to ∼ 1/9 of R_{ref} generating a voltage of ∼ 0.1 V_{dd} in the exposed state.

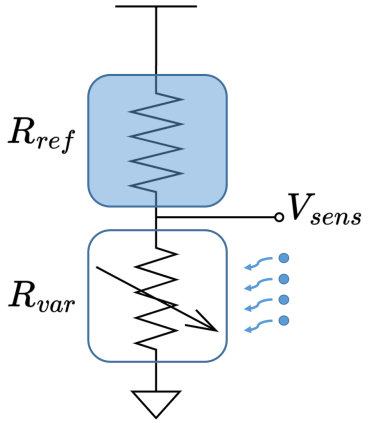

Figure 2.8: Electrical configuration of the sensor.

The typical resistance of the MoS_2 sensors of this size before exposure is around 10 $M\Omega$, and can be reduced by ∼100 times after exposure. For this thesis, we will assume $R_{var} = 10$

$M\Omega - 100\ k\Omega$ and $R_{ref} = 900\ k\Omega$ for the simulations. Consequently, a maximum current of $\sim 1\ \mu A$ is expected when used at V_{dd}=1 V.

This system part constitutes the largest load to which the *Si*-chip must supply regulated power. The sensor takes a few minutes to complete the resistivity change after chemical exposure, and several hours to return to its initial state. This causes smooth load changes that make the *Si*-chip have more relaxed transient response requirements.

The first MoS_2 sensor version was built to detect putrescine, however, any other type of sensor is valid for this system as long as it changes its resistivity and meets the area and power requirements. The MTL is currently working on *pH* and gas detection sensors.

2.5.3 Optical Communication

The microsystem uses a blue 10x15 μm^2 GaN LED to send light signals to the outside world. A test version was patterned at the MTL to be characterized. The measurements revealed that the LED requires a minimum voltage of 2.45 V and a current of 50 nA for the emitted light to be visible.

Due to the high turn-on voltage of μLEDs, using just the harvester voltage is usually not enough. This issue is usually addressed with the inclusion of a charge pump to elevate the voltage generated by the harvester. However, this solution is not valid when aiming for a 50x50 μm^2 system since the large capacitors used in the charge pump would occupy too much.

Instead, this system uses two GaN solar cells ($23 \times 35\ \mu m^2$) connected in series to power the LED. With this configuration, enough voltage is generated to turn on the LED. However, this approach comes with the drawback that the current generated is half of the current that could be produced if just one bigger solar cell ($46 \times 35\ \mu m^2$) was used. This translates into a power budget cut in half, as there is no room for a down converter in the system to effectively harness the full voltage of the two solar cells placed in series.

On the CMOS chip side, the sensor's analog output must be converted into a light pulse of varying duty cycle or frequency. The voltage-to-time conversion needs to be achieved by as few components as possible, prioritizing the area and power consumption over other features such as precision (an error of 1% seems acceptable). A linear conversion is highly desirable as it helps to minimize calibration errors.

Pulse lengths ranging from micro- to milliseconds seem reasonable since detecting 1 μs long pulses has been demonstrated for similar systems [6]. However, slower frequencies were aimed to further reduce the power consumption.

2.6 CMOS *Si* Controller

The block diagram of the second generation of *SynCells* is shown in Fig. 2.9 with the CMOS *Si* controller highlighted in blue. The microsystem consists of two 23x35 μm^2 GaN solar cells, a 10x15 μm^2 GaN LED, and a 10x25 μm^2 MoS_2 chemical sensor placed at the top level of the microsystem. At the bottom, there is a 50x50 μm^2 *Si* controller serving as a carrier to

the microsystem.

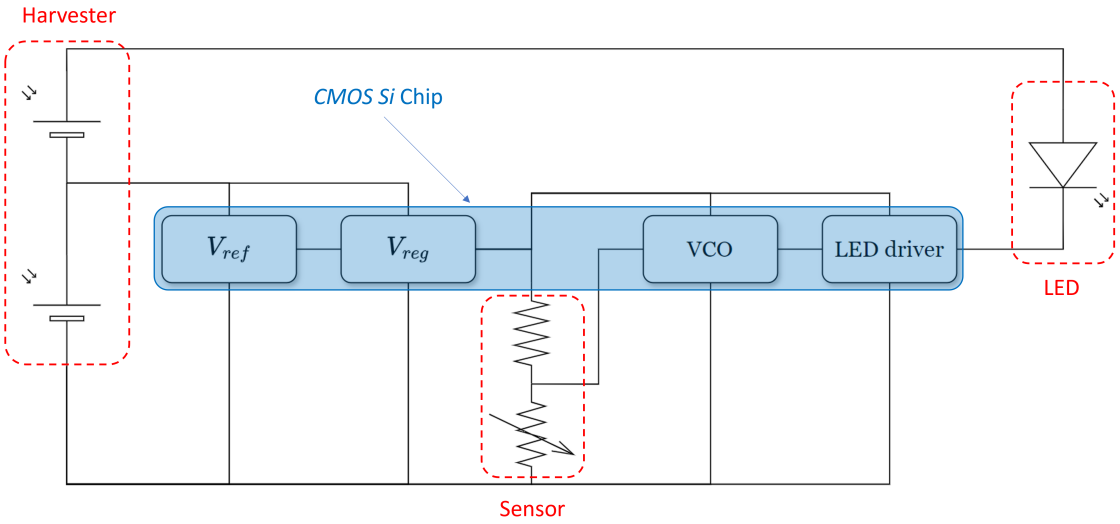

Figure 2.9: Block diagram of the chip in the second generation of *SynCells*.

The two solar cells are connected in series, which would generate an open circuit voltage of around 5 V. When turned on, a minimum voltage drop of ∼2.5 V is expected at the LED. On the other hand, the *Si* controller feeds directly from the first solar cell. Hence, it receives half of the total voltage, which can change significantly depending on the environmental conditions and operating point of the system.

The silicon chip, highlighted in blue in Fig. 2.9, is in charge of reading an analog voltage signal from a chemical sensor, converting it into a frequency-modulated signal, and using this signal to drive a small LED placed on top of the silicon chip. It integrates the following blocks that will be later described in detail within this thesis:

- A PMU, consisting of a voltage reference and a voltage regulator, is responsible for regulating the power produced by the solar cells as well as generating the corresponding biasing for each block of the system.
- A VCO that converts the sensor's output into a pulsed signal with the information linearly encoded in its frequency. The output of the VCO is then used by the LED driver to control the current flow to the LED, causing the LED to flash at a frequency proportional to the measured physical magnitude. In this way, the sensor information is communicated to the receiver, which captures the light pulses with a CCD camera.

2.6.1 CMOS *Si* Chip Interface

A 50x50 μm^2 *Si* platform for the *SynCell* has been fabricated using a 65 nm CMOS technology. The interface to the rest of the microsystem is shown in Fig. 2.10.

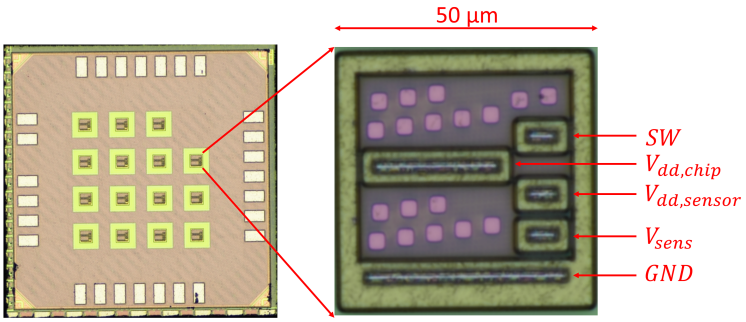

Figure 2.10: *Si* chip interface.

Despite the fabrication of each divisible block of the *SynCell* has been successfully carried out, the assembling is yet to be done. For this reason, we can only show its projected integration in Fig 2.11.

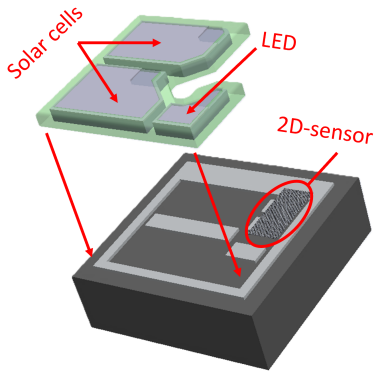

Figure 2.11: Virtual representation of the microsystem integration (© Kevin Limanta, MIT).

The interface of the *Si*-controller has a total of five custom pads to provide electrical connection points to the top-level devices. Additionally, a custom seal ring, shortcutted to ground, was included to surround the layout to provide mechanical support and noise isolation. A short description of each pad is provided in the following table:

Table 2.1: Si-chip connection pads to the *SynCell*.

Pad	Description	Size
GND	Ground connection from the solar cells to the *Si*-chip	46x6 μm^2
$V_{dd,chip}$	V_{dd} connection from the solar cells to the *Si*-chip	30x6 μm^2
$V_{dd,sensor}$	Regulated V_{dd} connection from the *Si*-chip to the sensor	10x6 μm^2
V_{sens}	Sensor's output connection to the *Si*-chip	10x6 μm^2
SW	LED's annode connection to the driver	10x6 μm^2

Chapter 3

Power Management Unit

3.1 Introduction

It is well-known that the precision of electronic circuits relies, among other contributors, on the stability of both supply and biasing sources. Delivering sufficient power to the core circuit while keeping the voltages and/or currents unchanged against the main sources of variability is an issue that every IC designer must face when thinking globally about each of the necessary blocks in the system. Variability normally comes from the power supply, temperature, fabrication process and changes in the operating point of the circuit such as load fluctuations.

Although it depends on the application requirements, the power management unit usually integrates a voltage regulator in charge of the above tasks. There are three main regulator topologies: Switched-capacitor, switching, and linear regulators.

The switched-capacitor regulators [31] also receive the name of charge pumps. They are employed in circuits because of their ability to generate voltages above and below the input voltage. However, their regulation is quite limited, and their efficiency, understood as the power delivered to the load over the power drawn from the source, is also very poor, making this type of regulator suitable only for applications that are not very stringent. These regulators are frequently used in non-volatile memories to generate a high enough voltage for writing and erasing data [32], in RF frontends [14] to convert the RF waves into a DC voltage or in internet of things (IoT) [33] applications among others.

On the other hand, switching regulators [34] are one of the most popular solutions today for many applications due to their very high efficiency close to 100% in some cases. They can raise and lower the output voltage above and below the input voltage and they present better regulation than the already mentioned charge-pumps, however, their need to use inductors is their biggest downside. High inductances require a large area, and quite often these components need to be placed off-chip.

Last, linear regulators [35] are the ones that, by difference, achieve the best regulation among all of them and require a lower number/size of components which translates into a lower area.

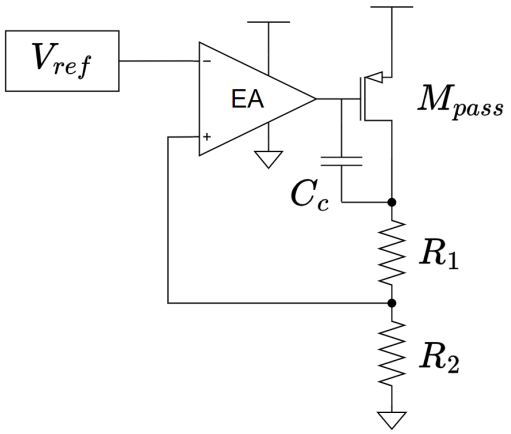

Figure 3.1: Typical linear regulator structure.

However, they can only reduce the voltage coming from the input and when the difference between this voltage and the regulated output increases the efficiency drops immediately. Usually, the decision of which topology to use is made based on efficiency and regulation criteria but, in the case of autonomous microsystems, area comes up as a very relevant factor and must be considered as well. Linear regulators are the topology that provides the best results in terms of regulation and area, making it the best option for the microsystem proposed in this work.

The basic structure of the linear regulator is shown in Fig. 3.1. It consists of:

- A voltage reference (V_{ref}) that provides a stable voltage used by the regulator to set the regulated proportional output.
- An error amplifier (EA), which is a high gain stage responsible for amplifying the deviation of the output voltage from the voltage reference.
- A pass transistor (M_{pass}), which controls the power flow from the input to the output.
- A sampling network ($R_{1,2}$), that feeds back the output voltage, in the correct proportion, to the EA to set the desired voltage value at the output of the regulator.
- A compensation capacitor (C_c), which ensures the stability of the regulator.

The main features that characterize linear regulators can be classified as:

- Static features: power efficiency, line regulation, load regulation and temperature behavior.
- Dynamic features: transient response and start-up time.
- Frequency-domain features: stability and PSR.

These features are discussed in the following sections, which explain the design considerations, trade-offs and challenges that a designer usually encounters when targeting regulators for autonomous microsystems scenarios.

3.2 Static Features

3.2.1 Power Efficiency

Power efficiency is defined as the ratio between the power delivered to the load and the total power drawn from the power supply. Two important features of the regulator play a key role within the context of efficiency. These are the quiescent current and the dropout voltage.

- The quiescent current (I_q) is the current intended to bias the EA, the pass transistor and the sampling network to keep the regulator on, as well as the current required by the voltage reference to reach its stable operating point. Ideally, it is desirable to keep this current as low as possible but its reduction comes together with some speed trade-offs which will be explained in the following sections. In the literature, for good design practice, it is considered that the quiescent current should not exceed 1% of the load current (I_L) [36].
- The dropout voltage, V_{drop}, refers to the minimum voltage difference required between the non-regulated input V_{in} and the generated output for a given load. This voltage drop directly translates into dissipated power that is not delivered to the load. As a result, it is common to use large pass transistor sizes to minimize this voltage drop.

The expression of the power efficiency of a regulator is:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{(V_{in} - V_{drop})(I_L)}{(V_{in})(I_q + I_L)} \tag{3.1}$$

From an efficiency point of view, linear regulators can be classified as high-dropout (HDO) or low-dropout (LDO). The main difference in their structure is that the pass transistor (M_{pass}) is implemented with a PMOS transistor for the LDO topology (Fig. 3.2.a), while a NMOS transistor is used for HDO regulators (Fig. 3.2.b). This has two main implications:

1. An HDO regulator occupies less area than an LDO to deliver the same current because the carrier mobility in NMOS is greater than that in PMOS.
2. The dropout voltage is larger for an NMOS ($V_{drop} = V_{th} + V_{DS,sat}$) than for a PMOS ($V_{drop} = V_{DS,sat}$). As a result, LDOs are more energy efficient than HDOs.

Since in the targeted applications, the currents demanded by the load are, likewise, very low, the size of the pass transistor is not so significant in relation to the rest of the circuit and therefore using an NMOS as the pass transistor does not bring any significant improvement in area. However, since the amount of power generated by the tiny power sources used in this kind of microsystem is extremely limited, it is important to make the most out of the harvested energy. At the same time, these microsystems usually work at low voltages not leaving enough headroom for an NMOS transistor to operate properly. For these reasons, the LDO topology is used in the designs presented in this work.

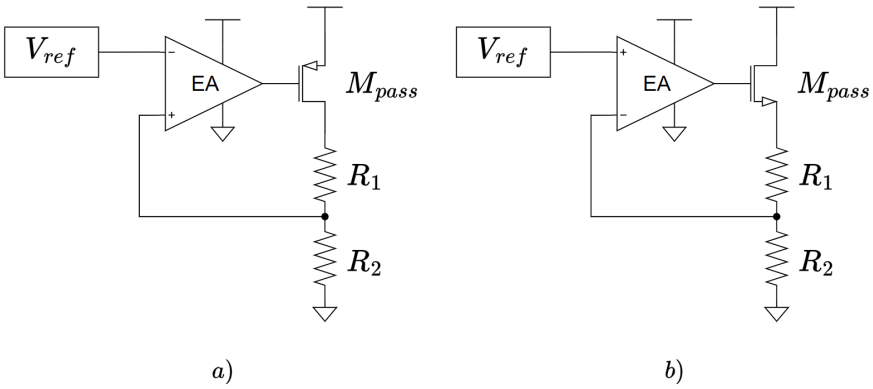

Figure 3.2: General diagram of: a) LDO topology, b) HDO topology.

3.2.2 Line Regulation

Ideally, once the supply voltage is high enough for the regulator to operate, the output of the regulator should remain invariant no matter what the input voltage is. In reality, there is some variation due to the finite EA gain. Line regulation (L_iR) is the parameter that quantifies the ability to mitigate the effect of input voltage (V_{in}) changes on the output of the regulator (V_{out}) once the steady state is reached. The line regulation is expressed as:

$$L_iR = \frac{\Delta V_{out}/V_{out}}{\Delta V_{in}} \tag{3.2}$$

Due to the fragile nature of the energy harvesters integrated into these microsystems, large variations in the supply voltage are likely to occur. Energy harvesters produce very unstable supply voltages, which can change significantly either with varying environmental conditions or with fluctuations in the system operating point. Consequently, special efforts should be made in line regulation, as it is crucial to endow the system with some robustness.

In LDO topologies, the line regulation is determined by eq. 3.3. On the one hand, the EA gain (A_v) and the feedback factor (β) play an important role in the line regulation. This is one of the reasons why high-gain EAs are always desirable in linear regulator designs. On the other hand, the voltage reference also exhibits some variation with respect to changes in the supply voltage. These variations are not attenuated, but sometimes even increased by the feedback, at the output of the regulator. Consequently, special attention must be paid to the voltage reference in order to achieve a good overall line regulation.

$$L_iR \simeq \frac{1}{\beta A_v} + \frac{\Delta V_{ref}/V_{out}}{\beta} \tag{3.3}$$

On the other hand, HDOs, despite not being chosen for this work due to their efficiency downside, it is worth mentioning that with an NMOS pass transistor, an additional layer of isolation with respect to the input voltage is added, since it behaves as a cascode transistor against variations coming from the power supply. In this case, the power supply variation

is attenuated not only by the EA gain, as is the case with the PMOS pass transistors, but also by the intrinsic gain of the NMOS pass transistor ($g_{m,pass}r_o$) following the expression of eq. 3.4. Consequently, HDOs may be an interesting option when line regulation and PSR are a priority and the power efficiency, as well as the voltage headroom, are not major concerns, such as in RF frontend regulators.

$$L_iR \simeq \frac{1}{\beta A_v g_{m,pass} r_o} + \frac{\Delta V_{ref}/V_{out}}{\beta} \tag{3.4}$$

3.2.3 Load Regulation

Similar to the line regulation, the load regulation (L_oR) quantifies the deviation in the output voltage (V_{out}) deviation caused by a change in the load current (I_l), once the steady state is reached. The load regulation is calculated as:

$$L_oR = \frac{\Delta V_{out}/V_{out}}{\Delta I_l} \tag{3.5}$$

The ability of the regulator to keep the output from varying as the load changes depends on the EA gain as well as the feedback factor. However, unlike line regulation, load regulation also relies on the transconductance of the pass transistor (eq. 3.6), which depends on its source-drain current. In other words, once the EA and the feedback network are designed, improving this parameter is directly related to increasing the biasing current of the pass transistor, which unfortunately leads to an undesired increase in the quiescent current.

$$L_oR \simeq \frac{1}{\beta A_v g_{m,pass}} \tag{3.6}$$

In particular, autonomous microsystems are not very prone to be affected by large load variations since they tend to employ loads that require very low currents, which are easily supplied. Therefore, in the literature, lower quiescent power is prioritized over load regulation when designing for autonomous microsystems. Consequently, the load regulation results within this context can not be compared to the typical LDOs load regulations nor being expressed within the same scale. However, to avoid further decay, it is in the designer's hands to properly design the EA to keep a high open loop gain not only at open-circuit state but also when the maximum load contemplated is applied.

3.2.4 Temperature Behavior

Another factor that can cause the regulator's output to deviate from the expected value is temperature. The temperature coefficient (TC) of the regulator is defined as follows:

$$TC = \frac{\Delta V_{out}/V_{out}}{\Delta T} = \frac{(\Delta V_{ref} + \Delta V_{os})/V_{out}}{\beta \Delta T} = TC_{Vref} + \frac{\Delta V_{os}/V_{out}}{\beta \Delta T} \tag{3.7}$$

where $\beta = V_{ref}/V_{out}$.

Some important conclusions can be taken away from 3.7:

- The temperature coefficient of the reference (TC_{Vref}) highly determines the temperature response of the regulator but it is not the only factor affecting the regulator's temperature behavior.
- The offset voltage of the regulator changes with the temperature as well, and makes the voltage difference between the reference and the feedback voltage not stay constant. This worsens the regulator's temperature coefficient.
- The effect that the offset drift has in the temperature coefficient increases with $1/\beta$. This means that the lower the voltage reference is the more challenging is to have a good overall TC.

3.3 Dynamic Features

3.3.1 Transient Response

During the transient state when a fast load current or input voltage change happens, the regulator's output may experience overshoot or undershoot. Large peaks in voltage can be hazardous and may result in the malfunction of the target circuit powered by the regulator. Therefore, large overshoot/undershoot must be avoided within the operating conditions considered for the system.

Attending to the origin of the voltage spike, the transient response can be classified into load transient, when the response is forced by a load current variation, and line transient, when the output transient is due to an input variation.

On the other hand, independently of the origin of the transient response, it is also important to separate two domains with clearly different transient responses:

1. Fast or large load or line variations can be challenging for regulators as they require quick or significant voltage changes at the output of the EA to be compensated. If the EA enters the slew region then the current that charges the compensation capacitor as well as the gate of the pass transistor can not be further increased. This results in a longer recovery time for the regulator to reduce the error between the desired output value and the actual value, leading to a greater rise in the output voltage excursion.
2. Slow or small load or line variations must be easily handled by good regulator designs. In this case, the EA never slews and the phase margin of the regulator mainly determines the settling time as well as the overshoot. While reduced phase margins achieve faster responses with higher overshoots, large phase margins get slower responses with lower overshoots. This trade-off should be considered and discussed with respect to the system's necessities. The regulator should be designed such that the system remains always within this domain.

A meticulous analysis during the transient state is most of the time hard as the pass transistor

experiences a shift in its operating region (i.e. saturation, subthreshold, triode). However, qualitatively-wise, in general, both load and line transient can be improved by enhancing the slew rate of the EA. In static-biased systems, which are the most typical ones, an improvement in the slew rate implies the undesirable increase of the quiescent current. However, there are adaptive biasing techniques that keep the quiescent current invariant in the steady state while raising the slew rate during the transient states.

The regulator transient response can also be improved by placing a capacitor that is large enough at the output to act as a filter. This capacitor helps to maintain constant output voltage by supplying current peaks when demanded by the load. However, despite this measure being very employed in systems where the die area is not hardly constrained, when targeting cell-size microsystems output capacitors are no longer a valid solution.

Focusing this parameter discussion more concretely around our target applications, as mentioned in previous sections, large load variations are not likely to occur in autonomous microsystems, consequently, load transient is not a priority in their design. The opposite happens with the line variations, therefore special attention must be paid to this parameter. More particularly, line transient is directly related to the PSR characteristic that will be discussed in the following section. The main difference between these 2 parameters is that PSR is a small signal parameter while the line transient belongs in the large signal domain. Nevertheless improving the PSR directly translates into a better line transient as well.

3.3.2 Start-up Time

The regulator start-up time is defined as the minimum time that the regulator needs to reach stable operation after being powered on. This feature is only especially relevant in systems where this block is turned on and off frequently to save power. Fortunately, autonomous microsystems do not usually aim for fast response times, where the start-up time is included.

However, in the targeted microsystems, a topology that minimizes the start-up circuitry can be very advantageous. Otherwise, the design could incur in a costly extra area and power consumption.

3.4 Frequency-domain Features

3.4.1 Stability

Regulators are feedback systems whose stability sets the loop response. The regulator's frequency behavior strongly determines the line and load transient when the EA does not slew. A careless frequency design can result in excessive ringing and instability during the transient states. Consequently achieving good system stability is always a priority.

The frequency response is determined by the number and location of the lower-frequencies poles and zeros. Usually, the lower the number of poles and zeros at low frequencies the easier it gets to stabilize the system. Therefore, the design for good stability starts with the EA topology selection. Single-stage EAs present only one pole at low frequencies while two-stage EAs bring already two low-frequency poles to the system. In general, the dominant pole of the

regulator is placed at the output of the EA. The high output resistance of the error amplifier, combined with any capacitance connected to this node, including the compensation capacitor or the gate capacitance of the pass transistor (as shown in Fig. 3.1), produces a large time constant. This time constant typically dominates the frequency response of the regulator.

In addition, depending on the pass transistor configuration, the output node may or may not bring another low-frequency pole. The common-source configuration in the LDOs topologies provides a high output resistance, as well as some gain, that together with the load capacitance creates a low-frequency pole. This output node pole is non-dominant, however, it is normally close enough to the dominant pole to make the system unstable making the regulator require a frequency compensation. It is important to notice that this output pole is not fixed at a specific frequency but instead shifts with respect to the current load. The frequency of this pole, p_2 (3.8), depends on the pass transistor transconductance, $g_{m,pass}$, which at the same time is directly proportional to the output current.

$$p_2 = \frac{g_{m,pass}}{C_L} \tag{3.8}$$

If we pay attention to 3.8 the lower the output current is the lower frequency this pole is located at. For this reason, in LDOs the worst stability scenario is given at the minimum load condition and, consequently, the designer must grant good stability at this point by ensuring that p_2 is placed at higher frequencies than the unity-gain frequency (UGF).

On the other hand, in HDOs the non-dominant pole of the regulator does not come from the output stage, due to the relatively low impedance that the NMOS pass transistor provides. Instead, it is set by the non-dominant pole of the EA which is normally placed at higher frequencies. This allows an easier frequency compensation and as well as setting the UGF at higher values.

Having higher bandwidths benefits the regulator making it react better to faster input or load stimulus and, as a result, the transient response is improved and the PSR starts degrading at a higher frequency. However, high bandwidth implies a trade-off as the stability gets compromised, since the dominant pole is placed closer to the non-dominant ones, and there is more external noise injected into the output.

3.4.2 Power Supply Rejection

The power supply rejection quantifies the regulator's ability to isolate the output from the ripple present at the input. As the typical power supplies for this kind of microsystems are very unstable achieving a good PSR becomes crucial. There are several paths for the input noise to advance to the output:

1. The supply noise coming from the voltage reference is reflected immediately at the output of the regulator, thus drastically deteriorating the overall PSR. This noise source can be minimized by selecting a high PSR voltage reference or placing a low-pass filter in between the voltage reference output and the EA input at the expense of extra area.
2. The input noise coming from the EA depends on the topology of the EA selected.

3. The input noise through the pass transistor depends on the type of pass device chosen. Its selection must be correlated to the EA topology in order to improve the PSR and will be explained later on in this section.

As an intuitive first approach, the amount of input noise that gets through to the output can be regarded as the result of a voltage divider, Fig. 3.3 between the input-to-output impedance (Z_{pu}) and the output-to-ground impedance (Z_{pd}).

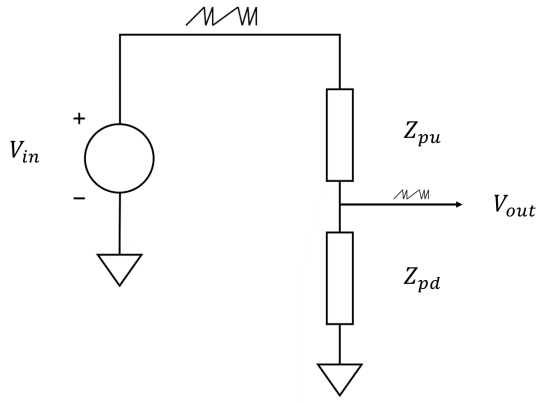

Figure 3.3: Conceptual description of PSR .

The lower the impedance to ground is the less ripple appears at the output. The ground impedance (Z_{pd}) is primarily determined by the parallel of the regulator's output resistance, the sampling network and the load impedance. Depending on the frequency, one of these three contributors will dominate over the others.

At low frequencies, the gain of the EA is high, which results in a low output resistance of the regulator due to the feedback loop. This ensures good supply rejection. Once the frequency rises above the bandwidth, the EA gain starts decreasing at a rate of 20 dB per decade and so the same happens to the PSR, which deteriorates until the UGF is reached.

At the UGF point, the EA no longer provides gain and the ground impedance is normally dominated by the sampling network. This sampling network doesn't attenuate input noise much, so the power supply rejection ratio drops close to 0 dB, shielding the output the least at this frequency range.

As the frequency keeps rising, the load capacitance starts decreasing the ground impedance and the PSR improves, ideally indefinitely with the frequency. However, the ESR of the load capacitance sets the minimum value the PSR can get at high frequencies.

On the other hand, the input-to-output resistance is determined by the combination of the EA's topology and the type of pass transistor selected for the design. Larger impedance values between input and output result in a smaller current change at the output when a voltage variation occurs at the input, leading, thus, to less output ripple. For a better understanding of the conduction of the ripple through the input-to-output impedance let's analyze briefly each case:

- In the case an NMOS pass transistor is chosen for the output stage, the ripple coming

from the input faces the drain of a source follower configuration which offers a relatively high impedance that makes it difficult for the ripple to go through. However, it is also clear that any noise present at the gate is fully duplicated at the output. Hence, for a good PSR response, an EA that does not transfer the supply ripple to the gate of the pass transistor is required.

- In a common-source configuration, a PMOS pass transistor may allow supply noise to easily pass through if no measures are taken to counter it. However, great isolation can be achieved if the input noise, present at the source of the pass transistor, is replicated at its gate. This would lead to ideally no small signal source-gate voltage in the pass transistor and, hence, no input noise contribution in the regulator output. For this reason, to improve the PSR characteristic, an EA that reproduces the input noise at the gate of the pass transistor would be beneficial.

There are two main methods to replicate efficiently the input noise at the gate of the PMOS pass transistor:

- The feed-forward technique uses a second transconductor and a feedback loop, between V_{dd} and the gate of M_{pass}, to copy the small-signal input perturbations at the gate of the pass transistor.
- The current mirror replica is another frequently used method. It consists of driving the gate of M_{pass} with a P-type current mirror, which lets the input noise pass through [37].

Among the two options, the current mirror replica is often preferred as it does not need any additional circuitry. The feed-forward technique would require additional power and area that can be very limited in certain scenarios, such as the autonomous microsystems discussed in this thesis. Besides, in the first case, a proper bandwidth and gain must be assured in the feedback loop so the overall frequency response of the regulator does not suffer any degradation before the UGF.

3.5 State of the Art and Related Works

3.5.1 Voltage References

To implement a voltage reference the first step is to find an invariant potential from which to build the structure. The bandgap potential, based on BJT junctions, is one of the most common solutions. However, BJTs fabricated in CMOS processes generally lack accuracy and require relatively high bias currents, compared to MOS transistors, to avoid large process variations [38, 39]. At the same time, most bandgaps references, and especially recent efforts to achieve low power designs [40, 41], include large resistors. Consequently, there is a complicated variability-power-area trade-off that makes their use for tiny autonomous microsystems difficult, as they usually end up requiring too much area and power [42] for what these microsystems can afford.

The smallest and lowest power consumption designs have been achieved so far with advanced CMOS technology nodes [43]. They normally rely on the threshold voltage potential [44] to address the above issues. The threshold potential provides good supply insensitivity and

a well-documented response to the temperature [45, 46, 47]. Additionally, unlike bandgap references, it allows a relatively easy way to generate low-voltage designs, which is beneficial for our target application. At the same time, they can be implemented with a very low number of transistors, as few as just two or three, making them ideal for designs with limited space. Despite all these advantages, they suffer from process variations as the threshold potential of the transistors is highly exposed to the deviations of the fabrication process. The smaller the node and the design the more significant these deviations are [48, 36]. As a result, most of them resort to trimming circuitry to compensate for it [49, 50].

CMOS-only references can be designed using the same approach as bandgap references. To achieve a temperature-stable voltage, two terms with opposite temperature coefficients are combined (either added or multiplied). One of these two terms usually has a tunable slope vs. temperature through proper device sizing. This allows for a first-order cancellation of the temperature effect around the desired operating point.

Most of the times, CMOS-only references can be viewed as a current source that produces a constant current, I_{ref}, and a transimpedance device that converts I_{ref} into a constant voltage similar to 3.4.a. Temperature compensation can be achieved either by using temperature-insensitive components or by using elements with opposite temperature coefficients. There are two commonly used CMOS-only topologies: the self-cascode MOSFET (SCM) reference [51], also known as 3-transistors reference (Fig. 3.4.b), and the 2-transistors reference [52] (Fig. 3.4.c).

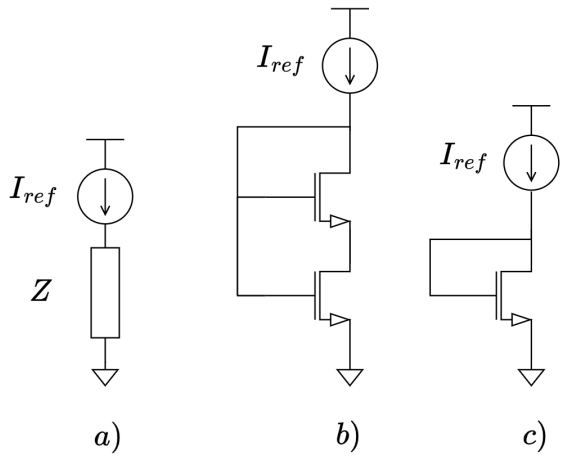

Figure 3.4: CMOS-only references: a) Conceptual diagram b) Typical 3T structure c) Typical 2T structure.

In both solutions, it is very common to exploit the technology's possibilities and make use of the most convenient device selection. Their different characteristics allow the designer to focus and enhance a certain parameter in the voltage reference. For instance, in [53], a native transistor was used as a current source to achieve high enough current to operate with zero voltage biasing, taking advantage of its very low threshold voltage. Similarly, in [54], the SCM made up of an I/O transistor and a regular transistor was chosen as the transimpedance element. The SCM converts the constant current flowing through it into a constant voltage at the output and generates a complementary to absolute temperature

(CTAT) voltage proportional to the threshold voltage difference between both transistors that compose the SCM. This CTAT voltage compensates for the proportional to absolute temperature (PTAT) behavior of the current source.

Different gate and bulk biasing is another common design variable that designers can take advantage of. The different configurations provide different advantages and drawbacks. [55] explains the difference between using current sources with gate-to-source and gate-to-ground configurations, resulting, the last one, in a PSR improvement.

On the other hand, bulk biasing can be used to shift the threshold voltage to develop a temperature compensation as in [56]. This allows for the use of only one type of transistor in the reference, translating directly into a reduction in the sensitivity to process variations.

Last, there is also the possibility of adding a feedback network either in the gate [57] or in the bulk [58] biasing to improve parameters like the PSR and the line regulation.

In general, CMOS-only solutions offer enough degrees of freedom for the designer to achieve a design that satisfies each application's requirements. However, developing a design with an area and a power budget as constrained as in cell-size autonomous microsystems still represents a challenging task, even with all the tools mentioned before. After this brief introduction of the CMOS-only references scenario and some of the most employed techniques, Table 3.1 summarizes the smallest voltage references in the literature, arranged in increasing order of size, and compares some of their key features. It becomes immediately easy to notice that most of these references would take an excessive fraction of the 2500 μm^2 available in the *SynCell* for the whole design. This paves the way for important research to emerge in order to reduce the size of voltage references to enable microsystems to be shrunk to the cellular scale.

Table 3.1: Comparison Ultra-Low Area Voltage References.

	[48]	[36]†	[44]	[59]	[60]	$[49]_a$	$[49]_b$	[61]	[62]
Technology (nm)	65	40	130	65	180	65	180	180	130
Area (μm^2)	104	480	665	840	900	900	1425	2500	3000
V_{dd} (V)	0.4-1.2	1.5-2.5	0.3-1.2	0.5-1.8	≥0.25	0.5-2.5	0.5-3.6	1.4-3.6	≥1.1
V_{out} (mV)	342.8	570	26	257.5	118.1	327.2	326.8	1250	800
σ/μ (%)	4.9	7	3.4	0.3	1.1	0.85	0.8	0.8	5
Min. Power (nW)	0.00042	151	0.04	0.0143	0.113	0.24	0.006	0.033	27.5
Line reg. (%/V)	0.47	5-8	0.188	0.02	0.3	0.33	0.044	0.31	2
PSR (dB)	-	-70†	-67.3†	-	-65	-40	-49	-41	-
	-	@ 915 MHz	@100 Hz	-	@100 Hz	@100 Hz	@100 Hz	@100 Hz	-
TC (ppm/ºC)	252.2	40	208	99.2	73.5	89.1-118.2	54-176	8-53	100
Temp. Range (ºC)	-40∼60	-55∼125	-25∼125	0∼100	-40∼140	-20∼80	-20∼80	0∼100	-40∼85

† Simulated result.

3.5.2 Low-Dropout Regulators

Many LDOs described in the literature are intended to operate in the mW load power range, which is not suitable for tiny harvesters that cannot consistently produce that much power.

However, some works have focused on developing LDOs that target much lower load powers in the μW range. These designs aim to achieve very low quiescent currents and reduce area occupation.

A good example of a design that optimizes its resources for energy harvesting applications is presented in [63]. This work describes a PMU that integrates, to the best of our knowledge, the smallest LDO design of the literature (0.001 mm^2) prior to this thesis. At the same time, its quiescent current consumption (100 nA) and targeted maximum current deliverable to the load (100 μA) are well suited to the limitations of the harvester discussed in their work. The main drawback of this work is that the required dropout voltage to deliver the maximum load is too high, around 0.4 V, which leads to reduced efficiency (73%) under these conditions. This issue usually comes as a result of an excessive minimization of the size of the pass transistor to save area in very constrained scenarios.

An excellent effort to reduce quiescent current consumption was presented in [64]. This work describes a sub-nA quiescent current linear regulator for a power management unit design aiming at energy harvesting in the context of self-powered IoT applications. The large power reduction led to a degradation in the transient response, resulting in a settling time as long as 13.6 ms for a moderate load step (10 nA to 1 μA). In this design, an NMOS capable of handling a 500 μA load current was selected as the pass device.

The work in [65] shows the importance of limiting the power budget when working with weak energy harvesters. They presented a 6 nA quiescent current LDO for RF energy harvesting with a maximum load current of 10 μA. The paper discussed various design considerations for RF LDOs, particularly an in-depth analysis to achieve good PSR at high frequencies. However, the slow transient response in the range of a few hundred microseconds remained the main drawback.

In [66] another LDO for energy harvesting is presented. In this case, ultra-low voltage operation was targeted and successfully achieved by using a bulk-driven input stage. The LDO managed to attain a quiescent current of 7 nA and a load current of 750 μA, while the settling time was close to 1 ms.

To summarize, energy harvesting applications often demand very low quiescent power designs as well as limited load currents. When considering static biasing, decreasing the quiescent current leads to a compromise in the regulator's speed during transient states, which may or may not be an issue depending on the application. Additionally, some of the cited works demonstrated that a significant area reduction can be achieved by targeting low load currents, in line with the harvester constraints.

3.6 Objectives

This chapter of the thesis aims to provide a power management unit that is efficient for autonomous microsystems. In such a context, energy harvesters are frequently used to power the circuit. However, these power sources are very weak and create major constraints for the design.

Firstly, the generated power is very limited. This means that the circuit's available power is significantly reduced and thus low-quiescent current designs are necessary. Secondly, the designer must also consider that large voltage variations are likely to occur in the harvester. Therefore, line regulation and PSR are also essential within this context.

In addition, we aim to push the size limits of these microsystems to enable new groundbreaking applications. Consequently, resistorless designs are mandatory since the space needed by integrated resistors to achieve low-power designs is not affordable in the autonomous microsystems context. Our goal is to keep the area at cell size scales. However, to achieve this, some features such as the maximum current deliverable to the load may need to be sacrificed. This is a suitable trade-off when microsystems are powered by weak sources that can only produce 10s of nW to 100s of μW regularly. Therefore, we focus this work on load currents below 100 μA while maintaining high efficiency. Therefore, I_L/I_q ratios greater than 1000 are pursued.

The fastest significant load change expected in the *SynCell* comes from the sensor, which takes at least several minutes to complete the change of its resistance. As a consequence, a slow transient response in the PMU is allowed. However, to extend the use of the PMU to faster sensors, we aimed for settling times below 100 μs in this work.

In the following sections, we will present two power management units:

- PMU I: It targets *in vitro* measuring applications, where the temperature remains stable thus no temperature compensation is needed. Such a scenario lets us focus on improving some of the most important features instead. Nevertheless, a first-order temperature compensation method will be also explained for this design.
- PMU II: It is designed to implement, within the lowest area possible, good supply and temperature dependency. This makes it highly suitable and easy to integrate into any autonomous microsystem that targets temperature-changing environments.

3.7 PMU I

In this section, we will describe the building blocks used for the first proposed power management unit. The PMU consists of a voltage reference and an LDO. The PMU described in this section is designed for *in vitro* measurements. The temperature stability of this scenario relaxes the constraints related to temperature variations, allowing us to focus more on parameters such as line regulation and power supply rejection. These parameters are crucial for mitigating the fluctuations from the very weak power supply of this microsystem.

3.7.1 Voltage Reference

Operating Principle

A simple way to generate a voltage reference is to make a constant current pass through a resistor. One popular approach for creating a constant current reference is the beta multiplier. This method is well-documented in the literature [67]. Its working principle is based on the

self-biasing technique, depicted in Fig. 3.5.a where the input of a current source is made to be dependent on its own output through a current mirror, establishing a loop that only allows for two stable points, as is represented in Fig. 3.5.b. It is important to avoid the zero-current state (point B) and aim for point A as the desired outcome.

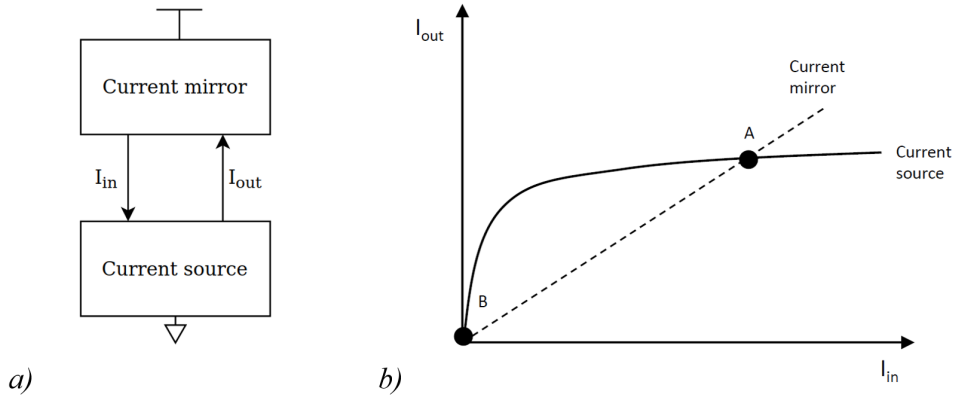

Figure 3.5: Beta multiplier principle of functioning. a) Self-biasing technique. b) Current source-current mirror intersections.

The traditional way of implementing the beta multiplier is shown in Fig. 3.6. The main drawback of this circuit is the necessity of a resistor, which requires an excessive area for low-power applications. Furthermore, this topology also suffers very poor fidelity to simulations and a lack of reproductivity in fabrication due to the low accuracy of on-chip resistors. Temperature compensation is another important drawback of this topology due to the lack of freedom when adjusting the parameters involved in it [68], even though, as mentioned before, this is not relevant to our field of application. On the other hand, very good line regulation can be achieved if the second-order effects that can make the operating point fluctuate, such as the channel length modulation and the body effect, are taken into account.

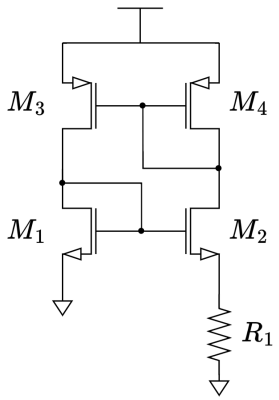

Figure 3.6: Beta-multiplier current reference.

Several topologies that avoid using on-chip resistors have been proposed from the original paper [67]. Due to its simplicity, we have based our design on the CMOS-only circuit presented

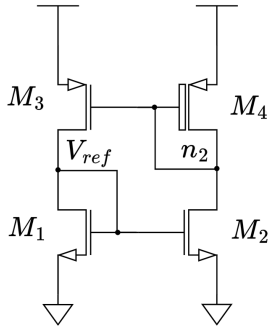

Figure 3.7: Current reference based on threshold voltage difference [69].

in [69]. It generates a current reference from the voltage threshold difference of two different transistors. In particular, a high threshold voltage (HVT) transistor is used alongside regular threshold voltage transistors. Its schematic is shown in Fig. 3.7. To briefly explain its operating principle let's assume that transistors M_1 and M_2 form a unity gain current mirror that forces the same current through transistors M_3 and M_4. However, due to the thicker gate oxide of transistor M_4, its threshold voltage is much higher than that of M_3. Therefore, in order for their drain currents to be matched, the aspect ratio of M_4 (W_4/L_4) must be sufficiently large to compensate for the threshold voltage difference, making $W_4/L_4 > W_3/L_3$ a necessary condition for proper operation.

If the zero-current state is avoided, the feedback loop formed by the current mirrors brings the circuit to an operating point where the gate-to-source voltage of transistors $M_{3,4}$ is such that makes transistor M_3 operate in the saturation region but keeps M_4 in weak-inversion, due to its higher threshold voltage. The desired stable operation point is the intersection of the quadratic I_{DS} vs. V_{GS} curve of M_3, typical of a transistor working in saturation, with the exponential curve of M_4, placed in the subthreshold region, as exemplified in Fig. 3.8.

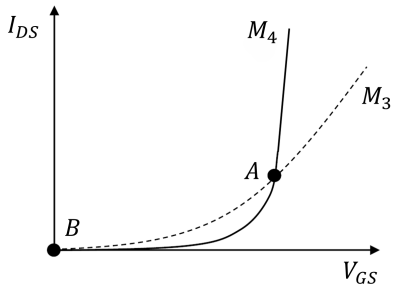

Figure 3.8: Intersection between the I_{DS} vs. V_{GS} curve of transistors M_3 and M_4 in the circuit of Fig. 3.7.

By numerically solving the system of equations formed by (3.9) to (3.11), the mathematical expression for the stable operation point (A in Fig. 3.5.b) can be obtained. As a result, a stable current is generated and converted into a voltage reference at node V_{ref}.

$$I_{DS3} = \frac{\mu C_{ox} W_3}{2L_3} \times (V_{GS3} - V_{TH})^2 \times (1 + \lambda_3 V_{DS3}) \tag{3.9}$$

$$I_{DS4} = I_0 e^{\frac{q(V_{GS4}-V_{TH0})}{nK_bT}} \times (1 + \lambda_4 V_{DS4}) \tag{3.10}$$

$$I_{DS1} = I_{DS2} \tag{3.11}$$

where I_0 is the scale current, V_{TH} is the threshold voltage, n is a fitting parameter, q is the the electron charge, K_b is the Boltzmann constant, T the temperature, λ is the channel length modulation parameter, C_{ox} is the oxide capacitance per area and μ is the carrier mobility.

However, this topology has several issues when it comes to isolating its output from supply perturbations. First, the stability of the operation point depends on λ. As technology nodes become smaller, the output resistance of transistors worsens and the supply dependency gets compromised. Second, the supply noise at the output depends on the noise coming directly from the supply, through M_3, and that coming from the $M_{2,4}$ branch, through the $M_{3,4}$ current mirror. This results in two paths that contribute to the propagation of the supply noise to the output and deteriorate the supply dependency of the reference.

To attenuate the two noise contributions coming from the power supply, we present in this thesis the circuit of Fig. 3.9.

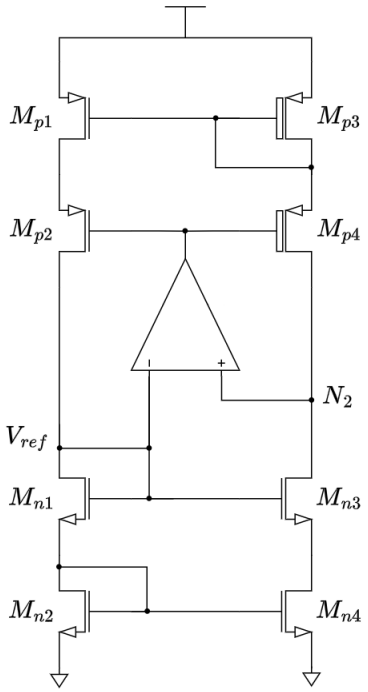

Figure 3.9: Proposed Voltage reference.

Two main measures have been applied in this design. First, the cascode technique increases the output resistance from R to $R' \simeq R^2 gm + 2R$, which enhances λ.

Second, an operational amplifier is placed in the circuit to make the voltage at node n_2 equal to the voltage at node V_{ref}. This provokes the variation of the V_{DS} voltage of the $M_{n3,4}$

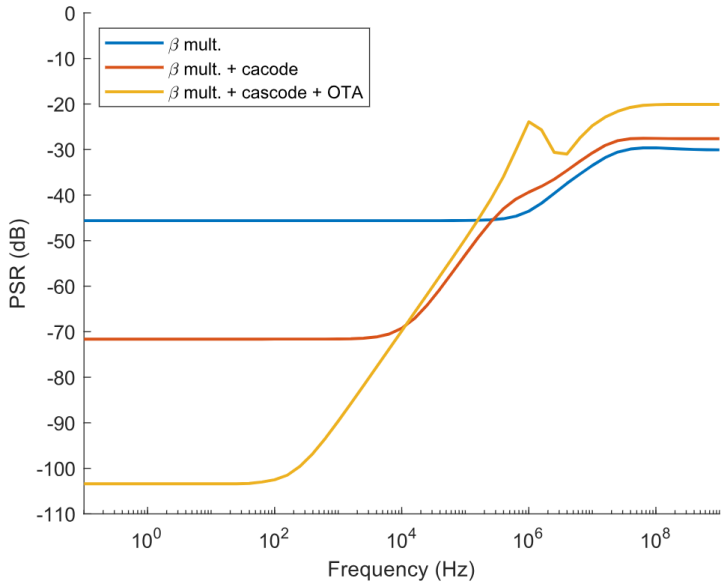

Figure 3.10: PSR simulation comparison between the β multiplier with and without cascode and OTA respectively.

current source to be much reduced when the voltage supply changes. Hence, the supply noise advancing through $M_{p1,p3}$ current mirror gets lessened by the amplifier's open loop gain. Another way to understand the effect of the opamp in the reference is that the operational amplifier drives the gate of transistors $M_{p2,p4}$ with the same fluctuations as they see at their sources (assuming $A_v = \infty$) to keep V_{n2} equal to V_{ref}. This has the same effect in the proposed voltage reference as if V_{DS4}, in equation 3.10, was made constant and independent of the changes in V_{dd}.

The simulation of how these two measures impact the supply dependency of the circuit is shown in Fig. 3.10. The graph shows the PSR of the circuit with and without the improvements. The cascode alone provides approximately 26 dB more isolation with respect to V_{dd}, while the cascode and the opamp together increase the PSR by 58 dB at low frequencies. This significant improvement applies also to line regulation, as these two features are correlated. Therefore, an outstanding supply dependency is achieved in this reference.

The operational amplifier, whose schematic is shown in Fig. 3.11, has a folded cascode topology, very suitable for low-power designs. This topology allows to obtain a 60 dB gain in only one stage. It must be noted that no physical capacitance was required since the high output resistance of the cascoded stage and the gate capacitance of transistors $M_{p2,p4}$(in Fig. 3.9) easily compensate the full loop, making the circuit stable in frequency. The V_{bp1} and V_{bp2} voltages are obtained directly from a stack of transistors connected as diodes. It has also been checked that any change in these biasing voltages, due to V_{dd} variations, has not a significant effect on the operational amplifier gain, nor in the power consumption, however, all the provided data in the results section is at the worst case scenario.

The output of this reference can be either a current, copied through a current mirror whose input branch would be composed of transistors $M_{n1,n2}$, or a voltage, directly taken out of

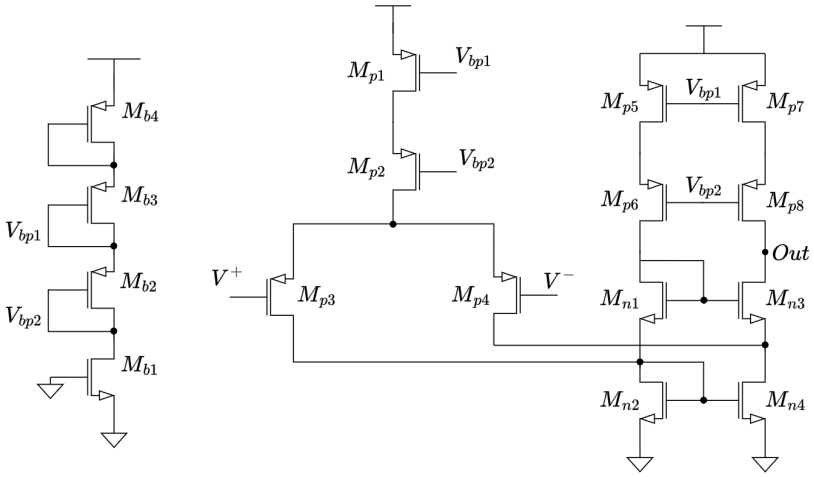

Figure 3.11: Folded cascode opamp designed for the current reference.

node V_{ref}. Both output modes present outstanding line regulation and PSR however, as the current reference is made to go through the transistors $M_{n1,n2}$ in diode configuration the fluctuations that could appear in the current would be attenuated by the exponential shape of the diode transfer characteristic I_d vs. V_d when converted into a voltage. Hence, this work provides better supply regulation when working as a voltage reference.

Regarding the physical design of this reference, the main source of variability comes from using transistors with different threshold voltages. Consequently, it is important that transistors M_{p1-p4} are equidistant to the edges of the n-well. Otherwise, the WPE effect would cause a systematic source of deviation in the output of this reference.

Temperature behavior and compensation

As previously mentioned, in the *in vitro* scenario, that this circuit targets, the temperature is expected to remain stable. This eliminates the need to develop a temperature-insensitive design. However, to broaden the potential applications of this design beyond temperature-stable environments, a method to obtain a temperature compensation for this design is presented below. It is worth mentioning that the temperature-compensated version was not fabricated as it would have required an additional 20% more power and around 30% more area, which is worth saving in the *in vitro* measuring context.

First, the graph in Fig. 3.12 displays the temperature response of the uncompensated reference. It shows a clear CTAT behavior that is primarily due to the threshold variation of the transistors that convert current into voltage, along with the reduction in carrier mobility. Both of these factors cause the output voltage to decrease with increasing temperature. Additionally, there is a slight CTAT behavior in the threshold voltage difference between transistors $M_{p1,p2}$ and $M_{p3,p4}$, but its impact on the temperature response is less significant. It can also be noted that the beta multiplier's current operating point also exhibits a CTAT behavior. Once the current drops below a certain limit, the reference ceases to function, typically occurring around 85°C.

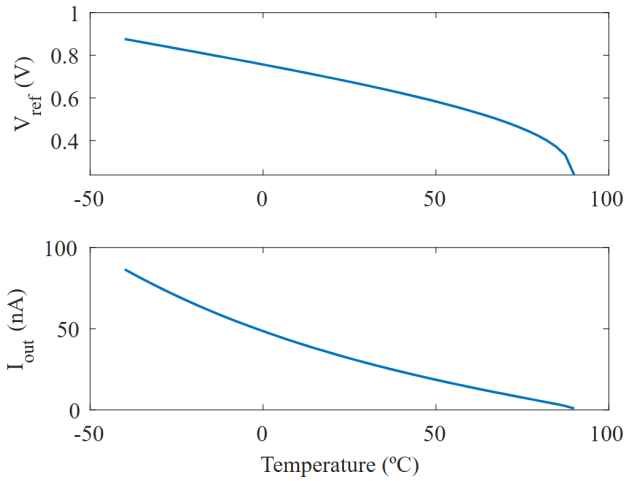

Figure 3.12: Temperature simulation of V_{ref} I.

Since the equation system that dictates the behavior of this voltage reference, eq. 3.9 to eq. 3.11, is only solvable through numerical methods, developing a model that accurately explains the temperature response of this circuit is quite challenging. Therefore, the temperature compensation process is based on iterative simulations to find the suitable transistor sizing.

The full schematic of the temperature-compensated reference is shown in Fig. 3.13. It is based on a SCM structure, which provides full flexibility on how the current source of Fig. 3.4.b is implemented. This current source can be directly carried out with the circuit of Fig. 3.9 taking advantage of the fact that its output can be either a current or a voltage.

The transimpedance of this circuit, which converts the current into a voltage, is composed of an I/O transistor (M_{n8}) and a core transistor (M_{n9}). Their threshold difference allows for the generation of a ∼300 mV voltage reference. Otherwise, if the same type of transistor was selected, the output would be only a few tens of mV, which would make it more complex to use in a typical LDO structure.

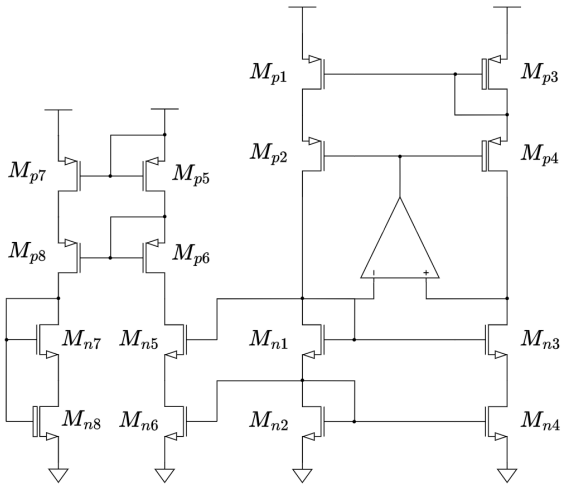

Figure 3.13: Temperature-compensated voltage reference schematic.

The SCM voltage references have been extensively described and used in the literature and, as long as the transistors are set to operate in weak inversion saturation ($V_{DS} > 4V_T$), their operating principle is described by the following equation:

$$V_{ref} = |V_{TH,n8}| - |V_{TH,n7}| - \frac{nK_bT}{q} ln \frac{I_{07}W_7L_8}{I_{08}W_8L_7} \tag{3.12}$$

where I_0 is the scale current, V_{TH} is the threshold voltage, n is a fitting parameter, q is the the electron charge, K_b is the Boltzmann constant and T the temperature.

The last term in eq. 3.12 provides an adjustable PTAT slope that can be set, through transistor sizing, to such a value that cancels out both the CTAT term coming from the threshold voltage difference between transistors M_{n8} and M_{n7} as well as the CTAT behavior of the current reference of Fig. 3.9. The simulated temperature coefficient of the voltage reference in Fig. 3.13 is shown in Fig. 3.14. It achieves a simulated temperature coefficient of 50 ppm/°C from -10°C to 50°C and 350 ppm/°C from -40°C to 70°C, which satisfies outdoor application's necessities most times.

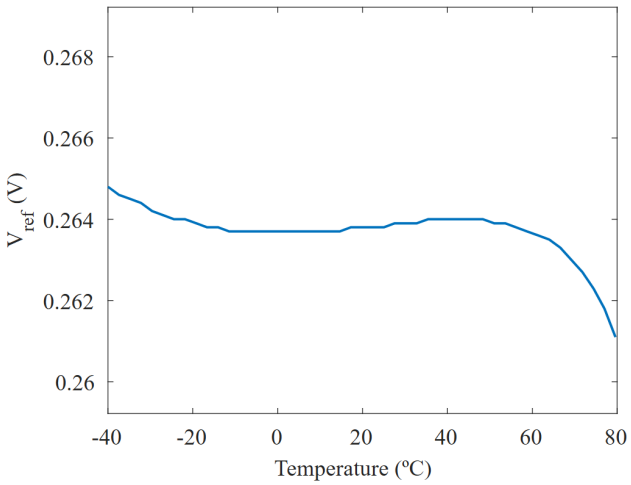

Figure 3.14: Temperature simulation.

3.7.2 Voltage Regulator

The voltage regulator design is illustrated in Fig. 3.15.

The dropout voltage of the regulator, V_{DO}, defined as the minimum voltage drop of the output voltage with respect to the supply voltage, is well known to be larger for an NMOS approach ($V_{DO} = (V_{GS} + V_{DS,sat})$), than for the PMOS counterpart ($V_{DO} = V_{DS,sat}$). This voltage drop translates directly into dissipated power that is not delivered to the load. Since the energy harvesters used in this sort of microsystem, such as photovoltaic cells, are very weak power supplies, it is very important to make the most of the energy collected. In addition, a PMOS output stage, unlike the NMOS version, adds some gain to the overall open-loop gain of the regulator which is also beneficial for parameters like the line regulation. For these reasons, a

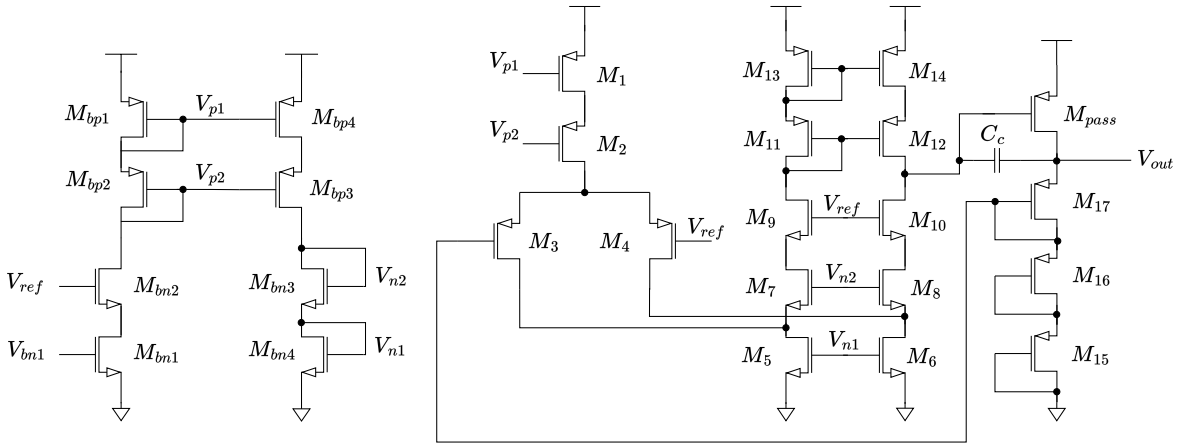

Figure 3.15: Complete schematic of the proposed PMU.

PMOS transistor was chosen as the pass device in this design. However, unlike most of the typical LDOs, the size of the pass transistor did not have to be large because autonomous microsystems typically handle relatively low currents, in the order of a few tens of pA to hundreds of μA. As a result, a significant area reduction is achieved.

A folded cascode topology was chosen for the EA. It is very suitable for low-voltage designs and provides high gain and only one dominant pole, which simplifies the full design of the frequency compensation and requires less area for the compensation capacitor. The complete schematic is shown in Fig. 3.35.

The current mirror in the EA is made with PMOS transistors because it has been demonstrated that the noise present in the supply voltage is completely replicated at the gate of the PMOS pass transistor [37]. This measure results in a PSR improvement since the gate noise of the PMOS pass device is equal to the noise present at its source and cancels it out at the output of the regulator.

The regulator biasing is generated from the reference voltages V_{bn1} and V_{ref} using transistors M_{bp1-4} and M_{bn1-4}.

Regarding the regulator stability, for capacitorless-LDOs with Miller frequency compensation, the non-dominant pole is set by the output stage, whose frequency location depends on the load current ($p_2 \simeq g_{m,pass}/C_L$). In fact, for lighter load currents the non-dominant pole shifts to lower frequencies, thus reducing the phase margin. Since the design is focused on low output currents, special attention was paid to the stability of the regulator. The Miller compensation was employed to take advantage of the output stage gain to reduce the capacitor size while ensuring that the non-dominant pole is always placed at higher frequencies than the unity gain frequency ($UGF \simeq g_{m,in}/C_c$). A minimum phase margin of 67°is guaranteed for a worst-case scenario of $I_{load} = 0$ A.

The output voltage of the regulator was designed to be 1 V to match the nominal voltage of the technology. A lower voltage may result in lower power consumption, however, but would make the design more demanding and add more complexity to our already constrained scenario.

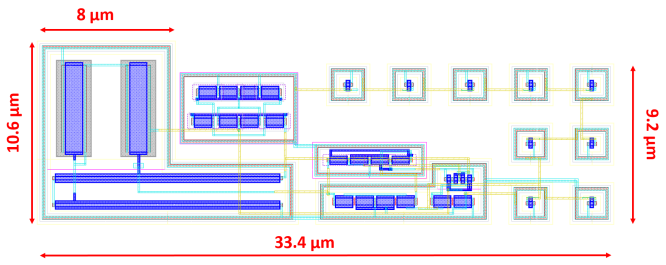

Figure 3.16: Layout of the proposed voltage reference.

For this regulator to provide an output of 1 V it is required to use a feedback factor of 2/3. The feedback network is implemented by equal-sized PMOS transistors in their own n-well in diode configuration working in the deep sub-threshold regime to reduce their static power dissipation. At the same time, these diodes make the regulator react smoother in transitions from high to low load currents. As the output voltage increases in the transient state, the diodes' impedance decreases exponentially providing a better sinking capability.

Load regulation, understood as the voltage variation in the output node after a load change happens, is another important parameter for regulators in general. However, there is a trade-off between the quiescent current drawn by the pass transistor and the load regulation itself. As clarified in (3.13), the load regulation depends on the pass device transconductance, which increases with its biasing current:

$$\frac{\Delta V_{out}}{\Delta I_{out}} = -\frac{1}{\beta A_v g_{m,pass}} \tag{3.13}$$

where β is the feedback factor and A_v is the regulator open loop gain.

In the context of autonomous microsystems, it is more important to keep the quiescent consumption under relatively low limits than to achieve outstanding load regulation, since large load currents and large load variations are not frequent. For this reason, the load regulation of this design, as well as that of some related works [65, 64], cannot be compared to the typical LDO load regulation, nor can they be expressed within the same scale.

3.7.3 Simulations and Measurements Results

Voltage Reference

The voltage reference was fabricated using a 65 nm CMOS technology. The layout is shown in Fig. 3.16. The differential pair, current mirrors, and current sources were matched using common centroid and interdigitation techniques. The biasing voltages for the operational amplifier are derived from a stack of transistors configured as diodes, with their bulk terminals connected to their sources. This setup cancels the body effect and ensures that each transistor provides the same voltage drop. However, this configuration requires a separate n-well for each device. No matching techniques were applied to the largest devices in this design, as doing so would have significantly increased the overall area.

One of the goals of this work was to reduce the die area as much as possible. This voltage reference only occupies a total of 320 μm^2 and its temperature-compensated version goes up to 420 μm^2, which places both of these references among the smallest references reported in the literature.

Twenty chips were measured in total. Half were tested naked at a probe station while the other half were packaged and mounted on the test PCB. It generates a simulated voltage of 0.671 V in a typical-case scenario. After fabrication, the average measured output voltage was $\mu = 0.677$ V with a standard deviation of $\sigma = 0.014$ V. The σ/μ inaccuracy observed in the measurements (2.068%) was significantly lower than what was expected from Monte Carlo simulations (Fig. 3.17). However, the number of measured samples is not sufficient to extract meaningful statistics. The Monte Carlo simulation gave an average voltage of $\mu = 0.665V$ with a standard deviation of $\sigma = 0.038V$ respectively ($\sigma/\mu = 5.7\%$). This variability is attributed to the use of transistors with different threshold voltages which leads to a certain inaccuracy when reproducing the same threshold voltage ratio across different samples.

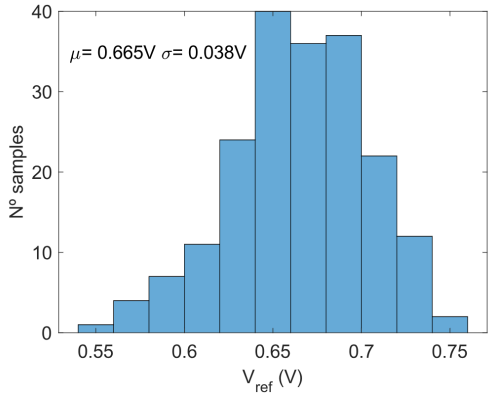

Figure 3.17: Monte Carlo simulation of the proposed voltage reference.

The DC supply dependency measurements of two samples of the proposed voltage reference is shown in Fig. 3.18. The typical case (TT) simulation was included in the plot for a better comparison of the results to the expected value.

As stated in previous sections, apart from area and power, we wanted to focus on developing a structure with very low supply dependency. This design has yielded outstanding simulation results in line regulation achieving a variation of just 0.001 $\%/V$ in the typical case simulation and 0.0034 $\%/V$ in the Monte Carlo simulation (Fig. 3.19) within the range of 1.5 V to 3 V.

Regarding the measurement results, the line regulation was determined in two samples giving a value of $0.0022\%/V$ and $0.0043\%/V$ for each sample respectively. These two values obtained stand within the standard deviation contemplated in the Monte Carlo simulation shown before and prove the outstanding line regulation of this design.

Fig. 3.10, in section 3.7.1, presented the typical case simulated PSR with an attenuation of -103 dB at low frequencies. The Monte Carlo simulation, shown in Fig. 3.20 gave an average PSR of 99 dB with a standard deviation of 6.6 dB. This parameter, alongside the line regulation obtained, allows us to state that this reference provides excellent isolation against

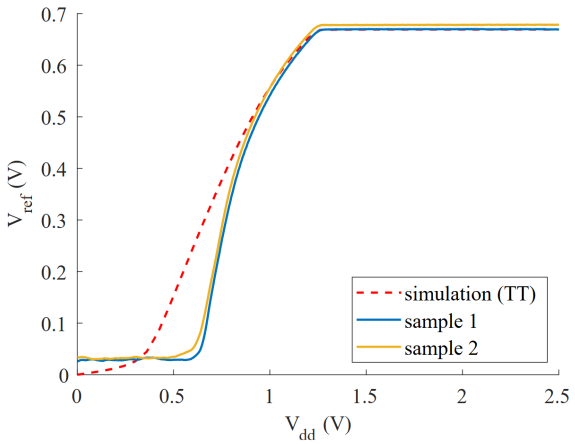

Figure 3.18: Simulation and measurements of the supply dependency of the proposed voltage reference.

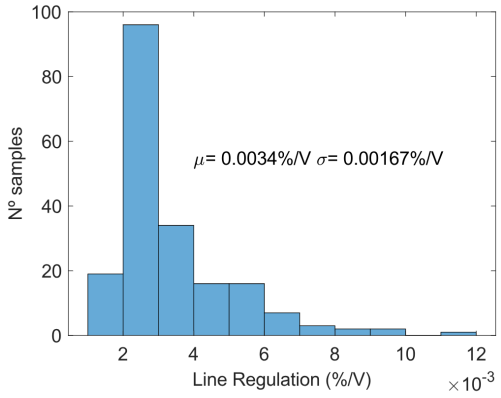

Figure 3.19: Monte Carlo simulation of the line regulation of the proposed voltage reference.

supply variations, very useful when targeting energy harvesters as the power supply.

The simulated current consumed by this reference is 60.6 nA, half of it through each branch. As previously mentioned, this reference can also be used as a 30.3 nA current reference, as proposed in the circuit of Fig. 3.13. However, the simulated typical case line regulation as a current reference rises to $0.0082\%/V$. Since the circuit in Fig. 3.13 relies on the stability of this reference as a current source, the line regulation of the temperature-compensated voltage reference is slightly worse than the uncompensated version (Fig. 3.9). The typical-case simulation shows a $0.0055\%/V$ line regulation within the same voltage supply range mentioned before.

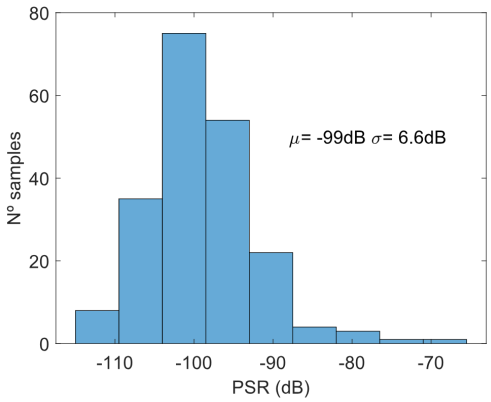

Figure 3.20: Monte Carlo simulation of the PSR at 1Hz of the proposed voltage reference.

Voltage Regulator

The proposed LDO was designed following the same guidelines as for the voltage reference described in the previous section, focusing on keeping the area and power consumption as low as possible while paying special attention to the supply dependency.

This regulator occupies a very reduced area of 200 μm^2, which satisfies the hard constraint of working under the cell size scale. The layout of this design is shown in Fig. 3.21. In particular, the differential pair, the current mirrors, and the current sources of the error amplifier have been matched using common centroid and interdigitation techniques. The feedback network, as well as the compensation capacitor, is implemented with PMOS transistors in their own n-wells, since they need to have their bulk terminals short-circuited to their sources. This cancels out the body effect in the devices of the feedback network and consequently, they all provide the same voltage drop.

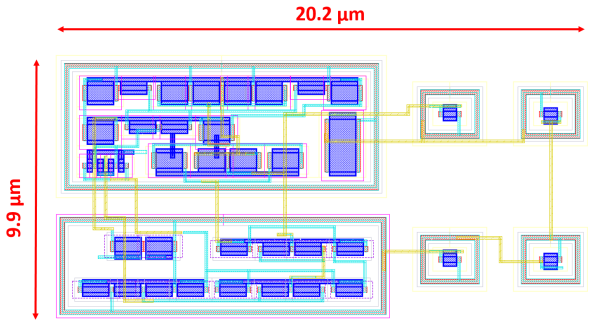

Figure 3.21: Layout of the proposed voltage regulator.

The output of this regulator was designed to be ∼1.005 V in the typical case simulation when using the voltage reference of Fig. 3.9 as the input. The LDO was measured across 10 fabricated samples giving an average output voltage of 1.0281 V with a standard deviation of 0.0357 V. The measured response of two samples to a supply voltage sweep is shown in Fig. 3.22.

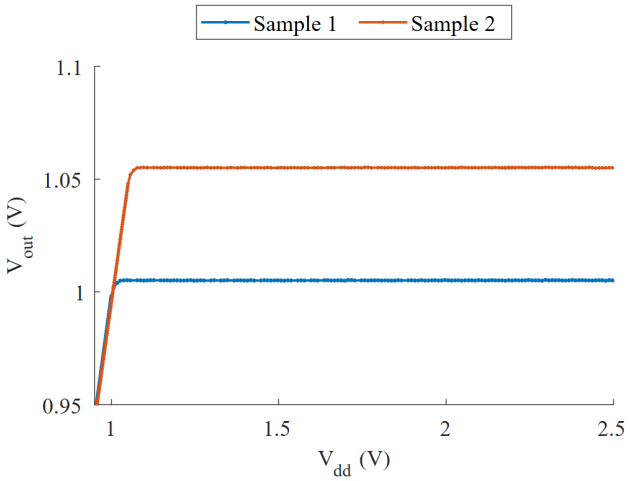

Figure 3.22: Measured output voltages of two samples of the proposed LDO.

The supply regulation was determined in two measured samples. Both samples demonstrated great isolation in terms of supply dependency presenting a line regulation of 0.0068%/V and 0.0081%/V respectively. Both line regulations are worse than the average expected from a 200-run Monte Carlo simulation (Fig. 3.23) but stay within the expected standard deviation.

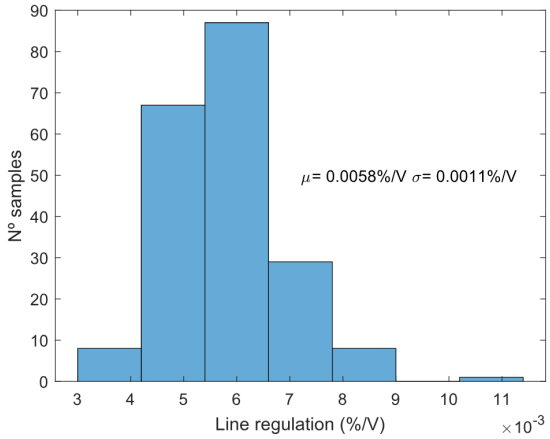

Figure 3.23: Monte Carlo simulation of the line regulation of the proposed LDO.

The typical case simulated PSR shows an outstanding attenuation of -97 dB and -80 dB at low frequencies for a load resistance of 10 MΩ and 100 kΩ respectively (Fig. 3.24). The Monte Carlo simulation of the PSR at low frequencies, shown in Fig. 3.25, presents an average value of -85.4 dB and a standard deviation of 4 dB. Hence, the combination of this LDO with the voltage reference presented earlier creates a highly reliable PMU that can withstand perfectly the large voltage fluctuations typical in autonomous microsystems.

To ensure that this PMU can handle the maximum load, which is the MoS_2 sensor, and also performs well with a small energy harvester, the maximum load current was chosen to be in the tens of microamps range. This amount of power can be consistently produced within such a limited space. Going beyond this range would waste area, as the pass transistor would

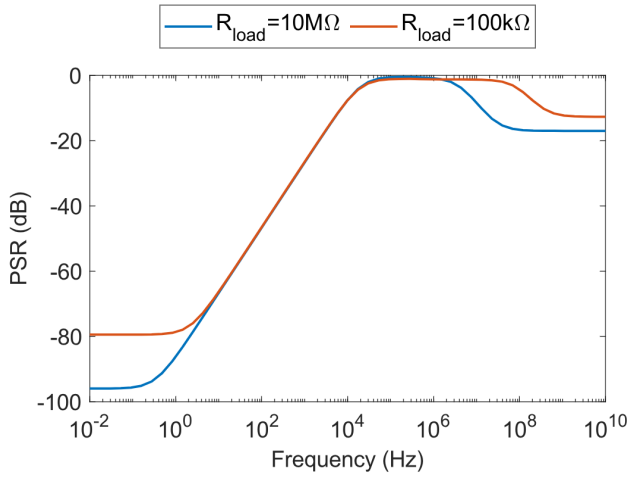

Figure 3.24: Typical case simulation of the PSR vs. frequency of the proposed LDO with C_{load} =100 fF and different values of R_{load}.

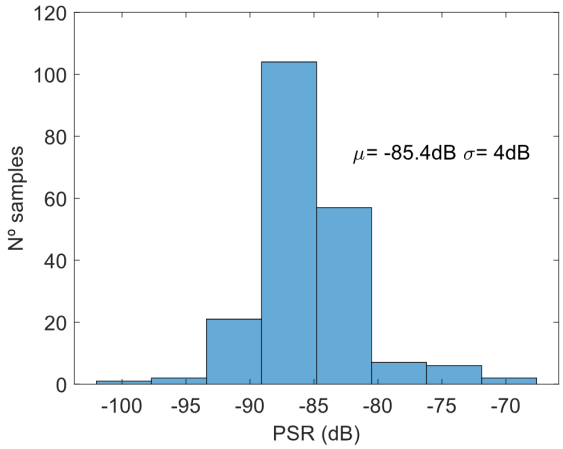

Figure 3.25: Monte Carlo simulation of the PSR of the proposed LDO at DC.

need to be larger, and the generated power would still be limited from a few nanoamps to a few hundred microamps, depending on the energy harvester and the power source intensity. However, it is unlikely that currents greater than a few microamps are needed for the *SynCell* microsystem.

The load regulation has been measured in two samples and is shown in Fig. 3.26. According to the measurements, this regulator can supply up to $\sim 30\mu A$ with a drop-out voltage of only 260 mV. It suffers a 0.067 mV variation at the output per microamp change in the load current. The simulated quiescent current consumption of this LDO is just 20 nA, which represents only 0.067% of the maximum deliverable load current. Hence this LDO can be considered highly efficient within this range.

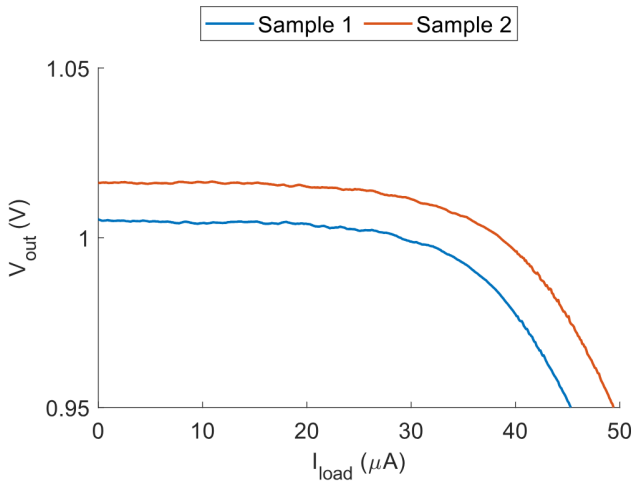

Figure 3.26: Measurement of the load regulation at $V_{dd} = V_{out} + 0.26$ V

.

Regarding the frequency domain characteristics of this regulator, Fig 3.27 shows the LDO loop gain for $I_{load} = 0$ A and $I_{load} = 1\mu$ A. Unlike many other designs, this LDO does not have stability issues when working with very low load currents, which usually happens in autonomous microsystems. The phase margin at the worst-case scenario (0 A) is 67°, which ensures correct stability even in such a situation.

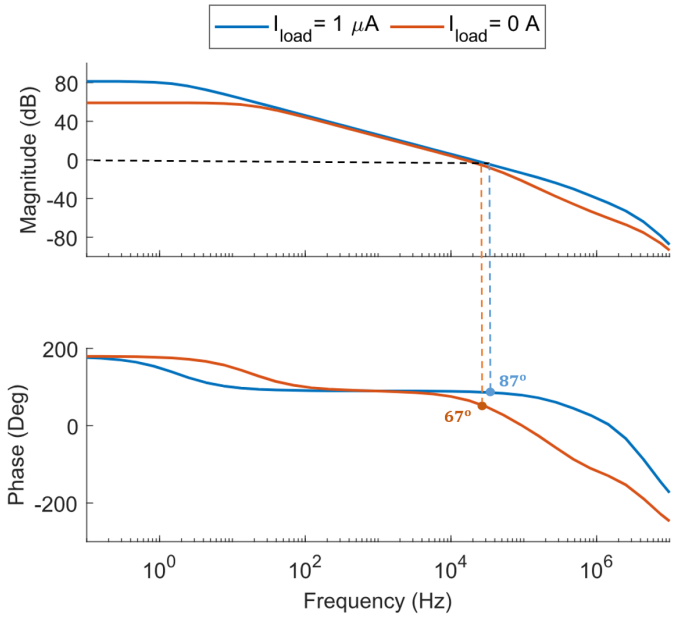

Figure 3.27: Simulation of the bode diagram of the proposed LDO for $I_{load} = 0A$ and $I_{load} = 1\mu A$.

The stability of the regulator can also be appreciated in the measured transient response of the LDO to a load change, shown in Fig. 3.28. In this measurement, a resistive load was commuted between $R_{load} = 100$ kΩ and $R_{load} = 10$ $M\Omega$ using a switch (V_{SW}) within 1 μs edge time. This is equivalent to a change in the output current from 100 nA to 10 μA. As

expected from the Bode diagram, no ripple is found in this measurement. The time required by the proposed LDO to recover from the load transient is ∼20 μs.

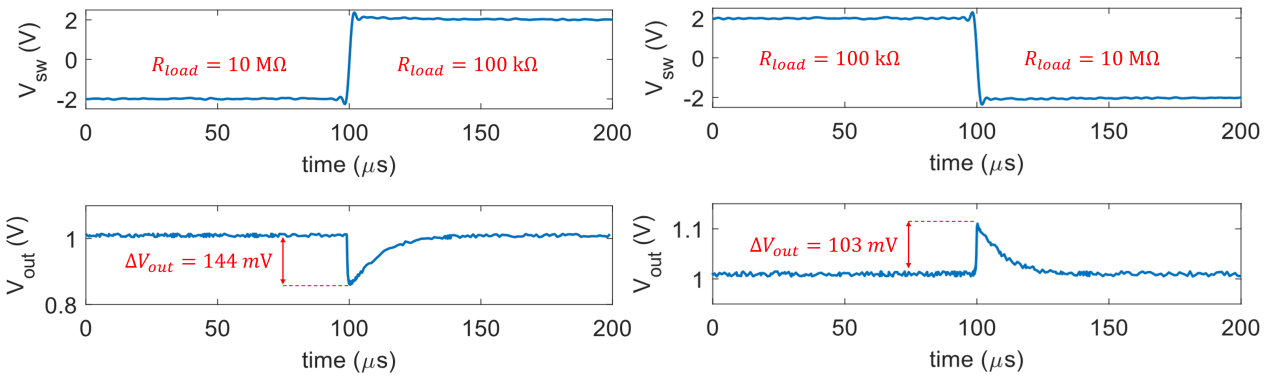

Figure 3.28: Measured transient response of the proposed LDO with a resistive load commuted between 10 $M\Omega$ and 100 $k\Omega$ in 1 μs.

3.8 PMU II

In the previous section, the proposed PMU achieved excellent results in terms of line regulation and PSR, which are two crucial parameters to consider in autonomous microsystems. However, since the first version of the microsystem was designed for in vitro measurements, the temperature was assumed to remain stable and no temperature compensation was carried out.

In the second version of PMU presented in this thesis, temperature-changing environments were targeted to enable more possible applications. In such scenarios, it is essential to develop a temperature-stable design since the precision of the system can be drastically affected by its temperature response. The need for a temperature-compensated design over a wide temperature range is then added to the already described area- and power-constrained scenario.

Satisfying all these requirements without giving up any important feature for autonomous microsystems presents a very challenging design scenario that not too many works in the literature can solve with solvency. Most temperature-compensated designs use bandgap references, which consume too much area and power for the restricted budget mentioned above. Some CMOS-only voltage references provide excellent results regarding temperature variation and power requirements [36, 61, 60]. However, when cell-sized microsystems are aimed, they are still far from meeting the area constraint, as they still require the addition of a regulator to supply power.

In this work we present a PMU composed of an LDO regulator and a voltage reference with ultra-low die area and quiescent power consumption, without any significant degradation in important features such as the line regulation, the temperature coefficient, or the PSR, making this design very suitable for autonomous microsystems applications. To the best of our knowledge, there is no other work that simultaneously addresses the design of a regulator and a temperature-compensated voltage reference with such reduced area and power requirements.

3.8.1 Voltage Reference

Most PMUs include a voltage reference and an LDO that follow a connection scheme similar to that shown in Fig. 3.29.a. In this structure, the reference voltage is generated by an independent section, V_{ref}, and is used to establish the value of the output voltage. However, we propose a structure in which the voltage reference is embedded in the feedback loop of the regulator around the EA (EA), as shown in Fig. 3.29.b, with the purposes detailed next.

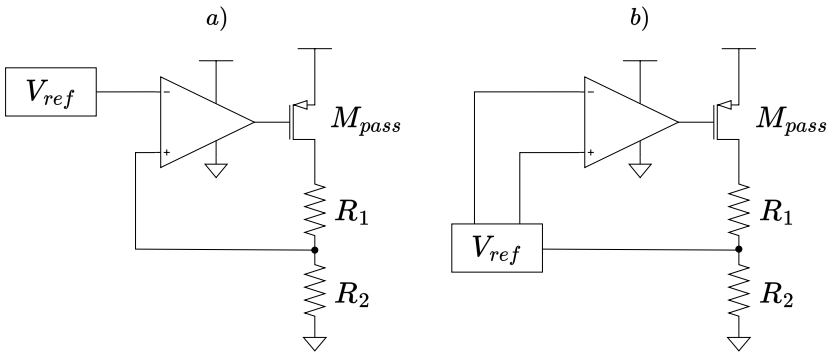

Figure 3.29: Conceptual scheme of a) a typical LDO with a voltage reference, b) an LDO with a voltage reference integrated into its feedback loop.

The main upside of this alternative is that the voltage reference takes advantage of the regulator's open loop gain through the feedback loop, to enhance parameters such as the line regulation or the PSR, while, at the same time, the LDO can deliver regulated power to the core of the microsystem.

In order to show the advantages of the proposed configuration for supply dependency, we assembled the same voltage reference inside and outside of the feedback loop with an ideal EA. Then the line regulation was simulated for different EA gains. The ratio between the line regulation of both configurations is shown in Fig 3.30. Up to one order of magnitude improvement can be achieved for high EA gains.

The topology of Fig 3.29.b uses the same circuitry to enhance parameters such as the line regulation or the PSR and to deliver regulated power to the core of the microsystem. As a result, the die area of the PMU is significantly optimized. In fact, this design occupies an area of the same order as the smallest reported voltage references [48, 36, 44], to generate not only a bias voltage but also a stable voltage supply to power the core of the microsystem. Unlike this design, none of the smallest voltage references reported to date can act as a power supply even for low-current demanding systems.

To implement this structure, the voltage reference of this work was set to rely on the threshold potential. The simplified schematic of the proposed PMUis shown in Fig. 3.31. The voltage reference block is based on the threshold voltage difference between an HVT metal-oxide-semiconductor field effect transistor (MOSFET) (M_1) and a regular MOSFET (M_2). This reference can be realized with as few as four transistors, making it very suitable for area-constrained applications. To explain the voltage reference principle of operation, let's first point out that the transistors $M_{3,4}$ work as current sources with the same bias voltage, so they

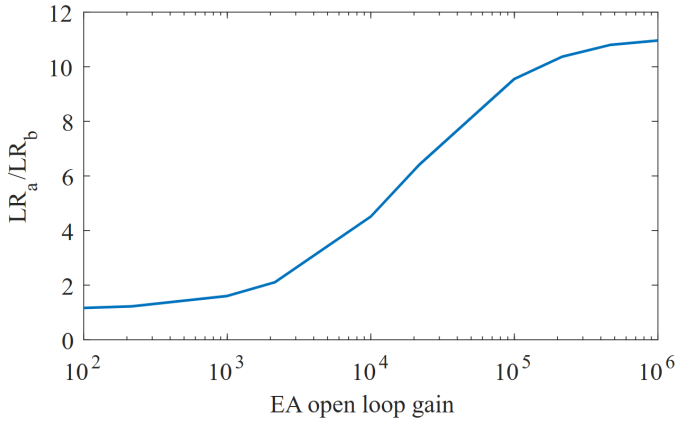

Figure 3.30: Ratio between the simulated line regulation of the regulator of Fig 3.29.a and that of Fig 3.29.b with the same voltage reference.

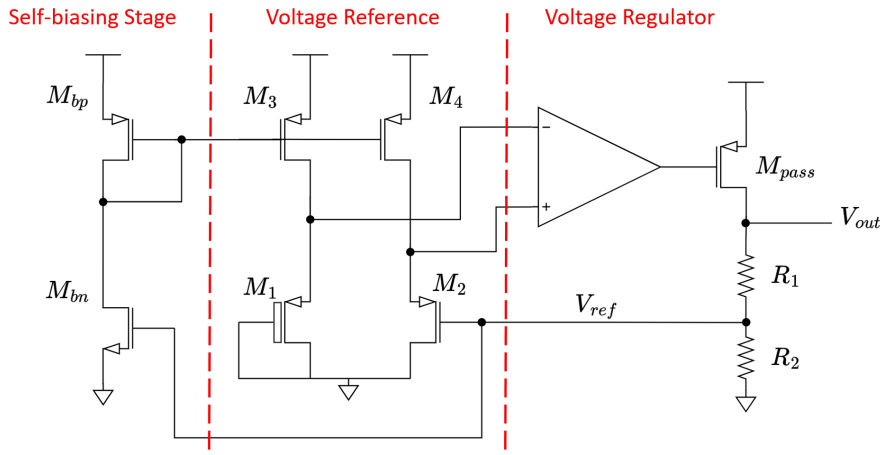

Figure 3.31: PMU simplified schematic.

both supply the same current to transistors M_1 and M_2. On the other hand, the regulator, due to its high open-loop gain and negative feedback, equals the voltages at the sources of both M_1 and M_2. Consequently, in order for these two transistors to draw the same current, the output stage of the LDO is forced, through the feedback network, to apply a voltage at the gate of M_2, V_{ref}, that compensates for the difference in threshold voltages between M_1 and M_2. Finally, the output voltage generated by the proposed circuit can be expressed by:

$$V_{out} = V_{ref}\frac{R_1 + R_2}{R_2} \tag{3.14}$$

At the same time, to make this design low power, every transistor is set to work in the deep subthreshold regime where the drain current of a transistor is governed by:

$$I_{DS} = I_0\frac{W}{L}e^{\frac{q(V_{GS}-V_{TH})}{nK_bT}} \tag{3.15}$$

where I_0 is the scale current, V_{TH} is the threshold voltage, n is a fitting parameter, q is the the electron charge, K_b is the Boltzmann constant, and T the temperature. Current I_0 is described by the following equation:

$$I_0 = \mu\sqrt{\frac{q\varepsilon_{s_i}N}{2\phi_s}}(\frac{K_bT}{q})^2 \tag{3.16}$$

where N is the doping concentration, ϕ_s represents the surface potential and ε_{s_i} is the relative electrical permittivity of the silicon.

Assuming the negative feedback is strong enough, we can equal the currents flowing through transistors M_1 and M_2, I_{DS1} and I_{DS2}, as well as voltages V_{S1} and V_{S2}, and resolve the equation for V_{G2} (V_{ref}) giving as a result:

$$V_{ref} = \frac{n_2}{n_1}|V_{TH1}| - |V_{TH2}| - \frac{n_2K_bT}{q}ln\frac{I_{01}W_1L_2}{I_{02}W_2L_1} + V_S(1 - \frac{n_2}{n_1}) \tag{3.17}$$

where the voltage V_S can be obtained from (3.15):

$$V_S = |V_{TH1}| + \frac{n_1K_bT}{q}ln\frac{I_{DS}}{I_{01}} \tag{3.18}$$

It can be observed that the voltage V_S introduces a dependency on the bias current I_{DS}. However, since n_1 and n_2 are very similar in (3.17), the dependency is small.

Note that for simplicity, no second-order effects were included in the equations, although they were considered in the design. In particular, the cascoding technique was used in the current sources of the voltage reference, as will be shown later, to attenuate the channel length modulation effect. Otherwise, the regulation of the supply voltage, among other parameters, would suffer a significant degradation. For the same reason, the entire design is self-biased to reduce the supply sensitivity of the circuit as much as possible. This not only results in a significant improvement in line regulation and the PSR at low frequencies, but also saves significant die area by eliminating the necessity of additional biasing or startup circuitry to achieve a stable operating point.

Temperature Compensation

Developing a temperature-stable design becomes crucial when considering outdoor applications or any other scenario where there is a significant temperature variation. Since it is implicit in the nature of transistors to vary their operating conditions with the temperature, preventive measures must be taken in the design. There are two conventional approaches, as explained in [70], to perform a temperature-compensated design. The first method is to add two terms with complementary temperature coefficients. The second method is based on multiplying two terms with complementary temperature coefficients. In this work, both methods are used because in view of the nature of (3.17).

To simplify the explanation of the temperature behavior of the voltage reference let's first assume that the slope parameters of the transistors M_1 and M_2 in Fig. 3.31 are equal, i.e., $n_1 = n_2 = n$, which in reality, for the technology and the transistors used in this case, does not carry a significant error as long as weak inversion saturation ($V_{DS} \geq 4\frac{K_b T}{q}$) is granted [43]. In this case then (3.17) is simplified as follows:

$$V_{ref} = |V_{TH1}| - |V_{TH2}| + Q \tag{3.19}$$

where:

$$Q = -\frac{nK_bT}{q} ln \frac{I_{01}W_1L_2}{I_{02}W_2L_1} \tag{3.20}$$

It is well known that the threshold voltage has a significant negative temperature coefficient [45]. According to the BSIM 4.5 simulation model, the behavior of the threshold voltage versus temperature is modeled by the following equation:

$$V_{TH} = V_{TH0} + K\left(\frac{T}{T_0} - 1\right) \tag{3.21}$$

where V_{TH0} is the threshold voltage at the nominal temperature T_0 and K is the temperature coefficient for the threshold voltage. Consequently, if V_{TH1} and V_{TH2} are subtracted, as in (3.19), their temperature dependence relies only on the difference of the temperature coefficients:

$$\frac{\partial(V_{TH1} - V_{TH2})}{\partial T} = \frac{K_1 - K_2}{T_0} \tag{3.22}$$

Since these two coefficients K_1 and K_2, are very similar to each other, some temperature compensation is already provided, as shown by the blue line in Fig. 3.32 extracted from simulations.

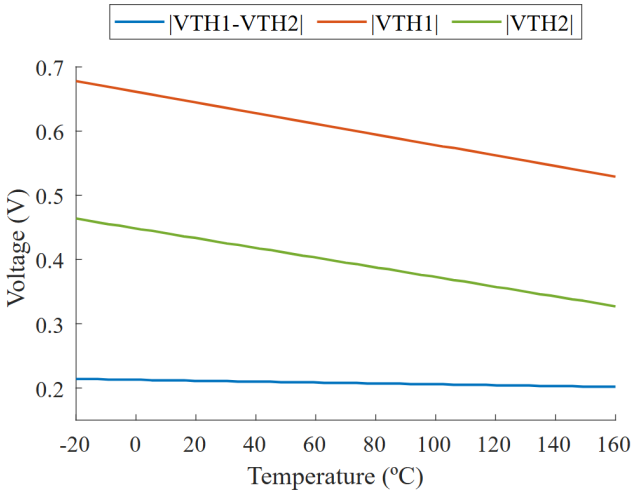

Figure 3.32: Simulation of the threshold voltages behavior vs. temperature.

A major improvement in the temperature compensation can be achieved by carefully designing the remaining term in (3.19), Q. The expression of Q can be split into the product of $-\frac{nK_bT}{q}$, which is clearly a CTAT term with a fixed slope, and $ln\frac{I_{01}W_1L_2}{I_{02}W_2L_1}$, which shows a PTAT behavior with a variable slope. The reason behind this PTAT response is a more pronounced degradation in the mobility of transistor M_2 relative to that of M_1 in the I_{02} and I_{01} terms with increasing temperature. Since the PTAT term is adjustable, it can be set to a value where the overall slope of Q cancels to some degree the temperature coefficient provided by the threshold voltage difference.

As mentioned before, I_0 is modeled by (3.16), where the carrier mobility μ, the thermal voltage $\frac{K_bT}{q}$ and the surface potential ϕ_s, which is modeled by (3.23), are the only temperature-dependent terms. However, when dividing $\frac{I_{01}}{I_{02}}$, the dependence of the surface potential temperature and the thermal voltages cancel each other out, and the only temperature contribution comes from the mobility ratios $\frac{\mu_1}{\mu_2}$.

$$\phi_s = \frac{K_bT}{q} ln \frac{N}{n_i} \tag{3.23}$$

In a first-order approach, the temperature behavior of the mobility can be modeled by:

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^m \tag{3.24}$$

If we combine (3.16) and (3.24), the expression in (3.20) can be rewritten as:

$$Q = -\frac{nK_bT}{q} ln \left(S \frac{\mu_{01}(\frac{T}{T_0})^{m_1}}{\mu_{02}(\frac{T}{T_0})^{m_2}} \sqrt{\frac{N_1}{N_2}} \right) \tag{3.25}$$

where S is the ratio of the geometries of the transistors M_1 and M_2:

$$S = \frac{W_1L_2}{W_2L_1} \tag{3.26}$$

The parameter Q is plotted against temperature in Fig. 3.33 for different values of S. Depending on whether the result of the logarithm is negative or positive, as a result of the selected S value, Q can have either a PTAT or a CTAT behavior respectively. As can be observed, Q has a quasi-linear behavior ($R^2 > 0.99$), and consequently (3.25) can be approximated by the first two terms of its Taylor series centered at T_0 (eq. 3.27):

$$Q \simeq \frac{-nK_bT_0}{q} ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) - \frac{nK_b(T - T_0)}{q} \left(ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) + m_1 - m_2 \right) \tag{3.27}$$

whose slope is given by (3.28):

$$\frac{\partial Q}{\partial T} \simeq -\frac{nK_b}{q} \left(ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) + m_1 - m_2 \right) \tag{3.28}$$

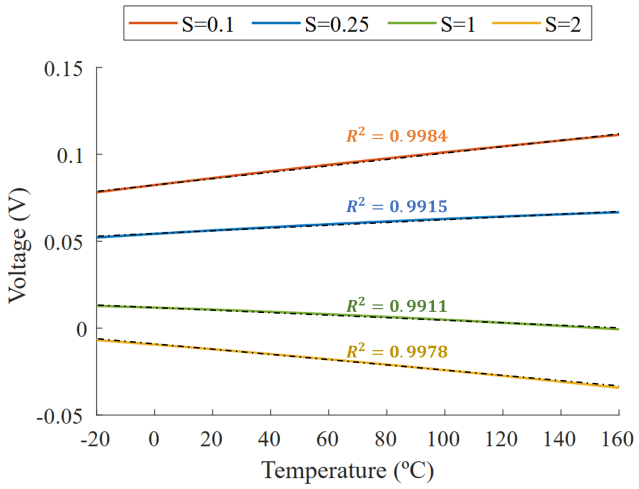

Figure 3.33: Q vs temperature for different values of S.

The value of $\frac{\partial Q}{\partial T}$ can be set by the geometries of S of the transistors M_1 and M_2, as shown in Fig. 3.33. When S is chosen such that $\frac{\partial Q}{\partial T}|_{T0} = |\frac{K_1 - K_2}{T_0}|$ the temperature effect at T_0 is canceled and a significant improvement in the overall temperature compensation is achieved over the whole temperature range of this design. Note that every single term in (3.28) other than S, which is the design variable, is either a known constant or a simulation parameter that can be obtained from the model given by the technology. Fig. 3.34 shows the theoretical temperature compensation that can be achieved following the mathematical development explained above.

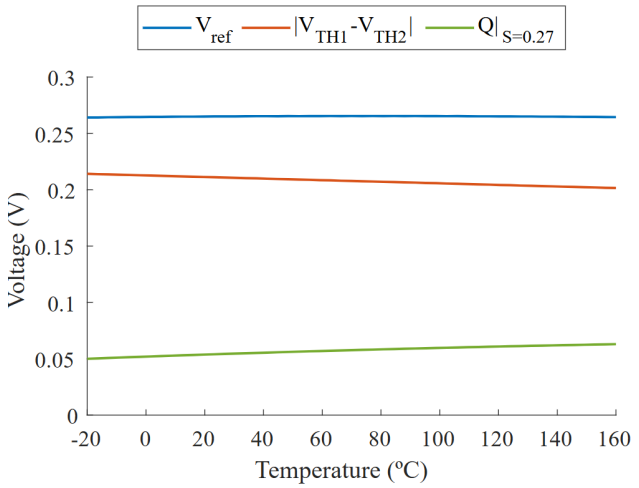

Figure 3.34: Theoretical representation of the temperature compensation of the design

It is also important to mention that since the mechanism available to tune the temperature compensation of this structure is based on pondering the $\frac{\mu_{01}}{\mu_{02}}$ ratio, it is essential to mitigate as much as possible the layout dependent effects that can affect the mobility ratio, such as the mechanical stress introduced by the STIs next to M_1 and M_2. To reduce this effect their diffusions were extended to move the STIs away from the channels. This layout measure,

unlike the option of adding a dummy transistor on each side, increases the drain and source capacitance to the bulk. However, it requires less area for similar stress mitigation. At the same time, large transistor sizes were used for M_1 and M_2, which also helped to reduce the compression of the channel.

Finally, if the consideration $n_1 = n_2$ is not assumed, a second iteration for S around the previously obtained value is needed to account for the slight deviation introduced in the temperature behavior. The theoretical value of S calculated from 3.19 to obtain the best temperature compensation was 0.27, and after the second iteration, the value was moved up to 0.275, meaning that the simplified model given by 3.19 is accurate enough to obtain a first estimate with an error of less than 2% to the final value, while at the same time greatly simplifying the calculation.

3.8.2 Voltage Regulator

The complete schematic of this PMUis shown in Fig. 3.35

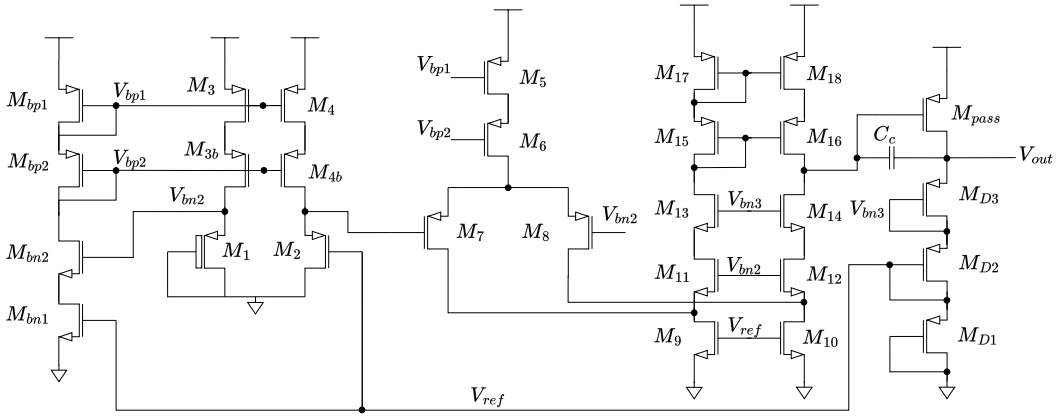

Figure 3.35: Complete schematic of the proposed PMU.

The voltage regulator used in this PMU is almost identical to the LDO presented in the previous PMU. For this reason, we believe it is not necessary to repeat its description. We will only detail the main differences.

- This regulator is designed to output a voltage of approximately 800 mV. This lower voltage helps to further reduce the power consumption of the system while remaining at a usable level for the sensor and the VCO. To achieve this output voltage, a feedback factor of 1/3 is required.
- The size of the pass transistor was increased to augment the maximum load current up to 40 μA. This results in around 30 μW of regulated power that can be delivered to the load, the same as in the former PMU (30 μA at 1 V).
- The biasing of the regulator is generated from a self-biasing stage, that depends on the regulator's output voltage.
- The minimum phase margin guaranteed for this design is 48°at I_{load} =0 A.

3.8.3 Simulations and Measurement Results

The chip photograph is shown in Fig. 3.36 with the proposed PMU highlighted in red, alongside a capture of the layout.

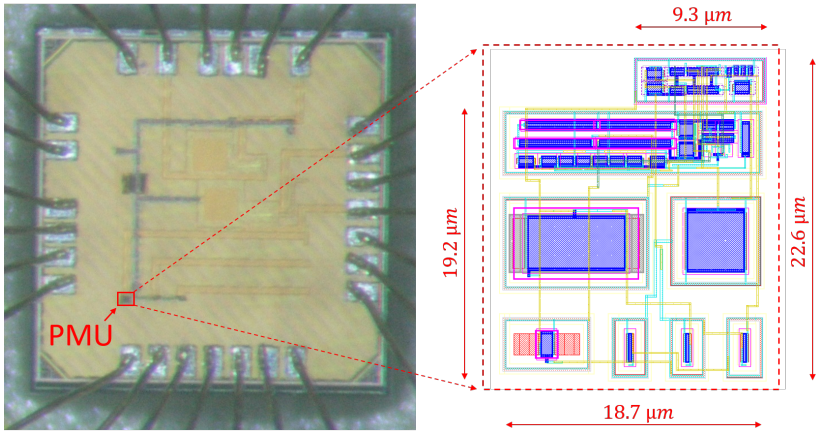

Figure 3.36: 1x1 mm^2 chip photograph and layout capture.

In this particular layout, the differential pair, the current mirrors, and the current sources were matched using common centroid and interdigitation techniques. The sampling network was implemented using transistors M_{D1-D3} in a diode configuration with their bulk terminals short-circuited to their sources. This cancels out the body effect, so they provide the same voltage drop. However, this requires a separated n-well for each device. Additionally, M_{D1} is interdigitated in between M_{D2} and M_{D3} to reduce the effect of any possible manufacturing gradient in the feedback factor. Transistors M_1 and M_2 were also implemented within their own n-well to prevent the body effect from degrading the voltage reference. Finally, their diffusions were extended to move the STIs away from the channels and minimize the effect of the mechanical stress on the mobility of the carriers, which is crucial for this temperature compensation.

The physical implementation of this design occupies a total area of 391 μm^2, making it one of the smallest voltage references reported in the literature. This work is compared to the smallest reported voltage references in the results section 3.9. It is worth noting, however, that, unlike the other references in this list, this circuit can also deliver a certain amount of regulated power, further emphasizing the area optimization of this design.

Measurements were performed using an Agilent 4156C Precision Semiconductor Parameter Analyzer, a VöTSCH VCL 4010 Temperature Chamber, and a Keysight MSO9104A Mixed Signal Oscilloscope.

The supply dependence of this circuit was measured in 16 samples. The average line regulation between 0.85 V and 1.85 V was found to be 0.173 %/V, which is slightly higher than the expected mean of 0.109 %/V from the 200-run Monte Carlo simulation shown in Fig. 3.38. The best and worst measured results were 0.025 %/V and 0.832 %/V, respectively. Figure 3.37 illustrates the supply dependency of V_{out} in two measured samples compared to the typical simulation case simulation (0.02 %/V).

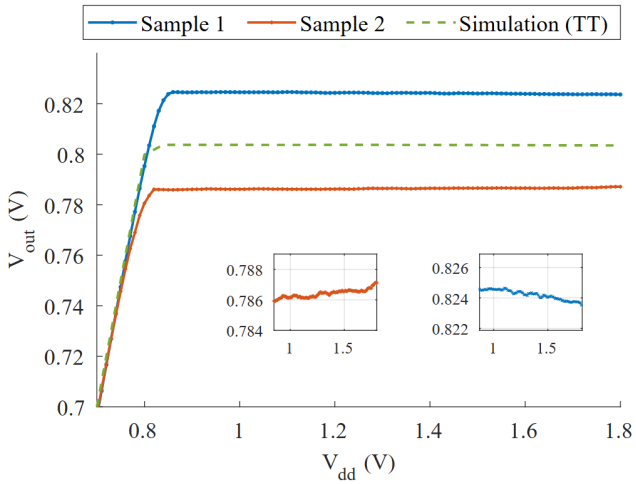

Figure 3.37: Measured supply dependency of V_{out}.

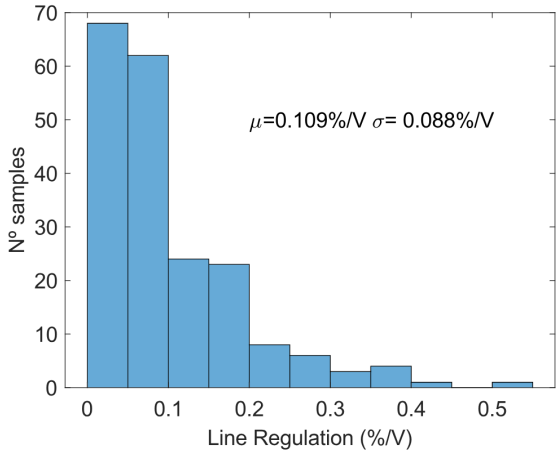

Figure 3.38: Monte Carlo simulation of the line regulation of the LDO.

The typical case and the Monte Carlo simulation of the PSR @1 Hz are shown in Fig 3.39 and Fig. 3.40 respectively. While the typical case simulation provides a best-case PSR of -87 dB at low frequencies, the average value obtained in the Monte Carlo simulation is -67.1 dB. These simulation results of the PSR prove this design's good supply dependency at low frequencies.

On the other hand, we focused on ensuring that the regulator had low temperature drift over a wide temperature range. Temperature compensation was an important aspect of the design. Fig. 3.41 shows the typical case simulation of the temperature behavior at $I_{load} = 4nA$ and $I_{load} = 4\mu A$. The regulator demonstrated an outstanding TC of 55 ppm/°C (between -10°C to 125°C) for the first case and 40 ppm/°C (between -30°C to 125°C) for the second case. We also checked how process variations affect this parameter through a 200-run Monte Carlo simulation (Fig. 3.42), where the average temperature coefficient obtained was 139.9 ppm/°C, with a standard deviation of 56.2 ppm/°C from -20°C to 125°C. Measurements of the temperature behavior of 5 samples are shown in Fig. 3.43. The average measured TC was 128.4 ppm/°C from 0 to 120 °C, with a best case of 96.5 ppm/°C and a worst-case

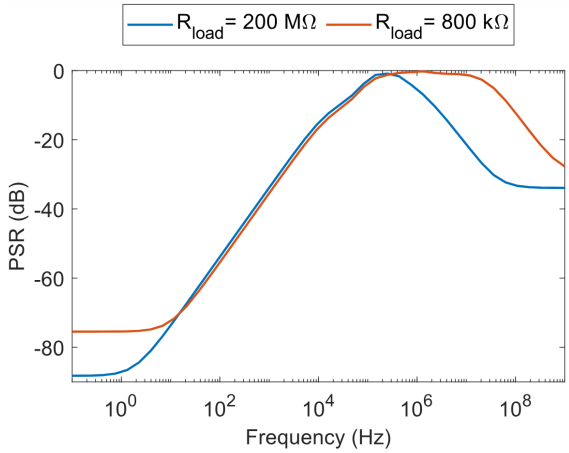

Figure 3.39: Typical case simulation of the proposed PMU's PSR vs. frequency with C_{load} =100 fF and different values of R_{load}.

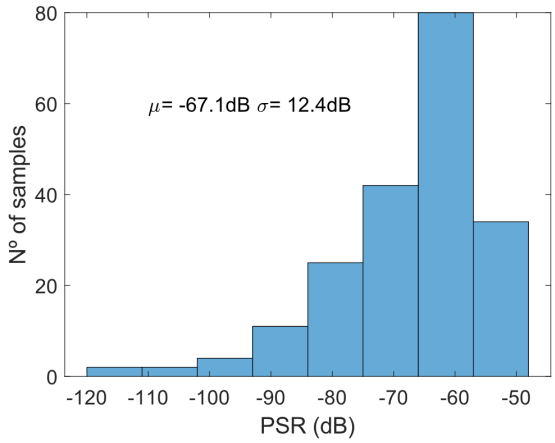

Figure 3.40: Monte Carlo simulation of the proposed PMU's PSR at 1 Hz.

of 163.8 ppm/°C.

At the same time, it is worth mentioning that, unlike this work, all the temperature coefficients reported in Table 3.2 would worsen when used alongside a linear regulator due mainly to the offset drift of the regulator with temperature, as can be seen in 3.7. This effect is exemplified in [36] where the typical case TCsimulated rises from 40 ppm/°C to 91 ppm/°C after including an LDO in the system [71]. Additionally, the effect that the offset drift has on the temperature coefficient increases inversely proportional to the feedback factor β. This means that the lower the voltage reference is the more degradation the TC would suffer due to the offset drift. This is especially problematic in low voltage references such as [44] (V_{ref}=26 mV) or [60](V_{ref}=118.1 mV).

In terms of power efficiency, this PMU can supply regulated power up to around 32 μW (40 μA @ 0.8 V) under high-efficiency performance. The regulator requires a drop-out voltage of 250 mV to supply the maximum load current, which meets the low drop-out standards of the topology. The average measured quiescent current is 18.4 nA, which constitutes less than

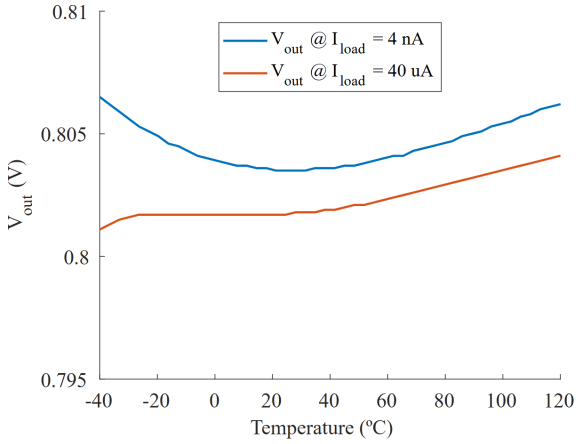

Figure 3.41: Temperature behavior simulation of the LDO from -40°C to 125°C at $I_{load} = 4nA$ and $I_{load} = 40\mu A$.

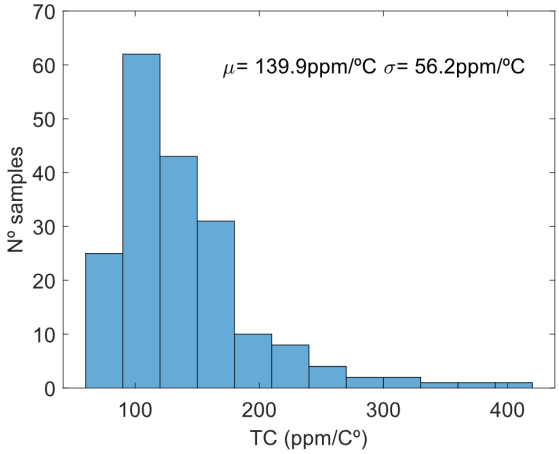

Figure 3.42: Monte Carlo simulation of the temperature coefficient of the LDO at $I_{load} = 20\mu A$ from -20°C to 125°C.

0.05% of the 40 μA that can be delivered to the load. Only about 1.5 nA (from simulations) of this quiescent current is used for the voltage reference, while the rest is distributed among the different branches of the LDO. Although both quiescent contributions can be reduced below 1 nA, it was a design decision not to do so. Minimizing the quiescent current would make the transient response too slow, even for the very relaxed response times of most autonomous microsystems. Biasing in the pA range usually results in settling times on the order of tens of ms [64].

Fig. 3.44 shows the measured load regulation of two samples. Both silicon prototypes were supplied with 250 mV more than their nominal output value. The average load regulation measured from 16 samples is 0.0381 $mV/\mu A$. As explained before, the load regulation of this tiny PMU cannot be compared or expressed on the same scale as the traditional LDOs because the significantly smaller size chosen for the pass transistor in this design reduces the output transconductance and consequently worsens the load regulation as well.

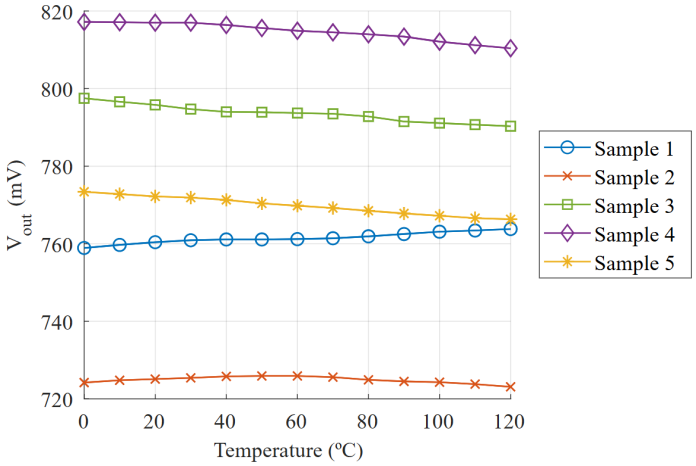

Figure 3.43: Temperature behavior of 5 samples measured from 0°C to 120°C.

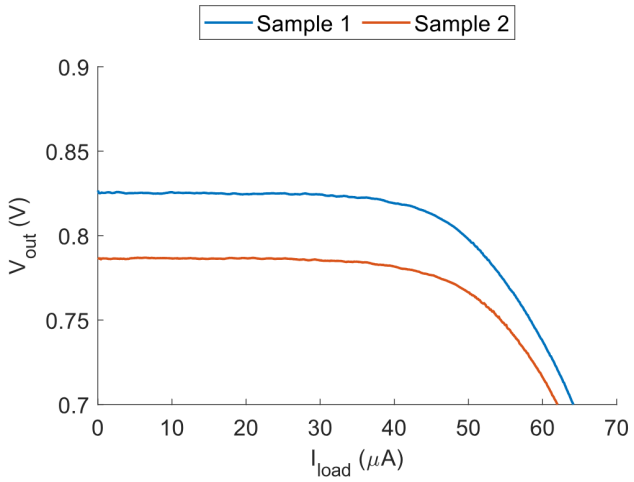

Figure 3.44: Measured load regulation at $V_{dd} = V_{out} + 250mV$.

The voltage reference present in this PMU outputs a typical case simulated value of 267.7 mV. Since the feedback factor chosen for the LDO is 1/3, the output of the LDO is set around 800 mV. A 200-run Monte Carlo simulation was performed and the results are displayed in Fig. 3.45. The simulation showed that the average voltage reference value is 271 mV, with a standard deviation of 26 mV. Measurements were made only at the output of the LDO, as it was a design decision not to make the voltage reference output accessible to avoid the measurement setup affecting the operation point of the circuit. The measured LDO output voltage from 16 samples was 777.9 mV with a standard deviation of 65.7 mV ($\sigma/\mu = 8.45\%$).

This relatively high process variation is attributed to the use of different transistor types on the one hand, and the use of a self-biased structure on the other. Although the self-biased structure introduces some process variation, it is advantageous as it improves supply regulation significantly. It also eliminates the need for an additional stable biasing circuit, saving space, which is crucial for this design.

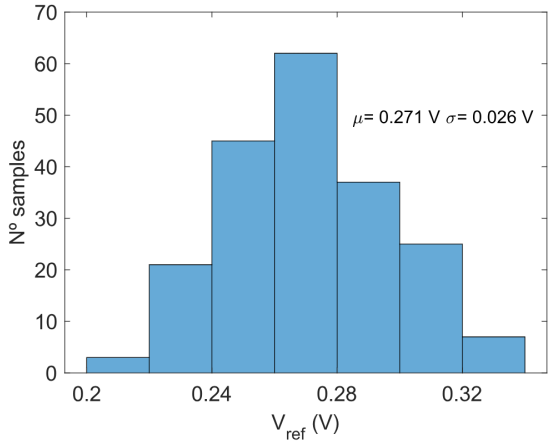

Figure 3.45: Monte Carlo simulation of the voltage reference.

On the other hand, using different types of transistors always introduces some process variation as well. Most researchers address this issue by including a trimming stage [49, 50]. However, this technique is not suitable for autonomous microsystems. Firstly, it comes with a significant area penalty. Secondly, post-fabrication calibration is not trivial in these very tiny microsystems.

Besides, most autonomous microsystems are usually designed to allow for even larger variations, due to their constrained area and power characteristics. For example, the microsystem presented in [12] allows for a variation of the core voltage going from 1.8 V to 0.3 V and uses a sub-nW clock [72] with an inaccuracy of $\sigma/\mu = 31.4\%$.

The transient response to a load change is shown in Fig. 3.46. In this measurement, a resistive load is switched from $R_{load} = 8.2\ M\Omega$ to $R_{load} = 50\ k\Omega$ at the output of the regulator. The switch was implemented with an external transistor driven by a pulse generator's signal (V_{SW}), whose edge time was configured to 1 μs. This is equivalent to a load current step from $I_{load} = 0.1\ \mu A$ to $I_{load} = 16.5\ \mu A$. First, the good stability of the regulator is demonstrated as there is no ripple at the output voltage during the transient response. Second, the maximum overshoot (162 mV) and undershoot (112 mV) remain within reasonable limits [36]. The response times of the proposed PMU for the described loading and unloading transitions are 29 μs and 13 μs respectively.

It must be remarked that many regulators have stability issues when working at very low load currents. However, this design was carefully compensated granting a phase margin of at least 48°in the worst-case scenario. Fig. 3.47 shows the loop gain bode diagram simulation for $I_{load} = 0A$ and $I_{load} = 1\mu A$ to showcase the stability of the design.

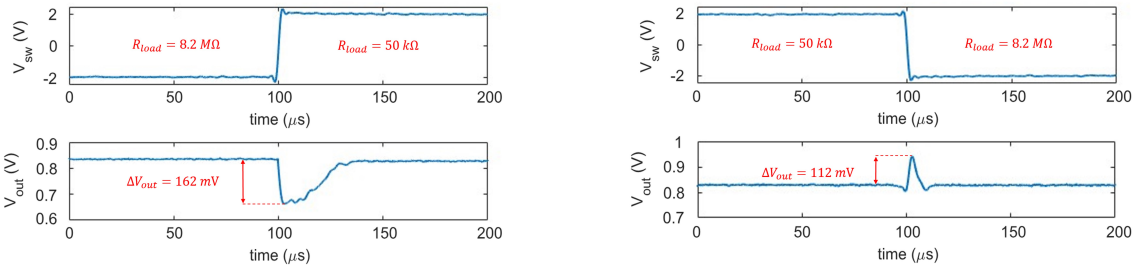

Figure 3.46: Measured transient response of the proposed PMU with a resistive load commuted between 8.2 $M\Omega$ and 50 $k\Omega$ in 1 μs.

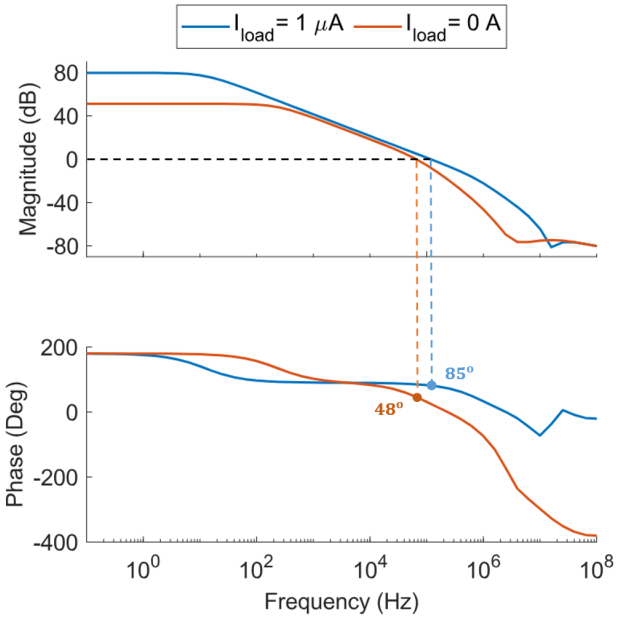

Figure 3.47: Simulated Bode diagram of the proposed PMU at $I_{load} = 0$ A and $I_{load} = 1\ \mu A$.

3.9 Results Comparison and Discussion

Designing a power management unit within an extremely constrained scenario of area and power is a truly challenging task. Most of the time, some performance has to be sacrificed to satisfy higher-priority requirements.

When working with weak energy harvesters as the power source, we found the following trade-offs to be suitable for autonomous microsystem designs:

- Significant area can be saved by making the size of the pass transistor smaller. This implies a reduction of the maximum deliverable load current, which should be set taking into account the energy harvester's capabilities. An excessively small pass transistor would lead to a high dropout voltage, which deteriorates the power efficiency.

- Load regulation can be sacrificed in order to reduce the quiescent power consumption, which is more relevant in autonomous microsystems.
- As long as the system tolerates it, a slower transient response can help to reduce the quiescent power consumption.

Another recommendable approach that has demonstrated to help in reducing the area and power of PMUs to the limits demanded in cell-size microsystems is exploiting the possibilities of the CMOS technologies. Opposed to the bulky BJTs designs, using different types of MOS transistors and leveraging their different threshold potentials has become a solid alternative to develop voltage and current references with very low requirements of area and power.

In this chapter, two different PMUs, composed of a voltage reference and an LDO, have been proposed using a 65 nm CMOS technology. Although both LDOs share similar features, the two voltage references were designed with very different approaches, leading thus to two PMUs that target very different scenarios.

The first PMU described in this thesis integrates a voltage reference to be used in stable temperature conditions, hence, no temperature compensation was needed. As a result, our main goal was to create a cell-size design, while developing a structure with excellent supply dependency and low power consumption.

On the other hand, the second proposed PMU presents a well-rounded design that includes an acceptable temperature compensation over a wide temperature range, which extends its potential applications to varying-temperature environments. Likewise, this PMU uses a novel topology that embeds the voltage reference in the regulator's feedback loop. This technique enhances the supply dependency of the voltage reference taking advantage of the open loop gain of the same regulator that is in charge of delivering regulated power. Consequently, a high optimization of limited resources, such as the area or the power consumption, is achieved.

Table 3.2 summarizes the performance of the proposed voltage reference for in vitro measurements (V_{ref} I) and the PMU for outdoor applications (PMU II) and compares them against only the smallest voltage references found in the literature. All the cited works in Table 3.2 utilize different variations of the SCM and 2T topologies, which require the fewest devices, resulting in more compact designs.

It can be easily noted in Table 3.2 that $V_{ref,1}$ outperforms all the cited works in terms of line regulation by at least one order of magnitude while consuming the second smallest area among them. These results emphasize the effectiveness of the techniques applied in V_{ref} I to reach a good supply dependency.

On the other hand, it is important to remark that, unlike the proposed PMU II, the works collected in the first table lack any kind of loading capability. Despite this significant improvement, it still ranks as the third smallest design, showcasing excellent area optimization. To put this into perspective, the LDO presented in [71] incorporates the voltage reference described in [36], and illustrates perfectly the area overhead required for an unbuffered voltage reference to have some loading capability. To compare [36] to our work we can take into account the loading capability per area of the reported in [71] to estimate the extra area that [36] would need to drive a 40 μA load, the same load as the proposed PMU in this work.

Indeed, the area needed by [36] would increase from 480 μm^2 to 750 μm^2, which is almost twice the area used in this design.

Last, Table 3.3 compares LDO I and PMU II to LDOs with similar target load and quiescent currents. It must be clarified that only [71] and the proposed PMU II include the voltage reference block in their design.

Low quiescent power LDOs, as mentioned earlier, tend to have a slower transient response (T_R) because the currents available to charge/discharge internal nodes are very limited unless adaptive biasing is applied [73]. The regulators listed in Table 3.3 have different speeds and quiescent consumption depending on their target applications. Therefore, to facilitate comparison, we have included the widely used figure of merit FOM_t in Table 3.3. This figure of merit, defined as 3.29, relates the response time of the LDO, T_R, the quiescent current, I_Q, and the load current step that the regulator has been proven to withstand, ΔI_{load}.

$$FOM_t = T_R \frac{I_Q}{\Delta I_{load}} \tag{3.29}$$

In view of the FOM_t results in Table 3.3, the proposed PMUs are not slow relative to their quiescent current consumption and the load current they can supply. This indicates an efficient use of limited resources.

In conclusion, two power management units for cell-sized autonomous microsystems implemented with a 65 nm technology have been presented. They integrate a voltage reference and a low-dropout regulator in a very compact area of 520 μm^2 and 391 μm^2 respectively. The reduced size of these PMUs makes them two of the smallest reported in the literature, which is a key feature when targeting cell-sized systems. The two designs proposed can efficiently supply up to 30 μW to the load while drawing a very low quiescent current. In particular, PMU I stands out for its extremely low supply dependency. Its main features make it highly suitable for applications with limited power sources, tight spaces and temperature-stable scenarios. On the other side, PMU II demonstrated good stability with respect to temperature and supply voltage while further reducing the area and the power consumption, hence showcasing an excellent compromise for most *Smart Dust* applications, including temperature-changing scenarios.

Table 3.2: Comparison of Results Against Ultra-Low Area Voltage References Related Works.

	V_{ref} I	PMU II	[48]	[36]†	[44]	[59]	[60]	$[49]_a$	$[49]_b$	[61]	[62]
Technology (nm)	65	65	65	40	130	65	180	65	180	180	130
Topology	β-mul.	split SCM	SCM	SCM	SCM	2T	2T	2T	2T	SCM	SCM
Area (μm^2)	320	391	104	480	665	840	900	900	1425	2500	3000
V_{dd} (V)	1.25-2.5	0.85-1.85	0.4-1.2	1.5-2.5	0.3-1.2	0.5-1.8	≥0.25	0.5-2.5	0.5-3.6	1.4-3.6	≥1.1
V_{out} (mV)	677	777.9	342.8	570	26	257.5	118.1	327.2	326.8	1250	800
σ/μ (%)	2.07	8.45	4.9	7	3.4	0.3	1.1	0.85	0.8	0.8	5
Min. Power (nW)	75	15.6*	0.00042	151	0.04	0.0143	0.113	0.24	0.006	0.033	27.5
Line reg. (%/V)	0.0022	0.173	0.47	5-8	0.188	0.02	0.3	0.33	0.044	0.31	2
PSR (dB)	-99†	-67.1†	-	-70†	-67.3†	-	-65	-40	-49	-41	-
	@1 Hz	@1 Hz	-	@ 915 MHz	@100 Hz	-	@100 Hz	@100 Hz	@100 Hz	@100 Hz	-
TC (ppm/ºC)	-	128.4	252.2	40	208	99.2	73.5	89.1-118.2	54-176	8-53	100
Temp. Range (ºC)	-	0∼120	-40∼60	-55∼125	-25∼125	0∼100	-40∼140	-20∼80	-20∼80	0∼100	-40∼85
Loading capability	No	40 μA	No	No	No	No	No	No	No	No	No

* The PMU average measured power consumption is 15.6 nW @$V_{dd,min}$. However, according to simulations, the voltage reference block only requires around 1.3 nW from the total.
† Simulated result.

Table 3.3: Comparison of Results Against Voltage Regulators Related Works.

	LDO I	PMU II	[65]†	[74]	[75]	[64]	[76]	[71]†	[73]†
Reg. Topology	LDO	LDO	LDO	DLDO	DLDO	LDO	LDO	LDO	LDO
Technology (nm)	65	65	-	65	65	180	180	40	65
Area (μm^2)	200	391	-	42000	48000	15000	4310	6700	200000
V_{dd} (V)	1.05-2.5	0.85-1.85	≥1.4	≥0.5	0.5-1	0.7-2.5	≥0.6	1.3-2	≥1
Dropout V. (mV)	260	250	200	50	100	300	100	200	200
Min. Power (nW)	20.4†	15.6	8.4	1350	0.373	0.679	3.5	1110.2	5
Line reg. (%/V)	0.0068	0.173	0.0025	0.688	-	-	0.636	5.7	0.5
PSR (dB)	-85.4†	-67.1†	-67†	-	-	-	-22.5	-28.5†	-
	@1 Hz	@1 Hz	@1 Hz	-	-	-	@10 Hz	@915 MHz	-
Loading capability (μA)	30	40	10	200	270	500	750	1000	50000
Loading per area ($\mu A/\mu m^2$)	150 e-3	102.3 e-3	-	4.8 e-3	5.6 e-3	33.3 e-3	174.0 e-3	149.2 e-3	250 e-3
FOM_t (ns)	40.4	33.7	113.4	9450‡	0.13	13192	1.286	640‡	1.4‡

† Simulated result.
‡ Estimated from the transient response.

Chapter 4

Voltage-Controlled Oscillator

4.1 Introduction

Analog-to-digital conversion is one of the first and most important steps to be performed in any system that works with signals from the physical world. Traditional ADCs perform this conversion by comparing the amplitude of the signal with respect to a given reference. However, they tend to be very area- and power-hungry for applications where these two characteristics are severely constrained.

In a microsystems context, digitization can be achieved in the time domain by using voltage-controlled oscillators, where the input signal is converted to a modulated frequency and the output can be easily digitized by measuring the frequency with counters. However, the main challenge with this type of conversion is to achieve a linear voltage-frequency response, since the resolution of the digitization is highly dependent on the linearity of the frequency provided by the VCO. Many VCO-based converters [77] include calibration circuitry, such as look-up tables (LUTs) [78], to linearize their performance, but these take up considerable area and power.

On the other hand, since autonomous microsystems do not need to be fast, a common approach to reduce power consumption is to operate at very low frequencies [12]. However, this is neither easy nor trivial when the large passive components required to generate slow time constants are not affordable, due to area constraints.

In this context, the design of a low-power cell-sized VCO with a linear voltage-to-frequency response is highly desired and useful. Hence, this chapter will discuss its design in detail.

4.2 State of the Art

Many VCOs have been proposed in the literature before. However, most of them target applications unrelated to this work with frequencies usually in the MHz to GHz range [79, 80]. Additionally, their power and area specifications are not suited to the requirements of cell-size autonomous microsystems.

The most commonly used strategies for designing very slow oscillators are based on the use of very low currents to charge/discharge capacitors. Some works use the transistor gate leakage current [81, 82] while others resort to the subthreshold leakage current [72, 83, 84, 85]. When limiting the research to only the works that fit within the highly constrained area and power budget, just a few oscillators become apparent.

For instance, in [81] transistor gate leakage current is used to charge and discharge a capacitor to carry out an oscillator used as a wake-up timer with ultralow-power (2 nW) and -area (480 μm^2) consumption. The main disadvantage of this topology is the high process variation exhibited, with a die-to-die σ/μ of 28 % and a within-die σ/μ of 12 % using a 130 nm technology.

On the other hand, other works such as [72] take advantage of the subthreshold leakage current to achieve very large time constants. They propose the use of positive feedback to sharpen the edges of the slow oscillating signal to reduce short-circuit currents. Hence, achieving power consumptions in the range of a few picowatts to hundreds of picowatts depending on the supply voltage. This work was used as the clock in an autonomous microsystem for in-vitro applications. PVT variations are, once again, the major issue of this work as their oscillator presented an inaccuracy of 31.4%.

These very weak currents make it possible to use relatively small passive devices to generate large time constants, thus allowing for reduced areas and power budgets. However, they raise some design concerns as these currents are very PVT-sensitive.

The impact of voltage fluctuations is usually mitigated by voltage regulators that provide steady voltages to the oscillator. Variations in manufacturing processes are often addressed through post-fabrication calibration. Temperature variations' effect is usually softened by restricting the use of these oscillators in temperature-stable environments since creating a temperature-compensated structure would result in a significant area penalty, as it occurs in [86], [87], and [88]. This penalty would make it impractical for use in cell-size microsystems.

Additionally, among the cited works, none of them can change linearly their frequency with respect to control voltage, and just [72] provides a method to tune, exponentially, the frequency. However, by doing so it loses its low-power characteristic.

4.3 Objectives

In our target scenario, both area and power are extremely limited, and consequently, voltage-to-frequency quantization [89] emerges as an interesting way to perform digitization.

The VCO described in this chapter was designed for the second generation of *MIT SynCells* [90]. It aims to convert the analog voltage from the sensor into a variable-frequency square-wave signal. The output of the VCO is then used by the LED driver to control the current flow to the LED, causing the LED to flash at a frequency proportional to the physical magnitude being measured. In this way, the sensor information is communicated to the receiver, which captures the light pulses with a CCD camera.

The frequencies of the VCO must be as slow as possible to reduce power consumption. At

the same time, a slower oscillating signal would facilitate the measurement setup. The VCO output will be eventually converted into light pulses of varying frequency. Although pulse lengths in the order of microseconds have been demonstrated to be readable in microsystems with similar communication approaches [6], a period in the range of milliseconds is easier to manage. Therefore, frequencies lower than 1 kHz were targeted.

The *Si*-controller of the *SynCell* occupies a total area of 50×50 μm^2. Hence, we aimed to use approximately one-third of the total area ($\sim 800\mu m^2$) in the VCO block to carry out the voltage-to-frequency conversion.

The power generated in the solar cell of the *SynCell* is mostly destined for the sensor and the LED leaving a very limited power budget for the *Si* chip. Hence, we want to restrict the power consumption of the VCO to the sub-nW range, which would also make its use easier in other microsystems.

Last, a linear voltage-to-frequency response, within the sensor's output range, is highly desirable to provide time-domain digitization with a more precise resolution. Otherwise, it would be challenging to distinguish between different input voltages.

Although analog-to-digital converters can provide faster and more precise conversions, it is important to note that no reported analog-to-digital converter (ADC) comes close to meeting these constraints of area and power. This is the reason why in this chapter we present a low-power and area linear VCO as a lightweight digitizer.

4.4 Sub-Threshold Leakage-Based Delay Element

Most oscillators designed for very slow frequencies currently use large R, L and C elements or frequency dividers that take up too much area. However, we can use the sub-threshold leakage currents of CMOS transistors to generate large time constants and positive feedback to create very steep slopes to reduce the short circuit currents. This approach results in ultra-low power consumption while keeping the area under very low limits. To achieve this, we used the element proposed in [72] as a starting point for our voltage-controlled oscillator. However, when this element is scaled down, important modifications are required, to achieve ultra-low frequency–area–power goals.

The delay element [72] is based on a thyristor structure, as is shown in Fig. 4.1. To explain how it works, let us assume that the input is low, which causes transistors M_1 and M_6 to be on and M_3 and M_4 to be off. This leads node N_1 to charge to V_{dd} and N_2 to discharge to GND. Consequently, transistors M_2 and M_5 are off. A transition from low to high of the signal `In` is then assumed. M_1 and M_6 are now off while M_3 and M_4 are turned on. The leakage current of M_5 is then used to charge C_2 and the leakage current of M_2 discharges the negative terminal of C_1. When the voltage on C_2 becomes greater than the threshold voltage, $V_{TH,n}$, M_2 becomes conductive, fully discharging N_1, which exponentially increases the conductivity of M_5 and, thus, the voltage on N_2. This positive feedback loop ensures that the transition of the output node N_2 is slow when all transistors are in the sub-threshold region and fast when the transistors are conducting. Although the overall power consumption is very low, peak currents in the microampere range have been observed during the short period when

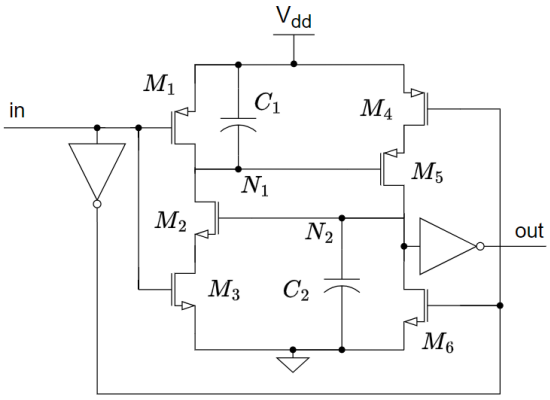

Figure 4.1: Leakage-based delay element.

the transistors are conducting. These currents represent an excessive power demand if energy harvesters were to power the system, and they must be significantly reduced.

Eventually, the delay provided by this circuit is given by

$$t_{d,M_5,C_2} = \frac{C_2}{I_{leak,M_5} - I_{leak,M_6}} \times V_{TH,n} \tag{4.1}$$

The full oscillator consists of N cascaded delay elements arranged and connected as a ring oscillator with a period N-times the delay of a single delay element.

At the same time [72] suggested a method to make the frequency controllable. By adding four transistors, the currents used to charge C_2 and discharge C_1 can be increased or decreased. However, their structure does not satisfy several design features that we consider critical for our target applications:

- The V-f response is highly non-linear; it follows an exponential equation, which results in a poor resolution when this VCO is used for time domain digitization.
- The power consumption grows exponentially with the control voltage, a critical drawback for ultra-low power systems.
- The input range does not support a rail-to-rail input swing, which is also necessary for time-domain digitization.
- Important current peaks, in the microampere range, were found in the structure presented in [72], which can cause some energy harvesters, such as *SynCell*'s solar cells, to collapse.

In this work, a highly linear VCO is presented to overcome all these issues.

4.5 Proposed VCO

The proposed VCO follows a ring oscillator structure with three delay elements connected in series as shown in Fig. 4.2. Consequently, the period is given by the addition of the three delays generated in the circuit as illustrated in Fig. 4.3.

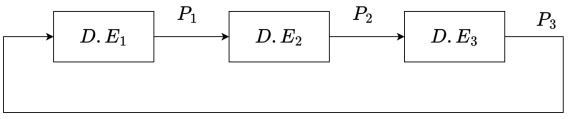

Figure 4.2: VCO composed of 3 delay elements.

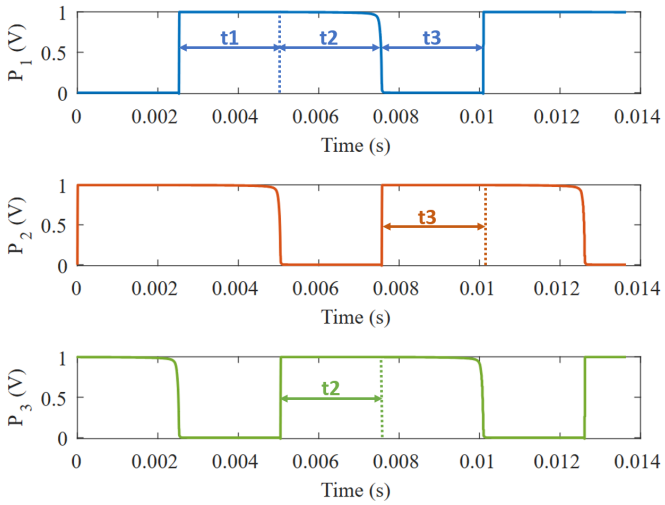

Figure 4.3: Transient simulation of the 3 phases of the VCO.

The thyristor-based delay element used to solve the aforementioned problems is shown in Fig. 4.4. The main goals of this design were: (1) to provide an ultra-slow frequency with reduced area; (2) to reduce the peak power, and (3), to generate an output frequency that varies linearly with an input voltage, while having no significant impact on area or power consumption.

4.5.1 Large Time Constants with Nanometer Technologies

The best way to reduce the area of microsystem circuits is to use a smaller technology node. This simple solution, which directly benefits the size of the circuits, comes with many other drawbacks and challenges. One of them, as explained in [91], is that leakage currents become more significant with smaller technology nodes.

Since the goal of our circuit is to generate very low oscillation frequencies, to dissipate as little power as possible, we first looked at methods of modifying and controlling the leakage currents that play a key role in the oscillator.

In our case, the leakage currents for 65 nm technology are significantly higher than for the 180 nm technology used in [72], thus leading to smaller time constants and, consequently, higher power consumption.

The main contributor to these currents is the subthreshold leakage current. Gate and body leakage can be disregarded, since simulations show them to be at least two orders of magnitude smaller. Therefore, the expression for the subthreshold leakage current is [92]

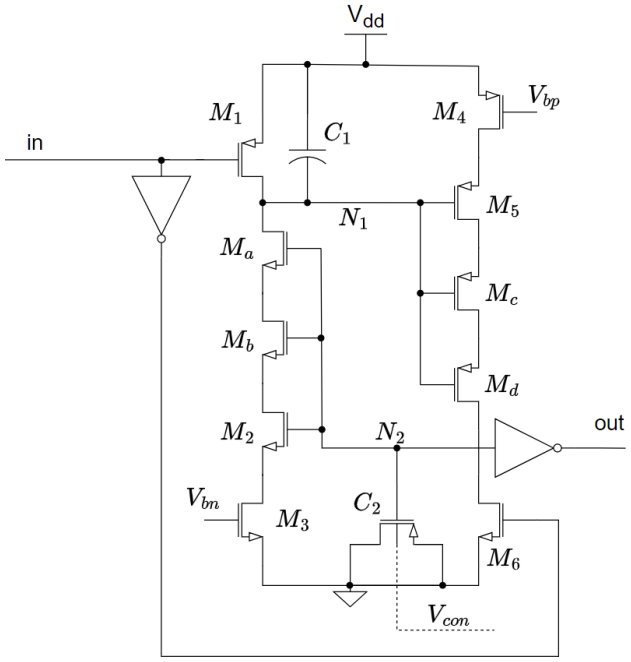

Figure 4.4: Proposed delay element with capacitance-tuning as voltage-control.

$$I_{DS} = I_S 10^{\frac{V_{GS}-V_{TH0}+\lambda_d V_{DS}+\gamma_d V_{BS}}{S}}(1 - 10^{\frac{-nV_{DS}}{S}}) \tag{4.2}$$

where V_{TH0} is the nominal threshold voltage and n is a fitting parameter. S is the subthreshold swing attending to the following equation:

$$S = n\frac{k_b T}{q} ln(10) \tag{4.3}$$

and

$$I_S = 2n\mu C_{ox} W/L(\frac{k_b T^2}{q}) \tag{4.4}$$

where μ is the carrier mobility, C_{ox} is the oxide capacitance per area, q is the the electron charge, K_b is the Boltzmann constant and T is the temperature.

In Equation (4.2), the drain-induced barrier lowering (DILB), which reduces the V_{TH}, is modeled by $V_{TH0} - \lambda_d V_{DS}$ and, similarly, the body effect is taken into account through $V_{TH0} - \gamma_d V_{BS}$. These two effects constitute a direct mechanism to reduce the leakage currents while the transistor is turned off ($V_{GS} = 0$ V).

We have taken two measures to minimize the DILB effect in Equation (4.2). First, it is known that the DILB effect has a greater impact on transistors with shorter channels. This is due to the depletion regions of the drain and source junctions depleting a larger fraction of the channel as the channel becomes shorter. This lowers the threshold voltage, V_{TH}, and causes an increase in the subthreshold leakage, which is more noticeable in smaller devices. For this reason, leakage currents can be significantly reduced by avoiding the use of minimum

channel lengths. Fig. 4.5 plots the period achieved at the output of the oscillator versus the channel length used for the thyristor transistors $M_{2,5}$ from the schematic shown in Fig. 4.1. In our 65 nm technology, it makes sense to move from 60 nm channel length to 200 nm, as in this region any variation will provide substantial improvements. Enlarging the channel much beyond 200 nm loses effectiveness, in terms of area, in obtaining the desired delay, as the slope in Fig. 4.5 decreases drastically.

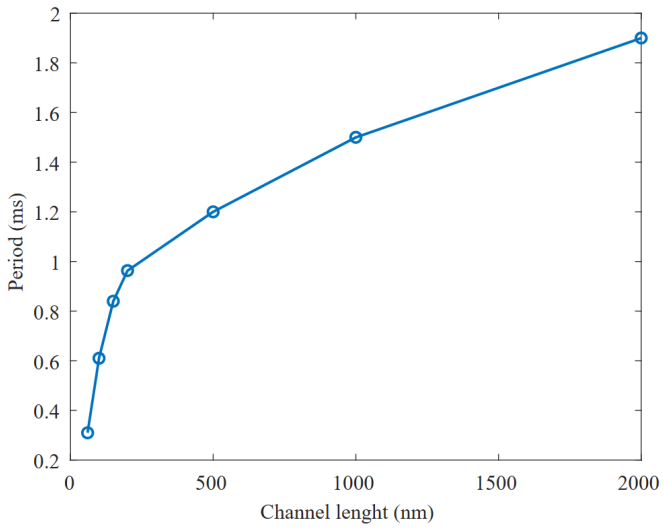

Figure 4.5: Influence of the channel length variation on the period of the generated signal.

Second, to further reduce the DILB effect, we decided to stack transistors M_{a-d} in Fig. 4.4, to reduce the V_{DS} voltage. This does not require much additional area, but it has a noticeable effect on the leakage currents, as $V_{DS2,5}$ is reduced from a value close to V_{dd} to just a few mV.

At the same time, to take advantage of the body effect, the bulk terminals of $M_{2,a,b}$ and $M_{5,c,d}$ were set to ground and V_{dd}, respectively. This increases their V_{TH} and helps to further reduce the subthreshold leakage.

On the other hand, the V_{TH0} in Equation (4.2) is another parameter that can be modified to achieve a larger delay. HVT transistors could have been used instead of standard transistors for the thyristor. This approach increases the threshold voltage by about ∼150 mV, which greatly reduces leakage currents. This reduction would translate into lower frequencies for the same area, or a reduction in capacitor size to save die area for the same target frequency. However, we ultimately rejected this option, due to the increased variability of this transistor type. Although the typical case simulations gave excellent results, we found multiple runs in the Monte Carlo simulation that did not oscillate at all. To solve this problem, the leakage currents needed to be increased, thus losing the main advantage of this technique. At the same time, this technique requires a higher minimum supply voltage (from 0.3 V to 0.7 V) for the oscillator to start operating, which can be another significant drawback in some cases.

Finally, it can be seen from Equation (4.1) that the leakage currents of the transistors $M_{1,6}$ should ideally be maximized, to increase the period. However, if they exceed a certain ratio to the $M_{2,5}$ leakage, the oscillator may stop oscillating. To avoid this, the currents of the

transistors $M_{1,6}$ are set to 10% of the $M_{2,5}$ currents. This ensures that the VCO operates correctly even under the high process variability characteristic of thyristor-based topologies.

4.5.2 Ultra Low Power Dissipation

Another issue with the design proposed in [72] that needs to be adjusted for our target application is the peak current. The short period of time that the transistors $M_{2,5}$ in Fig. 4.1 are on results in a very high peak current to charge or discharge both capacitors from V_{TH} to V_{dd} (or GND). Since the power supply in our case comes from a weak energy harvester, a high peak current will result in an unacceptably large voltage drop. For this reason, the M_3 and M_4 gates have been biased to a voltage ($V_{bn} = 0.23$ V and $V_{bp} = 0.77$ V, respectively) that will not significantly affect the leakage currents that charge/discharge the capacitors, but will limit the peak currents that occur when the positive feedback is activated. In other words, the bias voltages V_{bn} and V_{bp} limit the maximum currents through M_3 and M_4 to a few nA, and since the leakage currents used in the thyristor are in the order of tens of pA they are not affected; thus, the frequency of the oscillator remains unchanged.

With the same purpose of reducing the peak power consumption, the inverters are made current-starved with the same bias voltages, V_{bn} and V_{bp}. A simulation of how these bias voltages affect the peak currents is shown in Fig. 4.6, to illustrate the importance of setting the correct bias for transistors M_3 and M_4 if peak currents are to be monitored. The voltages V_{bn} and V_{bp} are generated by a robust power-management unit present in the chip containing this oscillator.

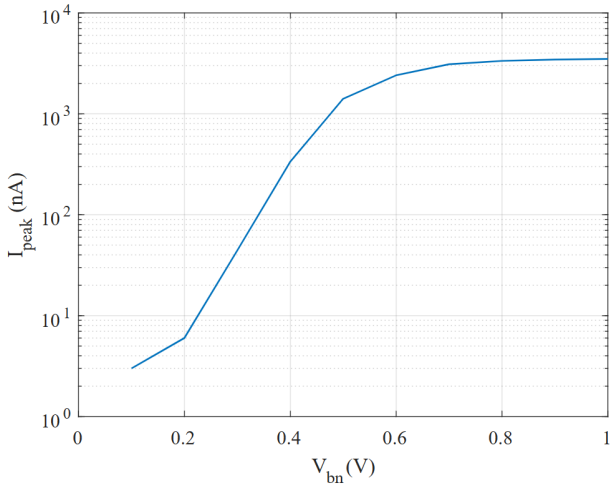

Figure 4.6: Simulation of the peak current drawn in the proposed VCO for different V_{bn} values.

4.5.3 Linearized Voltage-controlled Oscillator

When it comes to dynamically changing the output frequency of the oscillator, the RC time constant of the delay element must be tuned, with respect to the input signal. We propose an approach where the capacitance of the delay element is modified to produce a quasi-linear response.

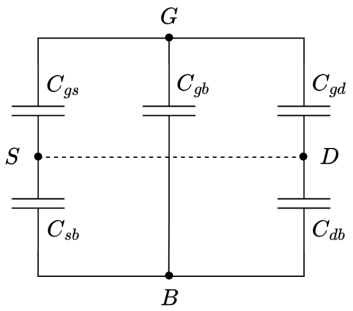

Figure 4.7: Parasitic capacitances model of a MOS transistor with source and drain connected.

The proposed structure is shown in Fig. 4.4. As can be seen, the capacitors used for this delay element are PMOS transistors with their source and drain terminals directly connected. CMOS transistors used as capacitors [93] are one of the most popular solutions to implement these passive components: firstly, they are available for any CMOS fabrication process without additional steps, which also translates into cheaper fabrication processes; secondly, they have the highest capacitance density of any option available in today's processes, which is why we have chosen them to produce large time constants in the smallest possible area.

The parasitic capacitance model of an MOS transistor is depicted in Fig. 4.7. It consists mainly of the following:

- Two overlap capacitances (C_{gs} and C_{gd}) similar to a parallel-plates capacitor and independent of the biasing voltage.
- Two junction capacitances (C_{sb} and C_{db}) resulting from the charge accumulation fluctuation around the depletion layer. These depend on the biasing voltage.
- The gate-to-bulk capacitance (C_{gb}), which has two components, one bias-dependent, the channel-to-bulk capacitance, and another one independent, the gate-to-channel capacitance.

After some simplifications, the effective capacitance between gate and source-drain (C_{eff}) can be expressed as:

$$C_{eff} = \frac{(C_{sb} + C_{db})C_{gb}}{C_{sb} + C_{db} + C_{gb}} + C_{gs} + C_{gd} \tag{4.5}$$

To vary the capacitance of the PMOS transistors (C_{eff}) used in the RC time constant of the VCO, the V_{gb} voltage must be tuned. This directly affects the parasitic capacitances C_{sb}, C_{db} and C_{gb} by thickening or thinning their depletion layers, which act as their dielectrics. Since the only voltage-dependent term in Equation (4.5) consists of depletion capacitances, the capacitance C_{eff}, according to the depletion capacitance theory [94, 95], follows a quadratic relationship with respect to the voltage (shown in Fig. 4.8), similar to

$$1/C_{eff}^2 = K_1 V_{con} + K_2 \tag{4.6}$$

where K_1 and K_2 are constants that can be obtained by simulation.

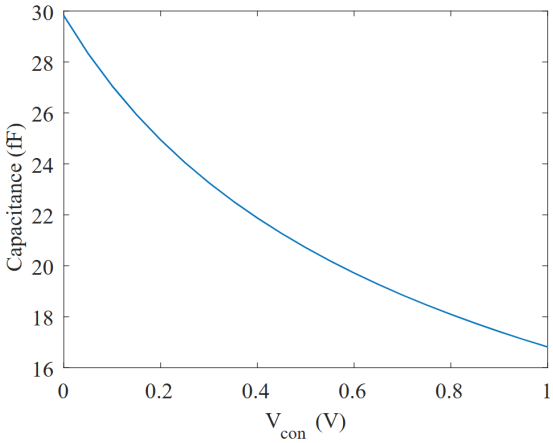

Figure 4.8: Simulation of the capacitance variation (C_{eff}) vs. V_{con}.

Combining Equations (4.1) and (4.6), and taking into account that $f = 1/T$, the following expression that correlates the frequency with respect to V_{con} is obtained:

$$f = \frac{\sqrt{K_1 V_{con} + K_2}}{D} \tag{4.7}$$

where D stands for

$$D = \frac{3V_{TH,n}}{I_{leak,M_5} - I_{leak,M_6}} \tag{4.8}$$

The expression given in Equation (4.7) can be linearized, with an R^2 factor greater than 0.99, as will be proved by experimental results in the following section, using a simple statistical regression model. The reason for this highly linear fit is the relatively small capacitance variation ratio K_1/K_2, which makes the square root present in Equation (4.7) almost flat in any available range of V_{con}. A graph showing how the linear regression fit evolves as a function of this ratio is shown in Fig. 4.9. The lower K_1/K_2, the more linear the frequency response becomes with respect to the input voltage. However, there is a trade-off concerning the VCO gain, since a K_1/K_2 ratio of 0 would result in an oscillator that no longer had the ability to change its frequency, so the higher the capacitance variation ratio the higher the VCO gain. For this reason, we conducted a study to discuss the different transistors that could be used as capacitors. The most relevant parameters discussed for the selection are summarized in Table 4.1, namely, the K_1/K_2 ratio, the area and the linearity. Since for our application a linear fit greater than 0.99 (R^2) is valid, all of them provide a sufficiently linear response. Next, we focused on getting the largest possible capacitance variation ratio, which directly translates into a larger VCO gain, where LVT and core PMOS stand out with similar values, but for a small improvement in K_1/K_2 the LVT transistor takes up more than 40% more area than the core transistor. Consequently, the core PMOS was chosen for this design.

Table 4.1: PMOS transistor types comparison for their use in the VCO.

PMOS type	K_1/K_2	cap. density (fF/μm^2)	linear fit (R^2)
Core	2.146	2.12	0.994
I/O	1.057	2.275	0.998
LVT	2.313	1.475	0.994
HVT	1.681	3.55	0.996

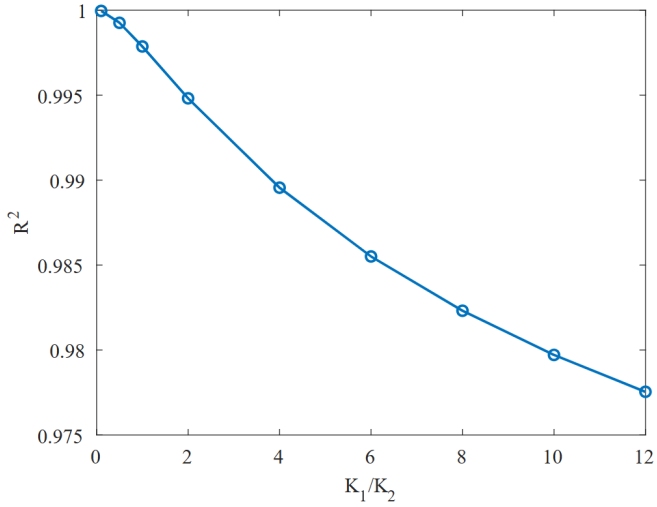

Figure 4.9: R^2 factor vs. K_1/K_2.

4.6 LED Driver

The output of the proposed VCO is used within the *SynCell* to blink a μLED with a frequency proportional to the sensor voltage. The system requires an LED driver to convert the VCO voltage pulses into controlled current pulses that energize the LED. The schematic of the LED driver, shown in Fig. 4.10, consists of a 80 nA current sink, biased from the PMU, and a switch that either cuts off or lets the current through to make the LED blink at the VCO frequency. Both parts are implemented using I/O transistors so the driver can handle the relatively high voltage of the solar cells. When the VCO output is low, the switch is turned off, so no current flows and the whole voltage generated by the solar cells drops at the driver. On the other hand, when the VCO output is high, the current imposed by the current sink flows through the LED, causing it to emit light. In this case, at least 2.45 V would drop at the LED, while the rest would do so at the driver. The driver was designed to require a minimum of 100 mV, which ensures that, in most cases, enough headroom is left for the LED to be turned on.

Driving the LED in this manner allows us to reach a high enough voltage to turn it on without using a charge pump, which would increase the silicon die area significantly [6]. Instead, two solar cells are required, which leads to either a double-size energy harvester or a halved power budget. In our case, we chose to sacrifice the available power to reach the targeted cell-size scale.

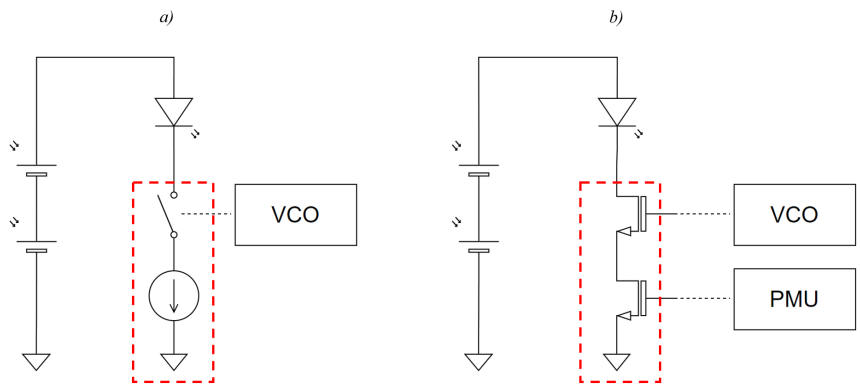

Figure 4.10: a) Conceptual representation of the LED driver, b) Schematic of the LED driver.

4.7 Results

Fig. 4.11 shows the fabricated CMOS silicon part of the MIT microsystem for which the oscillator was designed. The green rectangular shapes in the zoomed area are the probe pads that will later be used as the connection points for the rest of the microsystem through heterogeneous integration. The VCO, represented with a yellow box in Fig. 4.11, occupies an area of 592 μm^2.

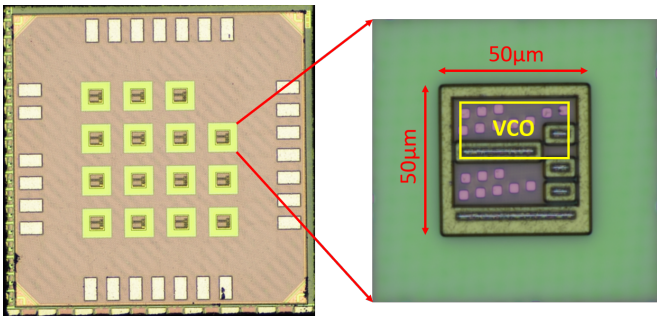

Figure 4.11: Fabricated chip with the proposed VCO highlighted.

The layout of the VCO is shown in Fig. 4.12. The six capacitors required for this VCO were implemented using PMOS transistors with a 700 nm/20 μm W/L ratio. They are placed on the right side of the layout. The capacitors with a fixed value are located at the top in the same n-well while the variable capacitors are at the bottom, each one in a separate n-well. On the left are the NMOS and PMOS parts of the delay elements isolated with their respective guard rings to prevent the circuit from latch-up. Transistors M_{a-d} and $M_{1,2,5,6}$ have 200 nm/500 nm W/L ratio and the rest remain at a minimum size of 200 nm/60 nm ratio.

The simulation and measurements of the proposed VCO are discussed in the following subsections.

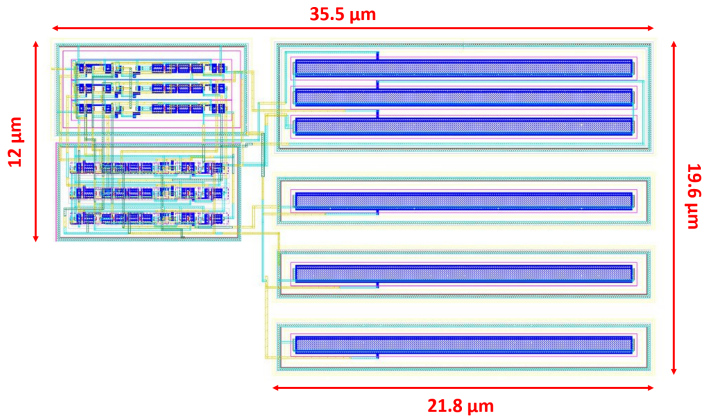

Figure 4.12: Layout of the fabricated VCO.

4.7.1 Simulation Results

The VCO circuit was first simulated using Virtuoso IC 6.1.7.715 from Cadence software.

The VCO response to the control voltage, V_{con}, at both nominal voltage (1 V) and minimum voltage (0.3 V), is shown in Fig. 4.13. At nominal voltage, the VCO outputs a frequency that ranges from 132.4 Hz to 167 Hz, which represents a gain of ∼26%/V. At the same time, the VCO response holds good linearity, as it can be approximated by a straight line with a coefficient of determination (R^2) of 0.994.

On the other hand, when the circuit is powered at the minimum supply voltage, $V_{dd} = 0.3$ V and the control voltage is swept from 0 V to V_{dd}, the absolute change in the capacitance is reduced but the linearity is further improved. Although the maximum frequency change also decreases (2.2 Hz to 2.46 Hz), the relative frequency shift per volt increases, due to the higher slope of the capacitance variation at lower bias voltages. As a result, when operating at 0.3 V we obtained a VCO gain of 36%/V and a coefficient of determination of 0.997. In both cases, the frequency change produced by this VCO is sufficient to perform an accurate voltage-to-frequency conversion.

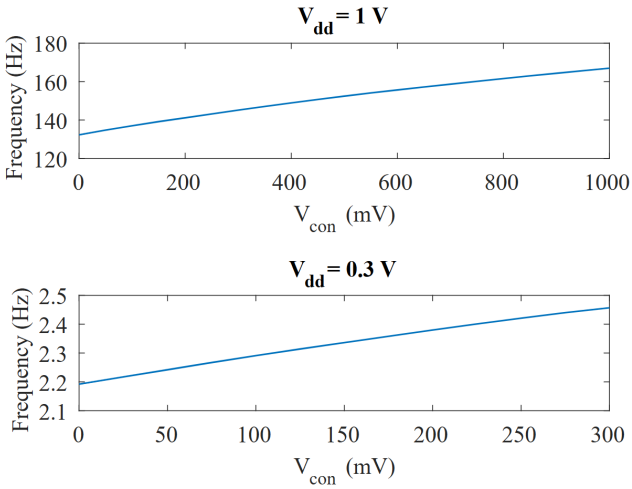

Figure 4.13: Simulation of the frequency variation vs. V_{con} at $V_{dd} = 1$ V (top) and $V_{dd} = 0.3$ V.

Although a factor of about 1.8 was observed between the corresponding minimum and maximum capacitance values (16.5–30 fF) for the maximum and minimum V_{con} possible voltages (as shown in Fig. 4.8), for the RC time constant and, hence, the oscillation frequency experiments only a ∼26% change was observed, as shown in Fig. 4.13.

If double-well technology were available, both capacitors C_1 and C_2 could be tuned simultaneously by using an NMOS transistor in its own p-well, with its source and drain tied to V_{dd}, acting as the capacitor C_1. As a result, the same principle could be used to achieve a highly linear response with a slope of ∼2 if a higher gain was required. A theoretical model simulation, including the four available transistor options, of how the frequency changes if both capacitors could be tuned simultaneously is shown in Fig. 4.14.

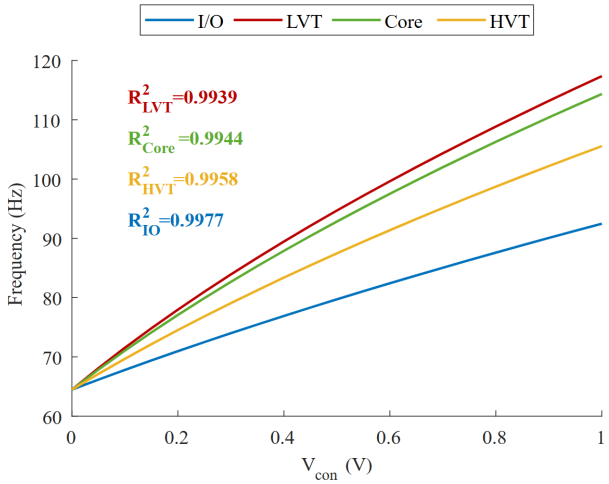

Figure 4.14: Simulation of frequency variation vs V_{con} for core, I/O, LVT and HVT transistors if both capacitances are tuned at the same time.

In terms of power consumption, the VCO consumes only about 200 pW at the nominal supply voltage and around 4 pW at 0.3V and remains almost invariant to the control voltage (200 pW

@ 0 V and 210 pW @ 1 V). It is important to note that the peak currents have been reduced to a maximum of 11 nA at the nominal supply voltage, which is low enough to be supplied by most harvesters without any significant impact.

Both the voltage (V_{dd}) and temperature responses are shown in Fig. 4.15. Although this VCO is intended for use in temperature-stable environments, the responses shown in Fig. 4.15 are quite convenient if a temperature-invariant oscillator is required. If the temperature range over which the oscillator is going to operate is not too wide, the frequency variations due to temperature and supply voltage can be considered linear, making it possible to neglect the temperature effect on the frequency if the oscillator's supply voltage comes from a specified CTAT generator that matches the observed slope. This has not yet been implemented, because in vitro operation is being considered, although it is planned for future versions of the MIT microsystem.

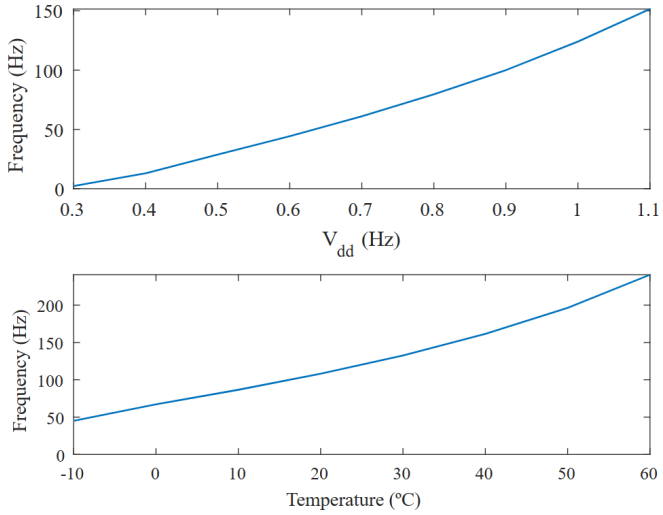

Figure 4.15: Simulation of frequency variation vs. V_{dd} and temperature at $V_{con} = 0$ V.

The Monte Carlo was also simulated for the nominal frequency of the VCO, shown in Fig. 4.16, giving a mean value of 124.075 Hz @ 0V and a standard deviation of 18.99 Hz ($\sigma/\mu = 15.3\%$). The corner analysis was also simulated, and the results are collected in Table 4.2.

Table 4.2: Corner Analysis simulation results at $V_{dd} = 1$ V.

Corner	Tuning range (Hz)	Gain (%/V)	R^2
TT	132.4 - 167.0	26.2	0.994
FF	212.0 - 270,1	27.4	0.988
FS	91.6 - 109.8	19.9	0.990
SS	85.6 - 120.6	40.1	0.995
SF	129.4 - 179.6	38.5	0.990

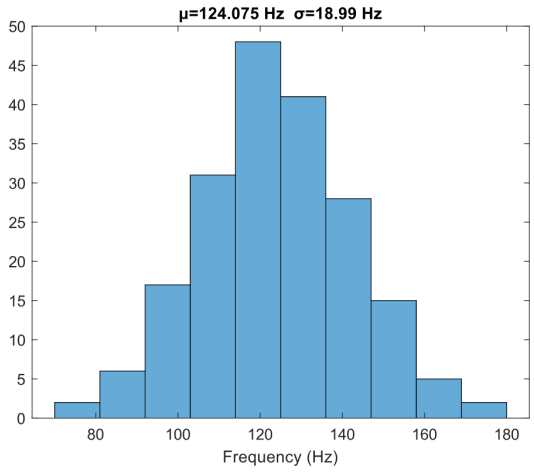

Figure 4.16: Monte Carlo frequency simulation.

4.7.2 Measurement Results

The measurement setup is shown in Fig. 4.17. The VCO drives a transistor acting as a switch (M_{sw}), which allows the current imposed by the current source, I_{DC}, to flow or not. These current pulses are converted into voltage pulses by a trans-impedance amplifier. The amplitude of the current pulses follows the relationship $I_{DC} \times R_1$, and their frequency is that of the oscillator, avoiding any possible load effect in the measurement. As also shown in Fig. 4.17, the oscillator as well as the switching device (M_{sw}) and the current source I_{DC} are on-chip elements, while the trans-impedance amplifier is placed off-chip, and it does not share the same power supply as the previously mentioned parts.

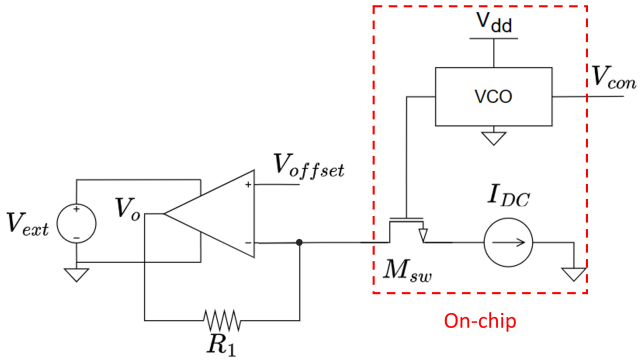

Figure 4.17: Measurement setup for the VCO.

A total of five samples from different dice were measured. Fig. 4.18 shows the transient measurement of one sample's output at minimum and maximum V_{con} values. Table 4.3 collects the frequency-related data from each sample. A factor of ∼2–3x can be noticed between the simulated and the measured frequency. This also happened, to a similar extent, in [72].

In our case, there are a few possible reasons for this simulation-to-measurement delta. First, the models used to estimate the leakage currents may not be precise enough to determine the

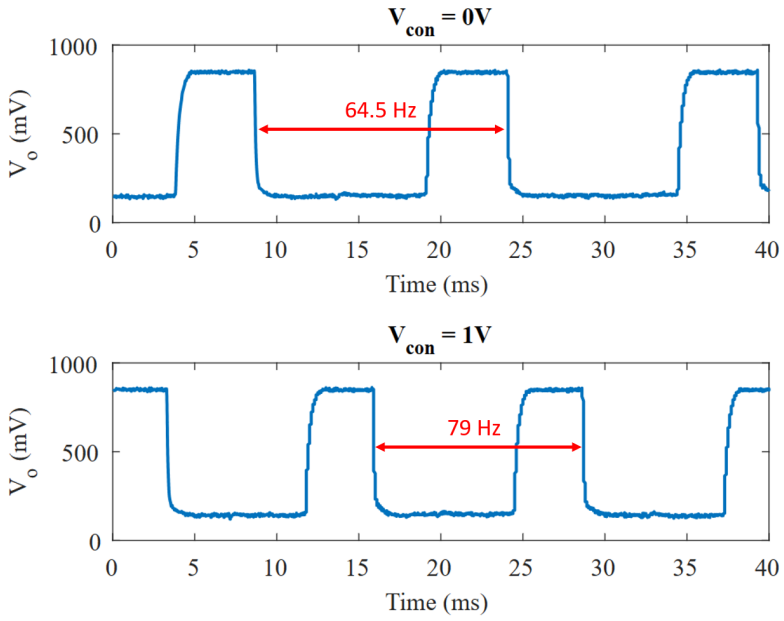

Figure 4.18: Transient measurements of the VCO at $V_{con} = 0$ V and $V_{con} = 1$ V.

Table 4.3: Collected data from the five measured samples at $V_{dd} = 1$ V.

VCO	Tuning range (Hz)	Gain (%/V)	R^2	linear approximation
1	46.9 - 58.2	24.1	0.997	$f = 11.7V_{con} + 46.98$
2	44.8 - 53.7	19.9	0.993	$f = 9.7V_{con} + 44.57$
3	64.5 - 79.5	23.3	0.997	$f = 15.7V_{con} + 64.19$
4	34.7 - 40.3	16.1	0.993	$f = 5.9V_{con} + 34.59$
5	28.3 - 34.0	20.1	0.994	$f = 5.9V_{con} + 28.35$

output frequency accurately. Another possible source of variation could be an unexpected parasitic capacitance. Since the capacitors used in the circuit are very low (as low as 16 fF, in the case of $V_{con} = 1$ V) any parasitic capacitance in a sensitive node, not accounted for in the post-layout simulation, can alter the output frequency. Finally, any deviation of the supply voltage from the simulation value will introduce a certain frequency delta between the measurements and the simulations. The measured VCOs are powered by a low-dropout regulator (LDO) designed to provide a 1 V output. However, process variations cause each LDO to report a different output voltage, with 0.967 V and 1.110 V being the minimum and maximum values. To account for this effect, the frequency of each sample was normalized. To perform the normalization, each LDO output was measured, and then a correction factor was applied to the measured frequencies of each sample, based on how the frequency changes with respect to the power supply. Fig. 4.19 shows the raw VCO measurements, and Fig. 4.20 shows the normalized responses. While there is a significant dispersion in Fig. 4.19, presenting a σ/μ of 13.69%, after the normalization it is largely reduced to 4.65%. This is a low value taking into account the nature of the currents that we use in this circuit. To put it into perspective, the other VCO found that uses the thyristor delay element [72] has a 30% dispersion in the

frequency between samples.

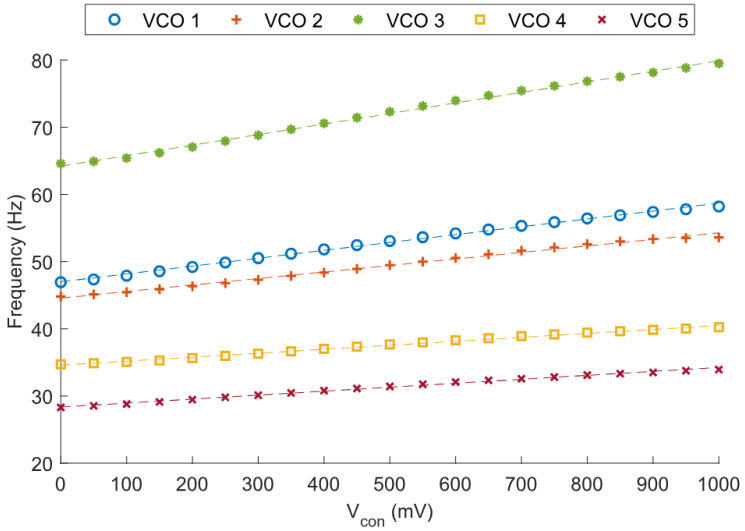

Figure 4.19: Frequency variation vs V_{con} through C-tuning for $V_{dd} = 1$ V.

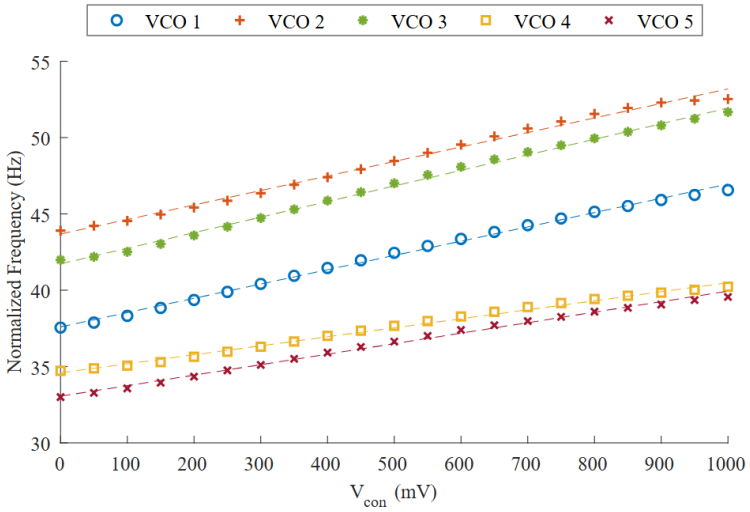

Figure 4.20: Normalized frequency variation vs V_{con} through C-tuning for $V_{dd} = 1$ V.

The power supply voltage disparity error can be minimized with the aforementioned normalization. However, due to the process variation effect, not only does the frequency at $V_{con} = 0$ V shift from one sample to another, but they also differ in their respective gains. Consequently, a 2-point calibration is required, to find out the conversion ratio between the frequency produced by the VCO and its input voltage. A straight line can be extrapolated from the two measured points and then used to model the VCO's behavior. Because of the linear nature of the VCO, the maximum relative error committed should be small. As long as the environmental conditions, such as the temperature, remain stable, the oscillation frequency should remain invariant, so the calibration only needs to be performed once. The resolution of the digitization will eventually depend on how many pulses the counter can

count in a full period, which can easily be large, due to the very slow time base generated by the oscillator.

Linearity-wise, the average coefficient of determination (R^2) measured is 0.995, with a standard deviation of 0.002 in such coefficients ($\mu/\sigma = 0.2\%$). This slight improvement of linearity with respect to the simulations ($R^2 = 0.994$) is directly correlated to the slight VCO gain reduction found in the measurements. The measured frequency variation shows a change of about 22 %/V in the control voltage when working at the nominal supply (1 V), and of about 27 %/V in simulations. This difference is mainly attributable to process variation.

To further examine the linearity of this oscillator, Fig. 4.21 shows the derivative of the measured frequency for each measured control voltage. Ideally, a straight line would give a flat derivative. However, in our case, some distortion occurs at control voltages close to the ground or V_{dd}, while the VCO presents a higher linearity at more centered voltages. Although the control voltage can be swept from GND to V_{dd}, we recommend restricting its range from $\sim$0.1 V_{dd} to $\sim$0.9 V_{dd} for a more precise linear approximation, which results in less error committed in the voltage-to-frequency conversion.

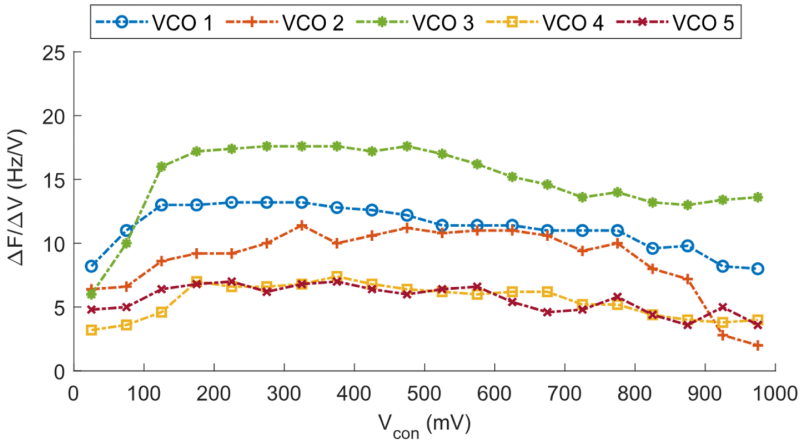

Figure 4.21: $\Delta F/\Delta V$ vs V_{con} for $V_{dd} = 1$ V.

A common source of uncertainty for every oscillator is the jitter, measured in the time domain, or the phase noise if we consider the frequency domain. In our case, we measured the average period of one sample to be 15.4 ms at 0 V, with a standard deviation of 0.19 ms, resulting in a 1.2% relative error. The measured jitter is shown in Fig. 4.22. To minimize the impact of jitter in our application, the system's reader records the oscillations for a sufficient period of time (e.g., 2 s) and uses the average of the n recorded periods for voltage-to-time conversion. This approach divides the error by the number of periods counted, leading to a considerable improvement in the relative error. At the cost of slowing down the measurement process, which is not a concern for our application, it makes a reasonable conversion possible.

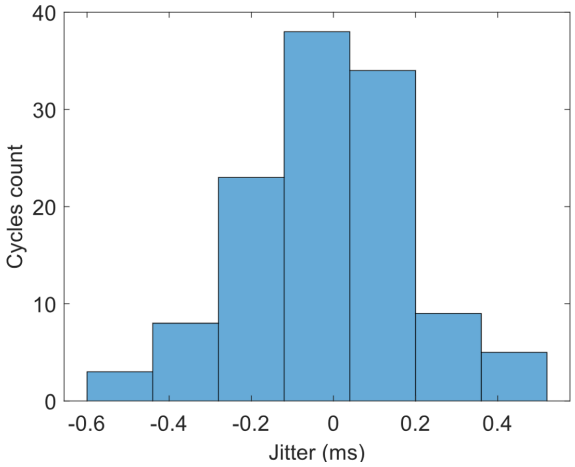

Figure 4.22: Jitter measurement of the proposed VCO at $V_{dd} = 1$ V and $V_{con} = 0$ V.

4.8 Results Comparison and Discussion

In the cell-size autonomous microsystems context area and power are the two major constraints. When the digitization of an analog voltage is needed, traditional ADCs are, most of the times, not a valid option since they are normally far from meeting these requirements.

A convenient solution to this constrained scenario is using time-domain digitization that can save substantial area and power at the expense of accuracy and speed compared to more conventional analog-to-digital converters. The resolution of the time-domain digitization is highly dependent on the linearity of the conversion, hence, a linear behavior is always desirable. On the other hand, speed is not a concern when working with slow signals such as that of biomedical applications or sensors that have a slow time response like the MoS_2 sensor of the *SynCell*. Consequently, as long as the minimum accuracy required by the application is met, the time-domain digitization technique is a suitable approach in autonomous microsystems.

In this chapter, an ultra-low-area-power-and-frequency VCO has been presented as a time-domain digitization method. The proposed VCO is based on using a sub-threshold leakage current-type delay element and provides a quasi-linear response while allowing rail-to-rail input range swing. It minimizes leakage and limits high peak currents which makes it a suitable fit alongside weak energy power sources. The oscillator occupies 592 μm^2, operates, on average, in the frequency range of 43.7 Hz to 53.0 Hz and consumes a maximum average power of 210 pW at nominal supply voltage. The proposed circuit shows an excellent frequency-area-power compromise not only for MIT *SynCells* but also for any smart dust application where the available space is very limited and the temperature remains stable.

A comparison with the existing literature has been made in Table 4.4. It is important to note that the data provided for this design, such as the frequency, are the average of all the measurements carried out, instead of specific sample results.

The VCOs that we found in the literature are centered in frequency ranges going from MHz to GHz, so they consume much more power, rendering them invalid for our microsystem and, thus, comparing this work to them may be meaningless. On the other hand, we found several

oscillators (without voltage control) that aim at similar area, power and frequency constraints as the one proposed here. Apart from these limitations, all of these designs have in common that they are intended to be used in temperature-stable environments, since designing a temperature-compensated structure would involve a significant area penalty, as in [85, 86, 87, 88].

The only VCO reported in Table 4.4 is $[72]_a$, since it commits to ultra-low frequency, area, and power, which is the reason why it is necessary to point out some important differences between our work and $[72]_a$ not collected in Table 4.4. First, our VCO allows a linear frequency control, which is the best approach for time-domain digitization, while the VCO reported in $[72]_a$ presents an exponential frequency response. The input range in $[72]_a$ is very limited, in some cases as constrained as just 50 mV. Our VCO, on the other hand, provides the full input voltage swing while maintaining the linearity. The current drawn by the VCO in $[72]_a$ exhibits an undesirable exponential behavior as a function of the input voltage, deviating from the ultra-low power paradigm, but in our proposal it remains almost invariant at a very low value. Although the proposed VCO uses a smaller technology node, which should have higher process variability, the standard deviation over the mean (σ/μ) of this design is half that of $[72]_a$, meaning that this design is less sensitive to process variations. Since the area of the VCO in $[72]_a$ was not reported and its power consumption is taken from the given graphs, where it is not very clear how much power it requires, their well-documented only oscillator version $[72]_b$ was also included in the comparison.

Table 4.4: Comparison of Results Against Previous Works.

Reference	**This work**	$[72]_a$	$[72]_b$	[83]	[84]	[81]	[82]	[96]
Oscillator principle	subth. leakage	subth. leakage	subth. leakage	subth. leakage	subth. leakage	gate leakage	gate leakage	digital with DLS
Process (nm)	65	180	180	250	350	130	55	180
V_{dd} (V)	0.3-1.2	0.2-1.8	0.2-1.8	2.5	3.3	0.6	0.29	0.4
Freq.† (Hz)	43.7-53.0	10-600e3	20	8.9	0.0308	0.09	-	-
Freq.‡ (Hz)	2.2-2.46	-	20	-	-	-	0.64*	4
Power (pW)	$4^{\ddagger}$-$210^{\dagger}$	7e3-350e6	$3^{\ddagger}$-$230^{\dagger}$	5.7e3	1.98e3	2e3	4.5	3.32
Area (μm^2)	592	-	630	-	25000	480	28	1600
Freq. control	yes	yes	no	no	no	no	no	no
Linear control	yes	no	no	no	no	no	no	no

* Frequency and duty cycle unstable in time. Max Freq. 2.36 Hz. Min Freq. 0.16 Hz.
† at nominal V_{dd}.
‡ at minimum V_{dd}.

Chapter 5

Global Verification of the CMOS Silicon Controller

Although the complete *Syncell* microsystem has yet to be assembled, its electrical behavior has been verified through simulations. In addition, the CMOS *Si* chip fabricated for the *Syncell* has been measured and shown to function correctly.

In this chapter, we will present the Spice models created for all the elements of the *Syncell*, which were necessary to perform an accurate simulation of the entire microsystem. After that, the simulation and measurement results will be presented.

5.1 Simulation Models

The LED and the solar cells were modeled to replicate the electrical behavior of the intended microsystem in the Spice simulations. Both models were built from the measurements carried out over the test versions of the LED and the solar cell fabricated at MIT facilities. Their simulation Spice models are described below.

5.1.1 LED

The LED was modeled with the circuit of Fig. 5.1 using the turn-on voltage, the I-V characteristic and the capacitance measured at MIT.

As previously anticipated, the LED requires a turn-on voltage of 2.45 V, which is modeled with a DC source (V_d) that causes the mentioned voltage drop.

The minimum current measured to emit visible light was 50 nA. We decided to drive the LED with 80 nA to have some headroom to account for the possible process variations. Further current increment would have meant a costly waste of the limited power resources. At the intended operating point, the measured LED presented a dynamic small signal resistance of 140 kΩ, which was included in the model as R_d.

Finally, the junction capacitance of the LED was also measured (at 50 kHz) giving around

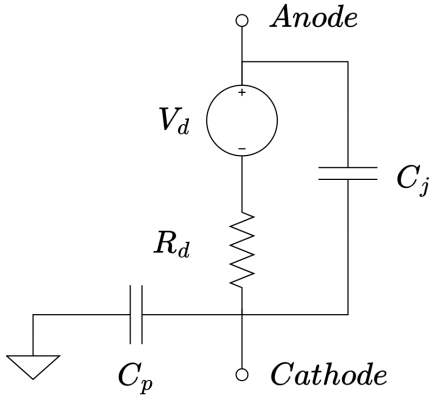

Figure 5.1: LED model.

250 fF. The custom pads used for the interconnection of the LED with the *Si*-chip were estimated to provide, according to their size and in comparison to the well-documented library pads, 50 fF parasitic capacitance. Both capacitances are contemplated in the model as C_j and C_p respectively.

5.1.2 Solar Cell

The solar cell model used in this thesis accounts for the power losses that take place in such component to have a more realistic behavior.

To fully understand the model we describe first the loss mechanisms of the solar cell followed by its Spice model.

Loss Mechanisms

The conversion efficiency of solar cells is typically low, around 15-20%. This is largely due to a multitude of loss mechanisms. Among these, the heat generated in the process stands out as one of the main sources of inefficiency and it cannot be avoided by any means.

To a similar extent, there will always be a certain loss due to the uncollected EHPs that recombine before reaching the other side. This effect becomes very significant in more defective crystalline structures with irregularities that can trap the minority charge carriers long enough to recombine.

Ohmic loss is another well-known effect present in all microelectronic devices. Metallic contacts to the solar cell introduce a resistance in series that, once the current is flowing to the load, takes away a fraction of the generated output power, worsening the efficiency.

When it comes to its fabrication process, it is very important to minimize as much as possible the metal structures built around the given solar cell employed to deliver the generated electric current to the rest of the system. All these metal wires partially block the incoming light, thus reducing the effective area of the actual solar cell due to shading.

Last, there is the forward current loss. When light energizes the solar cell, the concentration

of majority charge carriers increases in both diffusions as a consequence of minority charge carriers moving to the opposite region (I_{ph}). This develops a measurable voltage across the cell (V_{pv}) opposite to the built-in potential. As the V_{pv} voltage keeps rising, the cell starts to forward bias, causing a flow of majority charge carriers (I_{fw}). This forward current (I_{fw}) at the PN junction opposes the photogenerated current (I_{ph}) and constitutes one of the main loss mechanisms of a solar cell. This forward current, which increases with V_{pv}, is the reason why the solar cell cannot exceed the open-circuit voltage V_{oc} across its terminals. Hence, this effect is responsible for the elbow shape in the I-V characteristic of the solar cell.

Spice Model

In its simplest form, without considering any losses, a solar cell behaves more as a current source than a voltage source. Ideally, from 0 V up to the elbow shape of the IV transfer function, a little bit before the V_{oc} voltage, the supplied current remains almost the same regardless of the load. Hence, the model starts with a current source, I_{ph}, whose value must match the scaled *short-circuit current* of the real solar cell ($I_{sc} = 5.5\mu A, I_{ph} = 1.375\mu A$).

To make the model further resemble reality, it is necessary to incorporate the non-idealities and loss mechanisms previously mentioned.

The forward current loss is included in our model through a diode in parallel to the current source. Its voltage drop when drawing I_{ph} needs to be equal to the measured open-circuit voltage. Since the silicon devices available in the 65nm CMOS technology library have a much lower threshold voltage than a GaN diode, we have placed four *Si* diodes in series to achieve the desired voltage drop.

On the other hand, metallic contacts to the solar cell introduce a resistance in series R_s that, once the current is flowing to the load, takes away a fraction of the generated output power, worsening the efficiency.

The irregularities in the crystalline structure of the PN junction, which can trap EHP, can be modeled by a parallel resistance or shunt resistance (R_p). Normally the slope of the transfer characteristic near the short-circuit point is set by fine-tuning this parameter.

The final Spice model can be observed in Fig. 5.2 with the values of the parameters specified in table 5.1. The disparity in the nature between the *Si* model and the actual GaN solar cell imposes some inaccuracies near the elbow shape. We attempted to address this by adjusting the values of R_s and R_p to minimize the error at the elbow. However, this adjustment sacrifices some accuracy near the short-circuit and open-circuit points. To determine its accuracy, the fabricated GaN solar cell was analyzed using this particular model. In Fig. 5.3, we compare the model's behavior to the downscaled measured data of the fabricated solar cell. The simulation of the electric model presents slight inaccuracies, however, we consider it valid to carry out a rough first prediction of the operation point of the harvester.

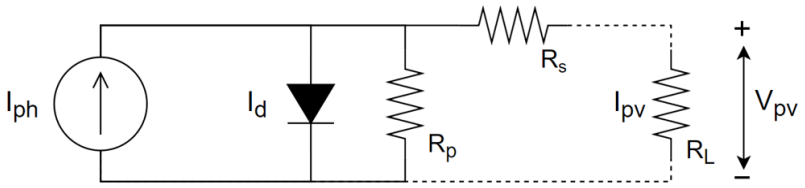

Figure 5.2: Solar Cell Model.

Table 5.1: Solar Cell Model Parameters.

Parameter	Value
I_{ph}	1375 nA
R_s	1000 Ω
R_p	10 $M\Omega$
$P-type$ diode width	400 nm
$P-type$ diode length	310 nm

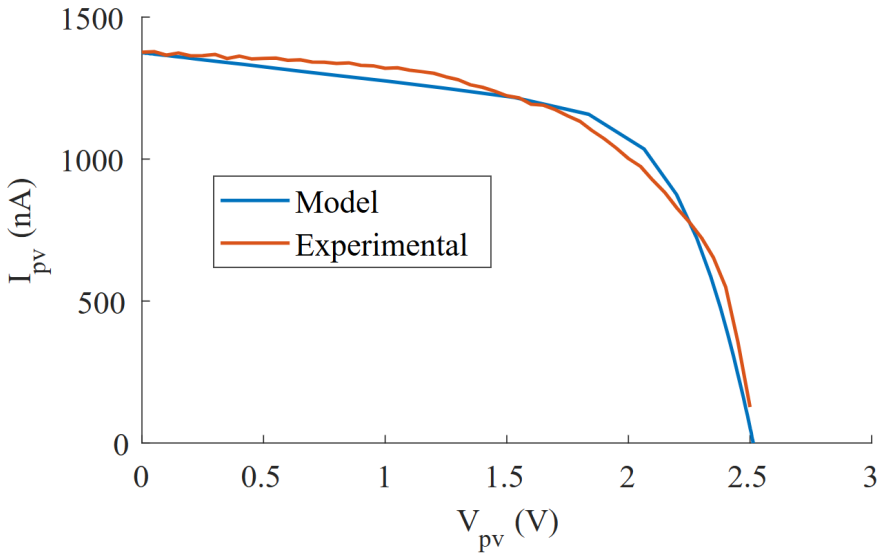

Figure 5.3: Silicon solar cell model simulation vs. the downscaled GaN experimental data.

5.2 Results

Fig 5.4 and Fig 5.5 show the transient electrical simulation of the *SynCell* using the PMU I and PMU II respectively.

The fastest the putrescine sensor can complete a resistance change after being chemically exposed is a few minutes. However, in our simulations, we have forced a full range change within 100 μs to reduce the simulation time. Although the system responds well under these simulation conditions, we expect it to have a smoother functioning with slower transitions.

As explained in chapter 2, the sensor is composed of two MoS_2 devices one acting as a variable resistor (R_{var}) and the other as a reference resistor (R_{ref}). They are set in a voltage divider configuration (see Fig 2.8) and the total resistance provided by the sensor (R_{sens}) is calculated as $R_{ref} + R_{var}$. In the simulation, we have used $R_{ref} = 900\ k\Omega$ and we have swept R_{var} from 100 $k\Omega$ to 10 $M\Omega$.

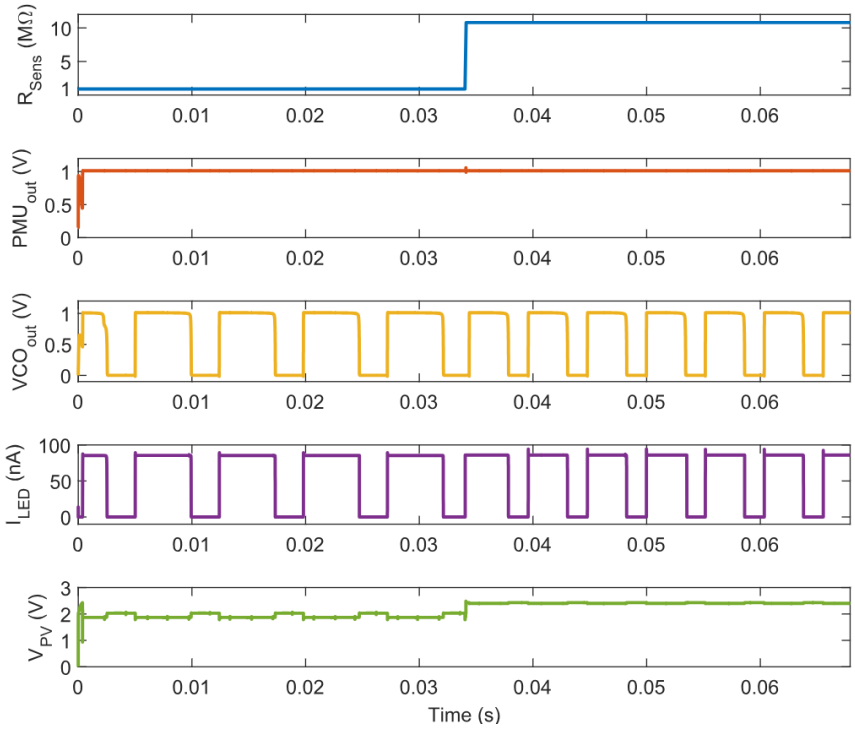

Figure 5.4: Simulation of the *Syncell* behavior with PMU I.

According to the simulations on Fig. 5.4 and Fig. 5.5, the *Syncell* boots up without any issues; however, the VCO frequency does not reach the correct operating frequency until its second cycle.

The voltage provided by the solar cell to the silicon chip (V_{PV}) fluctuates with changes in the current drawn. This occurs either when the LED is turned on and off or when the sensor alters its resistance. However, in both simulations, the PMU effectively mitigates these fluctuations, ensuring that the VCO frequency remains unaffected by the solar cell voltage.

The change in the sensor resistance causes the VCO to modify its frequency. The LED current

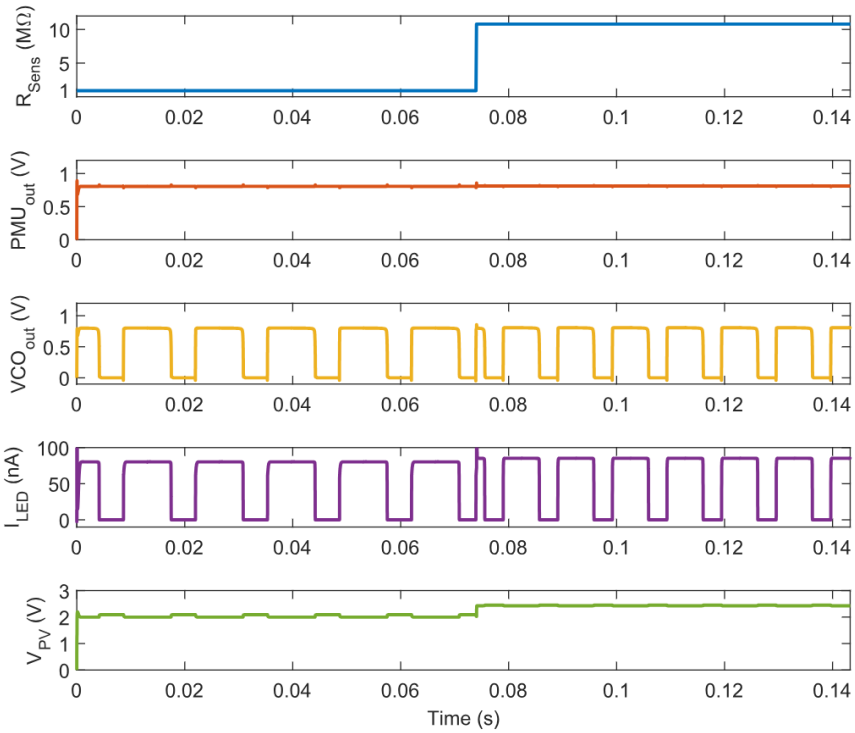

Figure 5.5: Simulation of the *Syncell* behavior with PMU II.

(I_{LED}) is switched on and off accordingly. However, the LED driver maintains the maximum I_{LED} current constant to prevent the LED from drawing unnecessary power.

Finally, the operation of the fabricated CMOS *Si* controller designed for the *Syncell* is shown in Fig. 5.6. The system, which was only fabricated with PMU I, reaches the correct operation after several milliseconds.

The LED current has been measured at the output of the LED driver with a transimpedance amplifier, following the measurement setup of Fig. 4.17. The square signal voltage measured at the output of the transimpedance amplifier had an amplitude of 1.89 V when the value of R_1, on Fig. 4.17, was chosen to be 22 MΩ. This is equivalent to a current of 86 nA, which is close enough to the 80 nA expected from simulations.

Both the voltage reference and the LED current were measured through operational amplifiers. Consequently, their waveforms are shifted in time with the delay of the amplifiers.

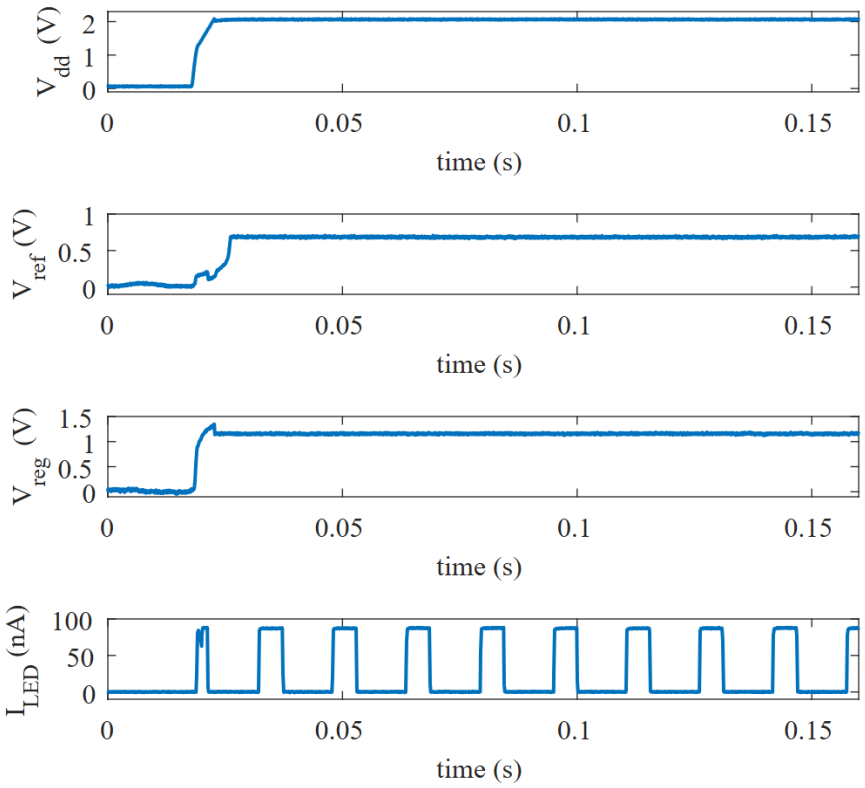

Figure 5.6: Transient measurement of the boot up of the CMOS *Si* controller designed for the *Syncell* at V_{sens} =0 V.

Chapter 6

Conclusions

Autonomous microsystems technology has evolved rapidly in recent years since the initial conception of the *smart dust* [97] in 2001, when it was proposed as a method for large-scale distributed sensing and computation. The miniaturization of sensors, actuators, and wireless communication systems has now reached a stage where these devices can be produced at a scale close to that of the size of biological cells. Cell-size autonomous microsystems can be deployed in environments where traditional sensors are either impractical or impossible to use. This leap into microscopic dimensions promises numerous benefits, especially in fields such as medicine, environmental science, or industrial monitoring.

For example, cell-size autonomous microsystems could be used to non-invasively monitor the condition of tissues, organs, or even individual cells. Unlike conventional imaging techniques, such as MRI or CT scans, these microsystems could provide real-time, localized data about cellular conditions with unprecedented precision. These capabilities are invaluable in the management of chronic diseases such as cancer or neurodegenerative disorders, where early detection is crucial for successful treatment.

Beyond biomedical applications, cell-size motes can be used to monitor equipment. These minuscule sensors could be deployed within machinery, at almost any place needed, to detect early signs of wear or failure, reducing the need for manual inspections and preventing costly breakdowns.

However, the miniaturization required to bring these electronic particles to the scale of cells, and thus unlock their transformative potential, comes with two major challenges:

- The primary limitation of cell-size microsystems is the extremely constrained space available. This causes a drastic reduction in functionality, which, in some cases such as in this thesis, forces a fully analog circuit design. Besides, microsystems with such a constrained area budget must tolerate higher process variability must be tolerated, since large transistor sizes or trimming techniques are unlikely to fit.
- Another severe limitation lies in the power supply for these microsystems. At such small scales, traditional battery systems are impractical. Therefore, energy-harvesting methods are required, but the amount of energy that can be collected at the cell-size

scale is remarkably small. This raises the difficulty of designing a microsystem that can work with such low power. To counteract the low power efficiency of energy harvesters when shrunk to the microscale, each building block in the system must consume the minimum amount of power that still ensures the proper operation of the system.

In particular, the second generation of the MIT *SynCells*, in which this thesis is involved, aimed from the beginning at an unprecedented area reduction to demonstrate sensing and wireless communication capabilities at the microscale.

SynCells are designed to harvest energy from the incident light through two solar cells. This is the most efficient harvesting approach when scaling down to the size of a biological cell. However, the generated power cannot be fed directly into the core of the system, but instead requires a PMU to provide regulation and withstand the fluctuations and instability of such a weak power source.

The severe constraints of power and area set up a complex design scenario that, in our case, required us to trade off certain performance aspects in the PMUs to achieve higher-priority objectives.

In our case, the PMU only required a voltage reference and a voltage regulator. A suitable way to reach the area target in PMUs is by optimizing their building blocks accordingly. The regulator's pass transistor is one of the bulkiest devices in typical LDOs designs. However, in this context, its size can be largely reduced to save area. This limits the maximum deliverable load current. However, the load current should be small for these microsystems and must be aligned with the capabilities of the energy harvester. If the transistor is too small, it can cause a higher dropout voltage, which decreases the overall power efficiency of the system.

At the same time, selecting a voltage reference topology implemented with a low number of transistors, combined with small-size devices, contributes to reaching the desired area reduction. This usually comes with the corresponding variability penalty.

On the other hand, load regulation and speed in the transient response may be sacrificed to reduce the quiescent consumption and meet the power requirements.

In this thesis, we have presented two PMUs designed for cell-size autonomous microsystems where the sacrifices mentioned above were made to achieve incredibly small designs with PMU I (section 3.7) and PMU II (section 3.8), occupying 520 μm^2 and 391 μm^2 respectively. Both designs would rank second and fourth among the smallest voltage references reported in the literature but, unlike the voltage references, the two proposed PMUs can deliver up to $\sim$30 μW of regulated power. To do so they require only 80 and 18.4 nA of quiescent current respectively, demonstrating the low power characteristic required.

In particular, the PMU I, designed for *in vitro* applications, focused on supply dependency by integrating a voltage reference with the best line regulation reported in the literature. Since its target scenario ensures a stable temperature, it did not include a temperature compensation. However, a method to achieve certain temperature stability in this voltage reference was also presented in this document.

On the other hand, the PMU II achieved a well-rounded design including a reasonable

temperature compensation that allows it to be used in temperature-changing environments. It also uses a novel structure where the voltage reference is embedded in the feedback loop of the regulator. The key benefit of this approach is that the voltage reference leverages the regulator's open-loop gain through the feedback loop, improving parameters like line regulation and power supply rejection. Simultaneously, the LDO regulator continues to provide regulated power to the core of the microsystem. This dual functionality results in a significant reduction in the PMU's die area, making the overall design more efficient.

Regarding the *SynCell* wireless communication, light pulses were chosen as the way to encode and transmit the sensor's information to the outside world. This task required the digitization of the sensor's output voltage. In a larger scale system, this would have been done through a traditional analog-to-digital converter. However, this approach cannot meet the area and power constraints of the cell-size scale. In this thesis, we developed a VCO (chapter 4), which serves as a lightweight time-domain digitization, that saves a large amount of area and power at the cost of sacrificing accuracy and speed compared to ADCs. It is based on subthreshold leakage currents to achieve ultra-low power operation. This approach allows the generation of large time constants while keeping the area within the required budget. The proposed VCO occupies only 592 μm^2 and reports an average power consumption of $\sim$200 pW with transient peaks controlled to only a few tens of nW. Its extremely low average and peak power consumption makes it a highly suitable design to be used alongside weak energy harvesters. Furthermore, it includes a quasi-linear control of the frequency, through bulk-biasing of the PMOS transistors used as capacitors, which eases the conversion resulting in higher accuracy.

All the building blocks of the *SynCell*, including the CMOS circuitry described in this thesis, still need the heterogeneous integration to be assembled. This technology is probably the least-matured among those required in the development of autonomous microsystems yet is one of the keys to making many ideas with breakthrough potential become a reality. Significant research is being conducted on this topic to solve the challenges that it brings to the table and thus make its use a feasible solution to be frequently resorted to.

6.1 Future Lines of Work

In this work, we have provided several CMOS building blocks that are suitable to the *SynCell* microsystem as well as to many other microsystems with similar contexts.

Although the proposed circuits reported good overall characteristics, some points of improvement have been identified to upgrade their performance:

1. To enable the use of the VCO in temperature-changing environments, a temperature-compensated design is required. This can be done through the use of CTAT voltage and current generators with a TC that opposes the current increment with temperature due to the respective threshold voltage reduction. We have already started to work on this line. However, developing a temperature compensation with leakage currents is not trivial and the results are left out of the scope of this thesis.

2. Applications with more stringent variability requirements may need a voltage reference less sensitive to process variations than the two presented in this work. Some published

works [56] achieve reduced variability by avoiding the use of different types of transistors. Instead, they work with bulk biasing to generate the desired threshold voltage difference and temperature compensation. This technique may require additional area and power, however, this trade-off could be worth exploring within the voltage references presented in this thesis.

On the other hand, from a more general point of view, we believe this thesis can help new researchers to keep adding layers to the autonomous microsystems research branch. For instance, The integration of cell-size sensing nodes, such as the *SynCell* and the proposed *Si* controller, within mobile mechanical microplatforms [98] can lead to unmatched advances in the biomedical world. Such tiny microrobots are normally powered by small energy harvesters and the generated power could be regulated by the proposed PMUs, which would be a highly suitable fit in terms of area and power consumption. On the other hand, a 2D material-based sensor alongside an ultralow-power and -area digitization block, such as the proposed VCO, can help a mobile microrobot like [98] move in the direction of the gradient of a certain chemical component concentration. All these features together can result in a microparticle that could potentially autonomously detect pathogens within the human body and carry out localized drug delivery [99, 100] to exterminate them. Similarly, the same concept could be applied to smart farming for plague control.

The integration of CMOS building blocks within micro-electromechanical systems (MEMS) is definitively one of the fields on which future research should focus on, as it could lead to immense advances. We hope that this thesis will inspire other researchers to continue contributing to the development of cell-size autonomous microsystems, serving as a gateway to numerous breakthroughs.

Bibliography

[1] Brett Warneke et al. "Smart dust: Communicating with a cubic-millimeter computer". In: *Computer* 34.1 (2001), pp. 44–51.

[2] Vikram Iyer et al. "Wind dispersal of battery-free wireless devices". In: *Nature* 603.7901 (2022), pp. 427–433.

[3] Mitsuo Usami. "An ultra-small rfid chip:/spl mu/-chip". In: *Proceedings of 2004 IEEE Asia-Pacific Conference on Advanced System Integrated Circuits*. IEEE. 2004, pp. 2–5.

[4] Xiao Wu et al. "A 0.04 mm 3 16nW wireless and batteryless sensor system with integrated Cortex-M0+ processor and optical communication for cellular temperature measurement". In: *2018 IEEE Symposium on VLSI Circuits*. IEEE. 2018, pp. 191–192.

[5] S O'Driscoll et al. "A 200μm$\times$ 200μm$\times$ 100μm, 63nW, 2.4 GHz injectable fully-monolithic wireless bio-sensing system". In: *2017 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*. IEEE. 2017, pp. 256–259.

[6] Sunwoo Lee et al. "A 250 μm $\times$ 57 μm Microscale Opto-electronically Transduced Electrodes (MOTEs) for Neural Recording". In: *IEEE Transactions on Biomedical Circuits and Systems* 12.6 (2018), pp. 1256–1266. DOI: 10.1109/TBCAS.2018.2876069.

[7] William Biederman et al. "A Fully-Integrated, Miniaturized (0.125 mm^2) 10.5 μW Wireless Neural Sensor". In: *IEEE Journal of Solid-State Circuits* 48.4 (2013), pp. 960–970.

[8] Yoonmyung Lee et al. "A Modular 1 mm^3 Die-Stacked Sensing Platform With Low Power I^{2}C Inter-Die Communication and Multi-Modal Energy Harvesting". In: *IEEE Journal of Solid-State Circuits* 48.1 (2012), pp. 229–243.

[9] Mohammad Hassan Ghaed et al. "Circuits for a Cubic-Millimeter Energy-Autonomous Wireless Intraocular Pressure Monitor". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 60.12 (2013), pp. 3152–3162. DOI: 10.1109/TCSI.2013.2265973.

[10] Marek Hempel et al. "SynCells: A 60$\times$ 60 μm2 electronic platform with remote actuation for sensing applications in constrained environments". In: *ACS nano* 15.5 (2021), pp. 8803–8812.

[11] Yang Li et al. "On-Chip Batteries for Dust-Sized Computers". In: *Advanced Energy Materials* 12.13 (2022), p. 2103641. DOI: https://doi.org/10.1002/aenm.202103641.

[12] Dominic A. Funke et al. "A 200 μm by 100 μm Smart Dust system with an average current consumption of 1.3 nA". In: *2016 IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2016, pp. 512–515. DOI: 10.1109/ICECS.2016.7841251.

[13] Reid R. Harrison et al. "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System". In: *IEEE Journal of Solid-State Circuits* 42.1 (2007), pp. 123–133. DOI: 10.1109/JSSC.2006.886567.

[14] Javier de Mena et al. "A Lightweight Analog RFID Frontend for Interfacing Sensors". In: *2024 XXXIX Conference on Design of Circuits and Integrated Systems (DCIS)*. Catania, Italy, 2024.

[15] Nesrine Jaziri et al. "A comprehensive review of Thermoelectric Generators: Technologies and common applications". In: *Energy Reports* 6 (2020), pp. 264–287. DOI: https://doi.org/10.1016/j.egyr.2019.12.011.

[16] Gerard Gadea et al. "Silicon-based nanostructures for integrated thermoelectric generators". In: *Journal of Physics D: Applied Physics* 51.42 (Aug. 2018), p. 423001. DOI: 10.1088/1361-6463/aad683.

[17] Rajiv Damodaran Prabha and Gabriel A. Rincón-Mora. "Drawing the Most Power From Low-Cost Single-Well 1-mm2 CMOS Photovoltaic Cells". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 64.1 (2017), pp. 46–50. DOI: 10.1109/TCSII.2016.2546907.

[18] Mohsen Safaei, Henry A Sodano, and Steven R Anton. "A review of energy harvesting using piezoelectric materials: state-of-the-art a decade later (2008–2018)". In: *Smart Materials and Structures* 28.11 (Oct. 2019), p. 113001. DOI: 10.1088/1361-665X/ab36e4.

[19] Yoonmyung Lee et al. "A Modular 1 mm^3 Die-Stacked Sensing Platform With Low Power I^2C Inter-Die Communication and Multi-Modal Energy Harvesting". In: *IEEE Journal of Solid-State Circuits* 48.1 (2013), pp. 229–243. DOI: 10.1109/JSSC.2012.2221233.

[20] Xianzong Xie et al. "Long-Term Bilayer Encapsulation Performance of Atomic Layer Deposited Al_2O_3 and Parylene C for Biomedical Implantable Devices". In: *IEEE Transactions on Biomedical Engineering* 60.10 (2013), pp. 2943–2951.

[21] John V. Faricelli. "Layout-dependent proximity effects in deep nanoscale CMOS". In: *IEEE Custom Integrated Circuits Conference 2010*. 2010, pp. 1–8. DOI: 10.1109/CICC.2010.5617407.

[22] Amirhasan Nourbakhsh et al. "Heterogeneous integration of 2D materials and devices on a Si platform". In: *Beyond-CMOS Technologies for Next Generation Computer Design* (2019), pp. 43–84.

[23] Javier de Mena Pacheco et al. "A Highly Linear Ultra-Low-Area-and-Power CMOS Voltage-Controlled Oscillator for Autonomous Microsystems". In: *Micromachines* 15.10 (2024), p. 1193.

[24] Javier de Mena Pacheco et al. "A Highly Power-and Area-Efficient PMU for Cell-Size Autonomous Microsystems". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2024), pp. 1–. DOI: 10.1109/TCSI.2024.3484537.

[25] Javier De Mena Pacheco and Marisa Lopez-Vallejo. "A 65nm Current and Voltage Reference with Improved Line Regulation for Implantable Biosensors". In: *2021 XXXVI Conference on Design of Circuits and Integrated Systems (DCIS)*. IEEE. 2021, pp. 1–5.

[26] Jing Cui et al. "What is the role of putrescine accumulated under potassium deficiency?" In: *Plant, Cell & Environment* 43.6 (2020), pp. 1331–1347.

[27] RA Edwards, RH Dainty, and CM Hibbard. "Putrescine and cadaverine formation in vacuum packed beef". In: *Journal of Applied Microbiology* 58.1 (1985), pp. 13–19.

[28] Xue-Feng Chen et al. "Engineering tunable biosensors for monitoring putrescine in Escherichia coli". In: *Biotechnology and bioengineering* 115.4 (2018), pp. 1014–1027.

[29] Ana Isabel González-Hernández et al. "Putrescine: A key metabolite involved in plant development, tolerance and resistance responses to stress". In: *International journal of molecular sciences* 23.6 (2022), p. 2971.

[30] M. K. Law and A. Bermak. "High-Voltage Generation With Stacked Photodiodes in Standard CMOS Process". In: *IEEE Electron Device Letters* 31.12 (2010), pp. 1425–1427. DOI: 10.1109/LED.2010.2075910.

[31] Roberto Pelliconi et al. "Power efficient charge pump in deep submicron standard CMOS technology". In: *Proceedings of the 27th European Solid-State Circuits Conference*. IEEE. 2001, pp. 73–76.

[32] Mir Mohammad Navidi and David W Graham. "A regulated charge pump for injecting floating-gate transistors". In: *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2017, pp. 1–4.

[33] Óscar Pereira-Rial et al. "Ultra-low-power low-input-voltage charge pump for micro-energy harvesting applications". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 70.1 (2022), pp. 154–165.

[34] Saurav Bandyopadhyay, Yogesh K Ramadass, and Anantha P Chandrakasan. "20μA to 100 mA DC-DC Converter With 2.8-4.2 V Battery Supply for Portable Applications in 45 nm CMOS". In: *IEEE Journal of Solid-State Circuits* 46.12 (2011), pp. 2807–2820.

[35] Joselyn Torres et al. "Low drop-out voltage regulators: Capacitor-less architecture comparison". In: *IEEE Circuits and Systems Magazine* 14.2 (2014), pp. 6–26.

[36] Asghar Bahramali. "Variability-aware design of front-end circuits for self-powered applications". PhD thesis. Telecomunicacion, 2021.

[37] Vishal Gupta, Gabriel A Rincón-Mora, and Prasun Raha. "Analysis and design of monolithic, high PSR, linear regulators for SoC applications". In: *IEEE International SOC Conference, 2004. Proceedings.* IEEE. 2004, pp. 311–315.

[38] Myungjun Kim and Seonghwan Cho. "A 0.0082-mm^2, 192-nW Single BJT Branch Bandgap Reference in 0.18-μm CMOS". In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 426–429.

[39] Yi-Wen Chen et al. "18.7 A 0.7 V, 2.35% 3σ-Accuracy Bandgap Reference in 12nm CMOS". In: *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE. 2019, pp. 306–307.

[40] Gajendranath Chowdary, Kalyan Kota, and Shouri Chatterjee. "A 1-nW 95-ppm/° C 260-mV Startup-Less Bandgap-Based Voltage Reference". In: *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2020, pp. 1–4.

[41] Youngwoo Ji et al. "A 9.3 nW all-in-one bandgap voltage and current reference circuit using leakage-based PTAT generation and DIBL characteristic". In: *2018 23rd Asia and South Pacific Design Automation Conference (ASP-DAC)*. IEEE. 2018, pp. 309–310.

[42] U Chi-Wa et al. "An 1 V Supply, 740 nW, 8.7 ppm/ºC Bandgap Voltage Reference With Segmented Curvature Compensation". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* (2023).

[43] Chutham Sawigun, Xiaolin Yang, and Carolina Mora Lopez. "Ultra-Low-Power Voltage References: Exploring picowatt-level design using CMOS and hybrid architectures". In: *IEEE Solid-State Circuits Magazine* 15.4 (2023), pp. 50–57.

[44] Arthur Campos De Oliveira et al. "A 0.12–0.4 V, versatile 3-transistor CMOS voltage reference for ultra-low power systems". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.11 (2018), pp. 3790–3799.

[45] Raymond Wang et al. "Threshold voltage variations with temperature in MOS transistors". In: *IEEE transactions on Electron Devices* 18.6 (1971), pp. 386–388.

[46] IM Filanovsky and Ahmed Allam. "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits". In: *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications* 48.7 (2001), pp. 876–884.

[47] Yu-Hsing Cheng. "Comparison of MOSFET threshold voltage extraction methods with temperature variation". In: *2019 IEEE 32nd International Conference on Microelectronic Test Structures (ICMTS)*. IEEE. 2019, pp. 126–131.

[48] Hui Wang and Patrick P Mercier. "A 420 fW self-regulated 3T voltage reference generator achieving 0.47%/V line regulation from 0.4-to-1.2 V". In: *ESSCIRC 2017-43rd IEEE European Solid State Circuits Conference*. IEEE. 2017, pp. 15–18.

[49] Mingoo Seok et al. "A portable 2-transistor picowatt temperature-compensated voltage reference operating at 0.5 V". In: *IEEE Journal of Solid-State Circuits* 47.10 (2012), pp. 2534–2545.

[50] Jing Wang, Xuan Sun, and Lin Cheng. "A picowatt CMOS voltage reference operating at 0.5-V power supply with process and temperature compensation for low-power IoT systems". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 70.4 (2022), pp. 1336–1340.

[51] Eric A Vittoz and Olivier Neyroud. "A low-voltage CMOS bandgap reference". In: *IEEE Journal of Solid-State Circuits* 14.3 (1979), pp. 573–579.

[52] Daniel C Guterman. *Simple NMOS voltage reference circuit*. US Patent 4,609,833. Sept. 1986.

[53] Mingoo Seok et al. "A Portable 2-Transistor Picowatt Temperature-Compensated Voltage Reference Operating at 0.5 V". In: *IEEE Journal of Solid-State Circuits* 47.10 (2012), pp. 2534–2545. DOI: 10.1109/JSSC.2012.2206683.

[54] Arthur Campos de Oliveira et al. "Picowatt, 0.45–0.6 V Self-Biased Subthreshold CMOS Voltage Reference". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 64.12 (2017), pp. 3036–3046. DOI: 10.1109/TCSI.2017.2754644.

[55] Arthur Campos de Oliveira et al. "A 0.12–0.4 V, Versatile 3-Transistor CMOS Voltage Reference for Ultra-Low Power Systems". In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 65.11 (2018), pp. 3790–3799. DOI: 10.1109/TCSI.2018.2859341.

[56] Qing Dong et al. "A 114-pW PMOS-only, trim-free voltage reference with 0.26% within-wafer inaccuracy for nW systems". In: *2016 IEEE Symposium on VLSI Circuits (VLSI-Circuits)*. IEEE. 2016, pp. 1–2.

[57] Chutham Sawigun et al. "A sub-nW scalable nMOS voltage reference with multi-loop regulation achieving 0.0126%/V line sensitivity". In: *2022 IEEE Asian Solid-State Circuits Conference (A-SSCC)*. IEEE. 2022, pp. 1–3.

[58] Xiaolin Yang et al. “An AC-Coupled 1st-Order Δ-ΔΣ Readout IC for Area-Efficient Neural Signal Acquisition”. In: *IEEE Journal of Solid-State Circuits* 58.4 (2023), pp. 949–960. DOI: 10.1109/JSSC.2023.3234612.

[59] Hayden Bialek, Matthew L Johnston, and Arun Natarajan. “A 6-transistor ultra-low power CMOS voltage reference with 0.02%/V line sensitivity”. In: *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE. 2020, pp. 1–4.

[60] Hongchang Qiao, Chenchang Zhan, and Yutian Chen. “A- 40° C to 140° C picowatt CMOS voltage reference with 0.25-V power supply”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.9 (2021), pp. 3118–3122.

[61] Inhee Lee, Dennis Sylvester, and David Blaauw. “A subthreshold voltage reference with scalable output voltage for low-power IoT systems”. In: *IEEE Journal of Solid-State Circuits* 52.5 (2017), pp. 1443–1449.

[62] Alessandro Parisi et al. “Nano-power CMOS voltage reference for RF-powered systems”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 65.10 (2018), pp. 1425–1429.

[63] Jarno Salomaa et al. “Power management system for ultra-low power energy harvesting applications”. In: *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2015, pp. 1086–1089.

[64] Shuo Li and Benton H Calhoun. “Sub-microamp energy harvesting and power management units for self-powered iot socs: Analog vs. digital implementations”. In: *2020 IEEE Custom Integrated Circuits Conference (CICC)*. IEEE. 2020, pp. 1–8.

[65] Puyang Zheng, Xiao Sha, and Milutin Stanaćević. “Analysis of the Sub-μ A Fully Integrated NMOS LDO for Backscattering System”. In: *2021 IEEE 34th International System-on-Chip Conference (SOCC)*. IEEE. 2021, pp. 52–56.

[66] Óscar Pereira-Rial, Paula López, and Juan M Carrillo. “0.6-V-V IN 7.0-nA-I Q 0.75-mA-I L CMOS Capacitor-Less LDO for Low-Voltage Micro-Energy-Harvested Supplies”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 69.2 (2021), pp. 599–608.

[67] Song Liu and R.J. Baker. “Process and temperature performance of a CMOS beta-multiplier voltage reference”. In: *1998 Midwest Symposium on Circuits and Systems (Cat. No. 98CB36268)*. 1998, pp. 33–36. DOI: 10.1109/MWSCAS.1998.759429.

[68] Sanghoon Lee and Edgar Sánchez-Sinencio. “Current Reference Circuits: A Tutorial”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.3 (2021), pp. 830–836. DOI: 10.1109/TCSII.2021.3049518.

[69] J. Georgiou and C. Toumazou. “A resistorless low current reference circuit for implantable devices”. In: *2002 IEEE International Symposium on Circuits and Systems. Proceedings (Cat. No.02CH37353)*. Vol. 3. 2002, pp. III–III. DOI: 10.1109/ISCAS.2002.1010193.

[70] Sanghoon Lee and Edgar Sánchez-Sinencio. “Current Reference Circuits: A Tutorial”. In: *IEEE Transactions on Circuits and Systems II: Express Briefs* 68.3 (2021), pp. 830–836. DOI: 10.1109/TCSII.2021.3049518.

[71] Asghar Bahramali and Marisa Lopez-Vallejo. “An RFID-based self-biased 40 nm low power LDO regulator for IoT applications”. In: *Micromachines* 12.4 (2021), p. 396.

[72] Dominic A Funke et al. “Ultra low-power,-area and-frequency CMOS thyristor based oscillator for autonomous microsystems”. In: *Analog Integrated Circuits and Signal Processing* 89.2 (2016), pp. 347–356.

[73] Zaitian Yang et al. “A LDO with 5-nA Quiescent Current and Improved Transient Response within a 50-mA Load Current Range”. In: *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2024, pp. 1–5.

[74] Yasuyuki Okuma et al. “0.5-V input digital LDO with 98.7% current efficiency and 2.7-μA quiescent current in 65nm CMOS”. In: *IEEE Custom Integrated Circuits Conference 2010*. IEEE. 2010, pp. 1–4.

[75] Shuo Li and Benton H Calhoun. “14.6 A 745pA Hybrid Asynchronous Binary-Searching and Synchronous Linear-Searching Digital LDO with 3.8× 10 5 Dynamic Load Range, 99.99% Current Efficiency, and 2mV Output Voltage Ripple”. In: *2019 IEEE International Solid-State Circuits Conference-(ISSCC)*. IEEE. 2019, pp. 232–234.

[76] Óscar Pereira-Rial, Paula López, and Juan M Carrillo. “0.6-V-V_{IN} 7.0-nA-I_Q 0.75-mA-I_L CMOS Capacitor-Less LDO for Low-Voltage Micro-Energy-Harvested Supplies”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 69.2 (2021), pp. 599–608.

[77] Joseph Hamilton, Shouli Yan, and TR Viswanathan. “An uncalibrated 2 MHz, 6 mW, 63.5 dB SNDR discrete-time input VCO-based $\Delta\Sigma$ ADC”. In: *Proceedings of the IEEE 2012 Custom Integrated Circuits Conference*. IEEE. 2012, pp. 1–4.

[78] John A McNeill, Rabeeh Majidi, and Jianping Gong. “Split ADC background linearization of VCO-based ADCs”. In: *IEEE Transactions on Circuits and Systems I: Regular Papers* 62.1 (2014), pp. 49–58.

[79] Zhenbiao Li and O KK. “A low-phase-noise and low-power multiband CMOS voltage-controlled oscillator”. In: *IEEE Journal of Solid-State Circuits* 40.6 (2005), pp. 1296–1302.

[80] Ting-Ping Liu. “A 6.5 GHz monolithic CMOS voltage-controlled oscillator”. In: *1999 IEEE International Solid-State Circuits Conference. Digest of Technical Papers. ISSCC. First Edition (Cat. No. 99CH36278)*. IEEE. 1999, pp. 404–405.

[81] Yu-Shiang Lin, Dennis Sylvester, and David Blaauw. “A sub-pW timer using gate leakage for ultra low-power sub-Hz monitoring systems”. In: *2007 IEEE Custom Integrated Circuits Conference*. IEEE. 2007, pp. 397–400.

[82] Yuya Nishio, Atsuki Kobayashi, and Kiichi Niitsu. “Design and calibration of a small-footprint, low-frequency, and low-power gate leakage timer using differential leakage technique”. In: *IEICE Transactions on Electronics* 102.4 (2019), pp. 269–275.

[83] Ajay Kumar Mahato. “Ultra low frequency CMOS ring oscillator design”. In: *2014 Recent Advances in Engineering and Computational Sciences (RAECS)*. 2014, pp. 1–5. DOI: 10.1109/RAECS.2014.6799627.

[84] Pablo Mendoza Ponce et al. “A 1.9 nw timer and clock generation unit for low data-rate implantable medical devices”. In: *2020 IEEE 11th Latin American Symposium on Circuits & Systems (LASCAS)*. IEEE. 2020, pp. 1–4.

[85] Anton Geläschus et al. “Low Frequency and Low Power Oscillator using Thyristor-Based Delay Elements for Optoelectronic Implants”. In: *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*. 2023, pp. 1–4. DOI: 10.1109/ICECS58634.2023.10382932.

[86] Yoonmyung Lee et al. “A sub-nW multi-stage temperature compensated timer for ultra-low-power sensor nodes”. In: *IEEE journal of solid-state circuits* 48.10 (2013), pp. 2511–2521.

[87] Seokhyeon Jeong et al. "A 5.8 nW CMOS wake-up timer for ultra-low-power wireless applications". In: *IEEE Journal of Solid-State Circuits* 50.8 (2015), pp. 1754–1763.

[88] Atsuki Kobayashi and Kiichi Niitsu. "Low-Voltage Gate-Leakage-Based Timer Using an Amplifier-Less Replica-Bias Switching Technique in 55-nm DDC CMOS". In: *IEEE Open Journal of Circuits and Systems* 1 (2020), pp. 107–114. DOI: 10.1109/OJCAS.2020.3007393.

[89] Jaewook Kim and Seonghwan Cho. "A time-based analog-to-digital converter using a multi-phase voltage controlled oscillator". In: *2006 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2006, 4–pp.

[90] Marek Hempel et al. "Technology and applications of 2D materials in micro-and macroscale electronics". PhD thesis. Massachusetts Institute of Technology, 2020.

[91] Nam Sung Kim et al. "Leakage current: Moore's law meets static power". In: *computer* 36.12 (2003), pp. 68–75.

[92] Jan Rabaey. *Low power design essentials*. Springer Science & Business Media, 2009.

[93] Behzad Razavi. *Design of Analog CMOS Integrated Circuits*. first. McGraw-Hill, 2001.

[94] Chenming Hu. *Modern semiconductor devices for integrated circuits*. Vol. 2. Prentice Hall Upper Saddle River, NJ, 2010.

[95] Jean-Paul Kleider et al. "Revisiting the theory and usage of junction capacitance: Application to high efficiency amorphous/crystalline silicon heterojunction solar cells". In: *Solar Energy Materials and Solar Cells* 135 (2015), pp. 8–16.

[96] Orazio Aiello et al. "A pW-power Hz-range oscillator operating with a 0.3–1.8-V unregulated supply". In: *IEEE Journal of Solid-State Circuits* 54.5 (2019), pp. 1487–1496.

[97] Bernard Marr. *Smart Dust Is Coming. Are You Ready?* https://www.forbes.com/sites/bernardmarr/2018/09/16/smart-dust-is-coming-are-you-ready. Acceso: 2022-10-28.

[98] Michael F Reynolds et al. "Microscopic robots with onboard digital control". In: *Science Robotics* 7.70 (2022), eabq2296.

[99] Wei Gao and Joseph Wang. "Synthetic micro/nanomotors in drug delivery". In: *Nanoscale* 6.18 (2014), pp. 10486–10494.

[100] Rohan Fernandes and David H Gracias. "Self-folding polymeric containers for encapsulation and delivery of drugs". In: *Advanced drug delivery reviews* 64.14 (2012), pp. 1579–1589.