High Efficiency Envelope Tracking Buck Converter for RF PA using GaN HEMTs

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***Abstract*—In this paper, application of a new technological solution for power switches based on Gallium Nitride and a filter design methodology for high efficiency Envelope Amplifier in RF transmitters are proposed. Comparing to Si MOSFETs, GaN HEMTs can provide higher efficiency of the Envelope Amplifier, due to better Figure Of Merit (lower product of on- resistance and gate charge). Benefits of their application were verified through the experimental results. The goal of the filter design is to generate the envelope reference with the minimum possible distortion and to improve the efficiency of the Amplifier, obtaining the optimum trade-off between conduction and switching losses.**

I. INTRODUCTION

In the modern world of communications today, the demand for broadband and wireless services is growing on a daily basis. The direct consequence of this development is the growth of the networks that have to provide these services and one of the problems is their energy consumption. The main reasons for the low efficiency of the radio base stations is poor efficiency of linear power amplifiers, employed to transmit the signal. There are a lot of techniques that are used in order to enhance the efficiency of RF PA, but two of them are mostly exploited lately: Envelope Tracking (ET) [1] and Kahn's Technique or Envelope Elimination and Restoration (EER) Technique, presented in Figure 1 [2]. Both techniques are based on the voltage modulation at the output of the power supply for RF PA. The converter that supplies the energy is the Envelope Amplifier.

The Envelope Amplifier in EER should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. A Synchronous Buck which can be used for this purpose, needs to fulfill the following requirements: reference tracking of modulating voltage, high linearity, low phase delay, high efficiency. The bandwidth of the converter, the ripple of the output voltage and the converter's efficiency depend on the selection of the switching frequency and the design of the output filter. In order to obtain high bandwidth, very high switching frequency is needed. This usually implies high switching losses and low efficiency of the converter.

Another important issue is the additional spectral components of the converter output voltage, created by the modulation of the duty cycle in order to reproduce the desired envelope. These spectral components are around the converter's switching frequency and its multiples.

In order to obtain high efficiency of the converter operating at high switching frequencies, we need transistors with good FOM (product of on-resistance and gate charge). New generation of Enhancement mode HEMTs built with Gallium Nitride on Silicon, presents an excellent replacement for Silicon power MOSFETs, because of promising conductivity and switching characteristics of GaN devices [3], [4], [5], [6].

There are two main objectives of this paper: the first one is to present the methodology for filter design in synchronous buck for RF PA and the second one is to show the advantages of GaN HEMTs comparing to Si MOSFETs.

II. OUTPUT FILTER DESIGN

The main objectives of the filter design in synchronous buck for RF PA are generation of the envelope reference with minimum possible distortion and high efficiency of the converter obtained by the optimum trade-off between conduction and switching losses.

Regarding the selection of a correct switching frequency, an analysis of the inter-modulation products induced by the PWM on the envelope signal is an important issue. It is assumed that the modulating signal with tone frequency f_{mod} yields duty cycle d(t) in the power stage [7]

$$d(t) = \frac{\alpha}{2}(1 + \sin(2\pi f_{mod} t)) \quad (1)$$

A single tone modulating signal is used to establish the Fourier series decomposition of the PWM signal at the input of the filter, using the Bessels functions of the first kind [7]. For a multi-tone like RF envelope, the analysis is very hard though [8] proposes a method to determine an equivalent single tone. The PWM spectrum for single tone modulation shows that no harmonics contribution of f_{mod} is present in the spectrum and most of the additional spectral components are concentrated in high frequency range, around the harmonics of the switching frequency f_{sw} [7]. In order to minimize the high frequency components, the switching frequency should be increased so that corresponding spurious frequencies fall in the frequency range where the attenuation of the LC output filter is high enough.

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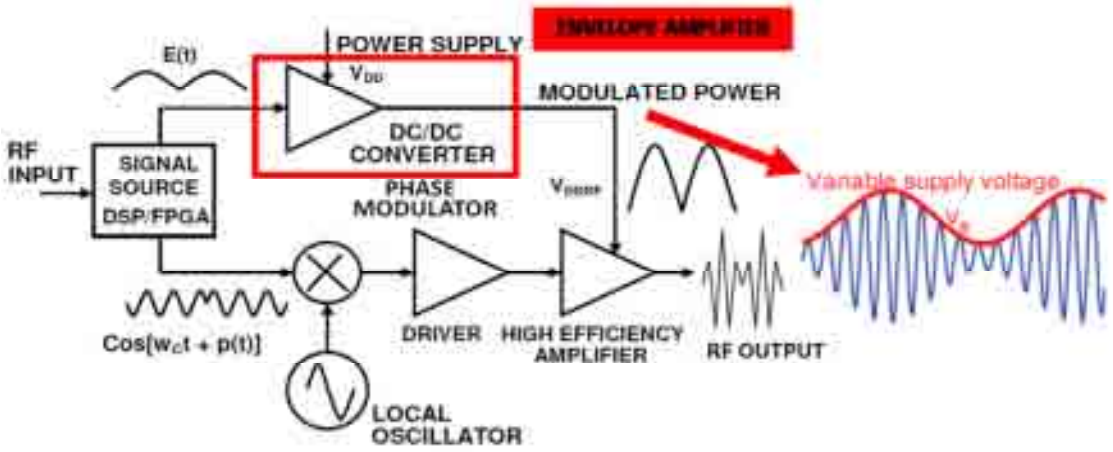

Fig. 1 Block Scheme of Kahn Technique Transmitter

The minimum switching frequency, f_{sw}, is

$$f_{sw} = f_0\, 10^{\frac{a_{tt}}{40}} \quad (2)$$

In the previous equation, a_{tt} is desired attenuation of the duty cycle to output voltage transfer function, $G_{vd}(s)$, in dB (Figure 3) and f_0 is the minimum resonance frequency of the filter which is given by

$$f_0 = \frac{1}{2\pi\sqrt{L_{MAX}C_{OUT}}} \quad (3)$$

C_{OUT} is the capacitance of the LC filter and L_{MAX} is the maximum value of the output filter inductance. Now we have to present the main criteria and the procedure for L_{MAX} and C_{OUT} determination.

The criteria for C_{OUT} determination is minimization of the conduction losses in MOSFETs, inductor and capacitor

$$P_{MOS} = R_{DSON}\, {i_{L\_RMS}}^2 \quad (4a)$$

$$P_L = R_L\, {i_{L\_RMS}}^2 \quad (4b)$$

$$P_C = R_{ESR}\, {i_{C\_RMS}}^2 \quad (4c)$$

as well as minimization of switching losses which will be presented in the next section.

Analysing the circuit from Figure 2, we obtain that the inductor to load current ratio is given by

$$\frac{i_L}{i_{LOAD}} = 1 + R_{LOAD}C_{OUT}\, s \quad (5)$$

and its frequency dependence is presented in Figure 4. From (5) we obtain the design parameter A

$$\frac{i_{Lmax}}{i_{LOADmax}}(j2\pi f_{MOD}) = A \quad (6)$$

where A ≥1. Assuming that the ratio of the maximum values of inductor and output current is set to A, for C_{OUT} we obtain

$$C_{OUT} = \frac{\sqrt{A^2-1}}{2\pi f_{MOD}R_{LOAD}} \quad (7)$$

Higher values of C_{OUT} correspond to higher values of A and higher conduction losses. Minimization of C_{OUT} provides lower conduction losses but gives us higher corner frequency of the filter, which implies higher switching frequency and higher switching losses. In order to decrease the corner frequency of the filter, we choose the maximum value for the inductance, L_{MAX}.

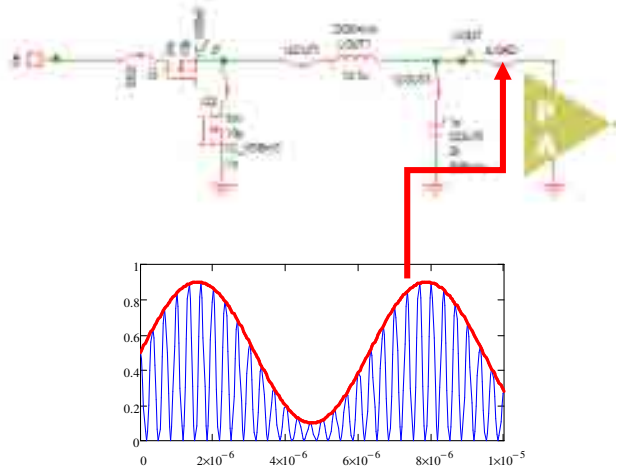

Fig. 2 Synchronous Buck for RF PA

Fig. 3 Duty cycle to output voltage transfer function

The criteria for L_{MAX} determination is to avoid duty cycle saturation. From $G_{vd}(s)$ we obtain

$$d(s) = {G_{vd}}^{-1}(s)v_{OUT}(s) \quad (8)$$

where d(s) (Figure 5) and $v_{OUT}(s)$ present the duty cycle and the output voltage in the frequency domain.

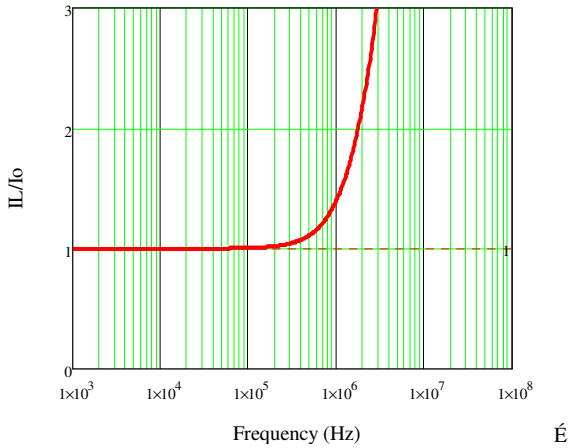

Fig. 4. Frequency dependence of inductor to load current ratio

If we set that for the maximum change of the output voltage equal to Δv_{OUT} we have $\Delta d=1$, we obtain

$$\frac{\Delta v_{OUT}}{V_{IN}}\sqrt{[1-L_{OUT}C_{OUT}(2\pi F_{MOD})^2]^2+\frac{L_{OUT}}{R_{LOAD}}(2\pi F_{MOD})^2}=1 \quad (9)$$

where V_{IN} is the input voltage of the converter. Solving the previous equation we obtain the value for L_{MAX}.

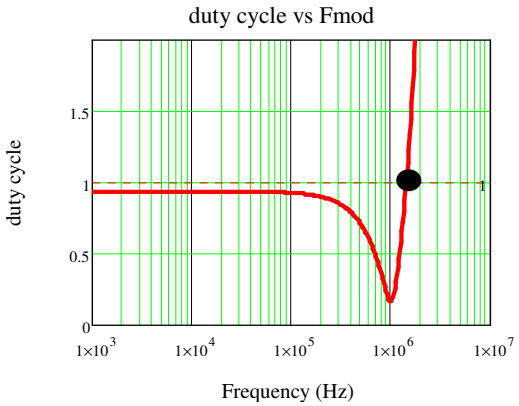

Fig. 5. Frequency dependence of the duty cycle

In order to determine the total losses dependence of filter design parameter A, the switching losses model is determined [9].

Regarding the switching losses in the converter, high-side losses are dominant, since high-side switch swings the full input voltage with full current through it. Drive equivalent circuit for high-side switch and high-side switching losses are presented in Figure 6 and 7.

The switching interval begins when the high-side driver turns on and starts to supply current to high-side gate to charge its input capacitance. There are no switching losses until V_{GS} reaches the threshold voltage, V_{TH}. Therefore, losses during the time interval t_1 are zero.

When V_{GS} reaches V_{TH}, the input capacitance C_{ISS} is being charged and the drain current is rising linearly until it reaches the inductor current. During the time interval t_2, the switch is sustaining the entire input voltage across it. The energy in the

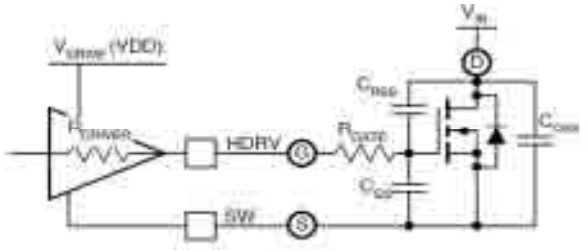

Fig. 6. High-Side drive equivalent circuit

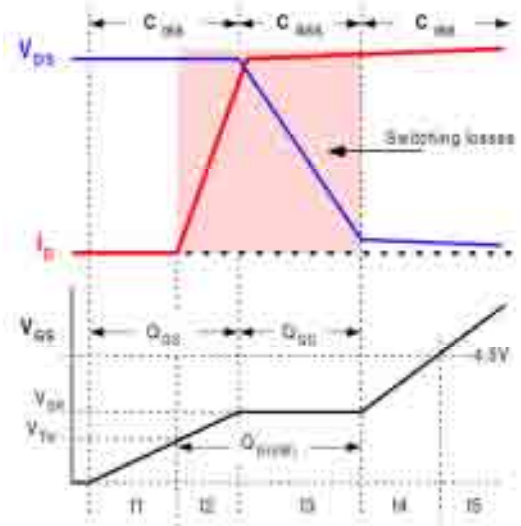

Fig. 7. High-Side switching losses

high-side transistor during t_2 is:

$$E_{t2}=t_2\left(\frac{V_{IN}I_{LRMS}}{2}\right) \quad (10)$$

where I_{LRMS} is a RMS value of inductor current.

When the time interval t_3 starts, all of the gate current will be going to recharge the capacitance between gate and drain, C_{GD}, and V_{DS} begins to fall from V_{IN} to zero. Therefore:

$$E_{t3}=t_3\left(\frac{V_{IN}I_{LRMS}}{2}\right) \quad (11)$$

During t_4 and t_5, the switch is just fully enhancing the channel to obtain its rated $R_{DS\ ON}$ at a rated V_{GS}. The losses during this time are very small comparing to ones in t_2 and t_3 and can be neglected in the analysis.

From (10) and (11), for high-side switching losses we obtain:

$$P_{sw\_hs}=\left(\frac{V_{IN}I_{LRMS}}{2}\right)(t_2+t_3)\,f_{sw} \quad (12)$$

Time intervals t_2 and t_3 are determined by the driver capability to deliver all of the charge required in that time period:

$$t_x=\frac{Q_{GX}}{I_{DRIVER}} \quad (13)$$

where x=2,3.

Low-side switching losses can be calculated in a similar way to high-side switching losses. Approximately, we obtain:

$$P_{sw\_ls}=\left(t_2V_F+t_3\frac{V_F+I_{LRMS}1.1R_{DS_{ON}}}{2}\right)I_{LRMS}\,f_{sw} \quad (14)$$

where V_F is a forward voltage drop on a body diode, R_{DS_ON} is on-resistance of a switch and t_2 and t_3 are time intervals presented in Figure 8. The drain current, drain-to-source and gate-to-source voltage of a low-side switch are also presented in Figure 8.

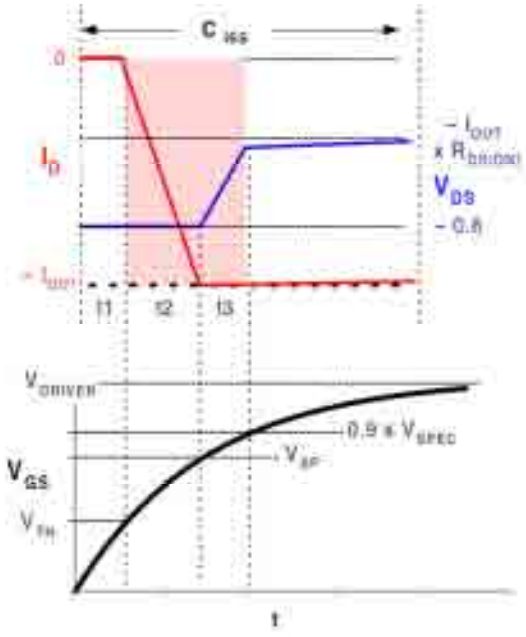

Fig. 8. Low-Side switching losses

From (4a), (4b), (4c), (12) and (14) we obtain the approximate model for the total power losses. If we implement the power losses model in Matlab, we obtain the losses dependence on the filter design parameter A, presented in Figure 9. The obtained curve is expected, because the lower values for A correspond to higher switching frequencies and dominant switching losses and higher values for A to dominant conduction losses. It can be seen that for A approximately equal to 1.4, efficiency has the highest value, i. e. this point corresponds to the optimum efficiency point.

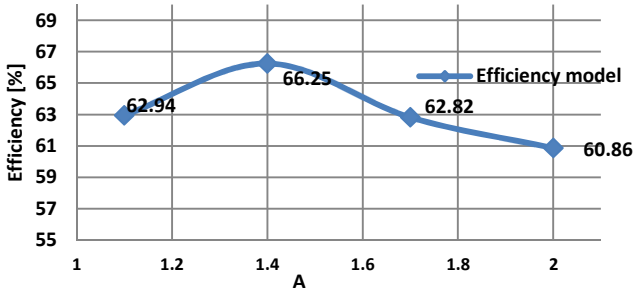

Fig. 9. Efficiency model for different filter designs

III. COMPARISON OF GALLIUM NITRIDE AND SILICONE DEVICES

New generation of GaN devices is very promising for high voltage, high temperature and high switching frequency applications, because of their superior conductivity and switching characteristics over Si devices. In the aim of reduction of power losses at high switching frequencies, GaN HEMTs present an excellent choice for Synchronous Buck in RF application [10]. In order to make the comparison between different devices for the same specifications, we define Figure Of Merit:

$$FOM = Q_G * R_{DS\,ON} \quad (15)$$

For the same specifications regarding the breakdown voltage and maximum drain current, Figure Of Merit for EPC 1015 GaN HEMT is 37.1 and for Si OptiMOS3 Power Transistor from Infineon [11] is 98.04 (Table 1). The calculated values showed 2.64 times better FOM for GaN.

Device	Type	V_{ds_max}[V]	R_{on}[mΩ]	Q_G[nC]	FOM
EPC1015	GaN	40	3.2	11.6	37.1
OptiMOS	Si	40	11.4	8.6	98.04

Table 1. Characteristics of the devices

IV. EXPERIMENTAL RESULTS

The first prototype was made using two EPC 1015 GaN HEMTs, two isolation chips ISO 721 and two EL7155 drivers (Figure 10) with XILINXs SPARTAN3 FPGA board in order to provide control signals.

In order to make a comparison with Si MOSFETs, the second prototype was built using OptiMOS Si power transistors from Infineon [11], with previously calculated value for FOM. Both prototypes were made exactly the same, regarding the PCB layout, isolation chips and drivers that were used, in order to make the precise comparison between the performance of GaN and Si devices.

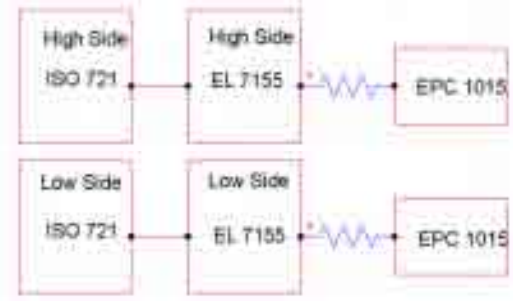

Fig. 10. Simplified schematic of a synchronous buck

The first measurements for both prototypes were made for a constant output power, at switching frequency equal to 4.7MHz, changing the duty cycle in order to provide different power levels at the output. The efficiency measurement is presented in Figure 11. Difference in efficiency is obvious especially for the low output power, which is the goal for the Envelope Amplifier.

During these measurments, the duty cycle change was bounded between 35% and 75%, because Si prototype was not able to generate it outside these boundaries. Detailed analysis showed distortion of the gate signals at the outputs of the drivers (Figure 12), because of their low current capability at 4.7MHz. In these conditions, GaN prototype was working properly because of the lower threshold voltage of GaN HEMTs, providing the duty cycle range from almost 0% to 100%, which is of crucial importance for RF envelope generation. If the whole range for a duty cycle cannot be produced, generated envelope is distorted which leads to errors in a signal transmission.

Furthermore, it is experimentally shown that overshoot in drain to source voltage of the low-side switch is significantly higher in the case of Si (Figure 14) comparing to the GaN

HEMT (Figure 13), due to higher leakage inductance of PG-TSDSON-8 Si transistor package. This fact limits the value of the input voltage that can be applied to the Si prototype.

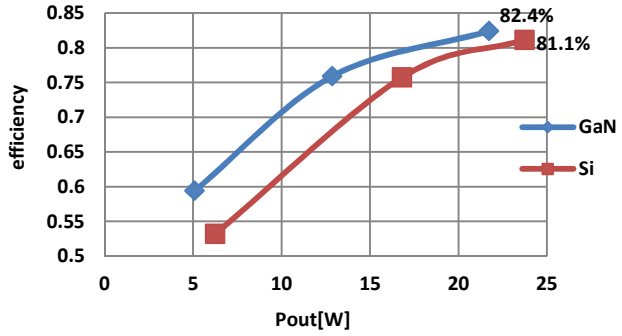

Fig. 11 . Efficiency measurement for Si and GaN prototype at 4.7MHz

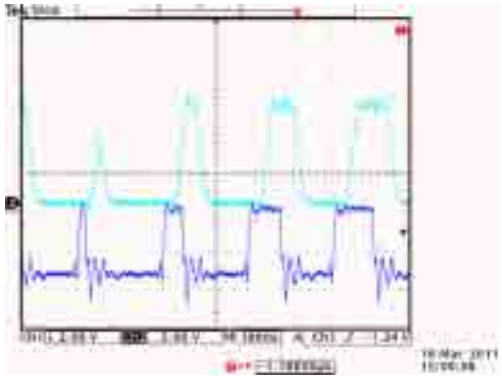

Fig. 12 . Signals at the output of the FPGA (down) and distorted signals at the output of the driver (up) for both prototypes

Speaking of filter design methodology, four designs were made, for four different values of paremeter A. For V_{IN}=24V and R_{LOAD}=15Ω, sinusoidal output voltage of 200kHz with the voltage swing of 21V was generated, using the prototype with GaN. Obtained results are presented in Table 2. As it was previously mentioned, lower A values correspond to higher switching lossess and higher A values to higher conduction losses. Experimental results showed good correspondence with the power losses model (Figure 15) and the highest efficiency for A around 1.4. For A=1.4, output voltage waveform is presented in Figure 16.

Next, 64QAM signal was generated, using the prototype with GaN HEMTs. With input voltage equal to 20V and switching frequency of 4.5MHz, the obtained RF sequence is presented in Figure 17. The obtained efficiency for average output power P_{OUT}=8.1W , including both drivers, was 70.3%. For the same switching frequency, prototype with Si MOSFETs could not generate this sequence because the obtained duty cycle was bounded between 35% and 75%.

Finally, Wideband Code Division Multiple Access (WCDMA) sequence was generated, using the GaN prototype (Figure 18). With switching frequency equal to 5MHz, envelope with the bandwidth of 500kHz was generated, with average output power equal to 7.5W. Measured efficiency including both drivers was 58%.

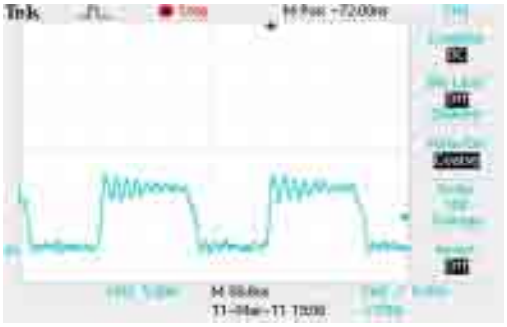

Fig. 13. Measured Vds of the low-side switch in GaN prototype for Vin=10V

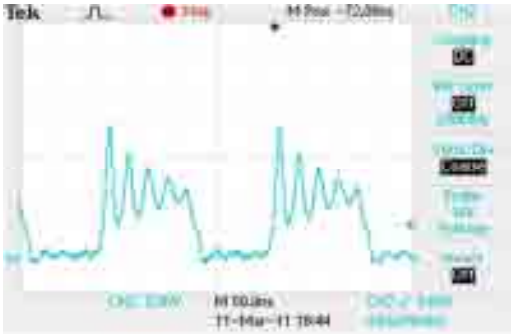

Fig. 14. Measured Vds of the low-side switch in Si prototype for Vin=10V

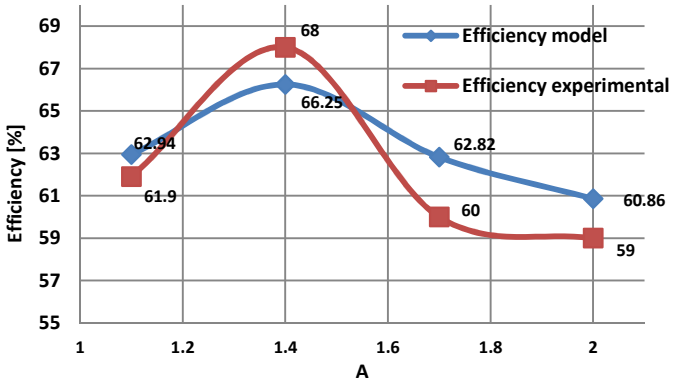

Fig. 15. Comparison of efficiency model and experimental results for different filter designs

	A = 1.1	A =1.4	A = 1.7	A = 2.0
f_{SW}[MHz]	5.9	4.2	3.7	3.5
L[uH]	8.7	8.9	8.1	7.4
C[nC]	18	40	56	66
P_{LOSSES}[W]	5.6	4.9	6.9	8.3

Table 2. Comparison of four different filter designs for the average output power of 10W

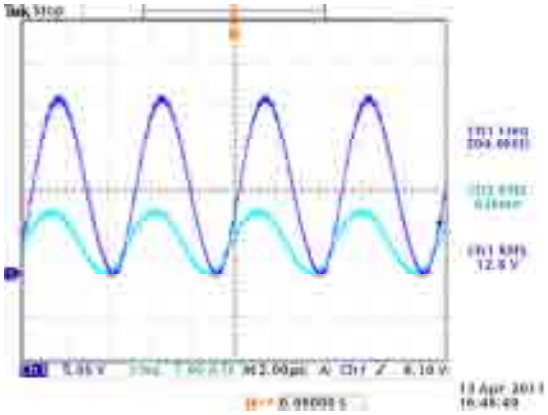

Fig. 16. Output voltage (dark blue) and inductor current (light blue) for A=1.4

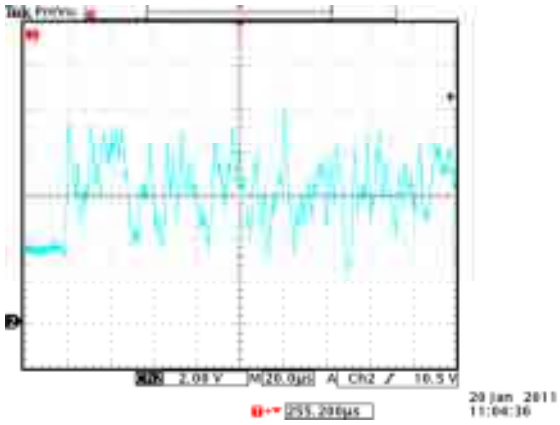

Fig. 17. Generated 64QAM envelope sequence with GaN prototype

V. CONCLUSIONS AND FUTURE WORK

Design of an Envelope Amplifier using new switching devices based on Gallium Nitride and filter design methodology for this application, were proposed in this paper. Regarding the filter design, dependence of the power losses on the design parameter A was derived and the efficiency optimum point was found. Experimental results showed good correspondence with the model and verified the proposed methodology. On the other hand, comparing to Si, application of GaN HEMTs showed higher efficiency for constant output power at 4.7MHz of switching frequency. Regarding the generation of RF sequence, prototype with Si was not able to provide the full range for the duty cycle at 5MHz of switching frequency, because of the drivers with low current capability and higher threshold voltage of Si devices. In other words, it wasn't possible to generate the undistorted RF envelope using the prototype with Si. In the same conditions, prototype with GaN generated WCDMA envelope with the bandwidth of 500kHz with efficiency equal to 58%, including both drivers.

Regarding the future work, it is necessary to increase the switching frequency in order to obtain a higher bandwidth of the RF signal. In order to do that, it is necessary to resolve the problem of drivers current capability.

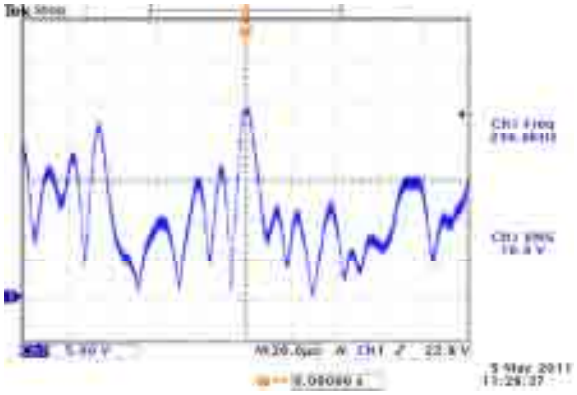

Fig. 18. Generated WCDMA signal with GaN prototype

Fig. 19. Prototype with GaN HEMTs

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