Serial or Parallel Linear-assisted Switching Converter as Envelope Amplifier: Optimization and Comparison

Miroslav Vasić, Oscar Garcia, Jesus A. Oliver, Pedro Alou, Jose A. Cobos
Universidad Politécnica de Madrid
Centro de Electrónica Industrial, CEI
Madrid, Spain

***Abstract*— This paper presents a theoretical analysis and an optimization method for envelope amplifier. Highly efficient envelope amplifiers based on a switching converter in parallel or series with a linear regulator have been analyzed and optimized. The results of the optimization process have been shown and these two architectures are compared regarding their complexity and efficiency. The optimization method that is proposed is based on the previous knowledge about the transmitted signal type (OFDM, WCDMA…) and it can be applied to any signal type as long as the envelope probability distribution is known. Finally, it is shown that the analyzed architectures have an inherent efficiency limit.**

I. INTRODUCTION

In modern wireless communication systems signals that provide high spectral efficiency (high transmission data rate) like OFDM are employed. These signals are generated by instantaneous modulation of the carrier's envelope and phase and therefore the linearity of the final stage power amplifier is of crucial importance. Another important issue for these amplifiers is their energy efficiency. Traditional linear power amplifiers (PAs), class A and class AB, have to be implemented applying "back-off" technique in order to obtain the desired linearity. However, due to high peak to average power ratio (PAPR) these solutions suffer from poor efficiency and in the case of hand held devices short battery life.

Techniques based on envelope tracking (ET) and envelope elimination and restoration (EER) have demonstrated their potential for next generation communication systems [1-3]. Both techniques have in common that it is necessary to modulate the supply voltage of the amplifier and it is done using an envelope amplifier (modulator) like in Figure 1. In the state of the art there is a wide variety of solutions for the envelope amplifier depending on the power it has to process and the required bandwidt. In [4-5] solutions based on simple buck converter are proposed, while in [1-3, 6-8] solution based on switching converter in parallel and series with a linear regulator are presented.

The main difference between these two architectures is how the energy is processed by the linear regulator. In the parallel linear assisted switching converter, the linear regulator supplies just a part of the output energy and the high efficiency of the envelope amplifier is provided by the buck converter that is used in parallel. In the second architecture, the linear regulator has to process all the output power. In order to obtain high efficiency the switching converter has to supply the linear regulator with variable voltage and minimize the input-output voltage drop of the linear regulator.

In this paper we present an optimization method for the envelope amplifiers based on a switching converter in series/parallel with a linear regulator. The optimization method uses the information of the transmitted signal, and the envelope amplifier is designed in order to obtain the highest efficiency.

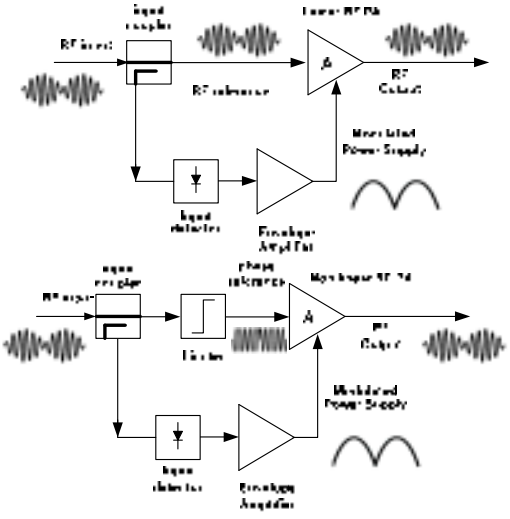

Figure 1. Simplified block schematics of radio transmitters based on ET (above) and EER technique (below)

This work has been supported by the Ministry of Education and Science of Spain for the project TEC2009-14307-C02-01

II. OPTIMIZATION OF THE PARALLEL LINEAR ASSISTED SWITCHING CONVERTER AS ENVELOPE AMPLIFIER

Figure 2 shows the envelope amplifier based on a linear regulator and a synchronous buck converter in parallel. The buck converter operates as a DC current source, while the linear regulator operates as a voltage regulator. The buck converter is controlled using a using simple hysteresis control, but the analysis can be easily expanded for other control types as well. The conventional approach is to set the DC current of the buck converter to be equal to the mean average DC current of the load [1, 2] (i.e the RF PA in this case). However in [9] it has been shown that this approach does not have to be the optimum one from the point of view of efficiency.

In this paper, an optimization process is performed in order to see the influence of each design parameter and to design an optimal envelope amplifier from the point of view of efficiency.

The optimization method is based on the following steps:

- Determine a precise model of the power losses in the switching converter
- For a specific RF signal, analyze the efficiency and volume inside the certain design space or design constraints. The analysis is performed by varying three independent variables of the system (average current of the inductor, width of the hysteresis band and the value of the inductor).

A. Power losses in the switching converter

The power loss in the switching converter can be divided in two parts: conduction losses and switching losses.

The conduction losses are present due to the resistance of the MOSFET and the total resistance (AC and DC) of the inductor. In the case of the buck converter, the power losses due to this mechanism can be expressed as:

$$P_{conduction} = (R_{ON} + R_L + R_S)I_{RMS}^2 \quad (1)$$

where R_{ON} is the resistance of the conducting MOSFET, R_L is the resistance of the inductor and I_{RMS} the effective value of the converter's output current and R_S is the resistance of the shunt resistance that is used to sense the current. In this paper the current is sensed by a shunt resistance that is in series with the buck inductor, while the voltage drop is measured by a wide bandwidth differential voltage amplifier. It is assumed that the MOSFETs are identical.

In order to calculate the power losses due to the switching process, we used a simple model of the MOSFET. It is assumed that the MOSFET behaves as an ideal switch, with linear capacitors between its terminals and that the driver that controls it is sufficiently fast so that the switching power losses are proportional to the charge, like in [10].

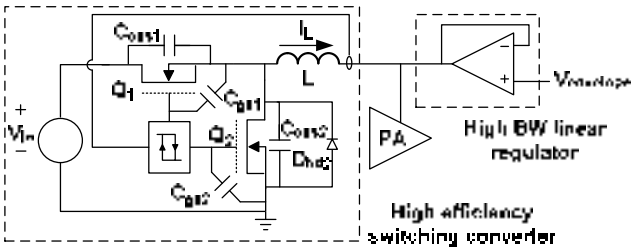

Figure 2. Envelope amplifier based on a buck converter in parallel with a linear regulator.

Whenever one switching cycle occurs, there are losses due to the parasitic gate capacitor and in one switching cycle the energy of these losses for one MOSFET is:

$$E_{gate} = Q_{gate}V_{gate} \quad (2)$$

where Q_{gate} is the total charge that has to be used to turn on the MOSFET and V_{gate} the supply voltage of the driver.

MOSFET Q_1 always exhibits power losses due to the charging and discharging of the parasitic capacitance between its source and drain. These losses are calculated as:

$$E_{Q1} = C_{oss}V_{in}^2 \quad (3)$$

where C_{oss} is the equivalent value of the parasitic capacitor and V_{in} the input voltage of the converter. In the case of Q_2 the power losses are different, because they depend on the value of the dead time that is applied and the inductor's current in the moment when Q_1 is turned off. Three different cases can be distinguished:

- The parasitic capacitance C_{oss} is not completely discharged during the dead time, the losses are:

$$E'_{Q2} = C_{oss}V_{oss}^2 \quad (4)$$

where V_{oss} is equal to the voltage across Q_2 in the moment when it is turned on.

- The parasitic capacitance C_{oss} is completely discharged and zero voltage turn on of the Q_2 is achieved

$$E'_{Q2} = 0 \quad (5)$$

- The parasitic capacitance C_{oss} is completely discharged and the body diode starts to conduct

$$E'_{Q2} = V_D I_L t_D + Q_{rr}V_{in} \quad (6)$$

where t_D is the duration of the dead time.

Additionally, whenever Q_2 is turned off, its C_{oss} is charged through Q_1 and the additional losses are:

$$E''_{Q2} = \frac{1}{2}C_{oss}V_{in}^2 \quad (7)$$

Therefore, the total power losses are:

$$P_{total} = P_{conduction} + \left(2E_{gate} + E_{Q1} + E'_{Q2} + E''_{Q2}\right)f_{SW} \quad (8)$$

where f_{SW} is the switching frequency of the converter.

If we analyze (8) it can be seen clearly that all the power losses are strongly related to the value of the switching frequency and the value of the inductor current.

In the case of the hysteresis control the switching frequency is not constant and it depends on the envelope amplifier's output voltage and the selected hysteresis band. If the envelope signal were a constant signal, the power losses would be easily calculated. However, having in mind that the envelope of the transmitted signal is changed dynamically, the switching frequency is going to change dynamically as well. In another words, it can be written:

$$f_{sw} = f_{sw}(v_{envelope}, \Delta I_L)$$
$$P_{total} = P_{total}(v_{envelope}, \Delta I_L) \quad (9)$$

Therefore, the aforementioned equations have to be modified using the information about the reproduced envelope. The information that is necessary is the voltage range of the envelope and its probability density function.

Equations (1)-(7) depend only on the parameters of the converter design such as type of MOSFET, input voltage, width of hysteresis, dc value of the inductor's current etc. However, in order to calculate (8) it is necessary to calculate the average switching frequency of the buck converter. It is done as:

$$f_{sw} = \left(\frac{L\Delta I}{\int_0^{V_{max}} (V_{in} - v_{out}) p(v_{out}) dv_{out}} + \frac{L\Delta I}{\int_0^{V_{max}} v_{out} p(v_{out}) dv_{out}}\right) \quad (10)$$

The last equation stands as long as the dynamics of the output signal is significantly higher than the average switching frequency of the inductor. In other words, it is assumed that during one switching cycle of the buck converter the output voltage sweeps all the possible values according to the probability of the envelope. Combining (10) with (8), it is possible to estimate power losses in the buck converter

B. Power losses in the linear regulator

The linear regulator behaves as a voltage source and its main purpose is to provide the necessary dynamics of the envelope amplifier. Whenever the current of the buck converter is higher than the current demanded by the load, it has to sink the excess of the buck's current. In the case when the load demands high current, it has to source the current. In an ideal case, the linear regulator can be supplied only with positive voltage source. However, it is not the case in the real implementation and, therefore, every sinking and sourcing of the current produces additional power loss. The power loss can be calculated as follows:

$$P_{lin.reg.} = \int_0^{R_{load}(I_{dc} - 0.5\Delta I)} V_{ee} \left(I_{dc} - \frac{v_{out}}{R_{load}}\right) p(v_{out}) dv_{out} +$$

$$+ \int_{R_{load}(I_{dc} - 0.5\Delta I)0}^{R_{load}(I_{dc} + 0.5\Delta I)} \frac{1}{2\Delta I} \left[V_{in} \left(\frac{v_{out}}{R_{load}} - I_{dc} - \Delta I\right)^2 - V_{ee} \left(I_{dc} + \Delta I - \frac{v_{out}}{R_{load}}\right)^2\right] p(v_{out}) dv_{out} +$$

$$+ \int_{R_{load}(I_{dc} + 0.5\Delta I)}^{v_{max}} V_{in} \left(\frac{v_{out}}{R_{load}} - I_{dc}\right) p(v_{out}) dv_{out} \quad (11)$$

It is important to notice that the size of the inductor's current ripple influences in the power losses of the linear regulator.

C. Overall efficiency of the envelope amplifier

The output power is calculated in the similar manner (it is assumed that the load is purely resistive) and it is:

$$P_{output} = \int_0^{V_{envelope\,max}} v_{envelope} i_{load} p(v_{envelope}) dv_{envelope} \quad (12)$$

Combining (10) - (12) the efficiency of the envelope amplifier can be calculated as:

$$\eta = \frac{P_{output}}{P_{output} + P_{conv.losses} + P_{lin.reg.losses}} \quad (13)$$

D. Optimization and experimental verification of the model

The optimization process has been performed for an envelope amplifier with the following specifications:

- Positive input voltage of the buck converter/linear regulator is 20 V
- Load is a 6 Ω resistor
- The output is the envelope of a 64QAM signal with 2 MHz bandwidth and ration of its peak and average power of 8.8 dB

Figure 4 shows the density of probability for the generated envelope.

During the optimization the value of the inductance, the hysteresis band and the buck's average current are varied. Figure 4 shows the estimated efficiency of the envelope amplifier for the fixed value of the inductance (32 μH in this case) and the aforementioned envelope reference.

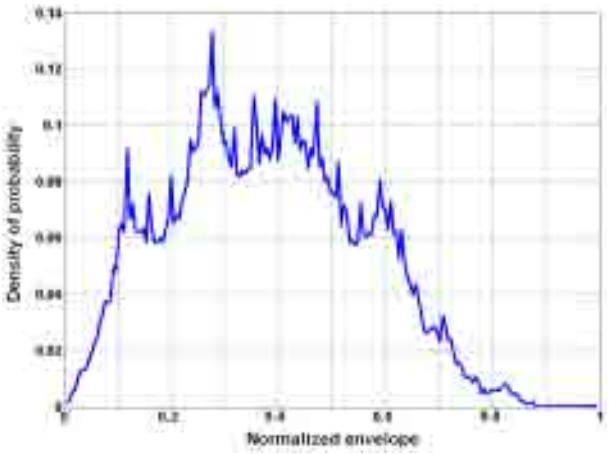

Figure 3. Desnity of probability of the reprodcued 64QAM envelope

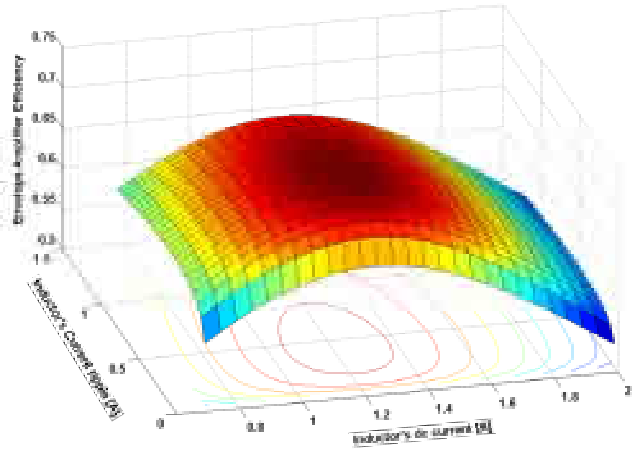

Figure 4. Efficiency of the parallel assisted switching converter depending on the inductor's dc current and its current ripple

In Figure 4 it can be seen that there is a point of maximum efficiency for the given value of the inductor. It is important to notice that the efficiency of the envelope amplifier depends on the value of the hysteresis band as well, although not as heavy as from the inductor's dc current. When the hysteresis band is small, the switching frequency is high, and the switching losses in the buck converter are high as well, which leads to overall efficiency degrading. On the other hand, if the band is too wide the switching losses are not the problem, but the conduction losses (due to high RMS current) in the buck converter and the power losses in the linear regulator as well. That is the reason for the decreased efficiency for the high current ripple.

One of the important results is that the optimum dc current for the buck converter is not necessarily the average current of the load. Figure 5 shows the efficiency of the envelope amplifier for different values of the negative voltage that is used to supply the linear regulator. In this figure it can be seen the heavy influence of this supply voltage on the overall efficiency and the optimal dc current. The necessary negative voltage supply is determined by the transistors that are employed in the linear regulator. Though the difference in efficiency when the buck converter is biased with the optimal and the load's average current is not significant in this case, it may vary sufficiently depending on the statistics of the transmitted signal, as it has been shown in [9].

If the value of the hysteresis band is maintained constant, by increasing the value of the inductor the switching frequency of the buck converter is decreased and, consequently, the switching losses as well. This leads to higher overall efficiency. Figure 6 presents how the overall efficiency is changed when the value of the inductor is increased. Theoretically, if the value of the inductor were sufficiently high, the switching frequency would be close to zero, and the buck converter would only have conduction losses. However, even in that case, when the efficiency of the buck converter is almost 100%, the overall efficiency would not overcome certain limit. In the case of the analyzed system, this efficiency limit is 74%.

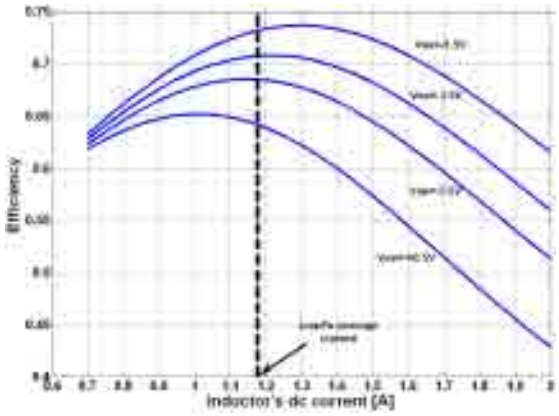

Figure 5. Efficiency of the parallel assisted switching converter dependence on the indcutor's dc curret and negative voltage supply

In this way it has been shown that the analyzed envelope amplifier has an inherent efficiency limit. Higher efficiency cannot be obtained, even if it were possible to use an ideal switching converter without losses. The reason for this is that there is always a part of energy processed by the linear regulator and its influence on the overall efficiency is obviously huge. Figure 5 shows the information regarding the volume of the magnetic that is necessary in order to obtain certain efficiency of the envelope amplifier. It is assumed that the volume of the inductor is proportional to its maximal stored energy. For the space-restricted applications, the information regarding the relation between possible efficiency of the system and the volume that is needed may be of crucial importance.

In order to prove the proposed theoretical optimization an envelope amplifier has been built with the earlier stated specification. The buck converter was implemented with BSZ097N04LS MOSFETs while the linear regulator was implemented as a class B PA, Figure 7. As it has been aforementioned, the linear regulator has to be supplied with a negative voltage as well. In this implementation, this voltage was selected as low as possible in order to guarantee the correct performance of the linear regulator and to minimize its power losses at the same time.

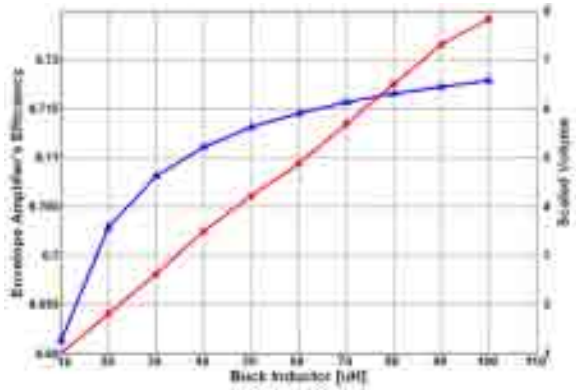

Figure 6. Dependence of the envelope amplifier's efficiency and ocupied volume on the value of the switching converter's inductor

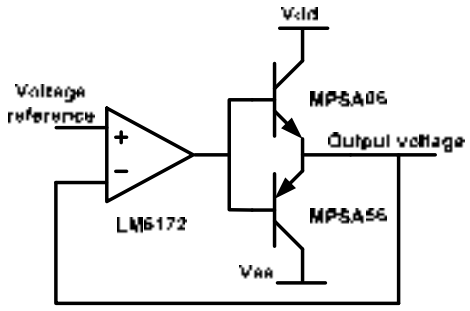

Figure 7. Simplified schematic of the linear regulator that is used in the parallel assisted switching converter

Figure 8 shows the output voltage of the implemented envelope amplifier and the current through the buck's inductor (for this experiment the buck inductor is 19 µH). It can be seen that the hypothesis regarding high dynamics of the output voltage in comparison to the low dynamics of the inductor's current is justified. Figure 9 shows comparison between the measured and calculated efficiency in the case when a 32uH inductor is used. The width of the hysteresis band was constant and maintained at 0.4A. It can be seen that the measured points correspond to the predicted efficiency.

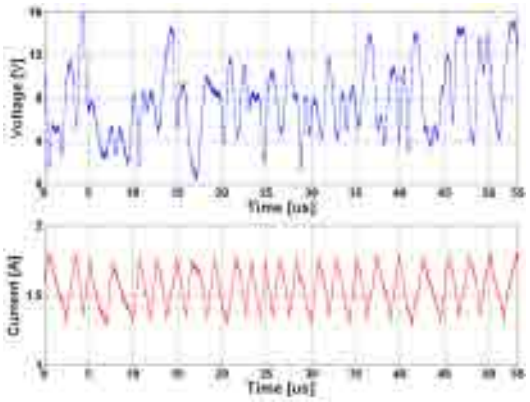

Figure 8. Voltage and current waveforms for the parallel assisted switching converter

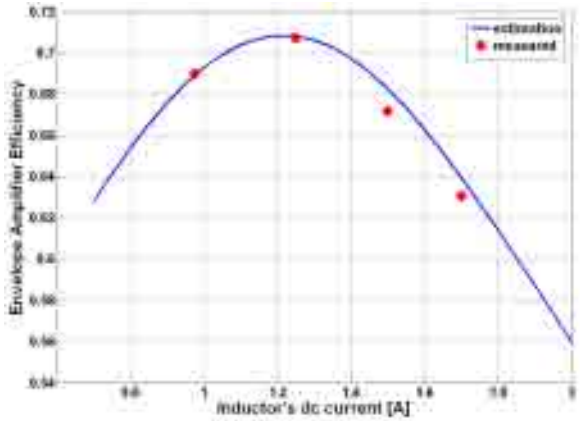

Figure 9. Estiamated and measured efficiency of the parallel assisted switching converter for different values of the inductor's dc current

Figure 10 shows the breakdown of the power consumed by the linear regulator and the buck converter. Once again, it can be seen that the measured power consumption matches with the calculated. This good matching is reflected, among other things, in the average switching frequency of the converter. The difference between the estimated and the measured average frequencies is not higher than 10%.

III. OPTIMIZATION OF THE SERIAL LINEAR ASSISTED SWITCHING CONVERTER AS ENVELOPE AMPLIFIER

Another possibility for the envelope amplifier is to use a multilevel converter in series with a linear regulator [3, 7] as it is shown in Figure 11. In this case, the linear regulator conducts the whole load current and the multilevel converter supplies the linear regulator with appropriate voltage levels in order to decrease the power losses in the linear regulator. Figure 12 shows the time waveforms for the envelope amplifier implemented with this architecture.

A. Power losses in the multilevel converter

Although the multilevel converter can be implemented using different architectures, in this paper only the architecture based on voltage cells is analyzed. In order to estimate the switching losses it is necessary to know the average switching frequency of each voltage cell which is the main problem in the analysis of this architecture.

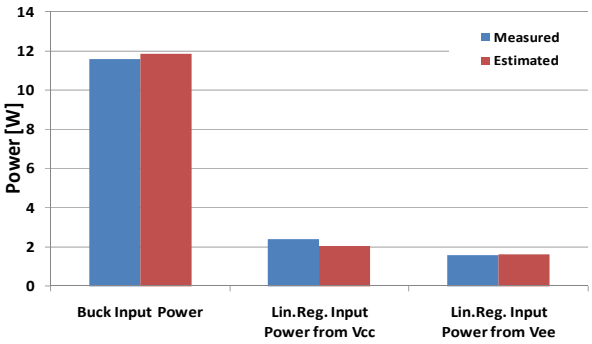

Figure 10. Breakdown of the power consumption by the linear regulator and buck converter in the parallel assisted switching converter

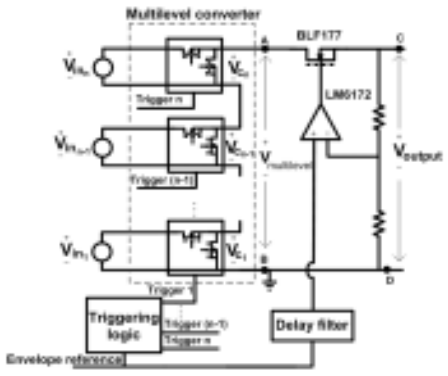

Figure 11. Simplified schematic of the envelope amplifier based on a multilevel converter in series with a linear regulator

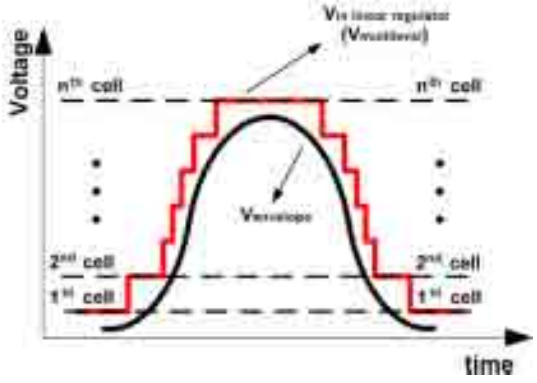

Figure 12. Time diagrams of the multilevel converter depending on the reconstructed envelope

Due to the nondeterministic signal that is transmitted it is necessary not only to know the distribution of the envelope, but also the distribution of the envelope's slope ($dV_{envelope}/dt$) as well. By analyzing the same 64QAM envelope from the previous section, it was possible to obtain this distribution. This distribution is a 2D distribution because it depends on the value of the envelope and its slew rate. Figure 13 shows the distribution of the envelope slope when the envelope is 10 V. It can be seen that the distribution is symmetrical, which means that there is equal probability that the envelope will rise over and fall under 10 V.

The average switching frequency for voltage level V_{level} is calculated in the following way. Let's assume that the samples of the envelope reference are generated with period T_{sample}, and that the maximal slew rate of the envelope is S_{max}, then the probability that a transition will occur at voltage level V_{level} is:

$$P_{transition} = \int_{V_{level}-S_{max}T_{sample}}^{V_{level}} \int_{S_{max}-\frac{V_{level}-v}{T_{sample}}}^{S_{max}} N(v,s)dsdv \quad (14)$$

Where $N(v,s)$ is a 2D distribution of the envelope and its slew rate. The average switching frequency at one voltage level is:

$$f_{avg} = \frac{P_{transition}}{T_{sample}} \quad (15)$$

Figure 14 presents the estimated and the real switching frequency for each voltage level. It can be observed that the estimation is very similar to the real switching frequency. Using this information with the information regarding the number of levels it is possible to estimate the efficiency of the multilevel converter and select the best distribution of the voltage levels in order to minimize the power losses.

The MOSFETs that are used in the voltage cells are not necessarily the same, because they do not have to withstand the same blocking voltage (equal to the cell voltage). Therefore, it is assumed that the employed MOSFETs use the same technology like the MOSFETs from the previous section, i.e. $R_{on}*C_{oss}$ is assumed constant. If this is assumed, then the MOSFETs employed in each cell can be optimized in order to obtain the minimal overall power losses per voltage cell. The power loss model is the same like in the previous section.

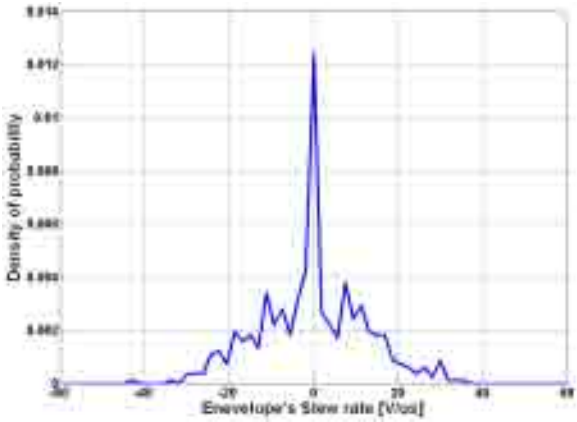

Figure 13. Distribution of the envelope slope when the envelope has value of 10 V

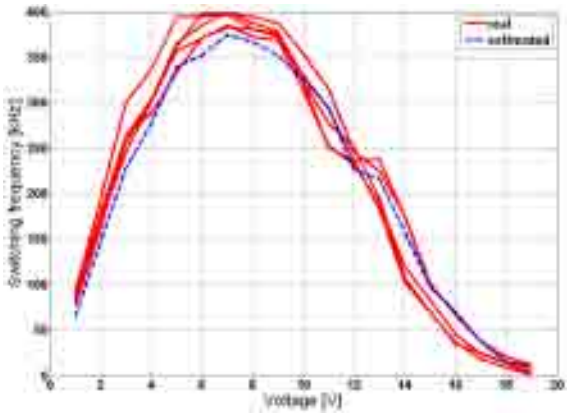

Figure 14. Comaparision of the real and estiamted swtiching frequency for the multilevel converter depending on the level of transition

B. *Power losses in the linear regulator*

Average power losses in the linear regulator are calculated as

$$P_{lin.reg.} = \int_0^{V_{env.max}} (v_{m\_level} - v_{envel}) \frac{v_{envel}}{R_{load}} p(v_{envel}) dv_{envel} \quad (16)$$

$V_{multilevel}$ is a function of the envelope that is being reproduced and using equation similar to (1)-(8) it is possible to optimize the number of voltage levels and their voltage distribution [7].

C. *Optimization*

The envelope amplifier in this section was optimized with the same 64QAM signal, as in the previous section. The results are presented in Figure 15. It is important to notice that because of the high PAPR of the envelope the equidistant voltage distribution is not the best one. Using optimized voltage levels, the power losses can be decreased up to 26% (in the case of three voltage levels). Depending on

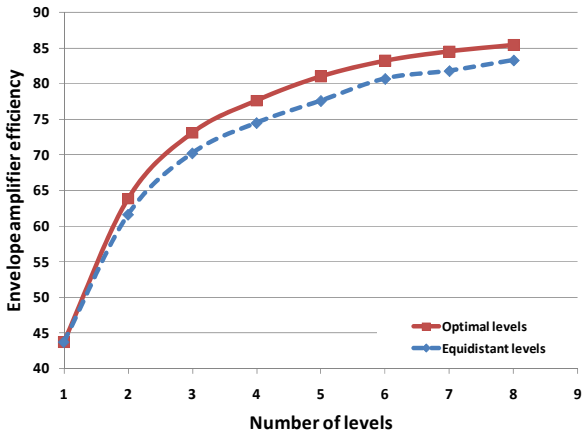

Figure 15. Efficiency of the envelope amplifier when it is implemented with optimized and equidistant votlage levels

the envelope distribution of the transmitted signal this difference can be lower or higher. For example in [7] the difference between the equidistant and the optimized voltage distribution was as high as 6%. If the number of levels is even more increased, the efficiency curve will start to fall

IV. COMPARISON

The envelope amplifier based on the multilevel converter can have a higher efficiency than a buck converter in parallel with a linear regulator for, approximately 10%. However, the envelope amplifier based on parallel linear-assisted buck converter has significantly lower complexity and higher robustness (lower number of components). For example, for the same efficiency of the envelope amplifier of 70-75%, the buck converter needs two transistors and one driver, but the multilevel needs six MOSFETs and three drivers. The maximum efficiency of the parallel architecture is limited because, as it is explained, there is always maximum efficiency that can be obtained even with ideal switching converter with no losses. The reason for that is the low dynamics of the buck converter, and the power losses come from processing the high dynamic part of the envelope. On the other hand, the efficiency of the envelope amplifier based on the multilevel converter depends on how close the voltage levels are to the output voltage and how big is the minimum voltage drop on the linear regulator's transistor. Unfortunately, in this case there is a trade-off between the desired efficiency and complexity (number of levels).

For both presented architectures, it is implicitly accepted that the voltage supply sources are available. However, normally, there is only one voltage source for the complete system that has to be used to generate all the needed voltages. The architecture that employs a buck converter in parallel with a linear regulator needs two voltage sources (one positive and the other negative), while the architecture based on *N* voltage cells needs *N* voltage supplies (isolated one from each other). Having in mind that the main voltage source can be a battery (in the case of mobile devices) or the electrical network (in the case of base stations) the solutions that have to produce the needed voltage sources can differ a lot and due to that reason the efficiency of this stage is not taken into account in this analysis. Nevertheless, for the well-specified application complete energy path from the principal voltage source to the RF PA should be taken into account when the optimization is performed.

V. CONCLUSIONS

In this paper a theoretical anal analysis and optimization methodology for the envelope amplifiers based on a switching converter and a linear regulator in parallel or series is presented. The optimization process is conducted in order to obtain the highest possible efficiency in the system having in mind the properties of the transmitted RF signal. For the parallel architecture it is shown that there exists an efficiency limit due to the fact that the linear regulator always has to process certain part of energy with low efficiency (due to low dynamics of the buck converter), while in the case of serial architecture the efficiency is due to the power losses in the multilevel converter. The analysis has shown that the envelope amplifier based on a multilevel converter and a linear regulator in series has higher efficiency of, approximately 10%, but the price for its higher efficiency is higher complexity.

REFERENCES

[1] H. Chin; D.F. Kimball, S. Lanfranco, P.M: Asbeck, "Wideband high efficiency digitally-assisted envelope amplifier with dual switching stages for radio base-station envelope tracking power amplifiers,"Microwave Symp. Digest (MTT), 2010 IEEE MTT-S International , May 2010

[2] J. Moon, J. Son, J. Kim, I. Kim, S. Jee, Y.Y. Woo, B. Kim, "Doherty amplifier with envelope tracking for high efficiency" IEEE MTT-S International Microwave Symp. Digest May 2010

[3] M. Vasic, O. Garcia, J.A. Oliver, P. Alou, D. Diaz, J.A. Cobos, A. Gimeno, J.M. Pardo, C. Benavente, F.J. Ortega, "High efficiency power amplifier for high frequency radio transmitters," IEEE APEC, Feb. 2010

[4] M. Hoyerby, M. Andersen, "Ultrafast Tracking Power Supply with fourth-Order Output Filter and Fixed-Frequency Hysteretic Control", IEEE Trans. on Power Electronics, Vol.23, Issue: 5, 2008,

[5] V. Pinon, F. Hasbani, A. Giry, D. Pache, C. Gamier, "A Single-Chip WCDMA Envelope Reconstruction LDMOS PA with 130MHz Switched-Mode Power Supply," IEEE International Solid-State Circuits Conf., ISSCC 2008. Feb. 2008

[6] V. Yousefzadeh, E. Alarcon, D. Maksimovic, "Efficiency optimization in linear assisted switching power converters for envelope tracking in RF power amplifiers",IEEE Intern.Symp.on Circuits and Systems,ISCAS 2005

[7] M. Vasic, O. Garcia, J.A. Oliver, P. Alou, D. Diaz, J.A: Cobos, "Multilevel Power Supply for High-Efficiency RF Amplifiers," IEEE Transactions on Power Electronics, on , vol.25, no.4, pp.1078-1089, April 2010

[8] P.F.Miaja, M.Rodriguez, A.Rodriguez, J.Sebastian, "A linear assisted DC/DC converter for Envelope Tracking and Envelope Elimination and Restoration applications," Energy Conversion Congress and Exposition (ECCE), 12-16 Sept. 2010

[9] J.T. Stauth, S.R. Sanders, "Optimum Bias Calculation for Parallel Hybrid Switching-Linear Regulators," Applied Power Electronics Conference, APEC 2007 - Twenty Second Annual IEEE Feb. 2007

[10] L. Goergens , J. Schoiswohl and M. Paolucci, "Advanced Design for Fast Switching Power MOSFETs", Professional Education Seminar, APEC 2011