Solution-processed organic devices developed by a novel cost-effective patterning technique based on electrical erosion

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***Abstract*— Application of arc erosion to the patterning of metallic contacts in organic devices is presented. A home-made systems and details of the working principles are described. Advantages and drawbacks of this novel technology are discussed.**

Keywords-component: arc erosion, electrical discharge, organic devices.

I. INTRODUCTION

From the past few years organic electronics industry stands at the brink of achieving large-scale mass production. Some of the key challenges going forward still reside with materials or device development, but manufacturing equipment or processes are receiving major attention. Initiatives in this line focus on solution-processing [1,2], large area deposition techniques and the use of flexible substrates.

There is agreement that roll-to-roll (R2R) technology is the best candidate to achieve these goals [3], and those patterning techniques compatible with R2R such as jet-printing [4], laser ablation [5] or imprint-lithography [6] are showing a huge development.

In this work we propose the use of arc-erosion as a novel patterning technique for conductive materials, which may overcome some drawbacks shown by the above mentioned techniques. This technique is generally dry and quick, saves many of the typical photolithographic steps and is believed to be compatible with a R2R system.

II. EXPERIMENTAL SETUP

For that purpose a home-made setup was built, including a steel (or tungsten) tip attached to a spring and mounted on a methacrylate support to ensure electrical insulation This probe is in turn attached to a PC-controlled, high precision XYZ micropositioner (Fig. 1). A pattern is designed with a vector-graphic design software, the resulting file is translated by the electronic controller, and engraved in the sample. Motion along each axis is carried out by a high precision PLS-85 MICOS linear stage, provided with a 2-phase stepper motor together with a closed loop system that improves accuracy and repeatability to about 1µm. The steel tip diameter determines the resolution. Commercial, 50 µm diameter tips have been used in this experiment. The maximum still speed provided by our system is 15 mm/s and working area is 10×10 cm^2. It will be shown that despite particular limitations of this prototype, the physical limit for the working speed may be very high (hundreds mm/s).

III. RESULTS AND DISCUSSION

The tip slides in contact with a conductive surface while applying a continuous small voltage. As the tip slides onto the surface, it leaves an insulating path of a similar width as the tip diameter (Fig. 2), which determines the resolution. If this path depicts a closed loop the inner region is insulated from the outer one. Thus, it allows making tracks and pads over those materials usually employed as electrodes in organic electronics, such as indium tin oxide (ITO), gold or aluminium.

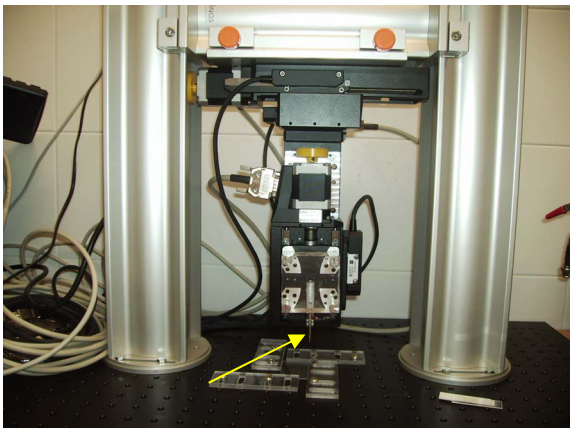

Figure 1. Experimental set up for arc-erosion patterning consisting of a computer-assisted XYZ micro-positioner. Yellow arrow marks the probe tip.

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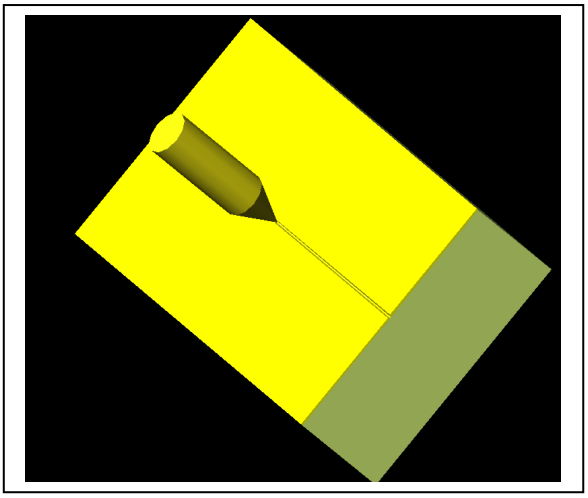

Figure 2. Sketch of a electrically biased tip sliding in contact with a conductive surface, leaving an insulating path of a similar width as the tip diameter.

This technique resembles electro-discharge-machining (EDM), which is widely used in industry for high accuracy cutting or shaping metals [7]. EDM works by applying high voltage pulses (thousands volts) between electrode and a metal piece in order to create arcs which erode the material by a thermo-electrical process. But, in contrast, we have implemented a system working efficiently with a continuous low voltage (around 10 V).

The operation principle of this technique lies in the creation of a sequence of very short electrical discharges, few tenths of µs long, during the tip motion. When a biased tip approaches an electroconductive material, at a sufficiently short distance the electric field between tip and material reaches the value for air breakdown, and a spark is generated. A small resistor (0.5 ohm) in series with the tip allows monitoring the currents involved, which resulted of several amps.

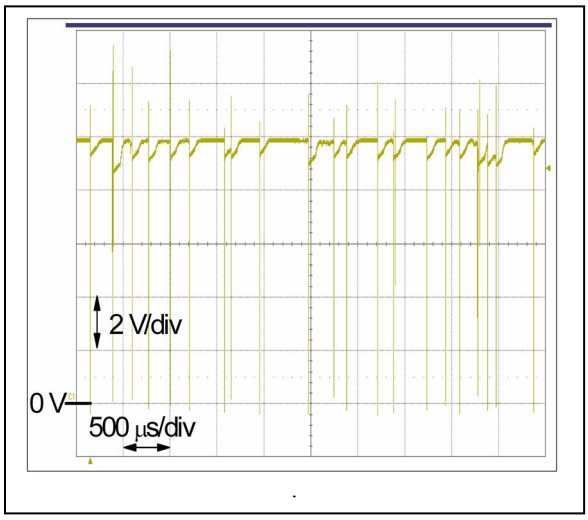

Figure 3. Monitored voltage at the tip during motion. The falls mean discharge processes. Tip speed was 1 mm/s, so a time division is equivalent to a 500 nm path.

Despite the power supply is protected against short-circuits with a current limitation stage, it includes a bypass capacitor (around 220 µF) at the output to filter high frequency signals. This capacitor may act as a charge supplier at a very high rate because it results directly connected to the tip via a low resistance path.

This electrical discharge is observed to remove or break material in the region underneath, creating an insulated zone around the tip (crater). This region holds an open circuit when the tip comes into contact with the surface. From this situation, as the tip resumes motion in the horizontal direction and approaches the boundary of the conducting region, a new spark will generate, and so on. As a result, the tip is leaving an insulating path during trip. Fig. 3 shows an oscilloscope screen capture, monitoring the voltage between tip and a Au(80 nm)/glass substrate over a time window of 5 ms. Tip speed was 1 mm/s. Reference bias voltage is 8 V. The sharp voltage falls down correspond to discharges. Subsequent monitoring revealed high-to-low transients lower than 50 ns.

The maximum tip speed for patterning is therefore determined by the recharge time of the capacitor and the diameter of the crater around the tip, i. e., capacitor should recharge in the interval taken for the tip to arrive to the next conductive region. Since external circuitry may be arranged to recharge capacitor in few microseconds (see Fig.3) and the diameter of the eroded region may exceed that of the tip by only a few micrometers, the operating speed may easily achieve tens cm/s. This range is comparable or higher than that used by ink-jet printing, and supports scalability of this technique.

It has been observed a correlation between crater diameter and operating voltage, in such a way that crater diameter grows with increasing voltage. This may lead to an undesirable waviness of paths, that is considered a disadvantage of the technique. On the other hand, there exists a voltage limit below which no material erosion is observed. These effects must be taken into account in order to decide the optimal working voltage. Table I summarizes the bias voltage used to erode different combinations of materials and substrates. They should be understood as the minimum voltage range at which we have obtained the best quality of paths.

TABLE I. OPTIMAL WORKING VOLTAGE USED FOR MATERIALS AND SUBSTRATE

Material	Bias (V)
ITO/glass	11-12 V
ITO/PET	2-3 V
Au/glass	6-8 V
Au/Cr/glass	9-10 V
Al/glass	1.5-3 V
Al/PET	1-1.5 V

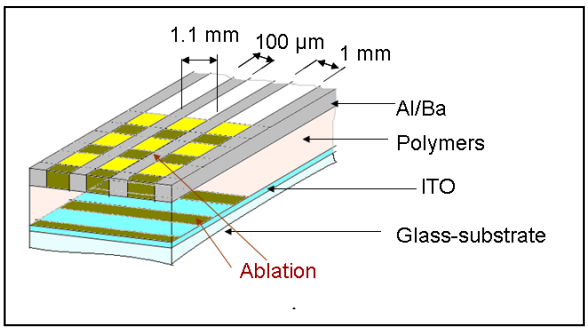

Figure 4. Layer structure and contact patterning (rows and columns) performed for a OLED-based passive matrix .

These results open the possibility of eroding stacked layers selectively. As an application, a 6 ×6 passive matrix of organic light emitting diodes (OLED) have been developed on electrodes (ITO for the anode and Al/Ca for the cathode) patterned with our technique (Fig. 4). A passive matrix structure is particularly suitable for this technique since damage on the active polymer layers is created in those paths around the pixels, where it does not matter performance.

Anode patterning (display columns) has been previously performed at 10.5 V. Next, PEDOT:PSS (50 nm) and an electroluminescent, commercial derivative of polyfluorene (PFO) (80 nm) have been spin-casted. Finally, a 150 nm thick Al layer has been evaporated on top of a thin Ba layer (few nm), in an inert atmosphere chamber. Finally, the display rows have been patterned on the Al/Ba cathode at 3 V. As expected, no damage on the ITO has been detected.

Fig. 5 shows a picture of the final device where the tracks structure in the cathode is slightly observed. Fig. 6 shows the current-voltage response recorded from a typical pixel. The noticeable leakage current may be preliminary attributed to crossing effects between adjacent pixels.

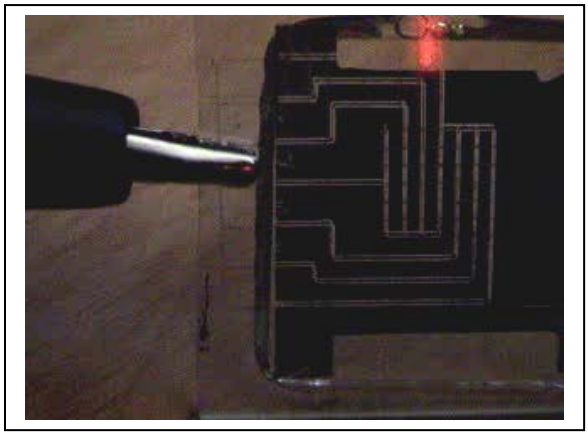

Figure 5. 6x6 passive matrix alphanumeric display prototype performed by arc-erosion technology. Patterning of the top cathode (Al/Ba) was carried out without damaging the bottom ITO anode pattern due to the different operating voltages to get the erosion.

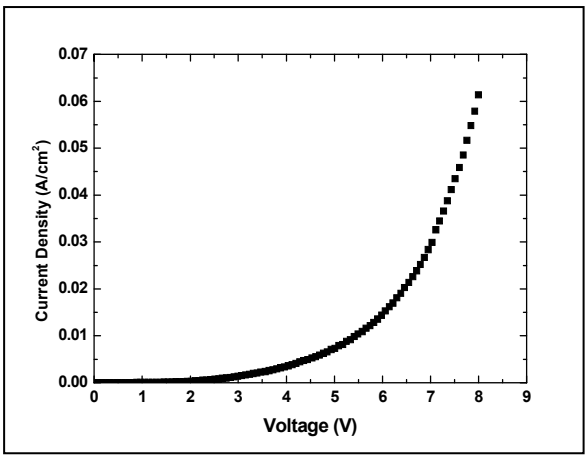

Figure 6. Current – voltage characteristic of a typical OLED of the passive matrix

IV. CONCLUSIONS

We have proposed a technique based in arc erosion in order to perform patterns on conductive materials, with straight applications in organic devices. Although arc erosion is a widely used procedure in metals industry, the way of applying this principle to organic devices is novel. This technique results easily scalable and may be considered as an alternative patterning technique compatible with a R2R production line, the speed and throughput being similar to those obtained by other printing techniques. Details of the procedure are currently subject of a spanish patent (P201030276).

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