Temperature-dependent high-frequency performance of deep submicron AlGaN/GaN HEMTs

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A study of the low temperature DC and RF performance of deep submicron AlGaN/GaN high electron mobility transistors (HEMTs) is reported. From 300 K to 100 K both extrinsic transconductance and drain current increase by ~30%, mainly due to the lowering of the optical phonon scattering that allows higher electron mobility. Source and drain resistances improve too, which contributes to the 15-20% increase of $f_t$ and f_{max}. The low temperature small signal model has also been extracted accurately at every 50 K. Inductances and capacitances remain constant in the range of temperatures measured. The intrinsic transconductance can be also considered temperature independent, but the output conductance decreases from 300 K to 100 K indicating a better confinement of the 2DEG. The HEMT performance obtained at 100 K can be reached at room temperature by reducing the parasitic resistances and improving the GaN buffer isolation.

1 Introduction AlGaN/GaN high electron mobility transistors (HEMTs) are being used in monolithic microwave integrated circuits (MMIC) for power applications at X band and above for the last few years . They take advantage of some interesting properties of III-nitrides, such as their intense piezoelectric fields, high breakdown field and saturation velocity, and good thermal conductivity, to provide high power at increasing frequencies and harsh environments. To fully understand the HEMT performance from a thermal point of view, a complete characterization of the devices should be done over a wide range of temperatures. For high temperatures (HT), Lee and Webb reported a temperature dependent nonlinear model on a 0.35 μm gate length device from 300 K to 423 K On the other hand, Nidhi has studied the impact of access resistance on HEMTs with high frequency performance for cryogenic temperatures This work completes the study at low temperatures (LT) by means of extracting the small signal model from 300 K down to 100 K at every 50 K.

2 Experimental $Al_{0.33}Ga_{0.67}N$/GaN HEMTs with 20 nm barriers were grown by metal-organic chemical vapour deposition (MOCVD) on SiC. A 0.6 nm AlN interlayer between the buffer and the barrier was used to improve the 2DEG transport properties. In order to achieve a non-alloyed low resistance ohmic contact ($R_c \approx 0.2$ Ω·mm), Si ions were implanted into the source and drain regions and then activated by annealing the sample at ~1280 °C in a MOCVD system with a N_2 and NH_3 ambient The sample was then passivated by SiN_x and a sacrificial Ge layer was deposited to decrease parasitic capacitances. Submicron gates were defined by e-beam lithography and dry-etched through the Ge and SiN_x layers. The gate region was treated by fluorine plasma for 10 minutes to decrease the gate leakage, and the AlGaN layer recessed by chlorine to improve the transconductance. Transistors have a gate length ~150 nm with gate-source spacing (L_{GS}) of 0.3 μm and drain-gate spacing (L_{DG}) of 1.1 μm. Gate widths are of 100 μm or 150 μm. The sheet carrier density (n_s) and Hall mobility (μ_H) were $1.1 \cdot 10^{13}$ cm^{-2} and 2000 cm^2/V·s.

S-parameter measurements from 300 K to 100 K were carried out using a cryogenic high frequency probe station, composed of a liquid nitrogen cooled wafer stage and a heater to control the temperature. The station was connected to an Agilent PNA E8361A network analyzer for the RF measurements and to an Agilent 4155B parameter analyzer for the DC characterization. For the on wafer RF measurements from 1 GHz up to 40 GHz, the electrical reference plane was established by an "off-wafer" LRRM calibration at each temperature.

3 Results and discussion Both drain cut-off current (I_{DSS}) and extrinsic transconductance ($g_{m,ext}$) increase around 30% from 300 K to 100 K as shown in Fig. 1, up to maximum values of 0.99 A/mm and 0.62 S/mm, respectively. This behaviour is related with the higher electron mobility in the 2DEG as devices are cooling, due to the reduction of the polar optical phonon scattering. This mechanism is dominant at 300 K, but becomes negligible as temperature decreases. At 100 K other types of scattering such as the alloy disorder are predominant with a temperature independent behaviour. Thus, the improvement in the HEMT performance saturates for T < 150 K.
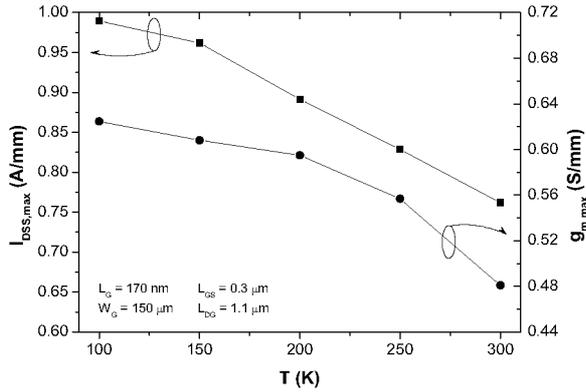

Figure 1 Maximum of drain current at V_{GS} = 0 V and extrinsic transconductance at V_{DS} = 8 V from 300 K to 100 K.
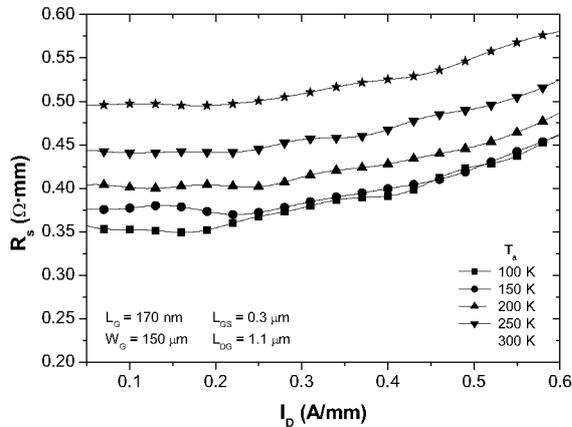
Figure 2 R_S for different drain currents. At each T, the minimum of R_S is obtained in the low field region for I_D < 0.2 A/mm.

The source resistance (R_S) has been extracted from specific DC measurements   For transistors with L_{GS} = 0.3 μm and L_{DG} = 1.1 μm, R_S decreases from 0.49 Ω·mm at 300 K to 0.35 Ω·mm at 100 K as is shown in Fig. 2. Drain resistance (R_D) can be also calculated as the difference between the on-resistance (R_{on}) and R_S, extracting R_{on} from the slope of the lineal region in I_D vs V_{DS} curves at low V_{DS}. For the same devices, R_D varies from 1.15 Ω·mm at 300 K to 0.65 Ω·mm at 100 K.

The measurements of the S-parameters allow the extraction of the current-gain (f_T) and power-gain (f_{max}) cut-off frequencies and the equivalent circuit parameters (ECPs). The f_T and f_{max} are estimated from $|h_{21}|^2$ and the unilateral power gain (U), respectively, assuming a 20 dB/decade linear decrease. As shown in Fig. 3, f_T increases ~16% from 300 K to 150 K, and stabilizes down to 100 K. The maximum of f_T occurs approximately at the same I_D for all temperatures under study   The f_{max} follows a similar evolution than f_T, increasing ~21% from 129 GHz at 300 K to 156 GHz at 100 K. Both f_T and f_{max} increases are related with the improvement of the parasitic resistances (R_S and R_D) as devices are cooled.
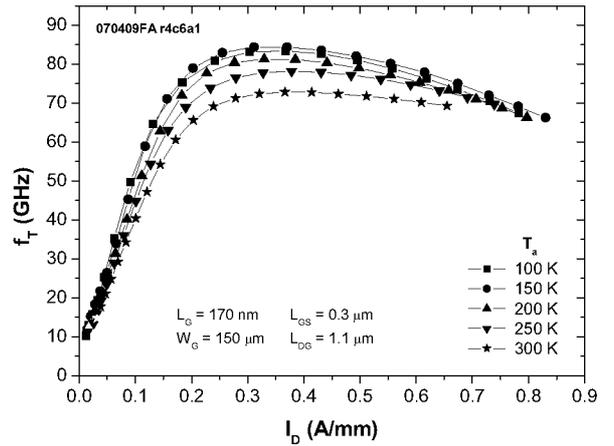

Figure 3 Evolution of f_T for different drain currents. The peak of f_T occurs at the same approximate I_D (0.3 to 0.4 A/mm) for all temperatures under study.

The small signal model has been extracted and simulated at different bias by means of ADS software. The equivalent circuit used was proposed by Dambrine et al.

The extrinsic resistances R_s and R_d have been previously calculated, and R_g is set as 1/3 of the gate metal strip resistance. From pinched HEMT measurements, extrinsic capacitances C_{pg} and C_{pd} are obtained. The extrinsic inductances L_s, L_g and L_d are calculated from cold measurements (V_{DS} = 0 V and V_{GS} ≈ 2 V)   Next, the intrinsic circuit parameters are deduced following   The equivalent circuit is simulated and fitted to achieve a good agreement between model and measured characteristics, especially for frequencies between 1 to 20 GHz (see Fig. 4). Inductances and capacitances for the extrinsic circuit are supposed constant with temperature. Regarding the
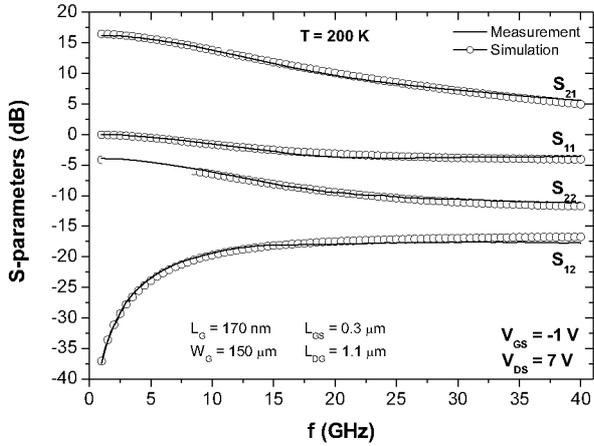
Figure 4 Comparison between the S-parameters measured with the network analyzer and simulated by ADS from the small signal equivalent circuit.
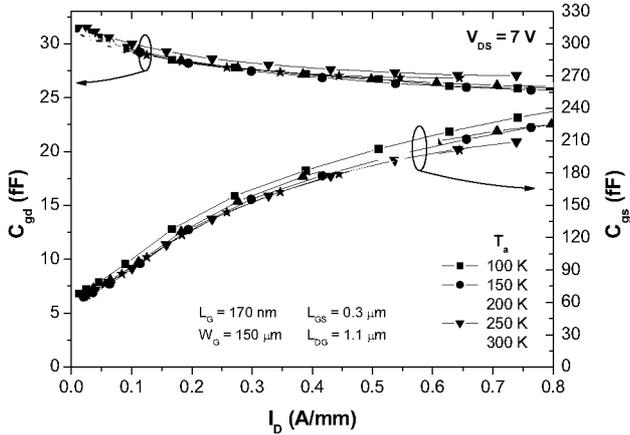
Figure 5 C_{gd} and C_{gs} temperature evolution for $V_{DS} = 7$ V with V_{GS} bias between -2 V and 0 V.

intrinsic circuit, all parameters have been calculated for different I_D (keeping V_{DS} constant). C_{gs} and C_{gd} can be considered temperature independent, since their variations are lower than 7%, as shown in Fig. 5.

In addition, the intrinsic transconductance ($g_{m,int}$) is almost constant with T, so $g_{m,ext}$ mainly depends on R_S as:

$$g_{m,ext} = \frac{g_{m,int}}{1 + R_S \cdot g_{m,int}}$$

The output conductance (g_{ds}) decreases ~30% as devices are cooled from 300 K to 100 K, likely due to a better confinement of the electrons in the heterostructure (see Fig. 6). In fact, simulations of the electron density across the transistor show that redistribution of the electrons in the AlGaN/GaN interface when the temperature is lowered (inset to Fig. 6), suggesting an improvement of the isolation of the GaN buffer.

Other intrinsic parameters (C_{ds}, R_i or τ) do not show a clear changes at low T.
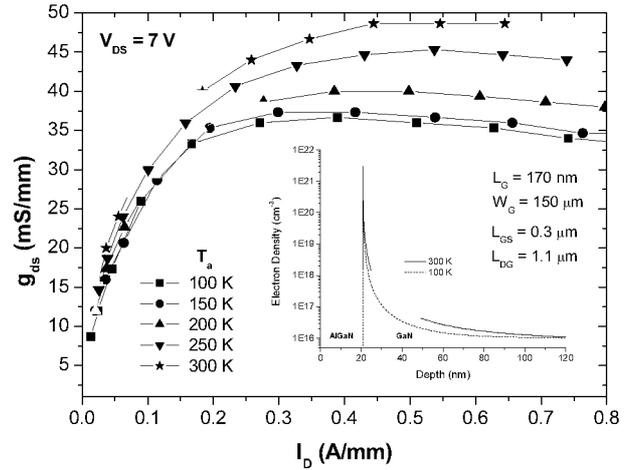
Figure 6 Output conductance evolution from 300 K to 100 K for different drain currents. In the inset, electron density simulations show that low temperatures improve the 2DEG confinement.

4 Conclusion Low temperature measurements allow the determination of the dominant limiting factors of the HEMT performance. From 300 K down to 100 K, R_S and R_D experience a clear decrease above 40 %, which improves not only the DC performance (I_D and $g_{m,ext}$) but also f_T and f_{max}.

Every 50 K the ECPs of several transistors have been extracted in an accurate way. Apart from the parasitic resistances behaviour, g_{ds} shows a significant reduction at low temperatures. This fact suggests a better buffer isolation, as also confirmed by the decrease of leakage currents and by the better 2DEG confinement deduced from simulations. Other parameters ($g_{m,int}$, τ, C_{gd}, C_{gs}) from the small signal model seem to be rather constant with temperature for this type of deep gate transistors.

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