

Current Self-balance Mechanism in Multiphase Buck Converter

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Abstract— Some of the recent applications in the field of the power supplies use multiphase converters to achieve fast dynamic response, smaller input/output filters or better packaging. Typically, these converters have several paralleled power stages with a current loop in each phase and an unique voltage loop. The presence of the current loops is necessary to increase dynamic response (by using current mode control) and to avoid current unbalance among phases.

The purpose of this paper is to demonstrate that in CCM, with a proper design, there is an intrinsic mechanism of self-balance that helps a lot in avoiding the current unbalance. Thus, in the buck converter, if natural ZVS is achieved in both transitions, the instantaneous inductor current compensates partially the different dc current through the phases.

The need for using n current-loops will be finally determined by the application but not by the converter itself. Using the buck converter as a base, a multiphase converter has been developed. Several tests have been carried out in the lab and the results show clearly that, when the conditions are met, the phase currents are very good balanced even during transient conditions.

I. INTRODUCTION

Interleaving technique was proposed long time ago [1-2]. In the last years, some applications make use of this technique to improve the performance of the dc-dc conversion. Dynamic response of VRMs is improved with it [3-4]; also, automotive 42/14V systems use it to reduce the size of input and output capacitors [5-7]; and other applications take advantage of this technique to improve a particular characteristic [8]. Most of the published papers regarding multiphase converters include a current loop in each phase to achieve two objectives:

- Improve dynamic response: by using a current mode control, a higher bandwidth can be achieved
- Balance the phase currents: dc currents differences are restored by the control

Each current loop needs several components increasing the cost of the power supply. Due to this, the number of phases is limited to 3 to 5 typically. Commercial ICs have been recently developed [9-10] to offer a compact solution. Moreover, multiphase converters allow bandwidths near $M \cdot f_s$ (M times the switching frequency) being M the number of phases [11].

However, there are many applications that do not require a very fast dynamic response, being possible to get rid of current loops. In CCM (Continuous Conduction Mode), the current unbalance depends mainly on duty cycle differences and parasitic resistance [12]. In most cases these parameters are

under certain limits allowing the operation of the converter without the aforementioned current loops. Since the duty cycle is the main responsible of the current unbalance, it is especially important the use of digital control that reduces the inequalities of the driving signals of the power MOSFETs. The use of a high number of phases together with digital control without current loops have been used successfully [13] in static conditions.

The objective of this paper is to propose a design for the power stage in CCM that improves the current balance without using current loops. If this were possible, designs with a high number of phases would become a realistic option in some applications.

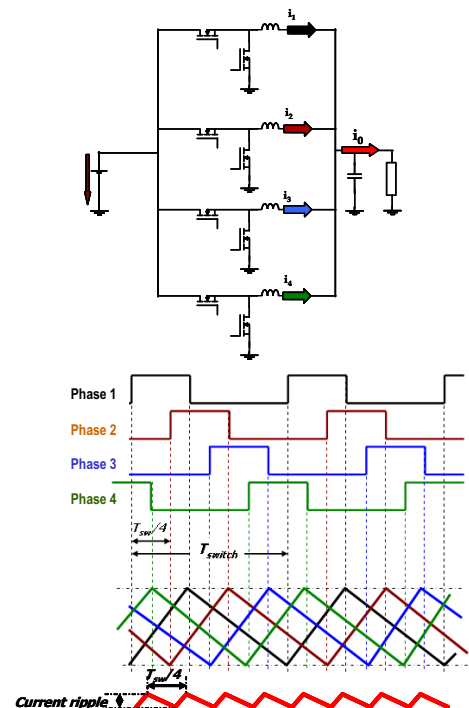


Figure 1.- Power stage of a 4-phase buck converter and main waveforms in steady-state conditions

II. PROPOSED DESIGN

Figure 1 shows the power stage of a 4-phases synchronous buck converter and its main waveforms. The main advantage of this approach is that phase currents are cancelled obtaining

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advantage in filter reduction and dynamic response (because L can be reduced).

Including a current loop is relative expensive because of the required electronic circuitry (sensor or resistor plus differential amplifier or current transformer) and a more complex control (M current loops). Therefore, the use of a high number of phases is not cost effective. The fact of having M current loops limits the existence of multiphase converters with a high number of phases. If current loops are not included, it is necessary to oversize all the phases to foresee certain current unbalance, depending on some parameters, especially parasitic resistance and duty cycle [11], in CCM (continuous conduction mode).

An interesting option that helps to reduce current unbalance is to design the converters with a phase current ripple higher than twice the average current value ($k > 200\%$), as shown in figure 2b (compared to fig. 2a that represent the typical design). This option is only possible if the buck converter is synchronous. Note that although there is a higher current ripple per phase, the interleaving technique considerably reduces the current ripple at the output. Moreover, if the number of phases of a multiphase converter were high, the waveforms tend toward this particular design because the average dc current per phase is small. There are some advantages of this design:

- Current balance is better (it will be explained in the next section)
 - There is natural Zero Voltage Switching (ZVS) in both transitions. This is an important advantage compared with the traditional design
 - Smaller inductance per phase.
- On the other hand there is an important disadvantage:
- Higher conduction losses caused by a higher rms current.

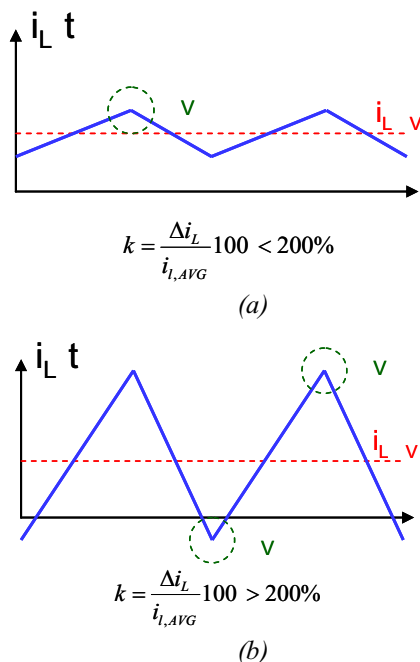


Figure 2 .- Current phase and parameter k for two different designs: (a) small current ripple ($k < 200\%$) and (b) high current ripple ($k > 200\%$)

Therefore, the application of this technique depends on the weight of conduction and switching losses of the converter. Note that for high switching frequency converters with many phases (small average current per phase), switching losses can be more important than conduction losses.

III. SELF-BALANCE OF THE PHASE CURRENTS

Each buck converter has two switches (see figure 3): the one that connects the input to the inductor (high side MOSFET or HSM) ; and the one that connects the inductor to ground (low side MOSFET or LSM). ZVS is achieved naturally in the turn-on of LSM with a proper timing of the gate signals of these transistors. In typical designs, the turn-on of the HSM is dissipative since the inductor current is always positive and there is no way to charge/discharge the parasitic capacitances. In case of designing the converter to have negative current in that transition, ZVS is achieved, with a similar mechanism. It will be seen that this also helps to improve the current balance without current loops.

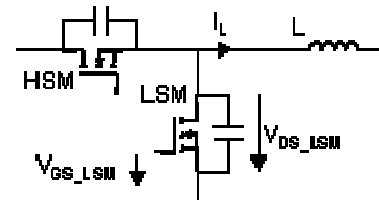
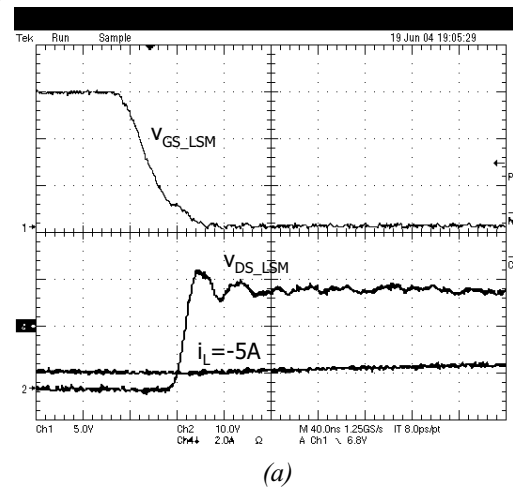
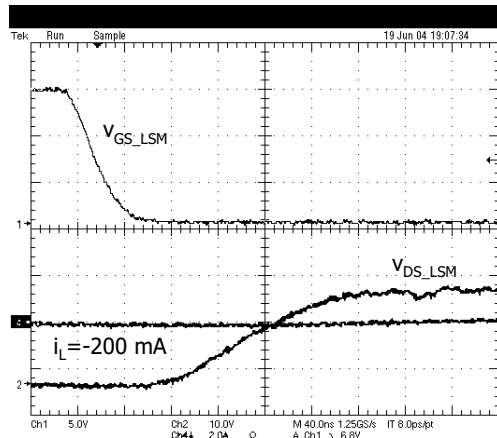


Figure 3 .- Power transistors and inductor of the synchronous buck converter. Parasitic capacitances have been drawn

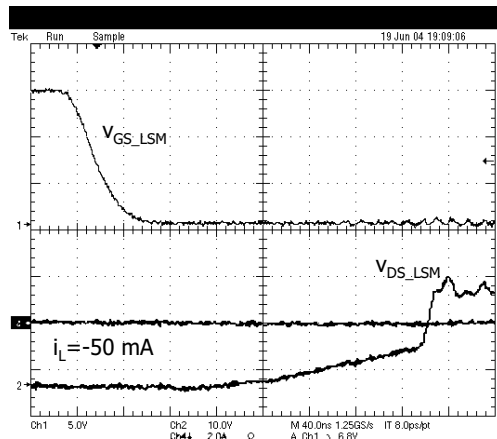
To explain the auto-balance of the currents, several images of the turn-off of the LSM taken with the oscilloscope are shown in figure 4. In four different conditions, V_{GS_LSM} , V_{DS_LSM} and i_L are shown.

When the turn-on of HSM takes place with ZVS, the speed of the charge/discharge of the parasitic capacitances is determined by the instantaneous inductor current and not by the gate-source signal of HSM. Therefore, a more (instantaneous) negative current produces a quicker transition increasing the voltage-second balance on the inductor and then increasing the average inductor current. This mechanism tries to compensate current unbalances since the phase with the smallest dc current, polarizes more its inductor and, as a consequence, the dc current is increased.

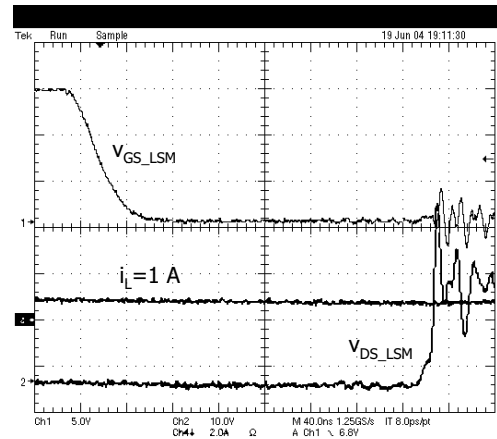




(b)



(c)



(d)

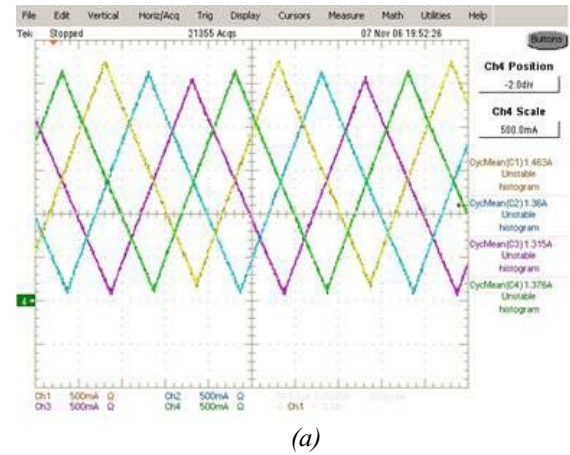
Figure 4.- Gate to source voltage of the LSM (5V/div), drain to source voltage of the LSM (10V/div) and inductor current (2A/div) for four different instantaneous inductor currents: (a) -5A (b) -0.2A (c) -0.05A (d) +1A

Figure 4d shows the V_{DS_LSM} voltage with no ZVS because instantaneous inductor current is positive (case of figure 2a). In the other three cases fig 4a, 4b and 4c, there is ZVS. It can be clearly seen that the higher the negative current, the shorter the switching interval (around 40 ns in fig.4a).

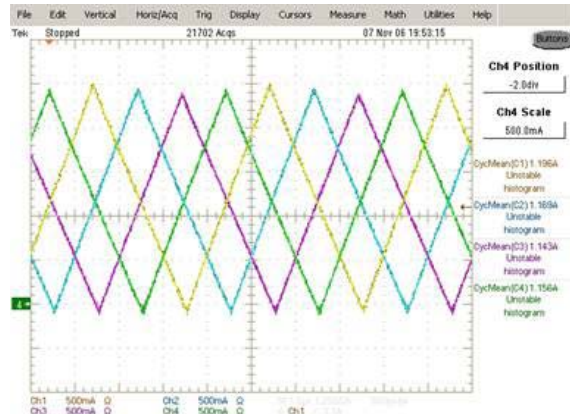
On the other hand, the smaller (but negative) the instantaneous current, the higher the switching interval. This is a well-known issue but the important thing is that this fact helps to compensate different dc currents in a multiphase converter. Thus, the phase with the most negative current changes its inductor voltage faster and, therefore, it tries to increase its average current value. The experimental results shown in the next section will help to understand this.

IV. EXPERIMENTAL VERIFICATIONS

A 4-phases synchronous buck converter without current loops has been built and tested. The main specifications are: $V_{IN}=28V$; $V_O=12V$; $P_O=60W$; and $f_s=250kHz$. The inductor has been designed to obtain a current ripple higher (but close) to 200% of the average phase current (current ripple equal to 2.5A being 1.25A the average phase current). In this condition, the instantaneous phase current is negative once the LSM is opened. Figure 5 shows the phase currents for $I_O=5.5A$ ($k<200\%$) and 4.7A ($k>200\%$). Note the position of the cursor pointing to zero current level.



(a)



(b)

Figure 5.- Current phases (a) with $k<200\%$ and (b) with $k>200\%$

In both cases, the currents are well balanced mainly because a digital control has been used, so there is high accuracy in the timing of the driving signals. However, if the current ripple is so high that there is negative current in the turn-off of the LSM, the balance is improved. In table I we can see that, with this design, phase #1 improves from +6% overcurrent to +3%.

Table I.- Measurements of dc currents for current ripple smaller ($k < 200\%$) and higher ($k > 200\%$) than twice the dc current

	$K < 200\%$		$K > 200\%$	
	DC PHASE CURRENT	% OVER THE AVERAGE	DC PHASE CURRENT	% OVER THE AVERAGE
PHASE #1	1.46 A	+ 6%	1.19 A	+ 3%
PHASE #2	1.36 A	- 1%	1.16 A	0 %
PHASE #3	1.31 A	- 5%	1.14 A	- 2%
PHASE #4	1.37 A	0%	1.15 A	- 1 %

To test the goodness of this design, an external 0.5% extra duty cycle has been applied to phase #4 (the control is implemented in a FPGA and this can be done easily). Note that differences in the duty cycle are the main responsible for current unbalance. Figure 6 and table II show the result of this experiment.

If $k < 200\%$ there is an obvious current unbalance, forcing to a 67% overcurrent in the phase this extra duty cycle (note that 0.5% duty cycle unbalance is a realistic value for many analog controllers). Of course, this result is not acceptable. However, designing with $k > 200\%$, the current unbalance is still very good even with this extra duty cycle (see figure 6b).

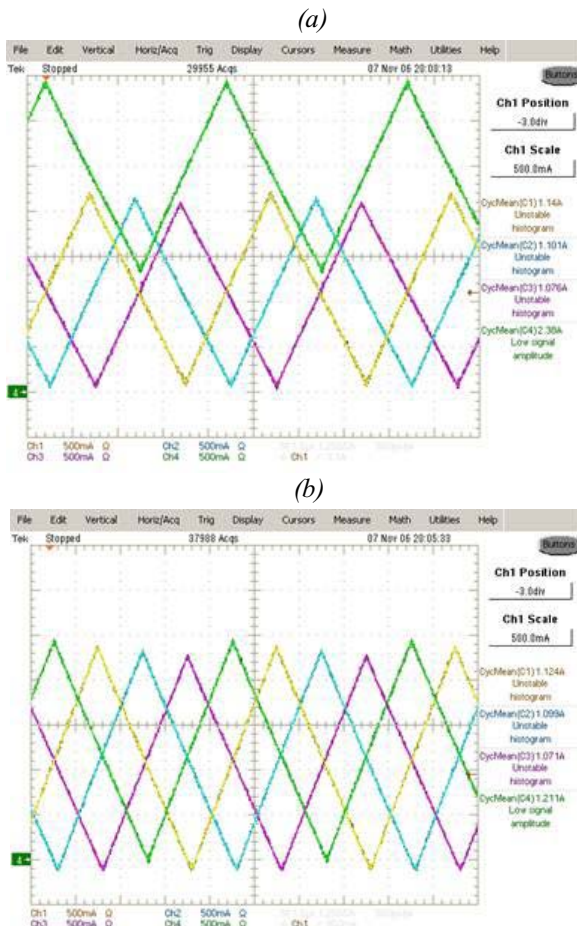


Figure 6.- Current phases (a) with $k < 200\%$; (b) with $k > 200\%$ introducing an extra 0.5% duty cycle in phase #4

Table II shows that phase #4 handles only 8% extra current, being the converter well balanced even when there is a large duty cycle unbalance. Measurements about actual V_{GS} duty cycles are also shown.

Table II.- Measurements of dc currents for current ripple smaller ($k < 200\%$) and higher ($k > 200\%$) than twice the dc current introducing an extra 0.5% duty cycle in phase #4

0.5% EXTRA DUTY CYCLE IN PHASE #4	MEASURED DUTY CYCLE	$K < 200\%$		$K > 200\%$	
		DC PHASE CURRENT	% OVER AVERAGE	DC PHASE CURRENT	% OVER AVERAGE
PHASE #1	46.82%	1.14 A	- 20%	1.12 A	+ 0%
PHASE #2	46.79%	1.10 A	- 23%	1.09 A	- 3%
PHASE #3	46.75%	1.07 A	- 25%	1.07 A	- 5%
PHASE #4	47.24%	2.38 A	+ 67%	1.21 A	+ 8 %

Additional experiments have been carried out introducing a much higher extra duty cycle in phase #4. Waveforms with $k > 200\%$ are shown in figure 7. As it can be seen, the current balance is still very good. In worst case, with a 2% extra duty cycle, phase #4 only carries +11% overcurrent. From these experiments, it can be concluded that designing with $k > 200\%$ improves the current balance in multiphase converters.

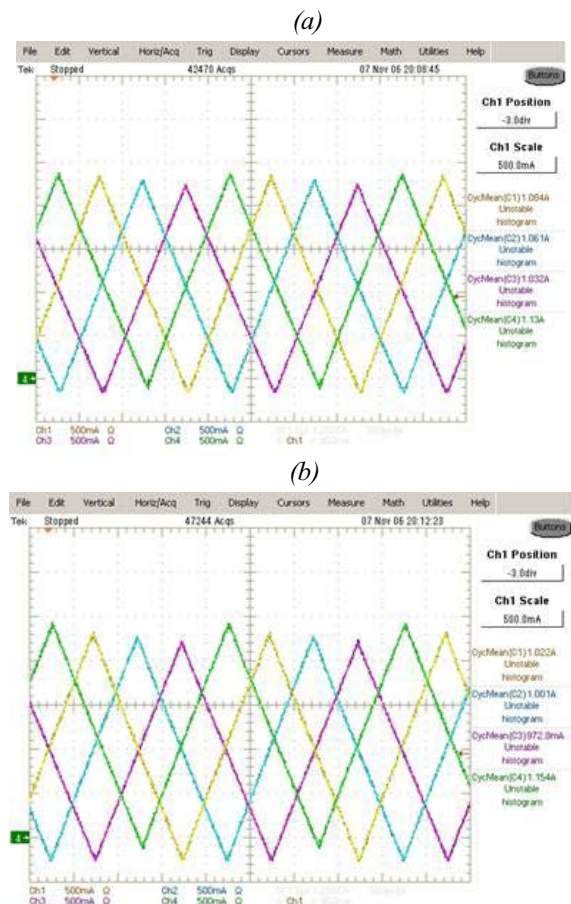


Figure 7.- Current phases for $k > 200\%$ introducing an extra (a) 1% duty cycle and (b) 2% duty cycle in phase #4

V. CONCLUSIONS

Multiphase buck converters have one current loop per phase to achieve current balance and high dynamic response. However, with a proper design, those current loops can be removed allowing cost-effective converters with a high number of phases. Designing with a current ripple higher than twice the average phase current, two important issues are achieved: better current balance and ZVS in both transitions. The instantaneous negative current during turn-off of free-

wheeling MOSFET, helps to compensate differences in dc currents. On the other hand, higher conduction losses will take place and, therefore, this decision should be taken with care depending on the specifications.

These results have been tested with a prototype showing very good current balance even introducing an artificial duty cycle unbalance in the control stage.

Since current loops are expensive, once the current loops have been removed, it is feasible to think in multiphase converters with a high number of phases.

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