Comparison of Two Different Cell Topologies for a Multilevel Power Supply to Achieve High Efficiency Envelope Amplifier

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***Abstract* -- A solution combining a multilevel converter in series with a linear regulator to obtain an envelope amplifier was presented recently in [1] for EER.**

Two possible implementations of the multilevel cell are compared. In [1], a two-state topology for the multilevel cell is proposed for the envelope amplifier. The three-state cell topology, proposed in this paper, has two main advantages: less number of cells and inputs and a simpler electrical and physical design. The comparison of the energy handled by each cell topology confirms several advantages of the three-state cell. Considerations to optimize the design of the multilevel converter for both cell topologies and experimental comparison between both cell architectures are enclosed.

***Index Terms* — Amplitude Modulation, DC-DC power conversion, envelope elimination and restoration (EER), multilevel systems, RF power amplifiers.**

I. INTRODUCTION

The autonomy of modern mobile and communication systems is directly related to their power consumption and efficiency. Low efficiency of these systems means reduced battery life and increased heat output. On a communication satellite system up to 50% of the total power can be used by the Power Amplifier (PA) in the transmitter [2]. Base stations are affected by the PA low efficiency. A base station has an overall efficiency of only 2%, and the PA has a poor 6% [3], which leads to bigger cooling systems and also to more expensive base stations. The transmitters usually employ digital modulations such as QPSK combined with spread spectrum techniques like CDMA or WCDMA. The modulated signals are later amplified by using highly linear, but low efficient linear amplifiers (class A or class B).

The transmitted signals have high peak-to-average power ratio (PAPR) and have the highest probability in the zone where linear amplifiers have very low efficiency (approximately 15% for class B). This is the main reason for low efficiency of these PA applied in RF systems.

The Kahn technique or EER is used to linearize a high efficiency PA by the simultaneous modulation of phase and envelope of the signal and combines a highly efficient, but nonlinear radio frequency power amplifier (RFPA) (class D or class E for example) with a highly efficient envelope amplifier (dc-dc converter) to implement high-efficiency linear RFPA [4].

The envelope amplifier should have fast dynamic response, high efficiency and minimal interference with the output spectrum of the transmitter. In the state of the art, several solutions for the envelope amplifier can be found, such as a simple buck converter (class S modulator) in [5], [6], multiphase buck converter in [7], three level converter in [8] or linear assisted switching amplifier [9], [10]. These solutions do not exceed the bandwidth of few hundred kHz and the output power is from the range of mW up to several tens of watts [11]. In [12], [13] a buck converter is integrated and the switching frequency is in the range of several MHz, but with small output power, in the range of mW.

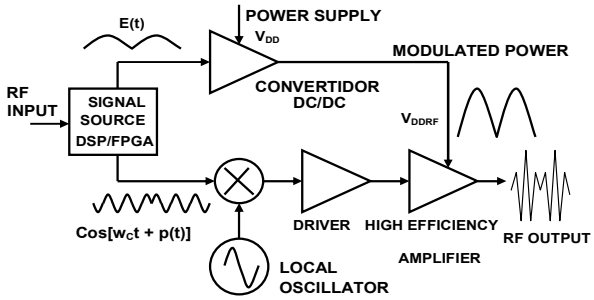

Fig. 1. Block Scheme of Kahn-technique Transmitter

A possible implementation for the envelope amplifier would be a dc-dc converter, as it is necessary a high efficiency for the solution. On the other hand, due to the high bandwidth requirements of the envelope reference, the switching frequency must be fives times higher than the requested bandwidth (for the bandwidth of 1 MHz it would be necessary to apply switching frequency of, at least, 5 MHz) [14]. As a result, the rise in the switching frequency decreases the efficiency of the converter and, as a consequence, the efficiency of the systems decreases too.

The second problem is the output filter of the converter, because its design can be very complicated due to very strict restrictions regarding the voltage ripple and spectral interference. In some papers, it is proposed to use double LC filter [5], but the use of this filter could decrease the maximum bandwidth.

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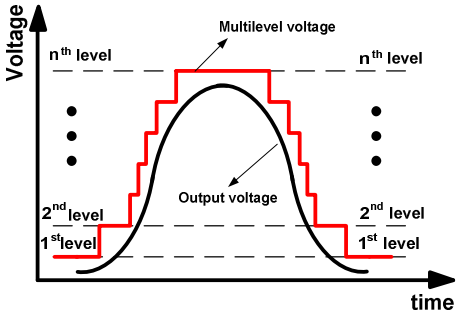

Fig. 2. Time diagrams of the proposed envelope amplifier

The solution presented in [1] does not need complicated filter design and it is not necessary to apply very high switching frequency in order to obtain the bandwidth of several MHz. The presented system can reproduce a sine wave or any other reference with maximal spectral component of 2 MHz, and give the instantaneous maximal power of 50 W.

Theoretical calculations in this work are presented for a sinusoidal waveform and for a CDMA signal. To carry out experimental measurements a sinusoidal waveform has been used. A CDMA signal, despite it was not available for experimental verifications, has been chosen to apply the theoretical calculations to a telecommunications signal, as it is known the amplitude density probability [15].

The application for the proposed solution is Digital Video Broadcasting (DVB), which requires a bandwidth of approximately 7.5 MHz and no distortion for the transmitted signal at 2 MHz.

II. Proposed Topology

The proposed topology consists of a multilevel converter in series with a high slew rate linear regulator. The main idea of the solution can be seen in Fig. 2. The multilevel converter has to supply the linear regulator and it has to provide discrete voltage levels that are as close as possible to the output voltage of the envelope amplifier. If this is fulfilled, the power losses on the linear regulator will be minimal, because they are directly proportional to the difference of its input and output voltage. However, in order to guarantee correct operation of the linear regulator, the output voltage of the multilevel converter always has to be higher than the output voltage of the linear regulator.

The linear regulator can be designed to have very high bandwidth, and it should filter all the noise that could come from the multilevel converter. It manages only a small fraction of the output power. Therefore, the multilevel converter does not need any filter at its output and the design of the complicated filter, as in the case of switched converters, is avoided. The block diagram of the proposed solution is presented in Fig. 3. In this block diagram can be appreciated an additional first stage, a multi output converter, which generates the input voltages of the multilevel cells.

As it can be appreciated on Fig. 3, the voltage input of the cell number one does not need any isolation, because the ground of this cell is connected to the ground of the output. The other voltage inputs will need isolation, provided by the first stage, and will be connected to each other in series configuration by the power switches of the cells.

There are several possibilities to implement the multilevel converter for this application [1]. The solution presented consists of independent voltage cells that are put in series in order to generate the output voltage as a combination of its voltages. These cells can be implemented to give just positive voltage (two-state cell), or to produce positive and negative voltage (three-state cell), Fig. 4. Each cell has associated an input voltage that is generated in the first stage by a dc-dc converter.

For the two-state cell, it gives a constant voltage when it is turned on, and when it is turned off, it gives zero. The output of this converter can be represented as:

$$V_o = \sum_{i=1}^{N} a_i \cdot V_i \qquad (1)$$

where N is the total number of the implemented cells. a_i takes the value of 0 when the i^{th} cell is turned off and 1 when it is turned on and V_i is the supply voltage of the i^{th} cell. For the three-state cell, possible values of a_i are 0, when the supply voltage of the cell does not contribute to the output voltage, 1 when the output voltage of the cell is V_i and -1 when the voltage input cell is connected inversely to the load ($-V_i$). Due to the negative voltage state of the three-state cell, it is necessary for the first stage of this cell to be bidirectional, because depending on the input signal amplitude density probability and on the value of the voltage levels, mean input power that is supplied by the dc-dc converter that generates the cell's voltage input can be negative.
The linear regulator is supplied by the multilevel converter and, depending on the current voltage level on its input and output, its efficiency will vary. If the transmitted signal codification is known (CDMA for example) [15], it is possible to optimize the multilevel cell's voltage and the number of levels, as explained in [1].

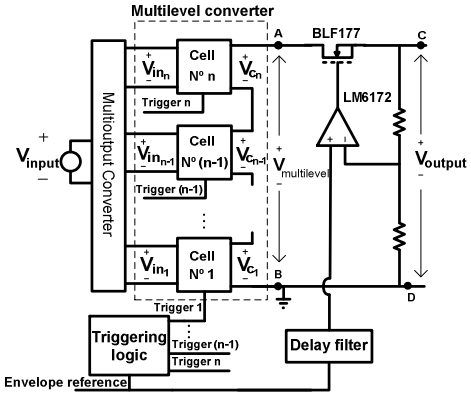

Fig. 3. Block diagram of the implemented envelope amplifier

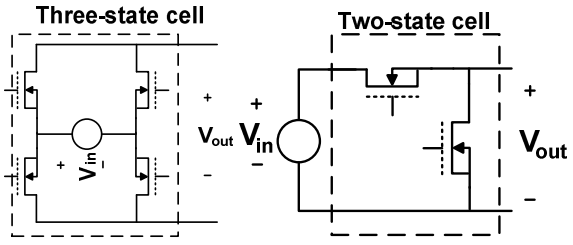

Fig. 4. Voltage cells that could be used as a solution to implement a multilevel converter

III. Design Considerations for the Optimization of the Number and Magnitude of the Voltage Levels of the Envelope Amplifier

The number of voltage levels of the envelope amplifier, to improve efficiency, quality of the transmitted signal and size of the converter, has to be established regarding the following design issues:

- Overall efficiency of the converter: more voltage levels implies better efficiency on the third stage but more power losses on first and second stages as a result of more cells and voltage inputs
- Simplicity: Complexity and size increase with the number of voltage levels
- Parasitic Components: As the number of levels rise, parasitic components of the layout, critical at high frequecies, become more important

To obtain an accurate model relating all this factors, some of them even difficult to quantify, is very complex. Hence, to determine the optimum number of levels is complicated.

However, to calculate the improvement in the efficiency of the third stage is feasible. The first increments in the number of levels have a strong impact in the efficiency. For example, regarding the specifications of this paper, described in section IV, there is an improvement of a 13% for a sinusoidal waveform and a 30% for a CDMA signal in the efficiency of the third stage as a consequence of increasing from one to three the number of voltage levels. This improvement becomes smaller for higher number of levels. For example, a transition from three to five voltage levels would imply improvements of 4% for a sinusoidal waveform and a 6% for a CDMA signal in the efficiency of the third stage. On the other side, a high number of levels penalize the efficiency and simplicity of the first and second stages.

Hence, depending on the specifications, the optimum number of levels must be determined regarding the complexity of the whole system and the efficiency improvement provided in the third stage by the considered number of levels.

The system specifications, demanding on terms both of frequency and power, have a strong influence on the operation of commercial available devices used on the prototypes. It is expected that wide band-gap materials, as GaN, can improve in the next years the performance of the proposed solution affecting also to the number of levels of the design.

Besides, not only it is important to determine the number of levels but also to decide the value of those levels.

Input voltage values of the cells have been optimized to improve the efficiency of the third stage (the linear regulator).

To apply this optimization it must be known the evolution on time of the signal (if it is periodical, as a sinusoidal waveform) or, for a communications signal, the amplitude density probability. Based on this information, an iterative differential algorithm has been applied. It calculates the best voltage levels values to maximize the efficiency of the linear regulator stage by integrating input and output power for each output voltage or voltage amplitude through all the possible amplitude values. The precision of the algorithm is selected by the number of intervals in which the possible amplitude values range is divided. The algorithm has been implemented using the mathematical tool Mathcad.

Using this optimization for a CDMA signal and a sinusoidal waveform, both from 0V-23V, the obtained level voltages are 12V, 18V and 24V for a 24V input. With the two-state cell configuration, it is achieved with three inputs: a main voltage of 12V and two cells of 6V. With the three-state cell, it can be achieved with two inputs: a main input of 18V and a cell of 6V. The optimized voltage levels are obtained by subtracting, adding or not connecting the bidirectional cell of 6V to the 18V main input.

IV. Comparison Between Two and Three State Cells Topologies

The specifications used for this comparison are: a maximum frequency of the reproduced signal of 2 MHz, a maximum output power of 50 W, input voltage of 24V and an output voltage range from 0V to 23V.

Main input refers to the higher voltage input, which is always connected to the load for this design.

Main advantages of three-state cell configuration over two-state one are:

- The number of cells is lower.
- The number of inputs needed to achieve the same levels configuration is lower. Generalizing this concept to n levels (n>2), if the number of levels is odd, (n-1)/2 inputs are saved compared to the state equivalent design. For an even number of levels, a two-state cell will be added to the three-state design, saving (n-2)/2 inputs.
- As a result of a multilevel converter with less inputs (less components and volume), electrical and physical design is more simple.

Disadvantages:

- Three-state cells inputs need to be bidirectional. It implies a more complicated control stage design and Synchronous Rectification (SR) technology must be used. On the other hand, as a result of the implementation of SR, the efficiency could be improved.
- There are more MOSFETs in each cell.

For both cell topologies there is no difference in the signal quality, the linear regulator stage and in the total number of MOSFETs for the same number of voltage levels design.

In order to optimize the design process of the first stage, a study of the energy handled by both types of cells for a three level prototype has been carried out. Results can be seen in Table I. Power handled by each voltage input has been obtained by adapting the optimization algorithm presented in previous section.

It can be seen, for both cell topologies, that the main input voltage of the first stage (the one with higher voltage) handles high percentage of the converter total input power.

TABLE I
POWER HANDLED BY EACH CELL TOPOLOGY FOR DIFFERENT REFERENCE SIGNALS

Signal	Cell Topology	Power Supply Voltage (V)	Power Handled (W)	% of power handled by auxiliary power supplies
CDMA	Two state	6	0.35	22.2
		6	2.95	
		12	11.53	
	Three state	±6	-2,62	13.1
		18	17,45	
Signal	**Cell Topology**	**Power Supply Voltage (V)**	**Power Handled (W)**	**% of power handled by auxiliary power supplies**
Sinusoidal Waveform	Two state	6	3.81	41.6
		6	5.11	
		12	12.5	
	Three state	±6	2.67	12.5
		18	18.75	

This effect can be seen for both input signals on both cell topologies as this input is always connected to the load and has higher voltage (12V and 18V) than the cells voltage inputs, 6V in this design. As no isolation is required for main input, as explained in section II, it can be designed to be a simple and independent power supply with very high efficiency. Comparing both cell topologies, it can be seen that the three-state configuration main voltage input handles more power than the two-state configuration one, which relies in a higher efficiency for the three-state architecture. On the other hand, if there is any input with negative mean input power, there will be more power managed by the first stage for the same output power that will reduce the advantages relating efficiency.

As a result of both topologies comparison, the transmitted signal amplitude density probability, the output power and the maximum spectral component of the transmitted signal must be known in order to decide which topology will be more suitable for the multilevel converter.

V. EXPERIMENTAL RESULTS

A photograph and experimental results for the two-state cell topology multilevel implementation can be seen on Fig. 5 and 6 and in Fig. 7, 8 and 9 for the three-state cell configuration.

As a CDMA test signal was not available, the efficiency of the system has been measured for several sinusoidal waveforms at 500 kHz and 2 MHz, with a resistance of 12 Ω as the load.

Comparing both prototypes, it can be observed a reduction on the magnetic components size of the first stage has been achieved for the three-state cell design as a result of the applied optimization based on results of Table I.

The first stage has been implemented for the three-state cell design with a 18V buck converter and a 6V flyback converter with SR. For the two-state cell design, just one magnetic component, bigger and heavier, processes all the first stage power. The switching frequency of the first stage for both prototypes is 50 kHz, low to improve the efficiency of this stage, which processes all the power of the converter.

Fig. 5. Photograph of the implemented envelope amplifier with two-state cells (top module contains second and third stages and at the bottom PCB the first stage, the multioutput converter).

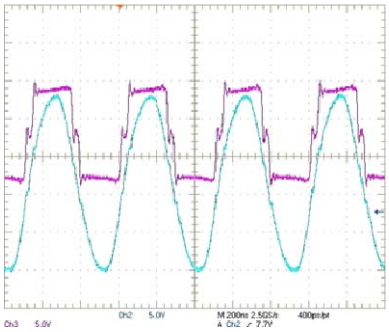

Fig. 6. Measured waveform of multilevel's (two-state cells) output voltage (top trace) and linear regulator's output voltage (bottom trace) at 2 MHz. Scales are 5V/div and 200ns/div

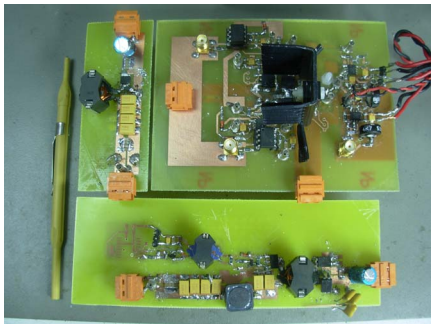

Fig. 7. Photograph of the implemented multilevel converter with three-state cell configuration. At the bottom and on the top-left side are the first stage modules and at the top-right side is the module containing the second and third stages

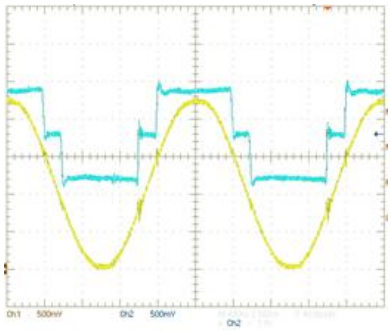

Fig. 8. Measured waveform of multilevel's (three-state cells) output voltage (top trace) and linear regulator's output (bottom trace) voltage at 500 kHz. Scales are 5V/div and 400ns/div

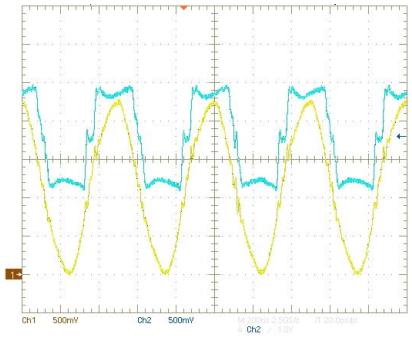

Fig. 9. Measured waveform of multilevel's (three-state cells) output voltage (top trace) and linear regulator's output voltage (bottom trace) at 2 MHz. Scales are 5V/div and 200ns/div

Table II shows the experimental comparison presented in [1] between the envelope amplifier with the two-state cell topology and the solution that consists in supplying the linear regulator with a constant voltage.

TABLE II

MEASURED EFFICIENCY OF THE IMPLEMENTED ENVELOPE AMPLIFIER FOR DIFFERENT SINE WAVES COMPARED WITH THE THEORETICAL EFFICIENCY OF AN IDEAL LINEAR REGULATOR SUPPLIED BY 23 V

Vsin(V)	*Sine wave frequency (MHz)*	*Measured efficiency of the flyback converter*	*Measured efficiency of the envelope amplifier*	*Theoretical efficiency of an ideal linear regulator supplied by 23V*
0-9	*2*	*94%*	*43.7%*	*29.3%*
5-14	*2*	*93%*	*58.8%*	*45.9%*
0-22.5	*2*	*91%*	*68.3%*	*73.4%*
0-9	*0.5*	*91%*	*43.3%*	*29.3%*
5-14	*0.5*	*91%*	*58.9%*	*45.9%*
0-22.5	*0.5*	*94%*	*69.7%*	*73.4%*

TABLE III

COMPARISON OF THE EFFICIENCY OF THE ENVELOPE AMPLIFIER WITH THREE AND TWO-STATE CELL CONFIGURATIONS FOR DIFFERENT SINUSOIDAL INPUT SIGNALS

Vsin(V)	*Sinusoidal waveform frequency (MHz)*	*Measured efficiency of the envelope amplifier with three-state cell configuration*	*Measured efficiency of the envelope amplifier with two-state cell configuration*
0-9	*2*	*48,4%*	*43,7%*
5-14	*2*	*53,4%*	*58,8%*
0-22,5	*2*	*63,6%*	*68,3%*
0-9	*0,5*	*47,6%*	*43,3%*
5-14	*0,5*	*59,5%*	*58,9%*
0-22,5	*0,5*	*71,8%*	*69,7%*

The multilevel implemented prototype has a size of 144mm x138mm, while the implementation with two-state cells, under the same specifications, has a size of 194mm x179mm.

It can be seen that the efficiency at low frequencies for all measured sinusoidal waveforms, 500 kHz, is better for the three-state prototype. The reasons are, mainly, that the first stage has better efficiency and also, with less influence, that the main input (with higher efficiency) handles more percentage of the power of the converter. At higher frequency, 2 MHz, the efficiency is lower due to additional parasitic components, that have more influence than the improved first stage efficiency. Those parasitic components, higher in the three-state configuration PCB, less optimized and constructed with a different technology, require a more dissipative RC snubber net to ensure the quality of the transmitted signal, which increases the power losses. At 2 MHz, only for the sinusoidal waveform from 0V to 9V, where there are no commutations (V_{out} < 12V), the three-state cell prototype has a higher efficiency.

VI. CONCLUSIONS

In this paper, an important modification of a solution for an enveloper amplifier for EER technique is presented. The solution consists of a multilevel converter in series with linear regulator. It is analyzed a new topology for the multilevel converter, a three state cell, and compared with an existing solution, the two-state cell topology. A comparison between both possibilities for the multilevel converter regarding the simplicity of the design, the number of inputs and efficiency is conducted. A study of the energy handled by each input with two different signals has been developed to compare both design options and to validate previous mentioned advantages of the three-state cell topology. In order to carry out the analysis, two prototypes have been made and the measured system's efficiency for various 500 kHz and 2 MHz sinusoidal waveforms is presented. Both prototypes can deliver up to 50W of instantaneous power. Comparing the measured efficiency of both solutions with the efficiency of the linear regulator, which is normally used as an envelope amplifier, the proposed solution has better efficiency up to 15%-18% for the two and three-state cell configuration respectively.

For a low number of voltage levels both cell architectures have similar behavior for the considered design specifications (as the first stage efficiency optimization could also be applied to the two-state cell topology). In this case, efficiency differences will be associated mainly to the energy handled by main inputs of each solution. The three-state cell topology will be a better design option for designs with a higher number of levels.

REFERENCES

[1] M. Vasić, O. García, J.A. Oliver, P. Alou, D. Díaz, J.A. Cobos, "Multilevel Power Supply for High Efficiency RF Amplifiers" IEEE Applied Power Electronics Conference, February 2009.

[2] G. D. Gordon and W. L. Morgan, "Principles of Communications Satellites",NY: Wiley, 1993.

[3] Steve Roy, "Energy Logic for Telecommunications",White paper from Emerson Network Power, September 2008.

[4] F.H. Raab, P. Asbeck, S. Cripps, P.B. Kenington, Z.B. Popovic, N.Pothecary, J.F. Sevic, N.O. Sokal, "Power Amplifiers and Transmitters for RF and Microwave"

[5] P. Midya, K. Haddad, L. Connell, S. Bergstedt, B. Roeckner, "Tracking power converter for supply modulation of RF power amplifiers," IEEE Power Electronics Specialists Conference, PESC. 2001, Vol. 3, Pages: 1540 – 1545.

[6] J. Staudinger, B. Gilsdorf, D. Newman, G. Norris, G. Sadowniczak, R.Sherman, T. Quach, "High efficiency CDMA RF power amplifier using dynamic envelope tracking technique," Microwave Symposium Digest., IEEE MTT-S International, Vol. 2, June 2000, Pages: 873-876

[7] A. Soto, J.A. Oliver, J.A. Cobos, J. Cezon, F. Arevalo, "Power supply for a radio transmitter with modulated supply voltage", Applied Power Electronics Conference, APEC '04, Volume: 1, Feb. 2004 Pages:392 – 398.

[8] V. Yousefzadeh, E. Alarcon, D. Maksimovic, "Three-level buck converter for envelope tracking in RF power amplifiers," IEEE Trans. on Power Electronics, Volume: 21, Issue: 2, March 2006, Pages:549 – 552.

[9] US Patent No. 6084468, Method and Apparatus for High Efficiency Wideband Power Amplification, July 2000.

[10] V. Yousefzadeh, E. Alarcon, D. Maksimovic, “Efficiency optimization in linear assisted switching power converters for envelope tracking in RF power amplifiers”, IEEE International Symposium on Circuits and Systems, ISCAS 2005, 23-26 May, pages:1302-1305 Vol. 2.
[11] F.H. Raab, B.E.Sigmon, R.G.Myers, R.M. Jackson, “L-Band Transmitter Using Kahn EER Technique”, Transactions on Microwave Theories and Techniques, Volume 46, Issue 12, Part 2, Pages: 2220-2225, December 1998.
[12] V. Pinon, F. Hasbani, A. Giry, D. Pache, C. Gamier, "A Single-Chip WCDMA Envelope Reconstruction LDMOS PA with 130MHz Switched-Mode Power Supply" Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International, pp. 564-636, 3-7, Feb. 2008.
[13] P.G. Blanken, R. Karadi, H.J. Bergveld, “A 50MHz Bandwidth Multi-Mode PA Supply Modulator for GSM, EDGE and UMTS Application”, IEEE Radio Frequency Integrated Circuits Symposium, RFIC 2008, 15-17 June 2008.
[14] L. Marco, E. Alarcon, D. Maksimovic, “Effects of switching power converter nonidealities in Envelope Elimination and Restoration technique”, IEEE International Symposium on Circuits and Systems, ISCAS 2006, 21-24 May 2006.
[15] V. Yousefzadeh, “Digitally Controlled Power Converters for RF Power Amplifiers”, PhD Thesis, August 2006.