System Linearity-Based Characterization of High-Frequency Multilevel DC-DC Converters for S-Band EER Transmitters

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***Abstract*—In modern telecommunications systems, the requirements for the amount and speed of transmitted data are increasing rapidly. For better spectral efficiency complex type modulations (QAM, OFDM) are used, resulting in high PAPR signals. As a consequence, when conventional linear amplifiers (classes A, AB) are used in transmitters, both prominent linearity and poor efficiency are assured. The efficiency of the transmitters can be significantly improved using some of the popular techniques: Kahn EER principle, ET technique, Doherty amplifier, and Chireix's amplifier. In this paper, two different approaches in supplying a 2.4 GHz class-E power amplifier (S-band) based on the EER technique are analyzed and compared. The consistent part of the EER transmitters is a switched-capacitor based voltage divider combined with a switching structure - analog multiplexer, in the envelope amplifiers and a class-E power amplifier. The analog multiplexer is assisted with a series linear regulator in the first system and a fourth order LC filter in the second system, providing supply modulation for the power amplifier. The systems are compared in terms of efficiency and system linearity using the standard metrics (EVM, ACPR). Special consideration is devoted to characterization of how the envelope amplifiers affect the quality of the RF output signal. It is shown that the tested EER transmitters can reproduce 16–QAM and 64–QAM signals up to 2.5 MHz, manifesting an average efficiency of about 32% with the first transmitter, and 16–QAM signals up to 660 kHz RF bandwidth and an average efficiency of 44% with the second transmitter. A software tool that accurately estimates the EA linearity is utilized and successfully tested on both EER transmitters.**

***Index Terms*—Multilevel DC-DC power converter, EER Transmitter, Nonlinear distortion.**

I. Introduction

DURING the last decade, significant effort has been dedicated to the optimization of RF power amplifier efficiency. Conventional linear amplifiers (classes A, AB) supplied by a constant voltage can exhibit excellent linearity, but also poor efficiency when amplifying signals with a high PAPR (Peak to Average Power Ratio). Since modern, spectral-efficient modulation schemes (QAM, OFDM) produce high PAPR signals (beyond 10 dB), the efficiency of the transmitters in telecommunication base stations is poor. Additionally, mobile communication devices suffer from a short battery lifespan due to the harsh working conditions.

The efficiency of RF amplifiers can be improved using several promising techniques, such as EER (based on Kahn's principle of envelope elimination and restoration technique introduced in [1]), ET (Envelope Tracking), Doherty's technique, Chireix's amplifier, (summed up in [2]) etc. or even by developing a codesign method defined as the signal split [3].

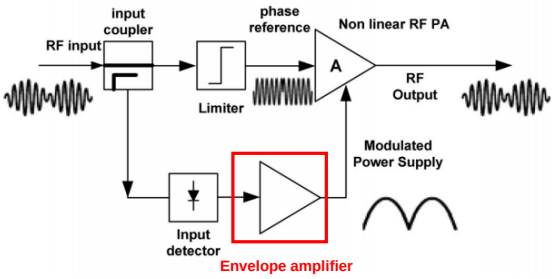

Fig. 1: Principle of Kahn's EER technique, with the waveforms of two-tone RF input signal.

The role of power electronics is indispensable in the first two of the aforementioned techniques: EER and ET. In this paper, two S-band transmitters based on the EER technique are analyzed. Two important parts of each EER based transmitter (Fig. 1) are the envelope amplifier (EA), also called the envelope tracker, which amplifies the broadband envelope of the input RF signal; and the nonlinear efficient switched-mode power amplifier, driven by the constant envelope narrow band phase signal. The EA is a fast dc-dc converter, with the objective of supplying a non-linear power amplifier with variable voltage in an efficient manner from an external stabilized voltage source. Only properly combined and synchronized supply voltage and phase drive can linearize the transmitter. On the cutting edge of development, different types of fast switched-mode power converter topologies for EAs have been proposed, which are usually buck type converters [4], three level buck converters [5], multilevel [6] and multiphase converters [7], [8], resonant switched-capacitor converters [9], or

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even combinations of two DC-DC converters with split power functionality for visible light communications [10], [11]. Fast bandwidth and compact power converters are becoming more feasible with the new emerging GaN high electron mobility devices. These devices are the key enabler of high frequency switching PWM converters, showing clear benefits compared to the Si MOSFET-based converters [12], [13].

The main drawback with envelope trackers is the dc-dc converter dynamics. The EA must be able to provide accurate tracking of the envelope reference, which requires high frequency commutations, but at the same time a high converter efficiency must be assured. To address this challenging trade-off, linear assisted power converter topologies have been proposed, where wide bandwidth lossy linear regulators (amplifiers) alleviate the bandwidth requirement of the switched-mode converters, while the switching frequencies maintain reasonable values. Different configurations have been introduced in literature, such as parallel configuration where the EA provides the bulk of the output current [14], [15], [16]; series configuration where the multilevel EA is used to reduce the voltage drop on the linear regulator [17], [18]; and hybrid series-parallel form, which comprises two switched-mode converters and one linear regulator, to reduce both the series transistor voltage and the output current of the linear regulator [19]. In all the configurations, the linear amplifier controls the EA output voltage.

Although the purpose of EAs is to supply PA in highly efficient manner, some other aspects of this process have to be taken into account, such as the bandwidth of the system and the output voltage ripple [20]. In this paper, two approaches based on EER technique are analyzed and compared in terms of the converter efficiency, bandwidth, and linearity. The same parts of both EAs are a switched capacitor based multilevel voltage source (voltage divider) and a switching structure, the so-called analog multiplexer, which selects the appropriate voltage level produced by the voltage divider. In the first approach, the shaping of the envelope signal is achieved in a dissipative way using linear regulator in a series, while in the second approach it is obtained with a PWM switched-mode converter with a fourth order output filter. The common approach in the literature is to make system efficiency the first priority. Regarding the converters' efficiency, the bottleneck of the first approach is the linear regulator conduction loss, while in the second PWM switched approach the switching losses in the analog multiplexer are the most pronounced disadvantage. Moreover, the second system is faced with more hardware restrictions: more severe layout design, the output filter imperfections, the resolution of digital PWM and delays in the driving circuits, which together contribute to significant signal deterioration.

Nevertheless, the focus of the research is to describe the effects of both the envelope tracker and power amplifier that together lead to the linearity aggravation of the whole system. The linearity of the transmitters is characterized employing the standard metrics from the telecommunications standards: EVM (Error Vector Magnitude) to describe in-channel distortion; and ACPR (Adjacent Channel Power Ratio) to describe out-of-channel emission, instead of using NMSE (Normalized Mean Square Error) metrics, which are typically adopted in the literature [21], [22]. A software tool intended for evaluation of envelope amplifiers is further exploited, without taking into account the non-linear effects of the power amplifier (AM-AM and AM-PM conversion). This tool is very convenient as it successfully predicts the effects of the EA on the transmitter linearity and can be employed in the optimization process for the design decisions of an envelope amplifier. Thanks to this analysis, critical findings, such as the minimum bandwidth of the linear regulator in the first analyzed EA, and the converter minimum switching frequency, filter type, filter cut-off frequency and time resolution in the second analyzed EA, can be successfully identified. These results are of the utmost importance in the design process of an EA. The preliminary considerations will be backed up with the experimental results of the EAs with resistive loading, and these results will be confirmed by the experimental results of whole EER transmitters as well. The analyzed EER transmitters can reproduce 16–QAM and 64–QAM signals up to 2.5 MHz manifesting an average efficiency of about 32%, with the first transmitter based on the Linear assisted EA and 16–QAM signals up to 660 kHz RF bandwidth and an average efficiency of 44%, with the second transmitter based on the PWM switched EA. The system linearity parameters are successfully predicted and confirmed by experimental results.

II. Analyzed Envelope Amplifiers

One of the key points for both approaches is the multiple voltage input. Both envelope trackers are supplied with a set of voltage levels. The multiple voltage input is provided using a switched-capacitor based multilevel converter, which operates as a voltage divider and three more voltage levels are provided from one single input voltage source V_{DC}, as shown in Fig. 2. Flying capacitor C_{fly}, together with two bulky capacitors, C_1 and C_2, is placed between two switching nodes in order to maintain the middle voltage at half of the input voltage V_{DC}. Two buck type structures consisted of transistors S_1, S_2 and S_3, S_4 produce pulsating voltage between V_{DC} and $V_{\mathrm{DC}}/2$ (v_{N1}); and between $V_{\mathrm{DC}}/2$ and ground (v_{N2}), in the two switching nodes. These pulsating voltages are filtered by small LC output filters, providing stable output voltages $(1+d)\,V_{\mathrm{DC}}/2$ and $dV_{\mathrm{DC}}/2$ at the output. The advantage of this converter is its high efficiency, especially when GaN transistors are used [23]. High efficiency is associated with low converter volume, also allowing low occupied space and low weight. All these advantages make this converter convenient to use in applications where weight and volume are critical. The second advantage of this converter is the possibility to modulate two of its output voltages by the means of duty-cycle d, which can be used in the optimization process of the overall envelope tracker, as explained in [24].

The essential part of both converters is a switching structure, whose role is to select an appropriate voltage level. This structure is denominated as an analog multiplexer. The other circuits implemented are a linear regulator, in the first approach, and a passive filter, in the second approach. These two systems are shown in Fig. 3 and Fig. 4, respectively. The figures show

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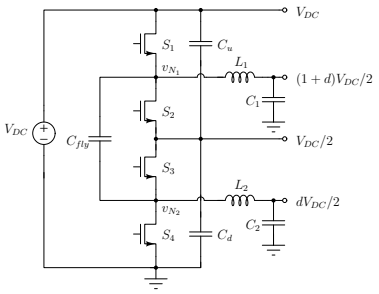

Fig. 2: Switched-capacitor based multilevel converter.

the complete schemes of the EER transmitters, consisting of the multilevel voltage source, the envelope amplifier and the RF power amplifier. In the first case, the EA is comprised of the analog multiplexer and a linear regulator (Fig. 3), while in the second EA the linear regulator is replaced with a passive LC filter (Fig. 4).

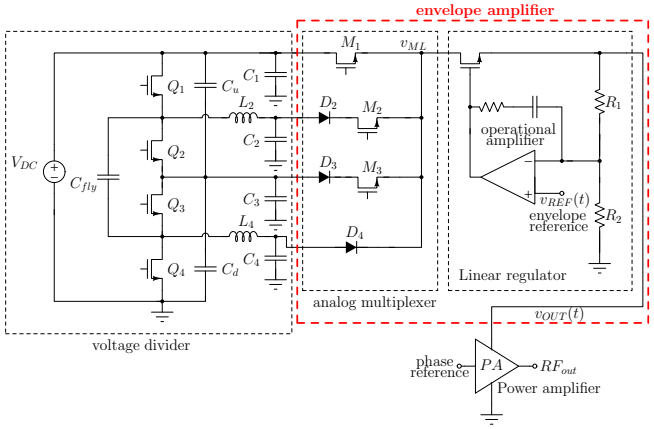

Fig. 3: EER transmitter based on Series linear assisted EA.

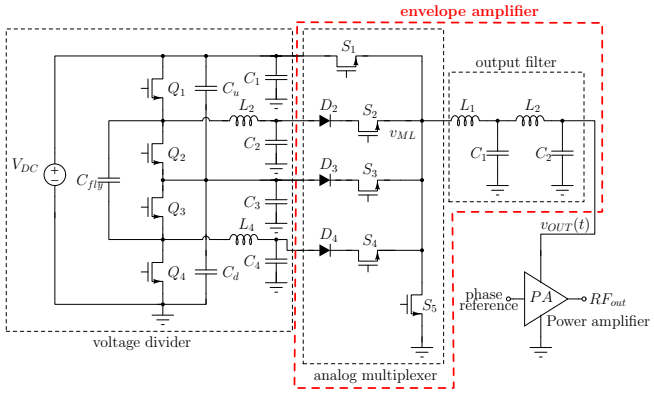

Fig. 4: EER transmitter based on PWM switched filter assisted EA.

A. Linear Assisted EA

Linear voltage regulators with a series transistor are suitable due to their relatively simple hardware requirements. Since they act as common drain amplifiers, high bandwidth and accurate tracking of reference voltage in a wide frequency range can be provided, with low output voltage noise. The main disadvantage of these power supplies is the fact that their efficiency depends on the drain to source voltage of the series transistor, which is the difference between the supply voltage and the output voltage. Instead of constant supply voltage, multilevel voltage is used, therefore the linear regulator operates as an active shaping filter which filters out the multilevel voltage and creates the smooth EA output voltage. Multilevel converter voltage should be close enough to the output voltage of the linear regulator to decrease the voltage difference across the series transistor in the linear regulator, but still high enough to avoid the triode (ohmic) region of the series MOSFET transistor in the linear regulator. To provide that functionality, the analog multiplexer is comprised of the switches that turn on the corresponding voltage level. MOSFET switches cannot block negative voltage, and block diodes D_2 and D_3 are put in series with the transistors M_2 and M_3, respectively (Fig. 3). These diodes can be replaced with the MOSFET switches placed in the reverse direction (two MOSFETs in series), but the diodes are used for the sake of simplicity. The operating principle of the linear assisted EA for $d = 0.5$ is shown in Fig. 5, where the state of the switches is depicted. Thanks to the peak detection function of the diodes, in the event that more than one switch is in the on-state, the $v_{\mathrm{ML}}(t)$ will always be the highest of the provided voltage levels. The voltage stress across the semiconductor components in the analog multiplexer is always lower than the V_{DC} voltage, with the maximum value of $(1+d)\,V_{\mathrm{DC}}/2$. The multiplexer switching frequency is defined by reference envelope signal dynamics, and the switching occurs when the reference signal crosses a certain threshold level. It is shown in [25] that this frequency does not exceed the highest frequency component in the spectrum of the processed RF signal (QAM or OFDM type), which reduces the switching losses of this converter, but also facilitates the layout design, which is a critical point for the high frequency power converter design.

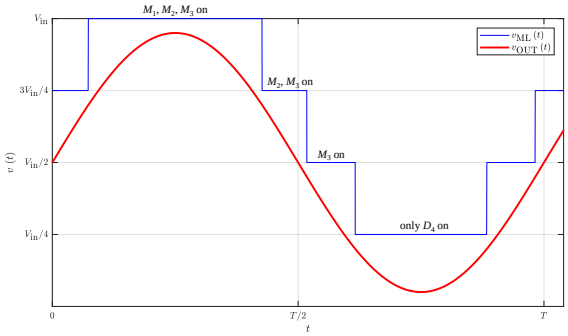

Fig. 5: The operating principle of the linear assisted EA: the voltage at the output of analog multiplexer $v_{\mathrm{ML}}(t)$ (the blue line) and the EA output voltage $v_{\mathrm{OUT}}(t)$ (the red line). The voltage difference between $v_{\mathrm{ML}}(t)$ and $v_{\mathrm{OUT}}(t)$ is always high enough for the MOSFET from the linear regulator to operate in the saturation region.

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B. PWM Switched Filter Assisted EA

The main disadvantage of the previous approach is efficiency limitation superimposed by the active filtering accomplished by the linear regulator. Instead of using an active filter at the output of the envelope tracker, a properly designed low-pass passive shaping filter can be employed to mitigate the efficiency problem. Nevertheless, in order to provide the exact replica of the envelope reference at the converter output (i.e. fast bandwidth of the output filter) and a small size of the filter elements, high frequency PWM switching must be utilized. The main concern in this approach is the critical trade-off between the converter size, the converter losses, and the converter bandwidth. In other words, for a given switching frequency, a converter with the fastest possible bandwidth must be designed. For example, in [26] a two phase buck converter with a fourth-order output filter is used. The advantage of that approach is the reduction of harmonics around the switching frequency, which allows the filter cut-off frequency to be set closer to the switching frequency. On the other hand, in [27], a two phase synchronous buck converter is used, where the value of the first inductor in the fourth-order output filter is modified in order to achieve zero-voltage switching (ZVS), and the rest of the filter elements are designed to fulfill the filtering specifications. The switching frequency harmonics can also be lower compared to the classical two-level buck converter if the modulated voltage at the filter input has smaller peak-to-peak variations. Instead of switching between maximum and zero voltage, the switching operation can be distributed between several voltage levels, like in [5], where the three level buck converter is used.

In this case, five voltage levels are applied, using the same voltage divider as in the linear assisted EA. The analog multiplexer is comprised of two additional MOSFETs, in order to provide controlled selection of two more voltage levels ($V_{DC}/4$ and 0) during the PWM switching process. The reconstruction of the PWM signal is carried out by the fourth order LC filter. The schematic of the entire system is shown in Fig. 4. The modulation process is divided into four sections. In each section, the duty-cycle has a value from 0 to 1 and controls the pair of corresponding transistors (S_0, S_1; S_1, S_2; and so on). The operating principle of the converter for a sine wave reference is shown in Fig. 6, again for $d = 0.5$ (the voltage divider duty cycle). This is exactly the same voltage reference used in the explanation in Fig. 5. The switching node voltage, which must be filtered ($v_{\mathrm{ML}}(t)$ from Fig. 6), has a more favorable shape than in two-level PWM modulation. The lower amplitude of the high frequency harmonics is, the lower values of inductors and capacitors in the output filter can be, in that way reducing the size and weight of converter. The drawback of this converter compared to the simple two-level buck converter is the increased number of MOSFET switches (5 MOSFETs in the analog multiplexer with the gate drivers and two auxiliary voltage supplies) and the necessity of a more careful layout design. The ZVS of the switches S_1 – S_4 in this configuration is precluded by the series diodes D_2 – D_4. Nevertheless, ZVS would be achievable if the diodes were replaced by MOSFETs, but this configuration is avoided in favor of simplicity.

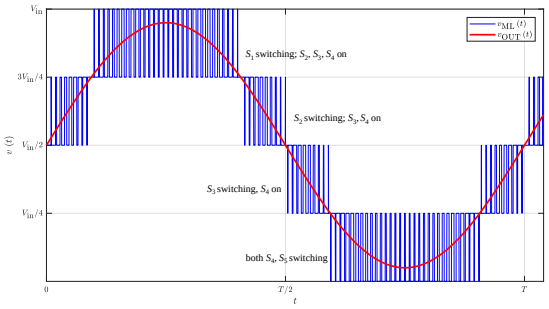

Fig. 6: The operating principle of PWM switched EA: The voltage at the output of the analog multiplexer $v_{\mathrm{ML}}(t)$ (the red line) and the EA output voltage $v_{\mathrm{OUT}}(t)$ (the blue line), for a biased sine wave reference. The output voltage ripple and the delay between $v_{\mathrm{OUT}}(t)$ and $v_{\mathrm{ML}}(t)$ introduced by the output filter is neglected.

By adding more dynamic elements to the converter, open-loop transfer function order increases, therefore closed-loop control may be hard to design. In this particular case, under the assumption that the drain supply terminal of the saturated power amplifier can be modeled approximately as a pure resistance [28] and that the inductors L_1 and L_2 operate in continuous-conduction mode (CCM) due to the current bidirectional switch (S_5) in the converter, the algebraic degeneration does not occur and the circuit is characterized by four state variables (i_{L1}, v_{C1}, i_{L2}, v_{C2}). The filter with a low Q-factor is designed according to the resistance value, so the amplitude–frequency response of the filter has a low overshoot. With such a design and neglected loading effects, unpredictable oscillations in the reference tracking cannot occur. Moreover, due to the constant supply voltage and CCM of both inductors, a linear relationship between the reference signal and output voltage is guaranteed. According to all these specific conditions, the highest converter bandwidth can be achieved when it operates in open-loop, which is also clarified in [29]. Nevertheless, if the output voltage waveform does not satisfy the required quality metrics, a pre-distortion algorithm of the reference voltage may be employed [27].

III. Methodology of the Linearity Comparison

In this section, special attention is devoted to the distortion which is provoked by the EA stage. In [30], it was stated that two main contributors to the intermodulation distortion (IMD) of an EER transmitter are the finite bandwidth of the envelope modulator and the difference in the delay between the envelope and phase signals. The analysis was based on a two-tone test signal, allowing the derivation of an analytical relationship between each of the system parameters and the IMD, keeping in mind that IMD for multi-tone signals is never larger than that of the two-tone signal. With the EA bandwidth $B_{\mathrm{EA}} = 2BW_{\mathrm{rf}}$, where BW_{rf} is the bandwidth of the processed RF signal [1], it is possible to achieve $(C/I)_{\mathrm{max}} = 37.53\,\mathrm{dBc}$.

[1]The RF signal bandwidth BW_{rf} is the bandwidth of the baseband signal $S(t)$ from Eq. 1, while the envelope signal bandwidth is significantly higher than BW_{rf}.

Nevertheless, power amplifiers also manifest the nonlinear behavior which is explained by two contributors that can significantly deteriorate the linearity: AM-to-AM conversion and AM-to-PM conversion. In [31] it was shown that the main reason for the AM-to-AM conversion was the transistor nonlinear drain-source current, while the main contributors for the AM-to-PM conversion were the transistor input impedance variation (seen as unilateral input capacitance which summed the gate-source and Miller reflected gate-drain capacitance) in the case of GaN HEMT based single ended PA; and the load impedance when the output matching network is out of resonance. The characterization of the transmission of modern digitally modulated signals (QAM, OFDM) is much more complicated than that of a two-tone signal. It is usually done via two parameters: EVM (Error Vector Magnitude) to describe in-channel distortion; and ACPR (Adjacent Channel Power Ratio) to describe out-of-channel emission.

A. Software Tool for Estimation of the FOMs

It may be very challenging to mathematically describe the influence of an envelope amplifier on the linearity of an EER transmitter. Instead of using a precise mathematical model for estimation of these two figures of merit (EVM, ACPR), a software tool is designed in Matlab as originated in [32], [33], and further utilized in [34]. This tool can be useful in comparing different topologies of the power converters in terms of the introduced distortion and to evaluate the effects of the delay mismatch, while the imperfections of a power amplifier are neglected (AM-to-AM and AM-to-PM conversion).

The simplified flow-chart diagram of the designed software tool is shown in Fig. 7. Firstly, a baseband signal $S(t)$ is generated, using the 2^n-QAM modulation scheme. This signal can be represented through its in-phase component $I(t)$ and quadrature component $Q(t)$, or through its envelope $E(t)$ and phase signal $\phi(t)$:

$$S(t) = I(t) + \mathrm{j}\,Q(t) = E(t)\,\mathrm{e}^{\mathrm{j}\phi(t)}. \tag{1}$$

The envelope $E(t)$ of the RF signal $S(t)$, which is the reference for the EA according to the Kahn-EER principle, is given by:

$$E(t) = |S(t)| = \sqrt{I(t)^2 + Q(t)^2}, \tag{2}$$

and the phase of the baseband signal $S(t)$ is obtained by atan2 function [35]:

$$\phi(t) = \arg\{S(t)\} = \mathrm{atan2}\,\{Q(t),\, I(t)\}. \tag{3}$$

This operation represents the elimination of the phase signal from the input baseband signal $S(t)$. The signal that should be transmitted (RF signal reference) is the real component of the RF signal:

$$V_{\mathrm{RF}}(t) = \mathrm{Re}\,\{S(t)\,\mathrm{e}^{\mathrm{j}\omega_{\mathrm{carrier}}t}\} = E(t)\cos\left(\omega_{\mathrm{carrier}}t + \phi(t)\right), \tag{4}$$

where $\omega_{\mathrm{carrier}}$ is the carrier frequency from the local oscillator. The translation of the phase spectrum to the carrier frequency is done in the phase branch, independently of the envelope signal.

Envelope amplifiers can be analyzed at the level of transfer function, where switching effects and non-linearities are not modeled. Another approach is to use the simulation results where the samples of the output voltage of the EA are obtained from the simulation, which may take into account the switching effects of the analyzed power converter, the limited resolution of digital PWM control and the influence of the circuit parasitics. Finally, the most accurate way to predict the behavior of an EA in the final EER transmitter is to take the measured samples of the output voltage from the real experimental prototype of the analyzed EA. The samples are then scaled and normalized to be comparable with the samples of the original envelope signal.

The implemented software tool takes into account only the distortion of the envelope signal, hence the phase signal extracted from the original modulated signal is simply combined with the envelope signal. In other words, the process of the envelope restoration is assumed to be ideal in order to quantify the impact of the EA only. The envelope samples are scaled and normalized to be comparable with the samples of the original envelope signal, but their position is affected during the modulation and filtering process of the real envelope amplifier. Intermodulation distortion caused by the different delays in the envelope and phase paths can be diminished by inserting the delay into the phase path. The optimal value of the delay is detected when the maximum of the cross-correlation between the original and the reconstructed envelope signals is recognized.

Once the restoration process is completed, the output transmitted signal can be compared with the original reference signal. Using the spectral power density of the output signal, the values for ACPRL and ACPRR can be calculated as:

$$\mathrm{ACPR_L} = 10\log_{10}\frac{\int_{f_c-B}^{f_c+B} S(f)\,df}{\int_{f_c-3B}^{f_c-B} S(f)\,df}, \tag{5}$$

$$\mathrm{ACPR_R} = 10\log_{10}\frac{\int_{f_c-B}^{f_c+B} S(f)\,df}{\int_{f_c+B}^{f_c+3B} S(f)\,df}. \tag{6}$$

where $S(f)$ is the power spectral density of the modulated signal, f_c is the central frequency of the occupied channel, and $2B$ is the channel bandwidth, without a guard interval between adjacent channels [36].

The peak and RMS values of EVM can be calculated using the information about the mismatch in the two constellation diagram:

$$\mathrm{EVM_n} = \sqrt{\Delta I_n^2 + \Delta Q_n^2}, \tag{7}$$

where n is index for the particular symbol, and ΔI_k, ΔQ_k are in–phase and quadrature measured component error, respectively.

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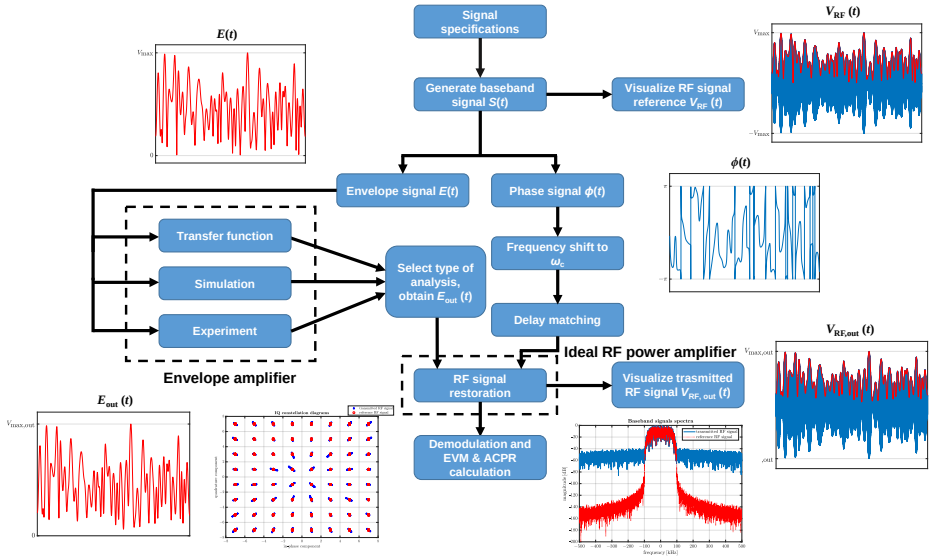

Fig. 7: Flow chart diagram of the described software tool for evaluation of envelope amplifier linearity with the key waveforms obtained by the tool and visualized in the case of a 64-QAM signal reference: the envelope signals $E(t)$ and $E_{\text{out}}(t)$, before and after processing in an envelope amplifier, the phase signal $\phi(t)$ and the corresponding RF signals modulated at the carrier frequency ω_{carrier}, $V_{\text{RF}}(t)$ and $V_{\text{RF,out}}(t)$ with their baseband signals spectra and the IQ constellation diagrams.

The expression (7) is used to determine peak EVM value (maximum error). However, a more typical evaluation of the in–channel distortion is done by taking the root–mean square value of EVM:

$$\text{EVM}_{\text{rms}} = \sqrt{\frac{\frac{1}{N}\sum_{n=1}^{N}|C_{o,n}-C_{m,n}|^2}{\frac{1}{N}\sum_{n=1}^{N}|C_{o,n}|^2}} \tag{8}$$

where, $C_{m,n}$ is the n–th normalized measured constellation point and $C_{o,n}$ is the ideal normalized constellation point nearest to $C_{m,n}$.

To summarize, this software tool is used to evaluate the behavior of the two envelope amplifiers in terms of the quality of signal reproduction. Moreover, this tool can be employed in the optimization process for the final choice of an envelope amplifier. Since the tool takes into account only the effects of EA and neglects the AM-to-AM and AM-to-PM distortion typical for RF PAs, the values of the figures of merit (EVM, ACPR) calculated by this method are roughly the theoretical limits that can be achieved, thus partially decoupling the effect of the EA and the RF PA on the system linearity. In other words, if the power amplifier used in the transmitter were ideal, these would be the parameters of the distortion of the transmitted signal.

B. High Level Analysis

The described software tool can be very useful during the phase of making design decisions. Regarding the linearity, the weak points of the EA from Fig. 3 are the bandwidth of the operational amplifier (gain-bandwidth product) and the parasitics of the series transistor in the Linear regulator, assuming that a digital-to-analog converter that provides the analog reference for the EA has a sufficient resolution. In the second analyzed EA from Fig. 4, special attention must be given to the design of the output filter. Other sensitive points are the PWM resolution and the carrier type. Although these issues are not critical for the linear assisted EA, in the purely switched-mode EA they are of crucial importance because the complete information of the envelope is encompassed in the pulse width of the control signals. To the best of the authors' knowledge, this analysis has not yet been conducted in the literature. The figures of linearity are evaluated for 64-QAM signal references, but the results are valid for all Rayleigh-distributed envelopes.

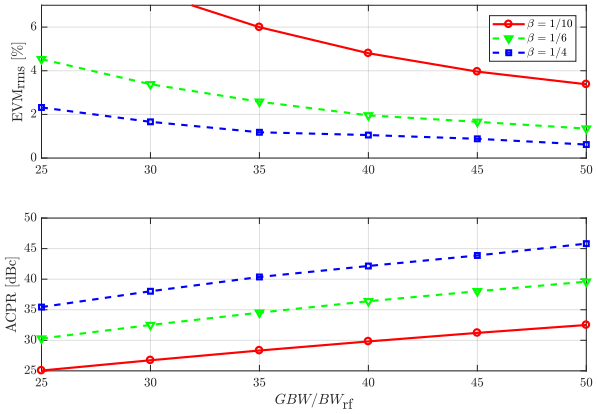

Fig. 8: Linearity of the system as a function of the ratio between the gain-bandwidth product of the operational amplifier GBW and the RF signal bandwidth BW_{rf}, for different values of return ratio β, for the EA from Fig. 3.

In the EA from Fig. 3, the series transistor in the Linear

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regulator is usually RF power MOSFET (or even GaN HEMT [37]), thus minimizing the effect of the parasitic capacitances of the transistor in MHz frequency range (e.g. up to 5 MHz). Assuming that the small-signal gain from the output of the operational amplifier to the EA output (v_{out}) is roughly 1 and that its maximum slew-rate is high enough to avoid non-linear distortion, the EA can be modeled using the transfer function of the operational amplifier $A(s) = GBW/s$, where GBW is the gain-bandwidth product of the operational amplifier. In Fig. 8 the linearity of the EER transmitter from Fig. 3 is shown for different values of the ratio between the gain-bandwidth product of the operational amplifier GBW and the RF signal bandwidth BW_{rf} and for three different values of the return ratio of the feedback loop $\beta = R_2/(R_1 + R_2)$, where the only non-ideal component is the operational amplifier. The value of β is chosen according to the needed output voltage swing of the EA and the voltage ratings of the operational amplifier. According to the simulation results, to achieve an ACPR > 40 dBc and EVM $< 3\,\%$, the product $\beta \times \frac{GBW}{BW_{\text{rf}}}$ roughly needs to have a value of at least 8.5, or written in a different way:

$$GBW > \frac{8.5 \times BW_{\text{rf}}}{\beta}. \tag{9}$$

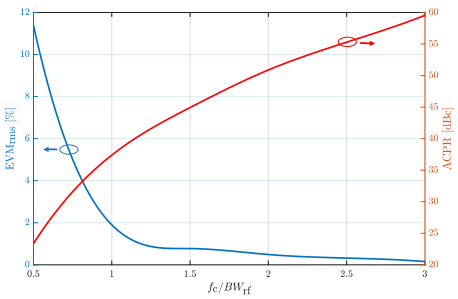

Fig. 9: Linearity of the system in the case of a fourth-order Legendre-type output filter as a function of the ratio between the filter cut-off frequency f_{c} and the RF signal bandwidth BW_{rf}, for the EA from Fig. 4.

The bandwidth of the EA from Fig. 4 is determined by the characteristics of the output filter, since the analog multiplexer can provide voltage levels with very low output impedance. The filter design for this type of application is based on standard filter prototypes with flat magnitude characteristics in pass-band, such as: Butterworth, Bessel and Legendre. Although passband ripple has a negligible effect in these filter prototypes, bandwidth, group delays and switching frequency ripple have to be taken into account [29]. The order of the filter for this type of application (both the input and the output of voltage source type) is always even: it consists of several LC sections. In this case, a fourth order filter is chosen. The quantitative evaluation of the filter types is also implemented in terms of two key parameters: EVM and ACPR.

The example in Fig. 9 shows the functionality of the software tool and the influence of EA output filter transfer function on EER transmitter linearity, for the EA shown in Fig. 4. Purely switched PWM EA is assisted with a fourth order Legendre-type output filter and modeled at the level of input-to-output transfer function. The RF signal (16-QAM or 64-QAM modulations) bandwidth is denoted by f_{BW}, and f_c is the cut-off frequency of the filter. The elements are calculated according to the load resistance of the EA, and the switching noise and all other system non-idealities are neglected. The curves show the following results: the ACPR of 45 dBc is achievable with $f_c/f_{\text{BW}} = 1.51$, and the EVM of 1% with $f_c/f_{\text{BW}} = 1.186$. These results are quite different from those seen in [30], where for $(C/I)_{\text{max}} \geq 45$ dBc, and the needed ratio is $B_{\text{EA}}/BW_{\text{rf}} \geq 4$. There are two main reasons for these discrepancies, which result in better performance with a lower f_c/f_{BW} ratio. First of all, a real filter prototype (Legendre) is used instead of the Fourier series truncation, and an example of QAM modulated signal is utilized instead of a two-tone test signal.

Since this analysis does not take into account the switching behavior of the EA, which is of crucial importance for the transmitter linearity, the following examples represent the simulation conducted using the described software tool analyzing the data from VHDL-AMS mixed-signal simulation, where the EA is simulated together with the control hardware. All the circuit parasitics, such as series resistances, forward voltage drops, and gate driver issues are neglected.

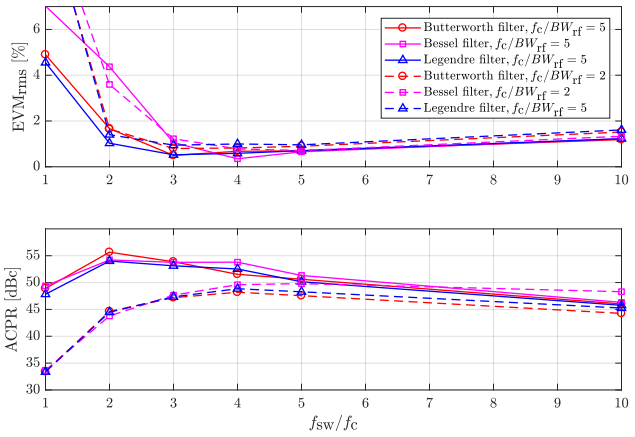

Fig. 10: Linearity of the system in the case of a fourth-order Butterworth, Bessel and Legendre output filters as a function of the ratio between the switching frequency f_{sw} and the filter cut-off frequency f_{c} with two different RF signal bandwidths BW_{rf}, for the EA from Fig. 4.

In order to identify the optimal output filter design alternative, the linearity of the system in the case of implementing fourth-order Butterworth, Bessel and Legendre filters is analyzed over the wide range of the converter switching frequencies ($f_{\text{sw}} = f_{\text{c}}$ to $f_{\text{sw}} = 10\,f_{\text{c}}$) for two RF signal bandwidths ($BW_{\text{rf}} = f_{\text{c}}/2$ and $BW_{\text{rf}} = f_{\text{c}}/5$), and a high resolution control hardware clock frequency ($400\,f_{\text{c}}$), as seen in Fig. 10. It can be seen that the Legendre and Butterworth filters satisfy the required system linearity even at $f_{\text{sw}} = 2f_{\text{c}}$, for both RF signals. Below this value the sampling rate of the envelope signal may be too low (especially in the case when $BW_{\text{rf}} = f_{\text{c}}/2$)) while the output voltage ripple takes on high values, provoking an increased distortion. Even

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though EVM strongly depends on the filter type at a low switching frequency, ACPR metrics show different behavior: these values do not depend on the filter type, but rather on the RF signal bandwidth. According to this simulation, the Legendre fourth-order output filter gains a mild advantage over the Butterworth filter at low frequencies, and consequently the Legendre filter is chosen for the final design. At high switching frequencies, both EVM and ACPR aggravate due to the finite time resolution effects, which are discussed below.

The digital PWM process is counter based and double-sided, counting from zero to a maximum value, and then from the maximum value to zero, thus creating a symmetrical triangular carrier. When PWM is implemented on the digital hardware (usually FPGA), the time resolution is given by the maximum achievable clock rate f_{CLK}. The resolution of the modulation expressed in the number of bits is:

$$n_{\mathrm{bits}} = \log_2\left(\frac{f_{\mathrm{CLK}}}{2\,f_{\mathrm{SW}}}\right). \tag{10}$$

Since the duty cycle of the control pulses is amplitude-quantized with the maximum number of achievable values, the theoretical value of the signal-to-noise ratio assuming a full-scale input sine wave from the range $[0, f_{\mathrm{SW}}/2]$ and a resolution of n_{bits} [38], is:

$$\mathrm{SNR} = 6.02\,n_{\mathrm{bits}} + 1.76\,\mathrm{dB}. \tag{11}$$

It is worth mentioning that this resolution applies not to the full range of the output voltage, but only to one quarter. In other words, the resolution of the output voltage is not $\frac{V_{\mathrm{IN}}}{2^{n_{\mathrm{bits}}}}$, as in the case of the simple two-level buck converter. In this case, the equivalent resolution is four times better, due to the five-level PWM modulation:

$$\Delta v_{\mathrm{out}} = \frac{V_{\mathrm{IN}}}{4 \times 2^{n_{\mathrm{bits}}}} \tag{12}$$

This means that with this type of modulation, the equivalent number of bits is

$$n_{\mathrm{bits,5L}} = 2 + \log_2\left(\frac{f_{\mathrm{CLK}}}{2\,f_{\mathrm{SW}}}\right). \tag{13}$$

Finally, the equivalent signal-to-noise ratio for this multi-level modulation in the sine-wave case is:

$$\mathrm{SNR}_{\mathrm{eq}} = 6.02\,n_{\mathrm{bits}} + 13.8\,\mathrm{dB}. \tag{14}$$

According to [39], this data is correlated with the theoretical limit of the EVM. For data-aided receivers, the relationship is

$$\mathrm{EVM} = \frac{1}{\sqrt{\mathrm{SNR}_{\mathrm{eq}}}}. \tag{15}$$

while this relationship is modified for non–data aided receivers, as stated in [40].

Firstly, the effects of the modulation carrier type are considered. The discussion for the signal-to-noise ratio and bit resolution have been conducted for symmetrical triangular double-update carrier (Eq. (10) - (14)), although another widely used option is a saw-tooth trailing edge single-update carrier. The

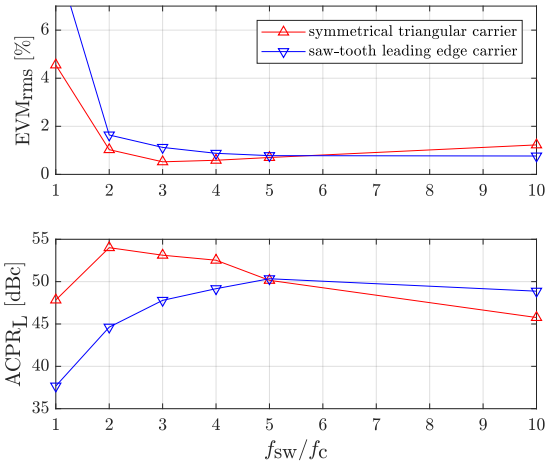

Fig. 11: Comparison of system linearity as a function of the ratio between the switching frequency f_{sw} and the output filter cut-off frequency f_{c}, in the case of a symmetrical triangular carrier and a saw-tooth trailing edge carrier for the analyzed PWM-switched five-level EA from Fig. 4, where $f_{\mathrm{c}}/BW_{\mathrm{rf}} = 5$ and $f_{\mathrm{clk}}/f_{\mathrm{c}} = 400$.

linearity comparison for these two cases is shown in Fig. 11. At low switching frequencies, the triangular carrier is more advantageous, because the sampling rate of the modulator is two times higher than in the case of the saw-tooth carrier. At high switching frequencies ($f_{\mathrm{sw}}/f_{\mathrm{c}} \geq 5$) the modulation based on the saw-tooth carrier starts to dominate due to slightly better resolution of modulation, and the linearity is better for this type of carrier. Globally, the best linearity is achieved with a symmetrical triangular carrier; therefore this type of carrier should be chosen. This linearity advantage can be explained by the small-signal transport delay of modulators, which is constant in the case of the symmetrical triangular carrier ($T_{sw}/2$), and dependent on the duty-cycle in the case of the saw-tooth trailing edge carrier ($D\,T_{sw}$) [41]. Hence better delay matching between the supply voltage and the phase drive can be achieved in the power amplifier if the symmetrical triangular carrier is utilized.

The effects of the finite time resolution of the control hardware are analyzed in two cases, when the ratio between the output filter cut-off frequency and the RF signal bandwidth has two different values ($f_{\mathrm{c}}/BW_{\mathrm{rf}} = 5$ and $f_{\mathrm{c}}/BW_{\mathrm{rf}} = 2$). The general conclusion is that the optimal value of the ratio $f_{\mathrm{sw}}/f_{\mathrm{c}}$ moves down with the reduced clock frequency of the control hardware, as can be seen in Fig. 12. At low values of the ratio ($f_{\mathrm{sw}}/f_{\mathrm{c}} < 2$) the distortion is pronounced due to the low switching frequency, while at the high values the dominant effect is pulse width resolution reduction and consequently all the curves are monotonically increase for $f_{\mathrm{sw}}/f_{\mathrm{c}} > 3$. The optimal values of the ratio $f_{\mathrm{sw}}/f_{\mathrm{c}}$ are in the closed interval:

$$\frac{f_{\mathrm{sw}}}{f_{\mathrm{c}}} \in [2, 4]. \tag{16}$$

In order to achieve an acceptable linearity, the ratio $f_{\mathrm{clk}}/f_{\mathrm{c}}$ should not be lower than 100, and the ratio $f_{\mathrm{c}}/BW_{\mathrm{rf}}$ should not be lower than 2, or in a different form:

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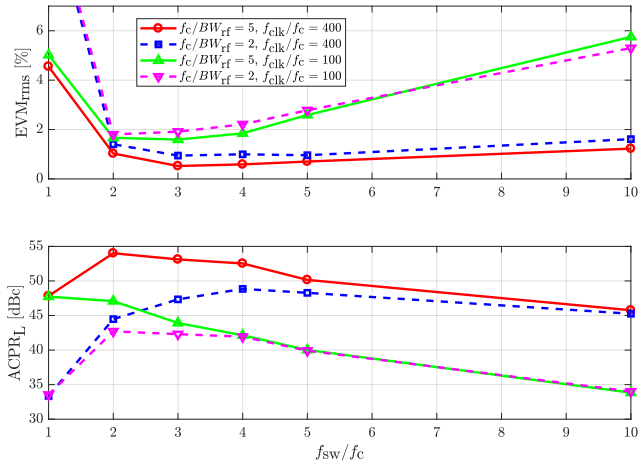

Fig. 12: Linearity of the system as a function of the ratio between the switching frequency f_{sw} and the output filter cut-off frequency f_c, for different values of RF signal bandwidth BW_{rf} and the digital control hardware clock frequency f_{clk}, for the EA from Fig. 4.

$$\frac{f_c}{BW_{rf}} \geq 2 \wedge \frac{f_{clk}}{BW_{rf}} \geq 200. \tag{17}$$

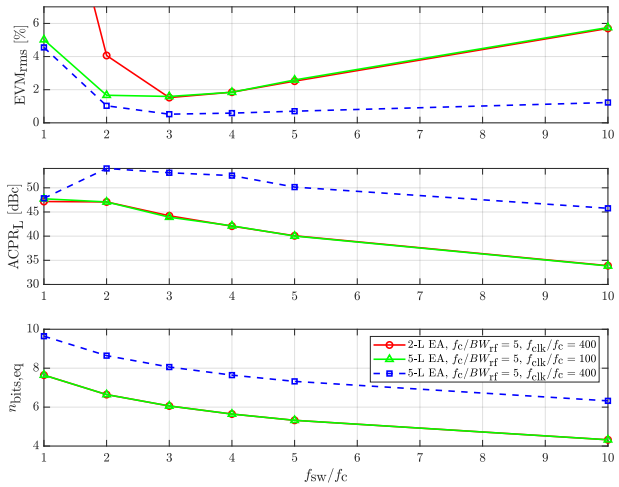

Fig. 13: Comparison of system linearity and the equivalent output voltage resolution in number of bits $n_{bits,eq}$ as a function of the ratio between the switching frequency f_{sw} and the output filter cut-off frequency f_c, for a simple two-level buck EA and the analyzed five-level EA from Fig. 4, with the same output filter.

Finally, the advantage in the number of voltage levels, seen as an increment in the signal-to-noise ratio (Eq. (11), (14)) and its corresponding reflections on EVM and ACPR, can be also proven by simulation. In Fig. 13, a comparison of system linearity as a function of the ratio between the switching frequency f_{sw} and the output filter cut-off frequency f_c is shown for a simple two-level buck EA and the analyzed five-level EA from Fig. 4, with the same output filter. It can be seen that at high values of f_{sw}/f_c, the behavior of the analyzed five-level EA is equivalent to the behavior of the two-level buck converter with a time resolution four times better. This is in accordance with Eq. (12), (14). In other words, in the case of 5-level modulation, the control hardware time resolution is less restrictive, while the acceptable linearity can be achieved at lower switching frequencies ($f_{sw}/f_c = 2$). The limitations expressed in number of bits n_{bits} reduces to $n_{bits} \geq 6$, which means that the minimal acceptable PWM resolution is 6 bits in the case of the simple two–level buck converter, while it is 4 bits in the case of the five level PWM switched EA.

IV. Design of Prototypes for the Analyzed EER Transmitters

A. Design of the Linear Assisted EA

Since this converter does not contain any dynamic element, its bandwidth is determined by the bandwidth of the operational amplifier (LM6172) used in the local feedback loop with the series transistor (BLF177). The reported gain-bandwidth product of the operational amplifier is 100 MHz. The return ratio of the feedback loop is designed to be about $\beta = 1/5$. According to Eq. (9), the maximum achievable RF bandwidth of the transmitter based on this EA, with ACPR > 40 dBc and EVM $< 3\,\%$, is about 2.5 MHz. Another concern in this design, which is not included in Eq. (9) is the finite PSSR (Power Supply Rejection Ratio) of the linear regulator. Although the voltage level switching (v_{ML} in Fig. 4) is proffered in order to boost the EA efficiency, it causes excessive voltage spikes in the output voltage v_{out}. In a general case, the PSRR is falling with the increased drive frequencies. The linear regulator stage is supplied with pulsating voltage whose transitions between two levels are as fast as 5 ns ($SR = 1.2$ V/ns). The spectral content of this voltage is pushed up to high frequencies, where the PSRR is low. In the parasitic capacitances of the series transistor, excessive currents are generated, which cause the deformation in the output voltage, seen as voltage spikes. This behavior changes the spectral content at higher frequencies of the EA output voltage, finally deteriorating EVM and ACPR at the power amplifier output. In order to protect the output voltage waveform from this noise, a PSRR improvement filter with damping can be used [42], placed between the analog multiplexer and the linear regulator stage. The dv/dt can also be successfully limited by adding an external miller capacitor, connected between the gate and drain of the transistors in the analog multiplexer. However, this solution results in some drawbacks such as increased switching losses and worsening of the shoot-through and/or cross conduction problem, as explained in [43]. Another option in this case is a small lossless LC filter between the EA and the RF PA, which is adopted in this design. The prototypes with Si transistors (FDMS7620S in the voltage divider, BSZ060NE2LS in the analog multiplexer and VSSAF3L45-M3 diodes) for the linear assisted switched capacitor based envelope tracker are fabricated and verified. The specifications are given as follows:

- Input DC voltage: 24 V;
- Output voltage range: $0 - 21$ V;
- Peak output power: 11.5 W;
- Average output power: 2 W;
- Maximum tested RF signal bandwidth: 4 MHz.

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TABLE I: The values of the output filter elements

f_c [MHz]	L_1 [μH]	C_1 [nF]	L_2 [μH]	C_2 [nF]
1.15	10.0	5.1	8.9	2.0

B. Design of the PWM switched EA

The bandwidth of the second converter is determined by characteristics of the output filter, since the analog multiplexer can provide voltage levels with very low output impedance. The distortion in the system affected by the output filter type, the ratio between the filter cross-over frequency and the converter switching frequency, and the effects of finite time resolution of the control pulses are well analyzed in the Section III. Additionally, hardware imperfections in this prototype can significantly contribute to the output signal distortion.

The gate driver is a source of two problems. Firstly, gate signal jitter introduces wideband noise to the converter output, mainly due to the digital signal isolators [44]. Additionally, at certain moments during the modulation process a very low (or very high) value of the duty-cycle may be required. The minimum pulse-width which can be provided by the driver (EL7158) is about 25 ns. This means that for a 5 MHz switching frequency, the minimum duty-cycle is 12.5 % (and the maximum duty-cycle is 87.5 %). This problem worsens with higher switching frequencies, which might introduce serious distortion in the output voltage. In this prototype, the switching frequency of 3 MHz is adopted. Finally, the output filter was designed for that switching frequency and with a bandwidth (cut-off frequency) of 1.15 MHz ($f_{sw}/f_c = 2.6$), following the guidelines stated in Eq. (16), (17). The measured values of the implemented filter elements are given in Table 1. These filter values are determined based on the assumption that the drain supply terminal of the saturated power amplifier can be modeled approximately as a pure resistance [28], with the value of about 45 Ω in this case. This prototype was made using Si-based semiconductors (BSZ060NE2LS transistors and VSSAF3L45 diodes), multi-layer ceramic chip capacitors and off-the-shelf Ferroxcube inductors (in the output filter). The specifications are the same as for the Linear assisted EA, except the maximum tested tracking bandwidth, which is only 700 kHz ($f_c/BW_{rf} = 1.64$) in this case.

C. Power loss estimations

Although the emphasis of this paper is put on the linearity analysis of the envelope amplifier, the power losses model is also presented in order to make the comparison more comprehensive. The losses in both envelope amplifiers can be separated into three groups: conduction losses in the analog multiplexer, gate driving and switching losses in the analog multiplexer, and the losses in the shaping filter. Except the expressions for losses in the output shaping filter, all other expressions for power loss estimation are unified and can be applied to both linear assisted and PWM switched envelope amplifier with small adjustments.

Conduction losses in the analog multiplexer, gate driving losses and switching losses in the analog multiplexer caused by the voltage-current coexistence on controlled switches during the turn-on and turn-off process ($P_{sw,on}$, $P_{sw,off}$) can be easily calculated using [45]. The losses associated with reverse recovery of the series diodes ($D_2 - D_4$) are neglected since Schottky diodes are utilized. Moreover, reverse recovery of the body diodes of the controlled switches does not happen either since these diodes are never polarized to conduct in the normal operation of the analog multiplexer, except for the switch S_5 in PWM switched EA (Fig. 4).

In order to properly evaluate the losses associated with the output capacitances of the switches and the junction capacitances of the diodes, a thorough analysis must be conducted. At the turn-on of each controlled switch, a forced commutation occurs provoking additional power loss, while each turn-off transition is self-commutated, as can be seen in Fig. 14. The corresponding dissipated energy at each one of the turn-on transitions can be calculated using the following expression:

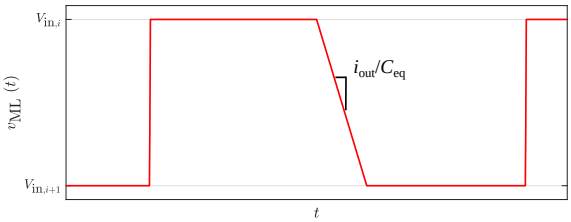


Fig. 14: The voltage of the switching node. Forced commutation at the turn-on transistor M_i (or S_i) is fast and determined by its turn-on time, while self commutation at its turn-off is slower with a slope i_{out}/C_{eq}, where C_{eq} is a charge-equivalent output capacitance of the switching node. High-frequency oscillations due to hard turn-on of the switch are not shown.

$$E_{dissipated} = E_{initial} + \Delta E - E_{final} \tag{18}$$

The initial and final energy of the system are defined as:

$$E_{initial} = \sum_{i=1}^{N_{sw}} E_{oss,i}(v_{oss0,i}) + \sum_{i=1}^{N_d} E_{j,i}(v_{j0,i}) \tag{19}$$

$$E_{final} = \sum_{i=1}^{N_{sw}} E_{oss,i}(v_{oss,i}) + \sum_{i=1}^{N_d} E_{j,i}(v_{j,i}) \tag{20}$$

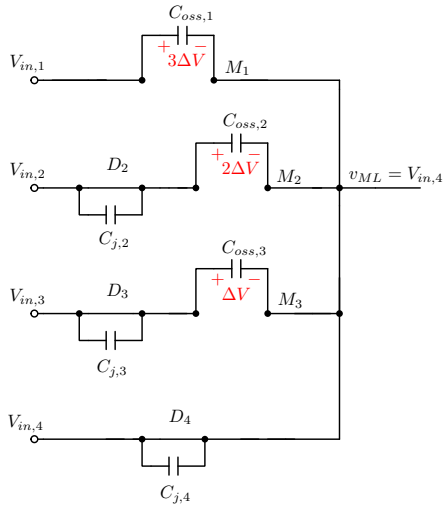
where N_{sw} is the number of controlled switches and N_d is the number of diodes in the analog multiplexer. The accumulated energy E_{oss} in C_{oss} of a conducting controlled switch and the accumulated energy E_j in C_j of a forward polarized diode is zero.

The energy delivered into the system by the input power sources is defined as:

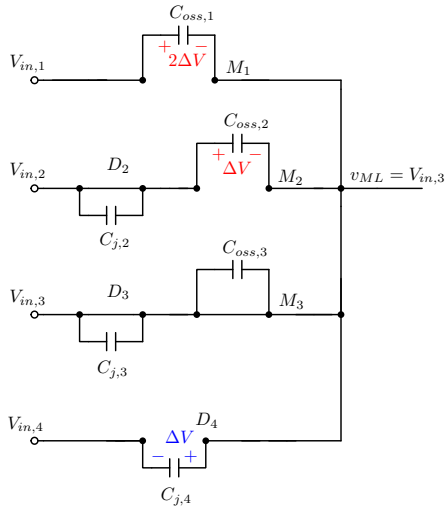
$$\Delta E = \sum_{i=1}^{N_{src}} V_{in,i} \Delta Q_i \tag{21}$$

where ΔQ_i is the charge delivered by each power source during the forced commutation.

For example, when the controlled switch M_2 in Linear assisted EA (Fig. 15) turns-on, the initial, final and delivered energy are described by Eq. (22)-(24) respectively, hence the dissipated energy during this transition is calculated using (18).



(a) Initial state.



(b) Final state.

Fig. 15: Accumulated energy in the parasitic output capacitances before and after the turn-on transition of the switch M_2. Forward voltage drops of the diodes are neglected.

$$E_{\text{initial}} = E_{\text{oss,1}}(3\Delta V) + E_{\text{oss,2}}(2\Delta V) + E_{\text{oss,3}}(\Delta V) \quad (22)$$

$$E_{\text{final}} = E_{\text{oss,1}}(2\Delta V) + E_{\text{oss,3}}(\Delta V) + E_{\text{j,4}}(\Delta V) \quad (23)$$

$$\begin{aligned}\Delta E = {} & V_{\text{in,1}}\Delta Q_{\text{oss,1}}(3\Delta V \to 2\Delta V) \\ & + V_{\text{in,2}}\Delta Q_{\text{oss,2}}(2\Delta V \to \Delta V) - V_{\text{in,4}}\Delta Q_{\text{j,4}}(0 \to \Delta V) \\ & + V_{\text{in,3}}[\Delta Q_{\text{j,4}}(0 \to \Delta V) - \Delta Q_{\text{oss,2}}(2\Delta V \to \Delta V) \\ & - \Delta Q_{\text{oss,1}}(3\Delta V \to 2\Delta V)]\end{aligned} \quad (24)$$

where ΔV is the difference between two adjacent input voltages $V_{\text{in},i}$ and $V_{\text{in},i-1}$.

The amount of charge $\Delta Q_{\text{j/oss}}(V_1 \to V_2)$ and energy $E_{\text{j/oss}}(V)$ is defined as follows:

$$\Delta Q_{\text{j/oss}}(V_1 \to V_2) = \int_{V_1}^{V_2} C_{\text{j/oss}}\, dv \quad (25)$$

$$E_{\text{j/oss}}(V) = \int_{0}^{V} C_{\text{j/oss}} \cdot v\, dv \quad (26)$$

where the curves for voltage dependent nonlinear capacitances C_{j} and C_{oss} can be found in Datasheet data of the devices [46], [47].

Similarly, the dissipated energy for all forced commutations can be calculated and the average power C_{oss}-C_{j}-related loss can be calculated keeping in mind the repetition rate of each transition.

The shaping filter in the case of Linear assisted EA is the linear regulator whose power loss $P_{\text{sf,LA}}$ is calculated as proposed in [25]. In case of the PWM switched EA, the losses in the output filter are estimated based only on the winding losses in the inductors L_1 and L_2, assuming that the current ripple is dominantly present in L_1:

$$P_{\text{sf,PWM}} = (R_{\text{dc,1}} + R_{\text{dc,2}})\, I^2_{\text{out,rms}} + R_{\text{ac}} I^2_{\text{ripple,rms}} \quad (27)$$

Finally, the total average power loss is:

$$P_{\text{total, EA}} = P_{\text{cond}} + P_{\text{g}} + P_{\text{sw,on}} + P_{\text{sw,off}} + P_{\text{oss,j}} + P_{\text{sf}}. \quad (28)$$

Based on the presented power loss model, the power loss estimations for both Linear assisted and PWM switched EA are shown in Fig. 16. In order to compare the performance of the analyzed envelope amplifiers, a breakdown of calculated losses is presented in Fig. 17, for the same 500 kHz 64QAM envelope reference and the same output power of $P_{\text{out}} = 2.46$ W. Calculated losses are divided into three groups as follows: conduction losses in the analog multiplexer, shaping filter losses, and losses caused by switching operations ($P_{\text{g}} + P_{\text{sw,on}} + P_{\text{sw,off}} + P_{\text{oss,j}}$). As a general conclusion, losses in Linear-assisted PA are much higher - over 3.5 times, and the losses in the shaping filter (linear regulator in this case) dominate with 93.4% of overall power losses. On the other hand, in PWM-switched EA the losses caused by switching operations prevail, with 75.9% of overall losses.

D. Design of the Suboptimal Class-E PA

In order to test the behavior of EER transmitters based on the previously analyzed EAs, a sub-optimal class-E power amplifier [48] (Fig. 18) has been designed, fabricated and tested for the peak output power of 10 W and carrier frequency range from 2.1 GHz to 2.6 GHz (S-band transmitter). Amplitude modulation (AM) of the class-E amplifier is possible due to the fact that the amplitude of the output voltage of the Class-E ZVS PA is directly proportional to the supply voltage, as explained in [49]. It is also reported that in practical realizations harmonic distortion of the envelope of the AM output voltage occurs. The switch SW in the prototype is

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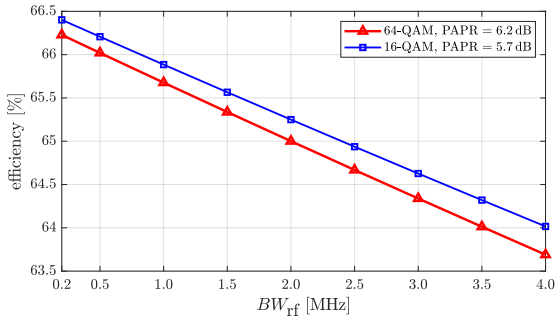
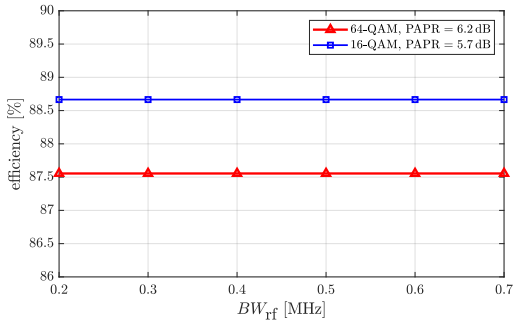
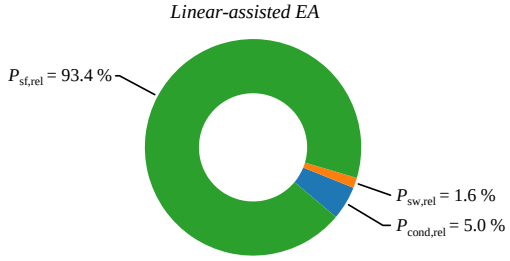


(a) Linear Assisted EA.

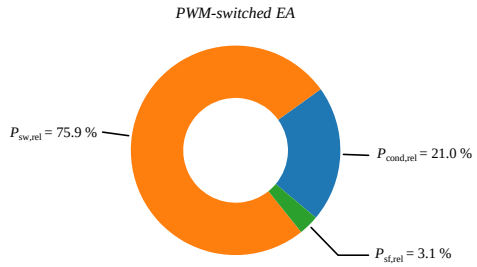


(b) PWM-switched EA, $f_{\mathrm{sw}} = 3\,\mathrm{MHz}$.

Fig. 16: Calculated efficiency of the analyzed envelope amplifiers for RF signals of different bandwidths BW_{rf}. The efficiency in case of processing of 64QAM signal is always lower than for 16QAM signal because of an elevated PAPR.



(a) Linear-assisted EA, $P_{\mathrm{loss}} = 1.27\,\mathrm{W}$, $\eta = 66.02\,\%$.



(b) PWM-switched EA, $P_{\mathrm{loss}} = 0.35\,\mathrm{W}$, $\eta = 87.55\,\%$.

Fig. 17: Breakdown of calculated power losses in both envelope amplifiers for a 500 kHz 64QAM envelope reference and the same output power of $P_{\mathrm{out}} = 2.46\,\mathrm{W}$.

depletion mode GaN high-electron mobility transistor (HEMT) with the technical details shown in Table II.

Although only the small non-linear output capacitance of the transistor is used, at these carrier frequencies the design

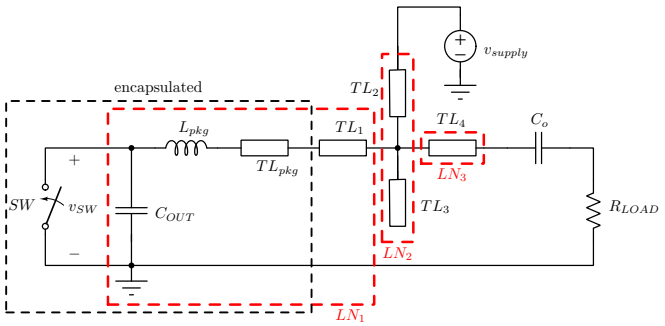


Fig. 18: Schematic of the suboptimal class-E power amplifier with depicted parasitics of the encapsulated GaN HEMT and matching networks LN_1, LN_3 which serve as $\lambda/4$ impedance transformers and LN_2 that serves as a parallel resonant tank.

TABLE II: Parameters of GaN HEMT utilized in suboptimal Class-E amplifier.

part number	$V_{\mathrm{ds,max}}$	C_{out}	P_{sat}
Cree CGH40010	84 V	1.3 pF	12.5 W

of nominal ZVS class-E PA is not possible since the conditions for ZVS and ZDS (Zero-Derivative Switching) cannot be satisfied [49]. Therefore, nominal class-E becomes suboptimal class-E PA [50]. An advantage of sub-optimal class-E PA over optimal class-E PA is the peak reduction of v_{DS} voltage, which is lower than $v_{supply} \times 2\pi \arctan\left(\frac{2}{\pi}\right) = 3.56\, v_{supply}$, which could potentially damage the GaN HEMT. Design of the resonant tank, input and output matching network, and RF choke inductor is based on microstrip transmission lines, since the distributed elements are sufficiently small and have lower losses than lumped elements in this frequency range. Double-reactance compensation principle is used since it permits a design of high efficiency PA in a wide frequency range [51]. As the design of the passive components is based on the transmission lines, four prototypes were implemented and the adjustments of the matching networks were done empirically in order to optimize the PA efficiency over the desired range of the supply voltage. The drain efficiency of all prototypes with respect to the supply voltage is shown in Fig. 19. It can be seen that the drain efficiency for the first and for the fourth prototype is always above 60%, in the range of interest, and the peak drain efficiency of the first prototype reaches 80 % and power-added efficiency reaches 76 %, for the peak output power at 2.4 GHz.

V. EER Transmitters Control

The target RF signals with the desired symbol-rate and roll-off factor were generated in MATLAB, modulating pseudo-random data in 16-QAM/64-QAM base-band modulator. In order to have a flexible design, where the synchronization of the envelope and the phase signal could be easily set and the delay between them finely adjusted, the control patterns have been stored in pulse function arbitrary generators [52]. Based on the RF signal envelope, control sequences for the envelope amplifiers have been created and stored, while unmodulated I

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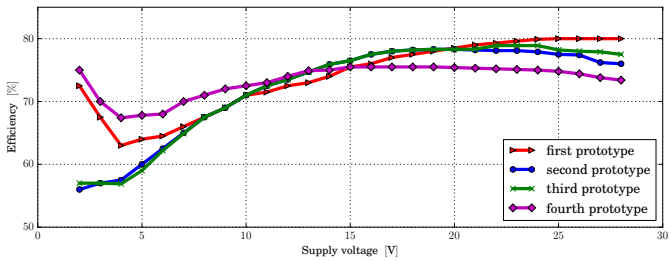

Fig. 19: Measured drain efficiency of the amplifiers for different supply voltages at 2.4 GHz.

and Q components of the constant envelope phase signal have been stored and then externally modulated at 2.4 GHz carrier frequency and fed to the driver for the class-E PA. Digital predistortion algorithms are not applied.

As already described, an important consideration for the switched-mode power converters is the pulse width resolution, especially in EER applications. Although this issue is not critical for the linear assisted EA where the analog reference for the EA is created in the direct digital synthesis process with a high resolution digital-to-analog converter and an anti-aliasing filter inside the signal generator, in the purely switched-mode EA this is of crucial importance because the complete information of the envelope is encompassed in the pulse width of the control signals. In this system, the time resolution is defined by the sampling frequency of the signal generator, which is given by (29):

$$F_{\mathrm{S}} = \frac{N_{\mathrm{max}}\, R_{\mathrm{sym}}}{N_{\mathrm{frame}}}, \tag{29}$$

where R_{sym} is the symbol rate of the test waveform ($R_{\mathrm{sym}} = \dfrac{BW_{\mathrm{rf}}}{1+\beta_{\mathrm{rc}}}$, β_{rc} is the roll-off factor of the raised-cosine filter used for pulse-shaping), N_{frame} is the number of symbols in a frame and N_{max} is the maximum length of the array of data points stored in the signal generator (2^{19}, in the case of Keysight 81150A pulse function arbitrary generator [52]).

According to Eq. (13), the equivalent resolution of the output voltage expressed in the number of bits is:

$$n_{\mathrm{bits,5L}} = 2 + \log_2\left(\frac{N_{\mathrm{max}}\, R_{\mathrm{sym}}}{2\, f_{\mathrm{SW}} N_{\mathrm{frame}}}\right). \tag{30}$$

Keeping in mind that the bit-resolution (Eq. 30) in this implementation is affected by the number of symbols in a frame, the number of symbols should be as small as possible. Nevertheless, this number should be as high as possible in order to have a valuable $I-Q$ representation of the demodulated signal. The minimum N_{frame} in the case of 16QAM modulation is adopted to be $N_{\mathrm{frame}} = 2^7$ and $N_{\mathrm{frame}} = 2^9$ in the case of 64QAM modulation, as a compromise between the signal deterioration caused by amplitude-quantization error and the suitable number for N_{frame}.

VI. Experimental Results

Photographs of both setups of EER transmitters are shown in Fig. 20.

Firstly, the behavior of both EAs is tested using a 50 Ω resistive load. In Fig. 21, the key voltage waveforms for the Linear assisted EA (the multilevel voltage and the EA output voltage) and for PWM switched EA (the filter input voltage and the EA output voltage) are presented, for a 1 MHz 64–QAM and a 312 kHz 64–QAM envelope reference, respectively. The samples of the envelopes are then saved and processed by applying the software tool and the preliminary values for the FOMs are obtained. The comparison of these values with the real values of the EER transmitters is presented in Subsection VI-C. A list of specifications for the experimental setups is included in Table III.

TABLE III: Specifications of the experimental setups

parts	part number
Input supply voltage	24 V
Max. RF PA supply voltage	21 V
carrier frequency	2.4 GHz
modulation type	16QAM and 64QAM
RF signal baseband bandwidth	up to 4 MHz
RF PA load	50 Ω

A. EER Transmitter with the Linear Assisted EA

The summary experimental results for the EER transmitter with the linear assisted EA is shown in Table IV. The bandwidth of the RF signal references varies from 1.56 MHz to 3.9 MHz. In Fig. 22 both time and spectral domain of the EER transmitter output voltage for a 3.9 MHz 64QAM signal reference are shown. As can be seen, an acceptable transmitter linearity can be achieved up to 2.5 MHz of RF signal bandwidth. The figures of merit are further worsened by the glitches in the EA output voltage, as already explained. The limitation in this case is imposed by the operational amplifier bandwidth, which controls the EA output voltage. This result is well in accordance with the result from Eq. (9), for $GBW = 100$ MHz and $\beta = 1/5$. Regarding the average efficiency of the power conversion, the approximate values of 32.5% and 28.5% are achieved in the case of 16QAM and 64QAM references, and the average output power of 1.95 W and 1.45 W, respectively. This difference is due to the different PAPR of the test waveforms. Since the switching frequency of the analog multiplexer increases for the faster RF signal bandwidth, the losses in the EA arise, so the average efficiency reduces.

B. EER Transmitter with the PWM Switched EA

The summary experimental results for the EER transmitter with the PWM switched filter assisted EA is shown in Table V. The bandwidth of the RF signal references in this case varies from 332.8 kHz to 665.6 kHz, for the converter switching frequency of $f_{\mathrm{sw}} = 3$ MHz and the output filter cut-off frequency of $f_{\mathrm{c}} = 1.15$ MHz. In Fig. 23 both time and spectral domain of the EER transmitter output voltage for a 665 kHz 64QAM signal reference are shown. As can be seen, an acceptable transmitter linearity can be achieved up to 500 kHz of RF signal bandwidth, in the case of 16QAM test references. In this case the ratio of the filter cut-off frequency and the RF

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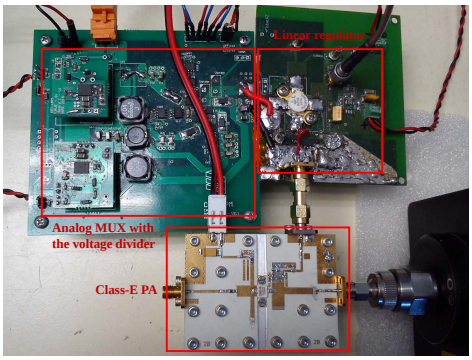
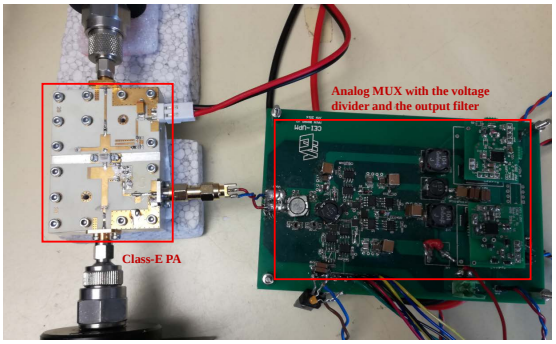
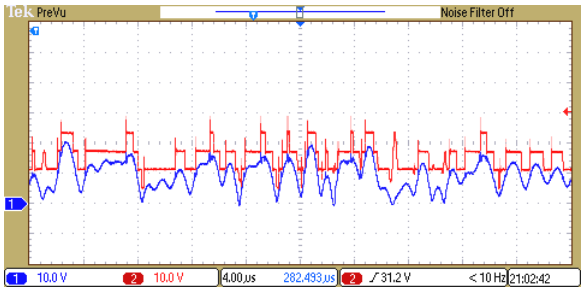


(a) A photograph of the first setup: Linear assisted EA with the class E PA.

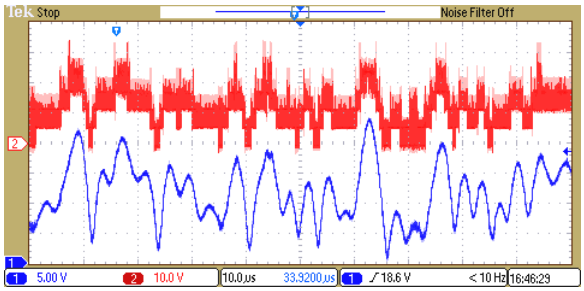


(b) A photograph of the second setup: PWM switched EA with the class E PA.

Fig. 20: Photographs of both EER transmitters setups.

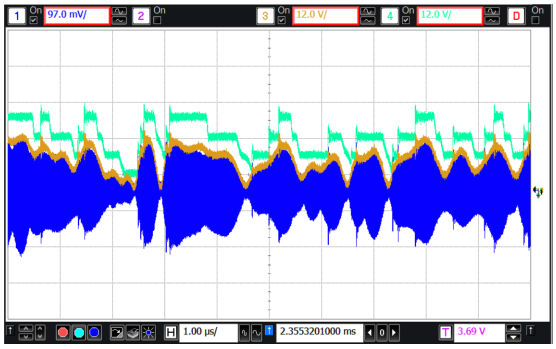


(a) Linear assisted EA: The multilevel voltage (red) and the EA output voltage (blue) in the case of a 1 MHz 64QAM signal. Scale: 10 V/div. Time scale: 4 μs/div.

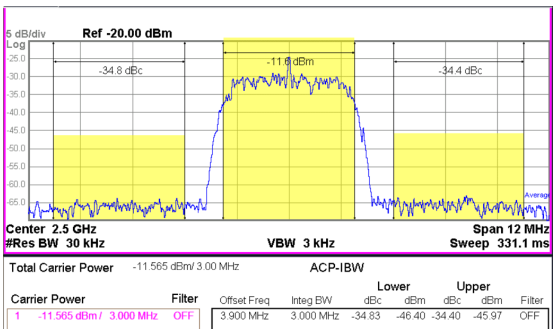


(b) The filter input voltage (red, scale: 10 V/div) and the EA output voltage (blue, scale: 5 V/div) in the case of a 312 kHz 64QAM signal. Timescale: 10 μs/div.

Fig. 21: The output voltage waveforms of both EAs in the case of a pure resistive load.



(a) Time domain voltage waveforms.



(b) Baseband spectrum of the output voltage.

Fig. 22: Experimental results obtained with the EER transmitter based on the Linear switched EA: the analog multiplexer output voltage, EA output voltage, and EER transmitter output voltage for a 3.9-MHz 64-QAM signal with the baseband spectrum.

TABLE IV: The summary of the experimental results for the Linear Assisted EA

RF signal bandwidth [MHz]	modulation type	PAPR [dB]	$ACPR_L$ [dBc]	$ACPR_R$ [dBc]	EVM [%]	output power [W]	efficiency [%]
1.56	16QAM	5.16	43.2	40.2	2.72	1.97	33.00
	64QAM	6.27	40.2	40.8	2.52	1.45	28.84
2.47	16QAM	5.16	41.0	39.7	2.90	1.97	32.67
	64QAM	6.27	40.2	40.3	2.73	1.45	28.47
3.9	16QAM	5.16	36.2	35.7	3.89	1.97	32.24
	64QAM	6.27	34.8	34.4	4.11	1.45	28.01

signal bandwidth is $f_c/f_{BW} = 2.3$, which is in accordance with Eq. (16). It turns out that this ratio is not enough in the case of 64QAM test references, since the transmitter linearity in this case is more jeopardized. Nevertheless, the limitations in this case are superimposed not only by the output filter bandwidth and the switching nature of the EA, but also with series voltage drops and the unpredicted behavior of the RF PA, which is not modeled. Regarding the average efficiency of the power conversion, the approximate values of 44% and 41% are achieved in the case of 16QAM and 64QAM references, and the average output power of $1.60\,\mathrm{W}$ and $1.15\,\mathrm{W}$, respectively. Once again, this difference is due to the different values of PAPR of the test waveforms.

C. Comparison with the Estimated FOMs

The values of the estimated FOMs, based only on the envelope signals measured on a resitive load (which are labeled as predicted values), are contrasted with the measured values obtained from both EER transmitters. The results are presented in Fig. 24 – 25. In the case of the Linear assisted EA, the predicted values of the FOMs were almost the same for both 16–QAM ad 64–QAM signals with the same baseband bandwidth and they are presented with the single line (Fig. 24). However, these values are different for the PWM switched EA and they are presented on two different lines.

Since the nonlinear behavior of the power amplifier described by AM–AM and AM–PM conversion is not modeled, some deviation in EVM and ACPR occurs. Another phenomenon that could lead to unpredicted signal deterioration is the loading effect of the power amplifier, as documented in [53]. The maximum differences between the values obtained by the software tool using the measurement results at a $50\,\Omega$ load and the values measured using the EER transmitters are as follows: $3.5\,\mathrm{dBc}$ and $4.86\,\mathrm{dBc}$, in the case of ACPR for the linear assisted and PWM switched EA, respectively, while in the case of EVM metrics these differences are $1.21\,\%$ and $0.5\,\%$. Even so, it can be concluded that there are no significant discrepancies between the predicted and the measured values of EVM and ACPR, especially in ACPR for both amplifiers, and a quite good estimation of the FOMs of an EER transmitter can be made by taking into account the behavior of the analyzed EA only.

VII. Conclusions

In this paper, two different approaches in supplying a 2.4 GHz class-E power amplifier (S-band) based on the EER technique are analyzed and compared in terms of the system linearity using EVM metrics to describe in-channel distortion, and ACPR metrics to describe out-of-channel emission. The employed envelope amplifiers are multilevel dc-dc converters based on the analog multiplexer assisted by the series linear regulator in the first system, and by the fourth order LC filter in the second system, thus providing supply modulation for the RF PA. Possible sources of non-linear distortion in both EAs are stated, and a software tool intended for linearity evaluation of envelope amplifiers is utilized without taking into account the non-linear effects of the power amplifier (AM-AM and AM-PM conversion). This tool can be successfully employed in the optimization process for the final choice of an envelope amplifier. The values of the figures of merit (EVM, ACPR) quantified by this way are roughly the theoretical limits that can be achieved. The acceptable values for the metrics adopted are as follows: $\mathrm{EVM}_{\max} = 3\%$ and $\mathrm{ACPR}_{\min} = 40\,\mathrm{dBc}$. In the case of Linear assisted EA, the minimum required gain-bandwidth product of the operational amplifier is proportional to the ratio between RF signal bandwidth and the return-ration of the feedback loop with a factor of 8.5. The Legendre type output filter is identified as the optimal solution in the case of PWM switched EA, with a cut-off frequency of at least two times higher than the RF signal bandwidth, which is less conservative than in [30], where a ratio $B_{EA}/BW_{rf} = 3$ for $(C/I)_{\max} = 41.87$ is proposed. The switching frequency should be at least two times higher than the cut-off frequency and a sufficiently good time resolution of the digital hardware controller ($f_{clk} > 100\,f_c$) should be maintained. It is shown that at low switching frequencies ($< 2\,f_c$), the system linearity is jeopardized due to the high switching ripple and low sampling rate of the envelope signal, while at high switching frequencies ($> 4\,f_c$), the dominant effect is the reduced PWM modulation resolution. Lower switching frequencies are beneficial from the point of view of power converter efficiency, and such a design is also less prone to hardware imperfections that arise with high switching frequencies. Using this methodology, the minimum switching frequency and the minimum digital control hardware clock frequency can be easily identified.

To back-up these assertions, two S-band EER transmitters are fabricated and tested. It is proven that the second EER is more prone to both hardware and control issues that limit the maximum bandwidth of the system, although its power conversion efficiency is superior to the first EA. The analyzed EER transmitters can reproduce 16–QAM and 64–QAM signals up to 2.5 MHz manifesting an average efficiency of about 32%, with the first transmitter based on the Linear assisted EA and 16–QAM signals up to 660 kHz RF bandwidth and the average efficiency of 44%, with the second transmitter based on the PWM switched EA. The estimated results based only on the EAs are well in accordance with the real results of the transmitters, particularly in the case of the ACPR values. With this tool, design decisions for the EA bandwidth, filter type, switching frequency, modulation carrier type, and control pulse resolution could be made without the need for the EA to be integrated with a power amplifier during the design and optimization process.

Acknowledgment

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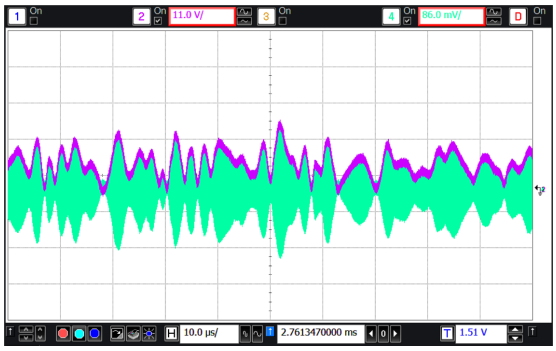
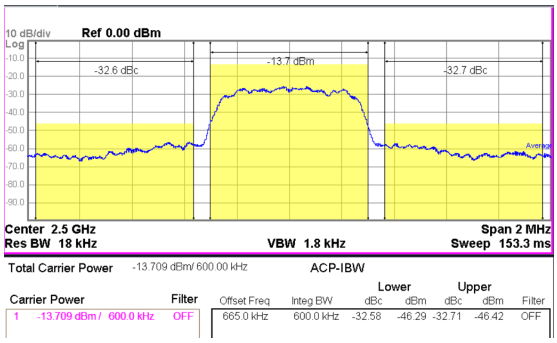


(a) Time domain voltage waveforms.



(b) Baseband spectrum of the output voltage.

Fig. 23: Experimental results obtained with the EER transmitter based on the PWM switched EA: EA output voltage and EER transmitter output voltage for a 665-kHz 64-QAM signal with the baseband spectrum.

TABLE V: The summary of the experimental results for the PWM switched EA

RF signal bandwidth [kHz]	modulation type	PAPR [dB]	$ACPR_L$ [dBc]	$ACPR_R$ [dBc]	EVM [%]	output power [W]	efficiency [%]
332.8	16QAM	5.1	36.7	37.3	1.28	1.58	43.95
	64QAM	7.6	33.5	33.5	6.42	1.13	40.43
499.2	16QAM	5.1	34.7	35.0	3.37	1.59	44.23
	64QAM	7.6	32.1	33.7	6.10	1.14	40.79
665.6	16QAM	5.1	34.4	34.2	4.49	1.60	44.51
	64QAM	7.6	32.6	32.7	6.03	1.15	41.14

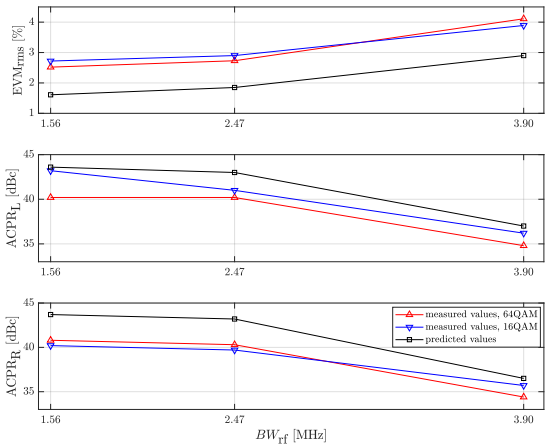


Fig. 24: Comparison of the predicted and measured EVM and ACPR values in the case of the Linear assisted EA.

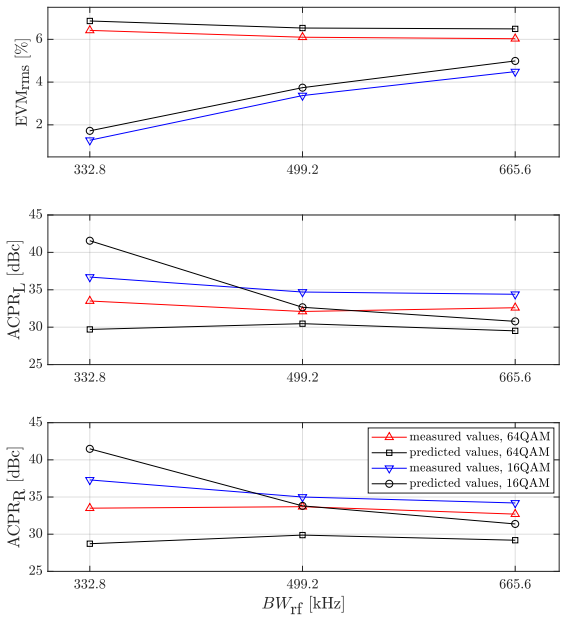


Fig. 25: Comparison of the predicted and measured EVM and ACPR values in the case of the PWM switched EA.

REFERENCES

[1] Leonard R. Kahn, "Single-Sideband Transmission by Envelope Elimination and Restoration",*Proceedings of the IRE*, 1952, pp. 803-806.

[2] Z. Wang, *Envelope tracking power amplifiers for wireless communications*, Artech House, Boston, 2014

[3] J. Hoversten, S. Schafer, M. Roberg, M. Norris, D. Maksimovic and Z. Popovic, "Codesign of PA, Supply, and Signal Processing for Linear Supply-Modulated RF Transmitters", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 60, no. 6, pp. 2010-2020, June 2012.

[4] O. García, M. Vasić, P. Alou, J. A. Oliver and J. A. Cobos, "An Overview of Fast DC-DC Converters for Envelope Amplifier in RF Transmitters," in *IEEE Transactions on Power Electronics*, vol. 28, no. 10, pp. 4712-4722, Oct. 2013.

[5] V. Yousefzadeh, E. Alarcon, D. Maksimović, "Three-level buck converter for envelope tracking applications", in *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 549-552, March 2006.

[6] M. Rodriguez, P. Fernandez-Miaja, A. Rodriguez, J. Sebastian, "A Multiple-Input Digitally Controlled Buck Converter for Envelope Tracking Applications in Radiofrequency Power Amplifiers", in *IEEE Trans. on Power Electronics*, Feb. 2010

[7] A. Soto, J. A. Oliver, J. A. Cobos, J. Cezon, and F. Arevalo, "Power supply for a radio transmitter with modulated supply voltage", in *Proc. IEEE Appl. Power Electron. Conf.*, 2004, vol. 1, pp. 392-398.

[8] M. Vasić *et al.*, "The Design of a Multilevel Envelope Tracking Amplifier Based on a Multiphase Buck Converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 6, pp. 4611-4627, June 2016.

[9] A. Cervera, M. M. Peretz, "Envelope Tracking Power Supply for Volume-Sensitive Low-Power Applications Based on a Resonant Switched-Capacitor Converter", in *IEEE APEC*, 2016.

[10] J. Sebastián, D. G. Lamar, D. G. Aller, J. Rodríguez and P. F. Miaja, "On the Role of Power Electronics in Visible Light Communication," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 3, pp. 1210-1223, Sept. 2018. doi: 10.1109/JESTPE.2018.2830878

[11] J. Rodríguez, D. G. Lamar, P. F. Miaja, D. G. Aller and J. Sebastián, "Power-Efficient VLC Transmitter Based on Pulse-Width Modulated DC-DC Converters and the Split of the Power," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1726-1743, Feb. 2019. doi: 10.1109/TPEL.2018.2830881

[12] Y. Zhang, M. Rodriguez and D. Maksimović, "Very High Frequency PWM Buck Converters Using Monolithic GaN Half-Bridge Power Stages With Integrated Gate Drivers," in *IEEE Transactions on Power Electronics*, vol. 31, no. 11, pp. 7926-7942, Nov. 2016. doi: 10.1109/TPEL.2015.2513058

[13] V. Ž. Lazarević *et al.*, "High Efficiency High Bandwidth Four-Quadrant Fully Digitally Controlled GaN-based Tracking Power Supply System for Linear Power Amplifiers," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*. doi: 10.1109/JESTPE.2018.2884959

[14] V. Yousefzadeh, E. Alarcon and D. Maksimovic, "Efficiency optimization in linear-assisted switching power converters for envelope tracking in RF power amplifiers," *IEEE International Symposium on Circuits and Systems*, 2005, pp. 1302-1305 Vol. 2.

[15] H. He, Y. Kang, T. Ge, L. Guo and J. S. Chang, "A 2.5-W 40-MHz-Bandwidth Hybrid Supply Modulator With 91% Peak Efficiency, 3-V Output Swing, and 4-mV Output Ripple at 3.6-V Supply," in *IEEE Transactions on Power Electronics*, vol. 34, no. 1, pp. 712-723, Jan. 2019. doi: 10.1109/TPEL.2018.2827396

[16] Y. Wang, X. Ruan, Y. Leng and Y. Li, "Hysteresis Current Control for Multilevel Converter in Parallel-Form Switch-Linear Hybrid Envelope Tracking Power Supply," in *IEEE Transactions on Power Electronics*, vol. 34, no. 2, pp. 1950-1959, Feb. 2019. doi: 10.1109/TPEL.2018.2835640

[17] M. Vasić, O. Garcia, J.A. Oliver, P. Alou, D. Diaz, J.A. Cobos, "Multilevel Power Supply for High-Efficiency RF Amplifiers," in *IEEE Transactions on Power Electronics*, vol. 25, no. 4, pp. 1078-1089, April 2010. doi: 10.1109/TPEL.2009.2033186

[18] Q. Jin, X. Ruan, X. Ren, Y. Wang and Y. Leng, "Step-Wave Switched Capacitor Converter for Compact Design of Envelope Tracking Power Supply," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 12, pp. 9587-9591, Dec. 2017. doi: 10.1109/TIE.2017.2716900

[19] Q. Jin, X. Ruan, X. Ren, Y. Wang, Y. Leng and C. K. Tse, "Series-Parallel-Form Switch-Linear Hybrid Envelope-Tracking Power Supply to Achieve High Efficiency," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 1, pp. 244-252, Jan. 2017. doi: 10.1109/TIE.2016.2595479

[20] L. Marco, E. Alarcon, D. Maksimović, "Effects of switching power converter nonidealities in envelope elimination and restoration technique", in *Proc. IEEE Int. Symp. Circuits Syst.*, 2006, pp. 3137-3140.

[21] P. F. Miaja, A. Rodríguez and J. Sebastián, "Buck-Derived Converters Based on Gallium Nitride Devices for Envelope Tracking Applications," in *IEEE Transactions on Power Electronics*, vol. 30, no. 4, pp. 2084-2095, April 2015. doi: 10.1109/TPEL.2014.2326046

[22] Y. Wang, Q. Jin and X. Ruan, "Optimized Design of the Multilevel Converter in Series-Form Switch-Linear Hybrid Envelope-Tracking Power Supply," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 9, pp. 5451-5460, Sept. 2016. doi: 10.1109/TIE.2016.2565459

[23] Q. Jin and M. Vasić, "Optimized Design of GaN Switched-Capacitor-Converter-Based Envelope Tracker for Satellite Application," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 3, pp. 1346-1355, Sept. 2017.

[24] M. Vasić *et al.*, "Envelope Amplifier Based on Switching Capacitors for High-Efficiency RF Amplifiers," in *IEEE Transactions on Power Electronics*, vol. 27, no. 3, pp. 1359-1368, March 2012. doi: 10.1109/TPEL.2011.2163646

[25] M. Vasić, O. García, J. A. Oliver, P. Alou and J. A. Cobos, "Theoretical Efficiency Limits of a Serial and Parallel Linear-Assisted Switching Converter as an Envelope Amplifier," in *IEEE Transactions on Power Electronics*, vol. 29, no. 2, pp. 719-728, Feb. 2014.

[26] J. Sebastián, P. Fernández-Miaja, F. J. Ortega-González, M. Patiño and M. Rodríguez, "Design of a Two-Phase Buck Converter With Fourth-Order Output Filter for Envelope Amplifiers of Limited Bandwidth", in *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5933-5948, Nov. 2014.

[27] Y. Zhang, M. Rodríguez, D. Maksimović, "Output filter design in high-efficiency wide-bandwidth multi-phase buck envelope amplifiers", in *IEEE APEC*, 2015, pp. 2026-2032.

[28] J. Hoversten, "Efficient and linear microwave transmitters for high peak-to-average ratio signals", Ph.D. dissertation, University of Colorado, May 2010.

[29] J. Sebastian, P. Fernandez-Miaja, A. Rodriguez, M. Rodriguez, "Analysis and design of the output filter for buck envelope amplifiers", in *IEEE Trans. on Power Electron.*, Jan. 2014

[30] F. H. Raab, "Intermodulation Distortion in Kahn-Technique Transmitters", in *IEEE Trans. Microw. Theory Techn.*, vol. 44, no. 12, pp. 2273 - 2278, December 1996

[31] L. C. Nunes, P. M. Cabral and J. C. Pedro, "AM/AM and AM/PM Distortion Generation Mechanisms in Si LDMOS and GaN HEMT Based RF Power Amplifiers", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 4, pp. 799-809, April 2014.

[32] D. Díaz, O. García, J. A. Oliver, P. Alou, J. A. Cobos, M. Patiño, and F. J. Ortega, "Design and optimization tool of a buck derived envelope amplifier for an eer rfpa," in *2014 IEEE 15th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2014, pp. 1-7

[33] Daniel Díaz, "High Efficiency Envelope Amplifier based on a Ripple Cancellation Buck Converter. Design, Optimization and Integration in an EER RFPA" (2014). *Tesis (Doctoral), E.T.S.I. Industriales (UPM).*

[34] V. Ž. Lazarević *et al.*, "A comparative analysis of two approaches in EER based envelope tracking power supplies," 2017 IEEE APEC, Tampa, FL, 2017, pp. 3252-3258. doi: 10.1109/APEC.2017.7931163

[35] Wikipedia contributors, "Atan2," *Wikipedia, The Free Encyclopedia*, [online] Available: https://en.wikipedia.org/wiki/Atan2

[36] Matejka, Stepan, "Analysis of Intermodulation Distortion in OFDM Based Transmitter Using EER Technique." *Radioengineering* 25.2 (2016): 391.

[37] Dongxue Li, M. Rodríguez, A. Zai, D. Sardin, D. Maksimović and Z. Popović, "RFPA supply modulator using wide-bandwidth linear amplifier with a GaN HEMT output stage," 2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL), Salt Lake City, UT, 2013, pp. 1-6. doi: 10.1109/COMPEL.2013.6626453

[38] W. Kester, *The Data Conversion Handbook*, Elsevier, 2005, ISBN: 0-7506-7841-0

[39] K. M. Gharaibeh, K. G. Gard and M. B. Steer, "Accurate estimation of digital communication system metrics – SNR, EVM and ρ in a nonlinear amplifier environment", *64th ARFTG Microwave Measurements Conference*, Fall 2004., 2004, pp. 41-44.

[40] H. A. Mahmoud, H. Arslan, "Error vector magnitude to SNR conversion for nondata-aided receivers", in *IEEE Transactions on Wireless Communications*, vol. 8, no. 5, pp. 2694-2704, May 2009.

[41] D. M. Van de Sype, K. De Gusseme, A. P. Van den Bossche and J. A. Melkebeek, "Small-signal Laplace-domain analysis of uniformly-sampled pulse-width modulators," 2004 *IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, Aachen, Germany, 2004, pp. 4292-4298 Vol.6. doi: 10.1109/PESC.2004.1354760

[42] M. Liu, D. Zhang, Z. Zhou, "Linear Regulator Design Considerations of the Serial Linear-Assisted Switching Converter Used as Envelope Amplifier", *IEEE Trans. on Power Electron.*, May 2016

[43] Guanghai Gong, "Hybrid Amplifier for AC Power Source Applications" (2008) *ETH PES PhD Thesis*

[44] M. Mauerer, A. Tuysuz and J. W. Kolar, "Low-Jitter GaN E-HEMT Gate Driver With High Common-Mode Voltage Transient Immunity," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9043-9051, Nov. 2017. doi: 10.1109/TIE.2017.2677354

[45] D. Graovac, M. Purschel, and A. Kiep, "MOSFET power losses calculation using the data-sheet parameters," Infineon Technol., Dresden, Germany, Jul. 2006, Appl. note

[46] BSZ060NE2LS Datasheet. Accessed: Jun. 17, 2019. [Online]. Available: https://www.infineon.com/

[47] VSSAF3L45 Datasheet. Accessed: Jun. 17, 2019. [Online]. Available: https://www.vishay.com/docs/89935/vssaf3l45.pdf

[48] F. H. Raab *et al.*,"Power amplifiers and transmitters for RF and microwave", in *IEEE Transactions on Microwave Theory and Techniques*, vol. 50, no. 3, pp. 814-826, Mar 2002.

[49] M. K. Kazimierczuk, *RF Power Amplifiers*, 2nd Ed. Wiley, 2014

[50] Z. Popović and J. A. García, "Microwave Class-E Power Amplifiers: A Brief Review of Essential Concepts in High-Frequency Class-E PAs and Related Circuits," in *IEEE Microwave Magazine*, vol. 19, no. 5, pp. 54-66, July-Aug. 2018. doi: 10.1109/MMM.2018.2822202

[51] F. J. Ortega-Gonzalez, D. Tena-Ramos, M. Patiño-Gomez, J. M. Pardo-Martin and D. Madueño-Pulido, "High-Power Wideband L-Band Suboptimum Class-E Power Amplifier," in *IEEE Transactions on Microwave*

Theory and Techniques, vol. 61, no. 10, pp. 3712-3720, Oct. 2013. doi: 10.1109/TMTT.2013.2279366

[52] Keysight 81150A and 81160A Pulse Function Arbitrary Noise Generator, Available online: http://literature.cdn.keysight.com/litweb/pdf/81160-91020.pdf (accessed date: 29 January 2019)

[53] Zhang, Yuanzhe, "High Frequency GaN Drain Supply Modulators for Radio-Frequency Power Amplifiers" (2015). *Electrical, Computer & Energy Engineering Graduate Theses & Dissertations*. 128.