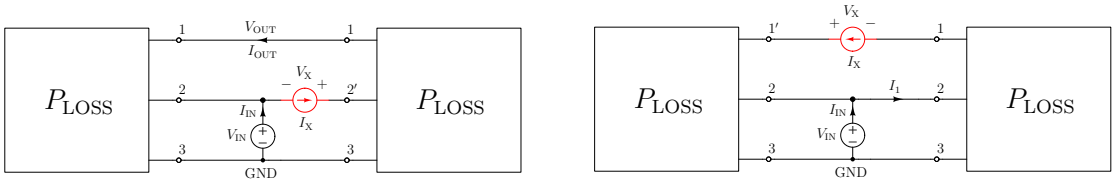


Fig. 4.19: Principle diagram of the back-to-back losses measurements of the open-loop operating voltage-fed converter: (a) Input current fed. (b) Output current fed.

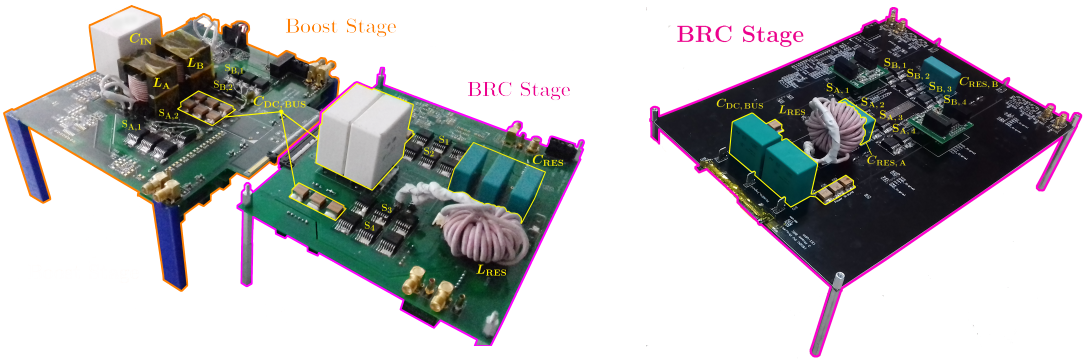
biggest in case of 1000-V PV string and 400-V ac grid connection, 85.19 % improvement in losses, and the smallest in case of 1500-V PV string and 800-V ac grid connection, 22.22 % loss improvement. This is also expected since in the case of 1500-V at dc and 800-V at ac side the difference between minimum dc bus voltage and maximum input voltage is the smallest. It is to say that in this case the allowed dc bus voltage variation at the input of the inverter stage is the smallest one. Still the output voltage profile of the hybrid topology presented in Section 3.1 (see the blue curve in Fig. 4.17) is the subject of optimization according to the yearly mission profile, grid connection, rated power, etc.

4.6 Back-to-Back Losses Measurement Technique for Voltage-Fed Converters Operating in Open Loop

As it was mentioned before, efficiency over 99 % is expected and due to this it was necessary to apply an appropriate losses measurements technique. Since multimeter measurements of the input and output power is not sufficiently precise and calorimetric method is time consuming and technically demanding, it was decided to proceed with back-to-back technique that represents a good compromise between previous two methods.

However, this method demands voltage and current loop to be closed. Since presented resonant stage operates in open loop, it was necessary to find another way to set a desired load value in which losses are going to be measured. The method that is proposed in [160] is not applicable to voltage-fed dc/dc converters.

Fig. 4.19 depicts the principle diagram of the opposition method that can be applied for the power losses measurements in the voltage-fed dc/dc converters that operate in open loop. It can be noticed that the two converters connected in back-to-back configuration and two isolated power sources are necessary, one to control operating point from the point of view of the input voltage (V_{IN}, I_{IN}) and another one to control the load condition (V_X, I_X). They can be arranged in two different ways. Fig. 4.19(a) represents the current feeding at the input side, while the load control at the output side is shown in Fig. 4.19(b). In both cases the value of the power losses is calculated according to the equation:



(a) (b)

Fig. 4.20: Photographs of the implemented prototypes: (a) Prototype of the proposed hybrid dc/dc topology. The two-phase boost is selected for the boost stage and single-phase BRC with the resonant inductor in DC side for the resonant stage. (b) Prototype of the two-phase BRC as another possibility for the resonant stage of the proposed hybrid dc/dc topology.

$$P_{\mathrm{LOSS}} = \frac{1}{2}\left(V_{\mathrm{IN}} I_{\mathrm{IN}} + V_{\mathrm{X}} I_{\mathrm{X}}\right) \tag{4.4}$$

For the measurements in this work, the schematic from Fig. 4.19(a) is used due to the safety reasons: voltage at the input (750 V) is half of the output voltage (1500 V) and in such a way it is further from the isolation limit of the power source (V_{X}, I_{X}) [± 1800 V positive terminal to power earth (PE)]. For both power sources, (V_{IN}, I_{IN}) and (V_{X}, I_{X}), it was used 15-kW PSI 91500-30 power source from the Elektro Automatik [169]. Voltages and currents are measured with Fluke 8808A multimeters [170].

4.7 Experimental Results

In order to justify the theoretical analysis conducted in the previous sections, several prototypes are built and tested in the laboratory. These prototypes are already discussed in Section 3.5. For sake of clarity, their photographs are repeated here in Fig. 4.20. Additionally, for the same reason, the details on the prototype designs are repeated in Table 4.3 and 4.4. The two-phase boost topology with 120-mΩ, 900-V SiC device is selected for the practical implementation depicted in Fig. 4.20(a). On the other side, BRC stage is tested separately for both analyzed 900-V SiC devices (120-mΩ and 65-mΩ) and all the analyzed variations. However, for the experiment of operation of the total hybrid topology, BRC stage is tested with the resonant inductor in DC side and 120-mΩ, 900-V SiC device.

Table 4.3: Specifications and Design of the Power Stage of the Prototype.

Nominal conditions		Boost	BRC	Total
P_{nom}		3 kW	4 kW	10 kW
$V_{IN,nom}$		330 V	750 V	1080 V
$V_{OUT,nom}$		750 V	1500 V	1500 V
$V_{IN,min}$		0 V	650 V	650 V
$V_{IN,max}$		750 V	750 V	1500 V
Sw. Freq.		64 kHz	13.2 kHz	/
MOSFET	Device	C3M0120090J	C3M0120090J	/
	N. in Par.	3	3	/
	Volume	4 x 3 x 427 mm^3	4 x 3 x 427 mm^3	8 x 3 x 427 mm^3
MOSFET Driver	Component	CRD-001	CRD-001	/
	Volume	4 x 24.65 cm^3	4 x 24.65 cm^3	8 x 24.65 cm^3
C_{IN}	Value	14 µF, 900 V		/
	Component	C4AEOBW5140A3JJ	/	
	Volume	43.51 cm^3		43.51 cm^3
$C_{DC,BUS}$	Value	2 x 12 µF, 900 V + 2 x 0.75 µF, 900 V		
	Component	2 x C4AEOBW5120A3FJ + 6 x B58031I9254M062		
	Volume	2 x 33.60 cm^3 + 6 x 340 mm^3		
C_{RES}	Value		4.5 µF, 900 V	
	Component	/	3 x C4AEOBU4150A1WJ	/
	Volume		3 x 6.93 cm^3	3 x 6.93 cm^3
L	Value	210 µH	74 µH	
	Core	PQ32/30	55071	
	Material	3C97	MPP60u	
	Gap	2.2 mm	/	/
	Wire	Litz 200 x 0.071 mm	Litz 100 x 0.2 mm	
	N. of Turns	48	34	
	R_{DC}	78 mΩ	83mΩ	
	Volume	2 x 26.7 cm^3	10.23 cm^3	63.63 cm^3
Weight		530 g	580 g	1.21 kg
Specific Power		5.75 kW/kg	6.71 kW/kg	8.26 kW/kg
Total Components Volume		200.6 cm^3	204 cm^3	404.6 cm^3

Table 4.4: Specifications and Design of Power Stage of the BRC Prototypes.

Nominal conditions		Single-Phase BRC	Two-Phase BRC
$P_{BRC,nom}$		4 kW	
$P_{BRC,max}$		7 kW	
$V_{IN,BRC,nom}$		750 V	
$V_{DC,BUS,nom}$		1500 V	
MOSFET	Device	C3M0065090J / C3M0120090J	
	N. in Par.	3	2 x 2
	Volume	4 x 3 x 427 mm^3	2 x 4 x 2 x 427 mm^3
MOSFET Driver	Component	CRD-001	
	Volume	4 x 24.65 cm^3	2 x 4 x 24.65 cm^3
$C_{DC,BUS}$	Value	2 x 12 µF, 900 V + 2 x 0.75 µ F, 900 V	2 x 5 µF, 900 V + 2 x 0.75 µF, 900 V
	Component	2 x C4AEOBW5120A3FJ + 6 x B58031I9254M062	2 x C4AEOBU4500A11J + 6 x B58031I9254M062
	Volume	2 x 33.60 cm^3 + 6 x 340 mm^3	2 x 17.36 cm^3 + 6 x 340 mm^3
C_{RES}	Value	4.5 µF, 900 V	2 x 1.5 µF, 900 V
	Component	3 x C4AEOBU4150A1WJ	2 x C4AEOBU4150A1WJ
	Volume	3 x 6.93 cm^3	2 x 6.93 cm^3
L_{RES}	Value	74 µH	
	Core	55071	
	Material	MPP60u	
	Gap	/	
	Wire	Litz 100 x 0.2 mm	
	N. of Turns	34	
	R_{DC}	83 mΩ	
	Volume	10.23 cm^3	
Weight		580 g	580 g
Specific Power		12.1 kW/kg	12.1 kW/kg
Components Volume Without Drivers		105.4 cm^3	67.7 cm^3
Total Components Volume		204 cm^3	264.9 cm^3

The results of the efficiency measurements of the hybrid topology from Fig. 4.20(a) in the nominal input/output voltage scenario under different levels of load are displayed in Fig. 4.21(a), and that of the nominal power curve scenario [see Table 4.3 and Fig. 3.2(b)] for different PV voltages are displayed in Fig. 4.21(b). It can be observed that the *Euro Efficiency* of 99.48 % under nominal input/output voltage conditions is achieved. Converter specific power is 8.26 kW/kg, and its power stage occupies 404.6 cm^3. It is obvious from Fig. 4.20(a) that the power stage components are not arranged optimally,

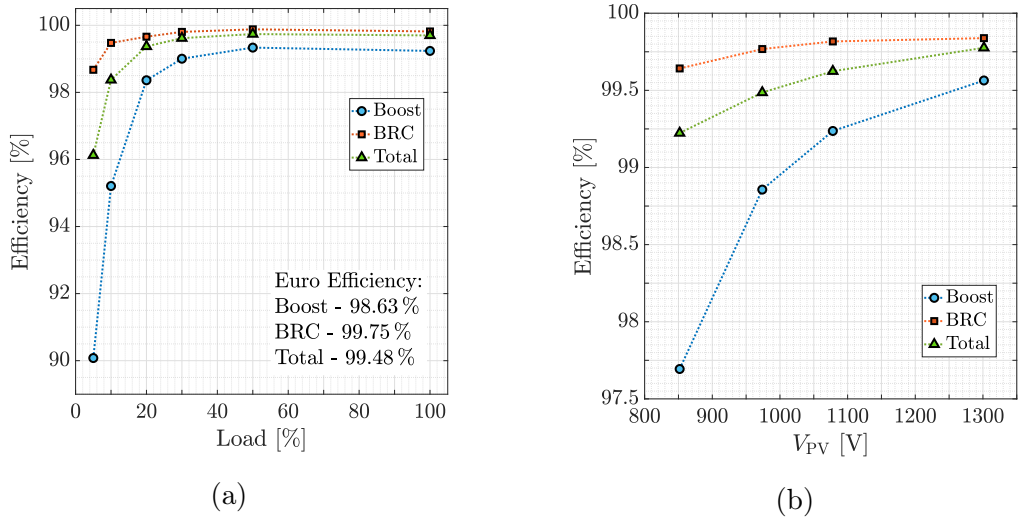
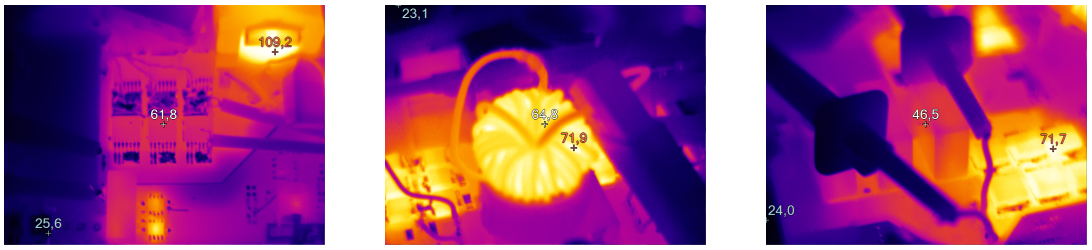


Fig. 4.21: (a) Measured efficiency at the nominal input/output voltage (see Table 4.3) under different loads. (b) Measured efficiency for nominal power curve [see Table 4.3 and Fig. 3.2(b)] in different points of PV voltage.



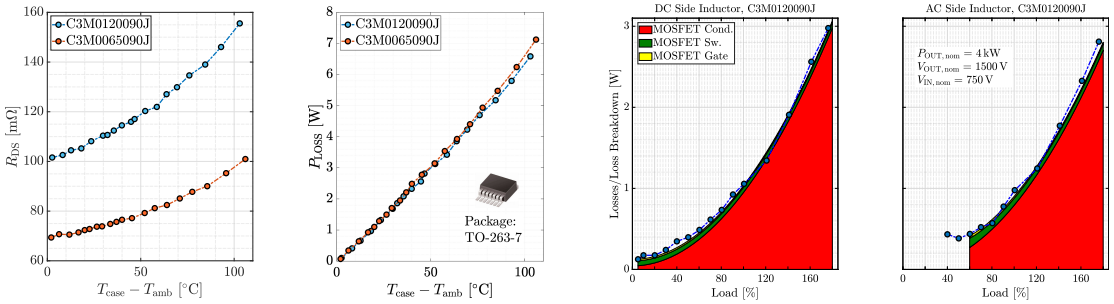
(a) (b) (c)

Fig. 4.22: Temperatures of the power stage components under the worst case conditions for each part of the proposed hybrid topology separately: boost stage ($P_{\mathrm{IN,\,Boost}} = 3\,\mathrm{kW}$ and $V_{\mathrm{PV}} = 1080\,\mathrm{V}$); BRC stage ($P_{\mathrm{IN,\,BRC}} = 7\,\mathrm{kW}$ and $V_{\mathrm{PV}} = 750\,\mathrm{V}$). (a) MOSFETs and inductor of the boost stage - temperature of the MOSFETs = 61.8°C and temperature of the inductor = 109.2°C. (b) Resonant inductor of the BRC stage - temperature of the inductor = 71.9°C. (c) MOSFETs and resonant capacitor of the BRC stage - temperature of the MOSFETs = 71.7°C and temperature of the resonant capacitor = 46.5°C.

which could be part of future work. For this reason, only the volume occupied by power stage components is discussed, rather than the power density of the complete prototype.

Operation under the worst case conditions is justified by the measurements of the temperatures of the power stage components for both parts of the hybrid topology. These measurements are displayed in Fig. 4.22. The worst case operating conditions for both stages are different from each other. For example, the worst case for the BRC stage is at $V_{\mathrm{PV}} = 750\,\mathrm{V}$, because, at this point, it processes maximum power (7 kW), while in the case of the boost stage, it is the nominal point ($V_{\mathrm{PV}} = 1080\,\mathrm{V}$, $P_{\mathrm{IN,\,Boost}} = 3\,\mathrm{kW}$), because the ripple of the inductor current and the switching frequency are maximal here.

In order to justify MOSFET loss model that is used in this work, 900-V SiC devices from Wolfspeed/Cree that are included in the optimization algorithm and that are considered for the prototype implementation are characterized in terms of losses versus temperature. Firslty, each device is forced in the permanent ON-state by applying constant $V_{\mathrm{GS}} = 15\,\mathrm{V}$. A range of dc currents is placed through the MOSFET's channel and voltage fall at the MOSFET and its case temperature are measured. The experimental setup is kept in each state for 20 min. DC current through the MOSFET and voltage fall on it are measured by the Fluke 8808 A multimeters. MOSFET's case temperature is measured by Fluke TI400 thermal camera. Ambient temperature for each measured state is also recorded. In this way, R_{DS} versus $(T_{\mathrm{case}} - T_{\mathrm{amb}})$ for both devices is obtained and depicted in Fig. 4.23(a). From the same set of measurements, it is possible to characterize MOSFET in terms of losses that are dissipated versus its case temperature. These results are given in Fig. 4.23(b). Both MOSFETs show the same behaviour in terms of losses versus case temperature. The reason for this is that they have the same package, TO-263-7. This set of data is much more appropriate to estimate MOSFET losses by measuring its

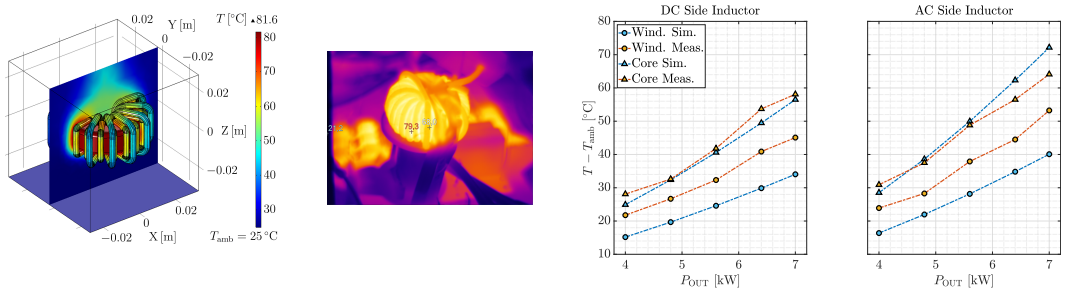


(a) (b) (c)

Fig. 4.23: Experimental verification of the applied MOSFET loss model. (a) R_{DS} measurements under different case temperatures for both 900-V SiC devices from Wolfspeed/Cree that are considered in the optimization algorithm. (b) Thermal calibration of the MOSFET. P_{LOSS} versus $(T_{case} - T_{amb})$ for TO-263-7 package. (c) Comparison of the estimated loss breakdown and measured MOSFET losses under different loads.

case temperature, compared to the thermal resistances, $R_{\Theta JC}$ and $R_{\Theta JA}$, and R_{DS} versus junction temperature given in the manufacturer's data sheets [117].

After MOSFET temperature characterization, its temperature is measured for BRC converter's [see Fig. 4.20(a), where the prototype is depicted] operation under different loads. According to the recorded temperatures, the losses in the MOSFET are determined and compared to the loss breakdown estimated by the MOSFET loss model that is applied in the optimization algorithm. This comparison is presented in Fig. 4.23(c). One can notice that estimated loss breakdown agrees significantly with measured losses per MOSFET. This way, applied loss model is confirmed as accurate.



(a) (b) (c)

Fig. 4.24: Temperature field distribution of the BRC with DC side inductor and $P_{OUT} = 7$ kW: (a) Finite Element simulation. (b) Experimental results taken by Fluke TI400 thermal camera. (c) Winding and core temperature rise for different load values, obtained by simulation and experimental results. Details on the inductor design can be found in Table 4.4.

Table 4.5: Thermal Conductivity of the Simulated Materials.

Iron powder [164, 171]	17 W/(m·K)
Air [172]	0.026 W/(m·K) (*)
Homogenized *Litz*, k_{eq} [173]	0.11616 W/(m·K)
(*) Material properties of Air are set dependent on temperature, according to the built-in model from COMSOL [172].	

The accuracy of the power losses estimation for the inductor is analyzed by comparing the thermal camera measurements with Computational Fluid Dynamics (CFD) thermal simulations, as shown in Fig. 4.24(a) and 4.24(b). In case the temperature of both cases matches, that would imply the power losses are accurately estimated.

Regarding the thermal measurements, the recommendations of [174–176] were followed and the images were post-processed with Fluke SmartView software – the surface temperature was averaged per zones in order to obtain reliable data. Still, there is some uncertainty associated to this measurements, which is related to the discrepancy of the measured surface emissivity and the background radiation (a tolerance typically of 2 °C or 2 % of the measured temperature [174, 175]).

As per the thermal simulations, performed in COMSOL Multiphysics, the fluid dynamics of the surrounding air and radiation are simulated to avoid the linearization of the boundary conditions (natural convection and radiation) [177], which might incur in inaccurate results. The ambient conditions of the experiments and material properties (summarized in Table 4.5) are recreated in the simulations. The thermal conductivity is assumed constant, taking its value at 90 °C, which is the maximum temperature reached in the experiments. *Litz* bundles are homogenized using the approach described in [173] to avoid excessive meshing elements. Power losses are assumed uniformly distributed, taking the estimated values using the approaches described in [93, 94] and [95, 97] for the core and winding, correspondingly.

Fig. 4.24(c) shows the comparison of the simulation results with the experimental measurements for DC and AC scenario, respectively. The simulated core temperature practically matches the measurements, while there is a constant offset on the winding temperature. This can only be explained by an underestimation of the thermal conductivity of the *Litz* bundles, k_{eq} (a change in k_{eq} would shift the temperature curve up or down –conduction is dominant and it is linear with losses-, while a mismatch in the winding losses would bend the curve –due to their non-linearity). Therefore, the inductor power losses calculation is validated.

Loss and efficiency measurements of the BRC stage at the nominal input and output voltage, $V_{\text{IN}} = 750\,\text{V}$ and $V_{\text{OUT}} = 1500\,\text{V}$, under different loads are depicted in Fig. 4.25. The results are provided for all the investigated variants of BRC and both included 900-V SiC devices. The measurements are done using the technique described in Section 4.6.

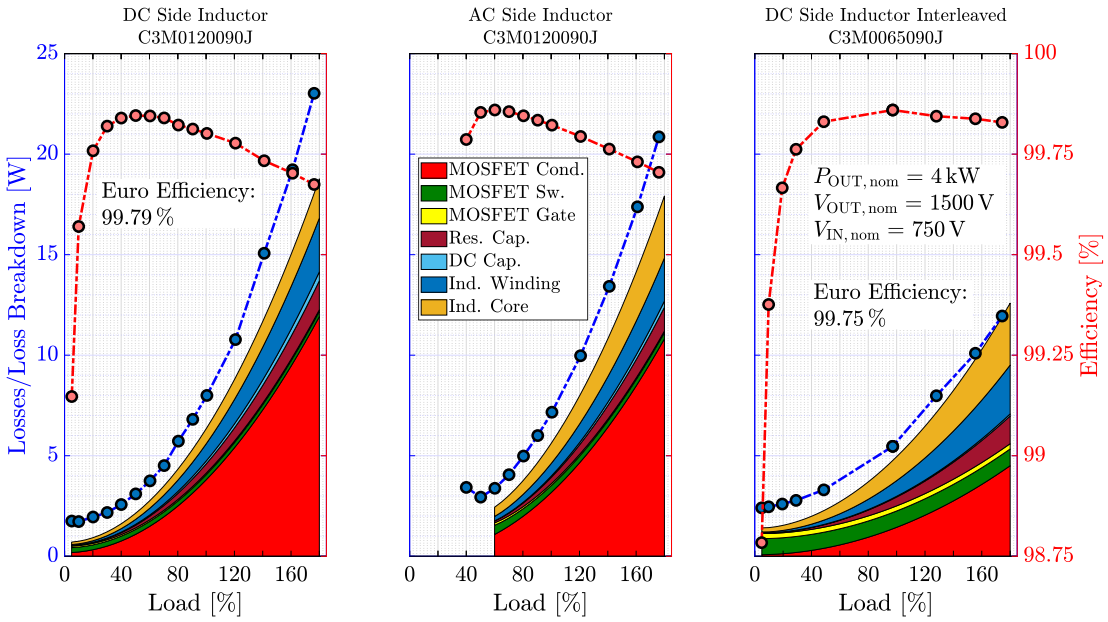


Fig. 4.25: Loss and efficiency measurements of all the analyzed BRC variants under different loads and for both 900-V SiC devices from Wolfspeed/Cree that are included in the optimization algorithm. Losses are measured by opposition method that is explained in Section 4.6. In order to justify applied loss models, estimated loss breakdown under different loads is also depicted in the figures.

Estimated loss breakdowns for corresponding cases are also given in the mentioned figure. Pretty good matching between measured and estimated results can be noticed. It is important to emphasize that during the analysis of the converter under different conditions, the resonant current model presented in Section 3.3.2 was used. This is another confirmation of the validity and utility of the proposed model. Measured peak efficiencies are 99.85 % for DC side inductor, 99.86 % for AC side inductor and 99.86 % for interleaved BRC. Finally, measured *Euro Efficiency* of 99.75 % for interleaved BRC and 99.79 % for single-phase BRC with DC side inductor are reported.

4.8 Chapter Summary

Full multivariable optimization of the hybrid, multi-level, PPP topology presented in Chapter 3 is conducted here. At the very beginning, a comprehensive review of the commercially available WBG devices and their Si conterpairs is given. The most suitable WBG devices from the point of view of the conduction and switching characteristics are selected to be included in the optimization algorithm. The switching characteristics are analyzed according to the C_{OSS} model presented in Appendix A.

Optimization algorithm is explained in details with all the constraints and design aspects included for all the previously analyzed topologies. The FCML boost topology from [58] is selected to be fully optimized and compared with the hybrid topology from the previous chapter.

Full multivariable optimization is conducted for the FCML topology analyzing different number of levels (3 to 6) with appropriately rated new classes of 650-V and 900-V WBG devices. It is concluded that due to the dominant conduction losses and gap in the voltage rating of the commercially available WBG devices between 650 V and 200 V, increase of the number of levels over 4 leads to the deteriorated loss and volume performances. Therefore, the FCML topology with 4 levels and 650-V SiC device is selected for the final comparison.

In case of the controllable, boost stage of the proposed hybrid topology, the two-phase and the three-level boost are compared. On contrary to the FCML topology, in this case the switches rating is changed from 900 V down to 650 V by passing from the two-phase to the three-level topology. With this appropriate voltage scaling that follows the increase of the number of levels, the three-level boost shows better performances than the two-phase solution.

The same algorithm is applied to all the BRC variants and it is concluded that AC side inductor scenario shows the best efficiency in the nominal operating point, while introducing interleaving technique in case of DC side inductor scenario does not bring any improvement in terms of efficiency. However, interleaving technique leads to the halving of the dc bus capacitor volume and significant reduction of dc bus voltage ripple (experimental verification shows that dc bus voltage ripple can be decreased up to 2 times for half the value of dc bus capacitance).

Optimization results of the resonant and the boost stage are combined and the total pareto front of the hybrid topology from Chapter 3 is obtained and compared with four-level FCML boost topology previously optimized. Results of the comparison show that losses of both topologies are in the same range, while hybrid, PPP topology provides lower occupied volume. The main reason for this is voltage rating of (input/output)/(dc bus) capacitors that is double in case of FCML topology. This shows the importance of voltage balancing of splitted dc bus capacitors of the hybrid topology provided by the resonant stage, beside the high efficiency already discussed.

Mini-boost concept presented in Chapter 2 is extended and standard boost topology that employs 1200 V rated IGBTs and diodes is replaced by the fully optimized emerging multi-level, hybrid and partial power processing topologies that employ new classes of 650-V and 900-V WBG, GaN and SiC, devices. Energy harvesting calculation from Chapter 2 is repeated for grid-connected systems with these fully optimized dc/dc topologies. New classes of 650-V and 900-V WBG devices employed in hybrid, multi-level, step-up dc/dc

topologies improve the energy delivered to the grid compared to the standard two-level dc/dc topologies with 1200-V Si modules in 1000-V PV system - losses in dc/dc stage during the year are decreased by up to 73.33 % for 400-V ac grid connection and by 56.67 % for 480 V ac voltage level. Additionally, multi-level topologies provide the possibility of use of 650-V and 900-V WBG devices in 1500-V PV systems. In this way the problem of high voltage derating and use of semiconductor devices rated for more than 1700 V is avoided.

A back-to-back losses measurement technique for voltage-fed converters that operate in open loop is presented. This method represents a good compromise between precision, time consumption and complexity to be implemented.

The previously described theoretical analysis related to the proposed hybrid topology is fully experimentally confirmed by building and measuring a 10-kW prototype of 8.26 kW/kg of specific power and 404.6-cm^3 of volume occupied only by the power stage components. The *Euro Efficiency* of 99.48 % in nominal input/output voltage conditions is achieved.

All the analysis related to the BRC stage is confirmed by detailed and comprehensive measurements of two prototypes of 4 kW of nominal and 7 kW of maximal power with reported euro-efficiency of 99.79 % and 12.1 kW/kg of specific power. Additionally, all the loss models applied in the optimization algorithm and the energy harvesting calculation program presented in this chapter are confirmed by detailed measurements, thermal calibration and FEA thermal simulations of the WBG devices and inductor designs employed in this work.