

Conclusions and Future Work

FOLLOWING a year in which global solar PV additions were stable or even contracted slightly, in 2019 the solar PV market increased an estimated 12% to around 115 GW [4]. The global total of 627 GW, which includes on- and off-grid capacity, compares to a total of less than 23 GW only 10 years earlier [4]. Fig. 5.1(a) depicts share of electricity production from solar in different parts of the world.

In the last 10 years, the efficiency of average commercial wafer-based silicon modules increased from about 12% to 17% (super-mono 21%). Fig. 5.1(b) shows average crystalline-silicon, commercially available PV module efficiency. Additionally, the price has dropped more than 5 times for the same period. This has led to both, decrease in the total PV system price and to decrease in the share of the total system price related to PV module. In 2015 module price represented 19.26% of total PV system costs [see Fig. 5.1(c)]. The rest was related to the installed non-module prices: hardware costs, such as inverters and racking equipment; and the wide assortment of soft costs, including such things as marketing and customer acquisition, system design, installation labor, permitting and inspection costs, and installer margins.

According to the all data presented, the bottleneck for the further decrease in PV system cost and efficiency and, thus, for the further increase in the global PV installation and decrease in the price of the electricity provided from PV is related to the power conditioning unit, the part of the system between PV string/array and the load.

Grid-connected PV systems account for more than 99% of the PV installed capacity compared to stand-alone systems (which use batteries) [5]. The most dominant PV inverter in the market is the string inverter [18]. The string inverter is very popular for small-to mediumscale PV systems, particularly for residential rooftop PV plants [5]. These applications represented a 37% of the PV market in 2015. In this case, a typical structure of the PV system is the string configuration where no PV strings are connected in parallel [17]. However, according to [11], the market share of string inverters in 2019 is estimated to be 61.6%. These inverters are mostly used in residential, small and medium commercial applications in PV systems up to 150kW. The case study in this thesis is a transformerless, string/multi-string, three-phase-grid-connected PV inverter for use in commercial/residential applications that is designed for operation in power range of 10kW - 30kW (see Fig. 5.2).

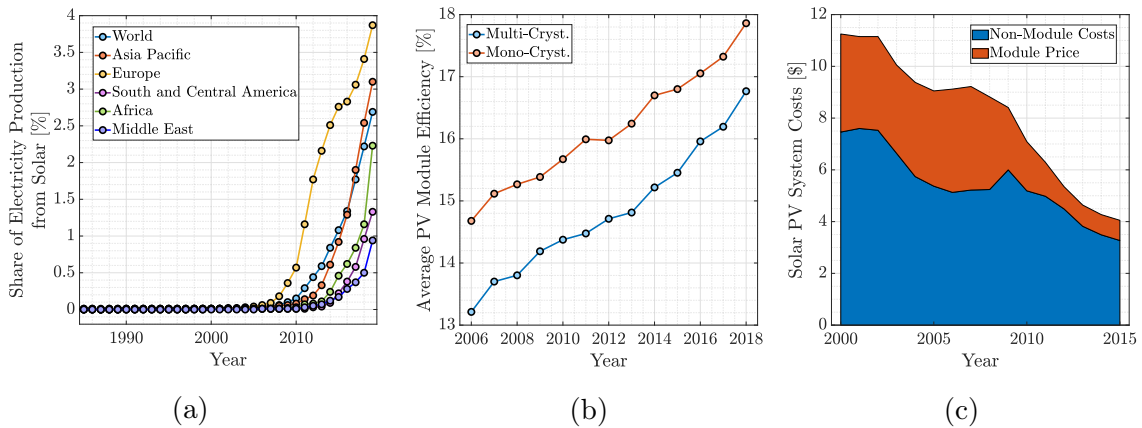


Fig. 5.1: (a) Share of electricity production from solar in different parts of the world. The data is taken from [3]. (b) Average crystalline-silicon, commercially available PV module efficiency. (c) Median residential solar PV costs in the United States, measured in real 2015\$. Installed non-module prices include hardware costs, such as inverters and racking equipment; and the wide assortment of soft costs, including such things as marketing and customer acquisition, system design, installation labor, permitting and inspection costs, and installer margins. The data is taken from [3, 11].

5.1 Dissertation Summary

5.1.1 Analysis on the System Level

The main objective of this thesis is the analysis of the operating principle, design aspects and full multivariable optimization of the hybrid, multi-level, partial power processing topology for use in a two-stage grid-connected 1500-V PV system [see Fig. 5.2(b)]. However, in order to justify the necessity of including a dc/dc stage in the system from Fig. 5.2(a), a lot of pre-analysis is conducted on the system level and its results are presented in Chapter 2. At the very beginning, a comprehensive overview of the literature on the comparison of 1000-V and 1500-V PV systems is discussed. All the results found in the literature are related to the financial benefits, increased input voltage

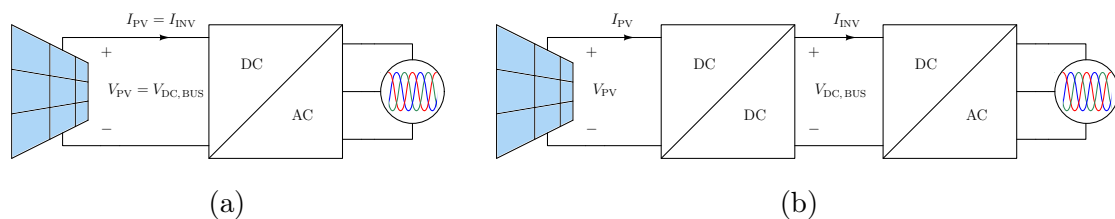


Fig. 5.2: The case study - transformerless, string/multi-string, three-phase-grid-connected PV inverter for use in commercial/residential applications that is designed for operation in power range of 10 kW - 30 kW. (a) One-stage. (b) Two-stage.

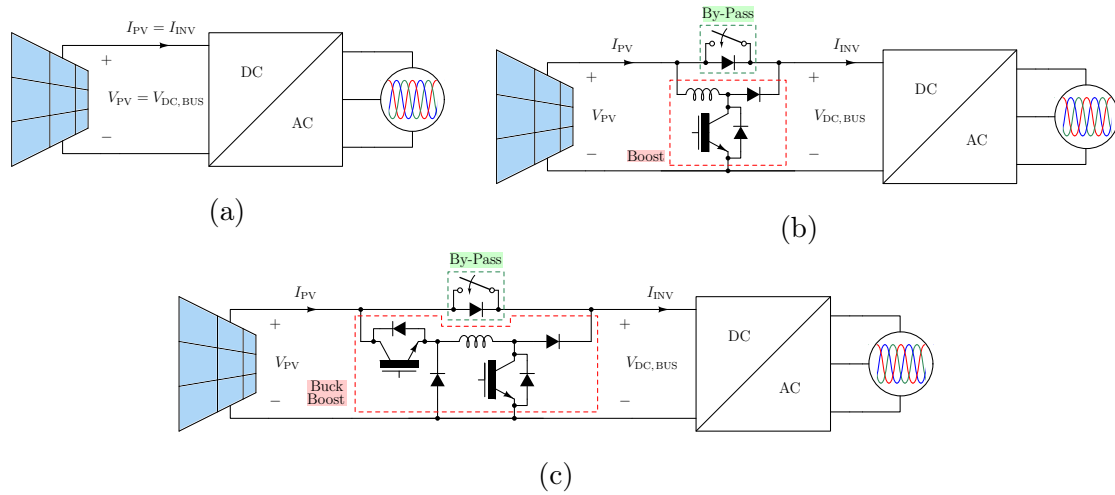


Fig. 5.3: Analyzed architectures. (a) One-stage grid-connected PV system. (b) Two-stage grid-connected PV system with mini-boost as dc/dc stage. (c) Two-stage grid-connected PV system with buck-boost as dc/dc stage.

range operation, reliability, etc. Nevertheless, none of the previous works deals with the subject of the energy harvesting on a year level.

In order to cover this question, one-stage architecture is compared to the two versions of two-stage system that employ the dc/dc topologies known from the literature: "mini-boost" [33] and "string optimizer" [34] (see Fig. 5.3). The program for the energy harvesting calculation is developed in MATLAB package. This program includes the real environmental conditions measurements in the sample location [70], real PV panel models available in the market [71], real converter designs and detailed loss models. The program is run for 1000-V and 1500-V PV systems with different ac grid connections: 400 V, 480 V, 600 V and 800 V.

Beside the influence of a dc/dc stage on the efficiency of the whole system, the impact on the compactness of the output filter of the inverter stage is also investigated. The design space concept developed in [82, 83] is refined in Chapter 2 and the analysis is extended to the variable dc bus voltage. The inverter's output *LCL* filter design is examined under the variation of the dc bus voltage in the full operating range and compared to the case when a dc/dc stage is employed to control the dc bus voltage to the minimum value.

5.1.2 Proposed Hybrid, Multi-Level, Partial Power Processing DC/DC Topology

Following the analysis on the system level conducted in Chapter 2, the hybrid, multi-level, partial power processing dc/dc topology that employs new classes of 650-V and 900-V WBG devices is proposed in Chapter 3 to be used as a dc/dc stage in the 1500-V PV

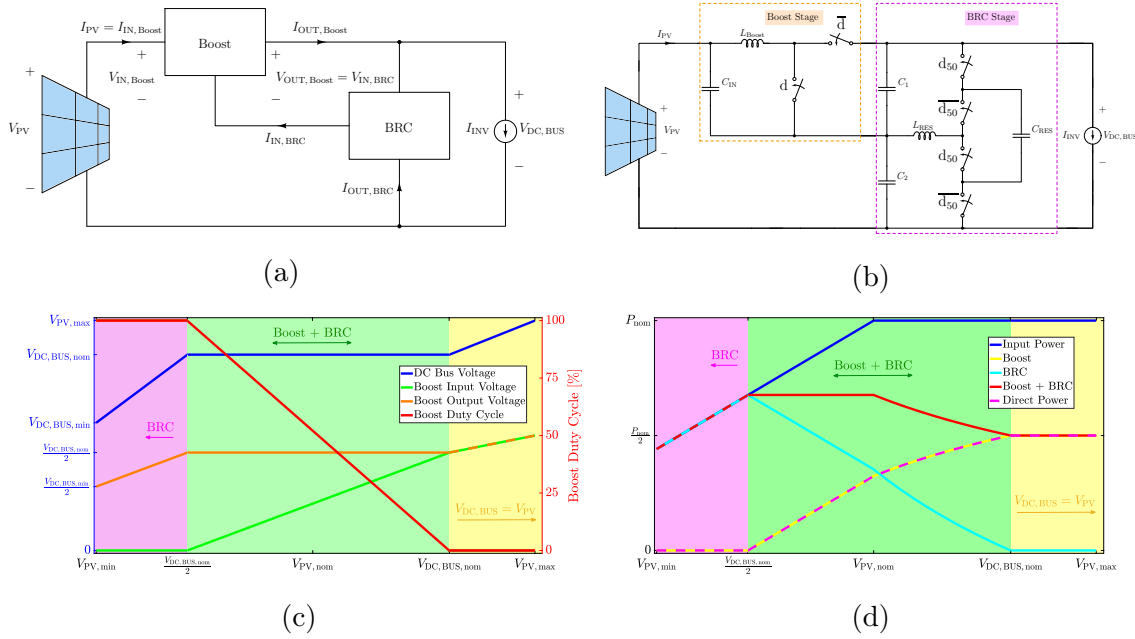


Fig. 5.4: Proposed dc/dc topology: (a) Block diagram, (b) Simplified schematic. Operating regions of the proposed dc/dc topology as a function of PV voltage: (c) Voltage controllability, (d) Power flow distribution between the stages.

system from Fig. 5.2(b). A block diagram and simplified schematic of the proposed dc/dc topology are presented in Fig. 5.4(a) and 5.4(b). It consists of two stages: 1) *Standard boost stage*: It is less efficient part of this architecture, but operates in a closed loop, and thus provides the possibility of controlling output voltage. 2) *Basic Resonant Cell (BRC) Stage*: It has a fixed ratio between output and input voltages (boosting factor) of 2. It operates in an open loop with a constant duty cycle of 50% and keeps equal voltage distribution between the dc bus capacitors [C_1 and C_2 capacitors in Fig. 5.4(b)]. This stage is driven in such a way that it does not have the possibility of the control of output voltage, but, on the other hand, processes the input energy very efficiently, and thus increases the efficiency of the presented architecture. Additionally, the BRC part increases the total boosting factor of the presented dc/dc topology. This behavior improves the operating voltage range of the PV array and energy harvesting capability of the grid-connected PV system.

The boost and the BRC part are not arranged in the standard series connection, but rather with output of the boost converter placed to the high-side dc bus capacitor of the BRC stage. This arrangement provides an additional direct path of energy flow from the input to the output, adding to the energy processed through the boost or the BRC stage. This means that the total energy is not processed by the converter, which increases the efficiency of the presented topology.

In Fig. 5.4(c) and 5.4(d), three operating regions of the presented topology can be observed in the following: 1) For V_{PV} voltages below $V_{DC,BUS,nom}/2$, the low-side switch of the boost converter is shorted, and the total input voltage is transferred to the low-side dc bus capacitor of the BRC stage that operates in an open loop with 50% of duty cycle. In this region, output voltage is not controlled, and the boosting factor is 2 [see Fig. 5.4(c)], which is the maximum value for this topology. The total input energy is processed by the architecture in this region [see Fig. 5.4(d)]. However, this processing is done in a very efficient way by the BRC part, while in the boost stage, only dc conduction losses of low-side switch and inductor winding are present. 2) In the middle region, both the stages are operative, and output voltage is controlled [see Fig. 5.4(c)]. Boundaries of this region are $V_{DC,BUS,nom}/2$ and $V_{DC,BUS,nom}$, and are determined by the saturation of boost duty cycle to its maximal and minimal values, respectively. $V_{DC,BUS,nom}$ represents a desired nominal value of the dc bus voltage that should be controlled. Energy that is processed by the converter becomes lower than the total input energy in this voltage range [see Fig. 5.4(d)]. 3) The behavior of the topology for V_{PV} voltages higher than $V_{DC,BUS,nom}$ is such that input and output are shorted by closing the high-side switch of the boost stage. In this region, the BRC converter still operates in order to keep proper voltage distribution between dc bus capacitors, but it does not process any power.

5.1.3 Full Multivariable Optimization of the Proposed DC/DC Topology

After the description of the operation principle of the proposed dc/dc topology, all the analyzed variants of its stages (see Fig. 5.5), control algorithms and design aspects presented in Chapter 3, full multivariable optimization for all the analyzed stages is conducted in Chapter 4. A comprehensive overview of the commercially available 650-V and 900-V WBG devices and their Si counterparts is provided. The optimization algorithm is explained together with all the design aspects, constraints, loss models, passive components and WBG devices included. In order to have a fair comparison with the state-of-the-art solution for the same application, the flying capacitor multi-level topology from [58], that is the first work to employ 650-V GaN devices in the 1500-V PV applications, is fully optimized by the described algorithm for the same specifications as the proposed hybrid dc/dc topology. Obtained pareto fronts of the separately optimized stages of the hybrid topology are combined and the total pareto front is obtained and compared with the one for the topology from [58].

Finally, all the optimized topologies are included in the energy harvesting comparison with the architectures Fig. 5.3. The MATLAB program described in Chapter 2 is used

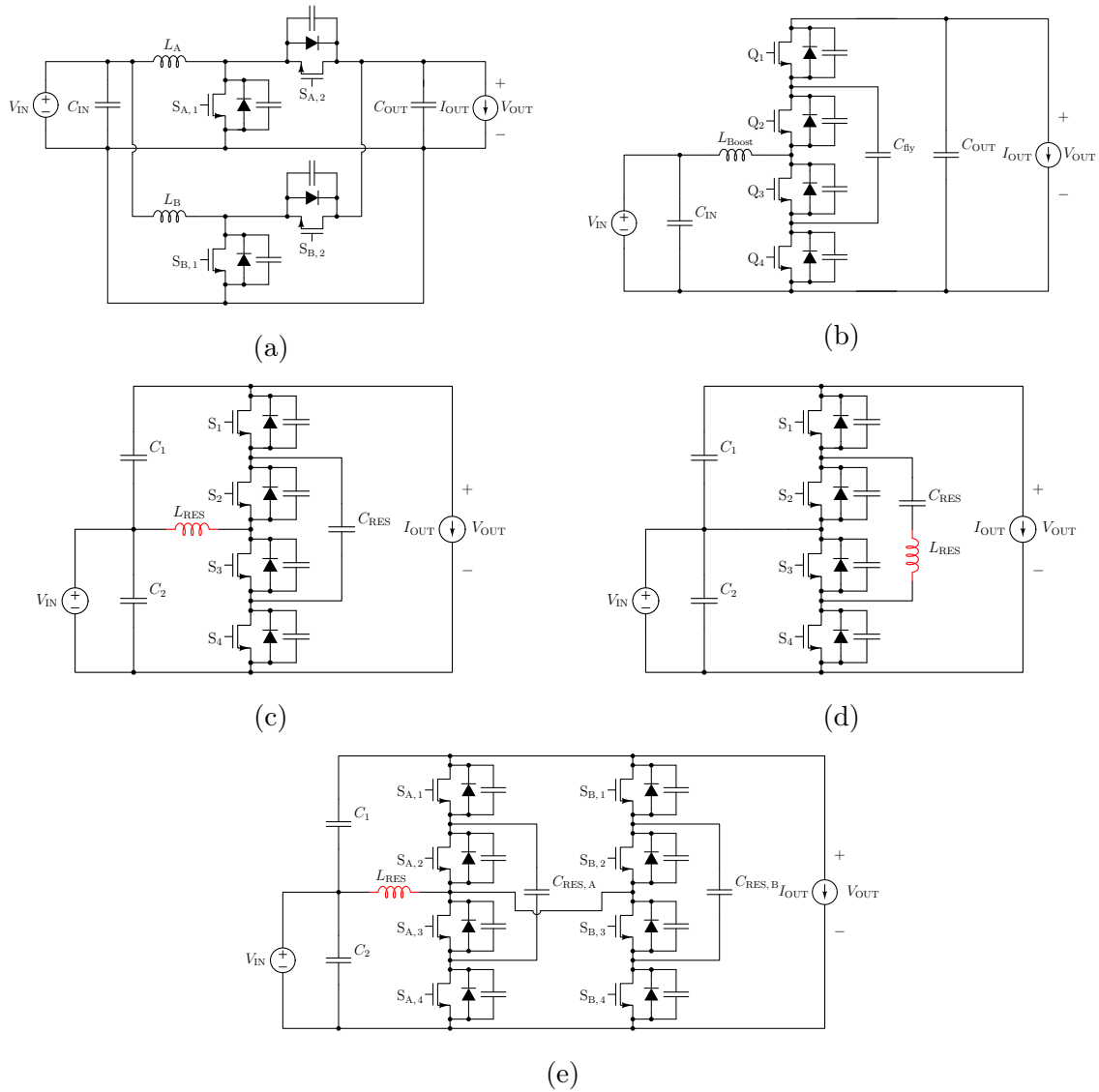


Fig. 5.5: Analyzed variants of the boost stage: (a) Two-phase boost, (b) Three-level boost. Schematics of the analyzed BRC topologies: (c) BRC with the resonant inductor in DC side, (d) BRC with the resonant inductor in AC side and (e) Two-phase interleaved BRC with a single resonant inductor in DC side.

to calculate losses in these topologies on a yearly level under the same environmental conditions in the sample location [70].

5.1.4 Appendices

During the investigation of the main subject of the dissertation, some auxiliary tools are developed and interesting, secondary effects are discovered. For sake of clarity and in order

to provide to the reader a better focus on the main subject, these results are presented in the part of appendices.

As discussed in Chapter 3 and 4, one of the main advantages of the proposed hybrid topology is that it obtains full ZVS transitions in all the switches under the all operating conditions. On the other side, analysis of ZVS conditions is strongly impacted by the non-linear C_{OSS} capacitance that highly depends on the switching voltage. A lot of authors deal with the subject of the modeling of MOSFET output capacitance and losses related to it [178–180]. However, these models are too complex and time consuming to be included in the optimization algorithm described in Section 4.2. In order to reconcile the model precision and its complexity, the model presented in [143] is refined and a simplified C_{OSS} model for the prediction of ZVS conditions in applications where switching voltages are in range of several hundreds of Volts is presented in Appendix A. This model is simple enough to be included in the optimization program without increasing the time consumption of calculations while simultaneously demonstrating high accuracy.

The analysis presented in Chapter 4 shows that achieving ZVS leads to the huge reduction of switching losses in the applications where blocking voltages are in the range 700 V - 800 V. Additionally, experimental results of Chapter 3 show that even partial ZVS operation in this kind of applications can lead to the excessive temperature increase and failure of the switching devices. For this reason, and for the sake of achieving higher efficiency under full operating voltage and load range, the work presented in this thesis assumes TCM operating mode with variable switching frequency (f_{SW}) and constant T_{ON} control. The main contribution of Appendix B is the investigation of the FC voltage imbalance control in the three-level boost converter under TCM operating mode with variable f_{SW} and constant T_{ON} control. The analytical analysis is conducted and the load range in which the natural FC balance is achieved is determined by the presented model. The compensation action is proposed to balance FC voltage in the operating ranges where it is not achieved naturally.

5.2 Conclusions and Contributions

5.2.1 Primary Contributions of the Thesis

The main contributions of the work discussed in this dissertation are listed here:

- The issue not covered by the actual literature is analyzed in Chapter 2 and detailed comparison of different architectures of grid-connected PV systems in terms of energy harvesting during the year is conducted for different ac grid voltage levels (400 V, 480 V, 600 V and 800 V) and 1000-V and 1500-V at the PV string side.

- Influence of the controllability of dc bus voltage on the compactness of the inverter's output filter is investigated in the same chapter.
- In order to reconcile two contradictory demands, high power density and controllability of dc bus voltage, Chapter 3 proposes a hybrid dc/dc topology that combines a highly efficient, non-controllable step-up RSCC with a controllable, but lower efficient boost topology. In the presented solution, all employed devices have to withstand half of the output voltage; therefore, new classes of 650-V and 900-V WBG devices present an excellent option, keeping in mind their superiority over 1200-V Si IGBTs.
- Full multivariable optimization of the proposed dc/dc topology is conducted in Chapter 4 and the results are compared with the ones for the stat-of-the-art topologies [58].

5.2.2 Conclusions Related to the Main Subject of the Thesis

The work described in the previous chapters resulted in the conclusions related to the main subject that can be summarized as follows:

- In case when the minimum dc bus voltage is in the middle of MPP variation during the year, for example 1000-V PV string with 400 V ac voltage level or 1500-V PV system with 600-V ac grid, the biggest portion of energy loss is due to the power mismatch (operation out of MPP point due to MPP voltage lower than the minimum dc bus or MPP power higher than covnerter's rated power). The inclusion of a dc/dc stage in these cases decreases the mismatch losses by 90.1 % and improves amount of the energy delivered to the grid from 92.29 % to 97.28 % of MPP energy available from the PV string.
- From the point of view of the influence of the variation of dc bus voltage on the compactness of the inverter stage, one can conclude that filter design with controlled dc bus voltage to a lower value gives more compact and efficient solutions than when a huge variation of dc bus is allowed. It is especially interesting to emphasize that, for the same efficiency, filter designs with lower dc bus voltage can occupy ≈ 50 % less volume compared to the case when dc bus varies in the full operating range. On the other hand, controllability of dc bus voltage demands a dc/dc stage to be employed between PV string and the inverter stage. This would increase total system volume. Therefore, it is necessary to design a very compact dc/dc stage in order to have a positive compromise between reduction of the inverter's output filter volume and addition of a new power processing stage in the system.

- The FCML boost topology from [58] is selected to be fully optimized and compared with the hybrid topology proposed in this thesis. Full multivariable optimization is conducted for the FCML topology analyzing different number of levels (3 to 6) with appropriately rated new classes of 650-V and 900-V WBG devices. It is concluded that due to the dominant conduction losses and gap in the voltage rating of the commercially available WBG devices between 650 V and 200 V, increase of the number of levels over 4 leads to the deteriorated loss and volume performances. Therefore, the FCML topology with 4 levels and 650-V SiC device is selected for the final comparison.
- Optimization results of the resonant and the boost stage are combined and the total pareto front of the hybrid topology from Fig. 5.4 is obtained and compared with four-level FCML boost topology previously optimized. Results of the comparison show that losses of both topologies are in the same range, while hybrid, PPP topology provides lower occupied volume. The main reason for this is voltage rating of (input/output)/(dc bus) capacitors that is double in case of FCML topology. This shows the importance of voltage balancing of splitted dc bus capacitors of the hybrid topology provided by the resonant stage, beside the high efficiency already discussed.
- New classes of 650-V and 900-V WBG devices employed in hybrid, multi-level, step-up dc/dc topologies improve the energy delivered to the grid compared to the standard two-level dc/dc topologies with 1200-V Si modules in 1000-V PV system - losses in dc/dc stage during the year are decreased by up to 73.33 % for 400-V ac grid connection and by 56.67 % for 480 V ac voltage level. Additionally, multi-level topologies provide the possibility of use of 650-V and 900-V WBG devices in 1500-V PV systems. In this way the problem of high voltage derating and use of semiconductor devices rated for more than 1700 V is avoided.
- The previously described theoretical analysis is fully experimentally confirmed by building and measuring a 10-kW prototype of 8.26 kW/kg of specific power and 404.6-cm³ of volume occupied only by the power stage components. The *Euro Efficiency* of 99.48 % in nominal input/output voltage conditions is achieved.

5.2.3 Secondary Contributions of the Thesis

As already mentioned, on the way to the results obtained on the main subject of this dissertation, some secondary contributions are obtained and they can be summarized as follows:

- Since the resonant current shape of the BRC stage influences the design of the magnetic components, as much as the design of the rest of the circuitry, one of the

contributions of Chapter 3 is developing the equations that describe the behaviour of the resonant current shape under different load and input voltage conditions, that is not possible by the simple assumption $i_{\text{RES}}(t) = \pi I_{\text{OUT}} \sin(\omega_{\text{RES}}t)$ that is presented in [126]. Actually, this solution is only valid under high loads, close to the nominal. Analytical equations presented in this work provide the possibility of analysis of different phenomena related to this resonant current shape that will be discussed later in the following sections. Additionally, with this solution it is possible to run an optimization of the converter under different conditions and in such a way to provide a pareto front based on the *Euro Efficiency*, that is very important in PV industry [130, 131], instead of the efficiency under nominal conditions.

- A back-to-back losses measurement technique for voltage-fed converters that operate in open loop is presented. This method represents a good compromise between precision, time consumption and complexity to be implemented.
- A simplified C_{OSS} model for the prediction of ZVS conditions in applications where switching voltages are in range of several hundreds of Volts is presented. This model is simple enough to be included in the optimization program without increasing the time consumption of calculations while simultaneously demonstrating high accuracy.
- It is shown by the detailed mathematical model and graphical explanations that, in the three-level boost topology, by controlling the negative value of the inductor current, necessary for obtaining ZVS transition in the switches, the flying capacitor voltage always converge to the ideal value of $V_{\text{OUT}}/2$, for the full input voltage range, as long as the load is higher than zero. Nevertheless, when the output consumption drops to the zero value, the mathematical model shows that in case for $V_{\text{IN}} > V_{\text{OUT}}/2$, the flying capacitor voltage will still converge to the ideal balanced value, while for boosting factor higher than 2, it is discovered that the charge balance of the flying capacitor is always zero, no matter on the deviation of $V_{C_{\text{fly}}}$ from the ideal value. This behaviour leads to the static instability of the flying capacitor voltage for $V_{\text{IN}} < V_{\text{OUT}}/2$ and no-load conditions.
- A very simple control modification is proposed to deal with the previously discussed issue. It assumes manipulation of the data already available in the FPGA control board and recalculation of the T_{ON} time in the second half of the switching period in order to obtain flying capacitor charge of the opposite sign than the $\hat{V}_{C_{\text{fly}}}$ perturbation.

5.3 Guidelines for the Future Work

Although the work presented in this dissertation is comprehensive, covers a lot of subjects and provides many useful results and contributions, still it represents only a good basis and starting point for the research that should be conducted in the future on this very interesting topic with a lot of questions pending to be answered.

5.3.1 Additional Investigation to Complement the Presented Design

The work presented in the previous chapters is primarily related to the design of the power stage, efficiency, compactness, thermal issues, etc. From the point of view of control, only the current loop in the boost stage with the variable switching frequency and TCM operating mode is discussed. Even this is discussed referring to the efficiency and thermal issues. Nevertheless, there are a lot of questions, related to the control, pending to be answered:

- Since the proposed hybrid, dc/dc topology is designed for the operation in PV systems, the MPPT is very important issue to be addressed [181–183]. It is necessary to test the operation of the proposed topology under real environmental conditions and variation of the operating point on a daily level and to find the most appropriate MPPT algorithm to be applied [181].
- Operation under variable conditions considers the change of the operating modes of the proposed dc/dc topology [see Fig. 5.4(c)]. However, the transitions between the operating modes are not covered in the previous chapters, but they are very important for the stable operation of the proposed topology in the application of interest. A lot of authors deal with the mentioned subject of change of the operating modes [139, 140, 184] and some of them could be considered to be applied on the topology from Fig. 5.4.
- Until now, the dc/dc topology is analyzed separately from the inverter stage. In order to address stability issues, it is crucial to test the proposed topology under the operation together with the inverter stage. Additionally, previously mentioned transitions between the operating modes of the dc/dc part will influence the operation of the inverter stage, since the MPPT algorithm is transferred between dc/dc and dc/ac part for different operating ranges. A similar problem is presented in [33].

As shown in Chapter 4, the driving circuitry occupies a significant part of the total converter volume. Due to this, the commercial drivers from Wolfspeed/Cree [165, 166]

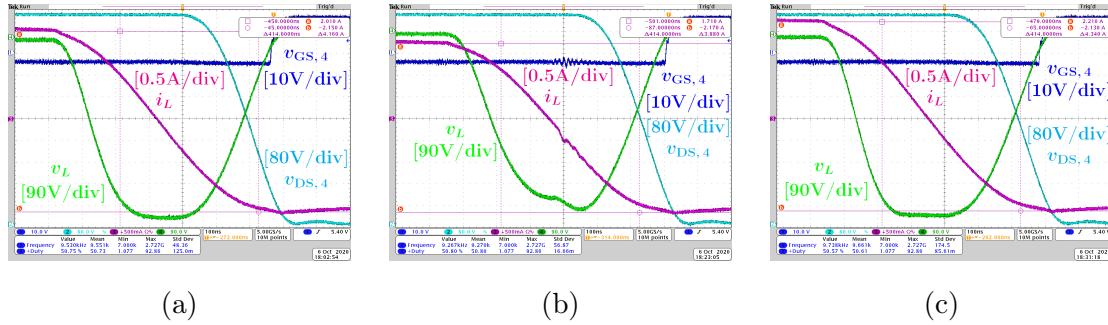


Fig. 5.6: Experimental verification of the prediction of the optimal ZVS conditions by the presented simplified model of the non-linear C_{OSS} . Results are presented for the single-phase BRC with the resonant inductor in DC side [see Fig. A.2(a)] and C3M0120090J device (three in parallel). The converter operates under the following conditions: $V_{IN,BRC} = 750\text{ V}$, $V_{OUT,BRC} = 1500\text{ V}$ and $P_{IN,BRC} = 1.7\text{ kW}$. Labels in the figure correspond to the ones in Fig. A.2(a). (a) Full ZVS transition with the optimal values of I_{pos} and I_{neg} ($I_{pos} = 2.01\text{ A}$, $I_{neg} = -2.15\text{ A}$ and $f_{SW} = 9.53\text{ kHz}$). (b) Partial ZVS transition ($I_{pos} = 1.71\text{ A}$, $I_{neg} = -2.17\text{ A}$ and $f_{SW} = 9.27\text{ kHz}$). (c) Full ZVS transition with oversized values of I_{pos} and I_{neg} ($I_{pos} = 2.21\text{ A}$, $I_{neg} = -2.13\text{ A}$ and $f_{SW} = 9.73\text{ kHz}$).

that are used in this work, need to be replaced and custom drivers to be designed in order to decrease the volume occupied. One of the techniques presented in the literature could be considered for this future investigation line [128, 167, 168].

Section 3.3.1 explains the operating principle and design aspects of the resonant stage of the proposed hybrid dc/dc topology. One of the main advantages of this topology are full ZVS transitions in all the switches under all the operating conditions. However, in order to obtain this feature, a certain value of the resonant current for starting the ZVS transition is necessary to be obtained. Calculation of this resonant current value and "optimal" ZVS conditions are discussed in Appendix A. In the same appendix it is experimentally confirmed that the full ZVS transition can be obtained with the resonant current value higher than the optimal one [see Fig. 5.6(c)]. However, in this case, the switching frequency of the resonant stage is higher, and the switching turn-off losses are increased. On contrary, without sufficiently high starting ZVS current value, no ZVS conditions are obtained (in most of the cases it is partial ZVS) [see Fig. 5.6(b)]. Additionally, it is also explained in the mentioned section and appendix that "the optimal" ZVS current value depends on the operating conditions. In all the measured points presented in this thesis, "the optimal" ZVS transitions are obtained manually by changing the resonant and dead times duration directly on the FPGA board for the previously set operating conditions. Nevertheless, for the final product design, it is necessary to provide the automatic adjustment of the resonant and dead times duration in order to obtain "the optimal" ZVS conditions under the all operating points. So, as a part of the future work could be considered a technique for optimal ZVS conditions detection in the BRC stage under different operating points.

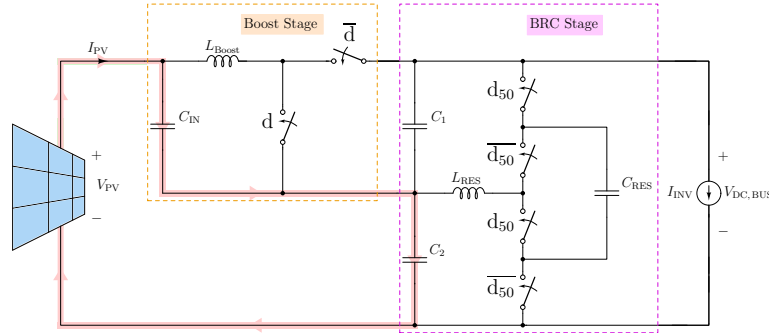


Fig. 5.7: Inrush current path of the proposed hybrid dc/dc topology.

An interesting solution is proposed by the authors in [119] where the switching node voltage is measured and according to its behaviour, the ideal ZCS conditions are detected.

Another issue that is not covered in this thesis is related to the surge start-up current of the proposed topology. Fig.5.7 shows the inrush current path that is marked in the red color and consists of the input capacitor of the boost stage (C_{IN}) and low-side dc bus capacitor of the resonant stage (C_2). The simplest way to avoid this issue is a soft start resistor placed between the converter and the PV string. One of the future actions to complement the current results could be the design of the less lossy soft start technique [185–187].

The reliability improvement of PV inverters is the important factor for reducing the cost of PV energy since it is closely connected to the annual energy production as well as the maintenance cost of PV systems [73,188]. Data indicate that the inverter is the element of the photovoltaic plant that has the highest number of service calls and the greatest operation and maintenance cost burden (the inverters constitute between 43 %, for the commercial, and 70 %, for the utility scale, of the PV power plant service requests) [189]. Therefore, it is required to extend the lifetime of the PV inverter from the current expected lifetime of 10-15 years to 20-30 years to balance the lifetime with other parts in the PV system [73]. Since the the proposed hybrid dc/dc topology is designed to operate as a part of the grid-connected string inverter, one of the future investigation lines could be related to the influence of the different environmental conditions and control strategies on its reliability and lifetime [190,191].

5.3.2 Adjusting the Proposed Hybrid DC/DC Topology to the Buck-Boost Operation

As concluded in Chapter 2, total output filter volume of the inverter stage can be reduced by $\approx 50\%$ controlling its dc bus at the minimum value. This design with a reduced filter size still will comply with all the application requirements. However, in order to have

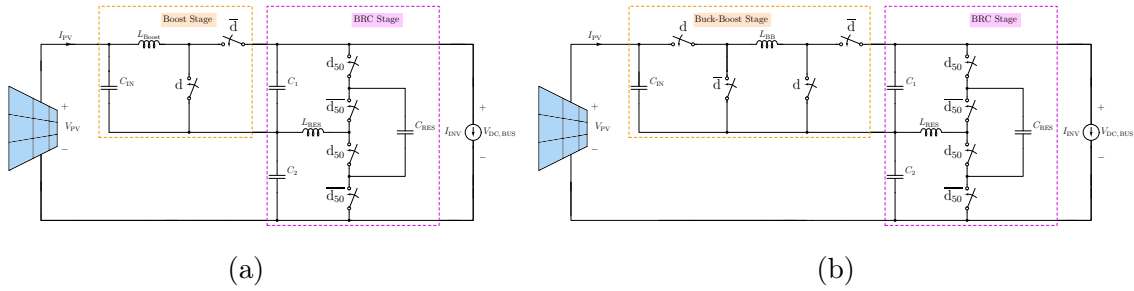


Fig. 5.8: (a) Proposed hybrid dc/dc topology. (b) Modification of the proposed hybrid dc/dc topology with included buck-boost operation.

less variation in the dc bus voltage it is necessary to insert a dc/dc stage between PV string/array and the inverter part. This means that there is a possibility of increase of the total system volume and losses. From the point of view of losses, it is already shown in Section 2.3 that inclusion of a dc/dc stage can improve significantly energy harvested from the PV string during the year - system losses can be decreased by up to 3.25 MWh in case of 22-kW system, 1500-V PV string and 600-V ac grid connection. Or in other words, considering the price of 160 \$ per MWh for residential-scale solar [192], 520 \$ per year is saved for a 22-kW system.

Additionally, in recent years a lot of authors are using new commercially available WBG devices rated for 650-V and 900-V in combination with multi-level and partial power processing concepts to design dc/dc topologies of very high efficiencies and power densities. The work presented in this thesis proposes a hybrid, partial power processing, multi-level dc/dc topology rated for 20 kW power and 1500-V PV system that occupies $\approx 0.8 - 0.9 \text{ dm}^3$. This is far below the improvement that can be achieved by the reduction of dc bus voltage variation. Still, one can notice that the mentioned topology can either boost PV voltage either be short-circuited. However, in order to control dc bus voltage around some value, a buck-boost operation is necessary.

A very interesting modification of the topology presented in Chapter 3 is given in [193] where the boost part of the hybrid topology, that is in charge of controlling a dc bus voltage, is replaced by the four-switches buck-boost topology (see Fig. 5.8). In this way, partial power processing concept is kept, and the topology is improved by added feature of reducing the input voltage. However, more work and investigation on the optimization of this topology is necessary to be done since it is known from literature that buck-boost topology is less efficient and compact than the boost converter. Anyway, the topology presented in [193] with the concept analyzed in details in this thesis is a very good candidate for a dc/dc stage that can control dc bus voltage at the input of the inverter stage and that can improve significantly the compactness of the inverter stage and of the whole system.

5.3.3 Extension of the Application Range of the Proposed Hybrid DC/DC Topology

PV systems reach the so-called *grid parity* when the LCOE reaches the cost of the electricity produced from traditional fossil fuels [40]. In order to further increase the contribution of PV in the total energy production, it is necessary to work toward large-scale PV plants. For the power levels approaching 100 MW, current value becomes high and increasing the voltage level in the point of common coupling (PCC) is required. This will result in higher ratio transformers or more transformation stages in series to connect to a MV or HV grid [43]. One way to avoid this issue is to increase the dc voltage level over 1500 V and to pass into the MV level at dc side. Increase of the voltage level on both, dc and ac side, would decrease losses in the cables by $\approx 50 - 60\%$ [40], but on the other hand will cause the change of standards that the power processing systems need to comply with. A medium voltage dc-collection grid approach has been explored in large-scale offshore wind power systems and has been shown to improve conversion efficiency due to the elimination of several conversion stages [41]. An important component of a medium-voltage dc-collection grid is a dc/dc step-up converter [41]. Large-scale PV system architectures with reduced transformer stages can be realized by using high-gain dc/dc converters [43].

All the results discussed in this dissertation on the hybrid dc/dc topology presented in Chapter 3 represent a very good basis for the further investigation in the field of the MV dc-collection grids. The same concept can be applied for the voltages higher than 1500 V. This will penalize the blocking voltage of the semiconductors and the higher rated devices than the ones analyzed in this work should be considered. In order to reach the appropriate power level, a parallelizing of a dc/dc stage for the single central inverter could be considered. Of course, as already mentioned, it will be interesting to investigate the fulfillment of the standards in the MV voltage range by the dc/dc topology proposed in this thesis and compare it to the state-of-the-art solutions [41, 194, 195] in terms of efficiency, power density, complexity, cost, etc.

APPENDICES

Analysis of ZVS Conditions

ONE of the key performances of the dc/dc topologies analyzed in the Chapter 3 and 4 is obtaining the full ZVS transitions in all the switches under the all operating conditions. On the other side, analysis of ZVS conditions is strongly impacted by the non-linear C_{OSS} capacitance that highly depends on the switching voltage. A lot of authors deal with the subject of the modeling of MOSFET output capacitance and losses related to it [178–180]. However, these models are too complex and time consuming to be included in the optimization algorithm described in Section 4.2. In order to reconcile the model precision and its complexity, the model presented in [143] is refined and a simplified C_{OSS} model for the prediction of ZVS conditions in applications where switching voltages are in range of several hundreds of Volts is presented in this appendix. This model is simple enough to be included in the optimization program without increasing the time consumption of calculations while simultaneously demonstrating high accuracy.

A.1 Approximated C_{OSS} Model

As previously discussed in Chapter 4, a model in which ZVS conditions could be predicted is presented in [143]. In Fig. A.1 a curve provided by the manufacturer and approximation of MOSFET C_{OSS} capacitance are presented:

$$C_{OSS} = \begin{cases} C_0, & \text{if } V_{DS} < V_0 \\ C_1, & \text{if } V_0 \leq V_{DS} < V_{DS,max} \end{cases} \quad (\text{A.1})$$

where C_0 is value of C_{OSS} for $V_{DS} = 0$ V and C_1 is value of C_{OSS} for $V_{DS} = 900$ V. The value of V_0 is selected in such a way that the accumulated charge (Q_{OSS}) and energy (E_{OSS}) are relatively close for approximated capacitance and curve provided by manufacturer. It is obvious that this model highly overestimates Q_{OSS} and E_{OSS} for low values of V_{DS} . However, in this particular case, MOSFET blocking voltages are expected to be half of the dc bus voltage (750 V) plus the ripple in the resonant capacitor (up to 130 V) in the BRC stage (as discussed in Section 3.3.1). Therefore, this model can be accepted as an effective compromise between simplicity and accuracy, which is verified by experimental results.

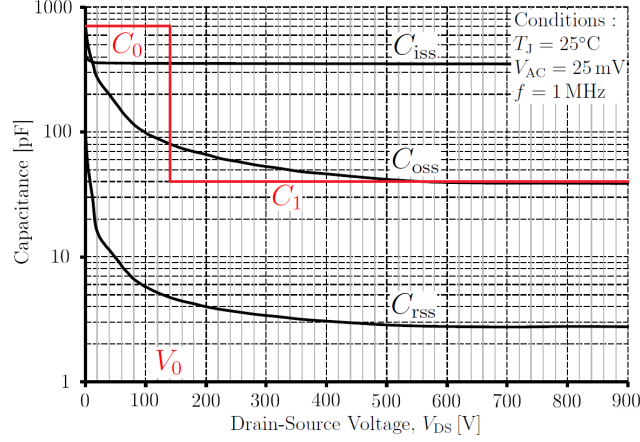


Fig. A.1: Parasitic capacitances of C3M0120090J MOSFET. Black curves are provided by the manufacturer, and red curves are the approximated values.

According to this approximation, capacitance that in [143] is denoted as *linear charge-equivalent capacitance* can be calculated as:

$$C_{Q,eq}(V_{DS}) = \frac{\int_0^{V_{DS}} C_{OSS}(v) dv}{V_{DS}} = \begin{cases} N_{mos}C_0, & \text{if } V_{DS} < V_0 \\ N_{mos} \frac{C_0V_0 + C_1(V_{DS} - V_0)}{V_{DS}}, & \text{if } V_0 \leq V_{DS} < V_{DS,max} \end{cases} \quad (\text{A.2})$$

where N_{mos} is the number of MOSFETs in parallel. It should be mentioned that in (A.2) case $V_{DS} < V_0$ is presented only in order to emphasize its existence. However, as mentioned in the previous paragraph, this scenario highly overestimates accumulated charge and also will not be present in any of the operating points in this particular case.

Also in [143], a model for losses calculation in case of partial ZVS is presented. Here are listed equations for calculation of the parameters that determine partial ZVS losses, according to the previously explained C_{OSS} approximation. Parameters are denoted in exactly the same way as in [143].

Thus, the charge accumulated in C_{OSS} for certain blocking voltage (V_{DS}) is:

$$\begin{aligned}
Q_{OSS}(V_{DS}) &= \int_0^{V_{DS}} C_{OSS}(v) dv = \\
&= \begin{cases} N_{mos}C_0V_{DS}, & \text{if } V_{DS} < V_0 \\ N_{mos}(C_0V_0 + C_1(V_{DS} - V_0)), & \text{if } V_0 \leq V_{DS} < V_{DS,max} \end{cases}
\end{aligned} \tag{A.3}$$

while for the same voltage level, accumulated energy in C_{OSS} can be estimated as:

$$\begin{aligned}
E_{OSS}(V_{DS}) &= \int_0^{V_{DS}} vC_{OSS}(v) dv = \\
&= \begin{cases} \frac{N_{mos}C_0V_{DS}^2}{2}, & \text{if } V_{DS} < V_0 \\ \frac{N_{mos}(C_0V_0^2 + C_1(V_{DS}^2 - V_0^2))}{2}, & \text{if } V_0 \leq V_{DS} < V_{DS,max} \end{cases}
\end{aligned} \tag{A.4}$$

Initial energy at the beginning of the ZVS transition is:

$$E_{initial} = E_{oss}(V_{DS}) + \frac{LI_{off}^2}{2} \tag{A.5}$$

where I_{off} is the value of the inductor current at the beginning of ZVS transition. The remaining ΔV voltage in the case of partial ZVS transition is calculated as:

$$\Delta V = \begin{cases} V_{DS} - \sqrt{\frac{V_{DS}^2}{2} + K_1}, & \text{if } \Delta V \leq V_0 \\ & \text{and } V_{DS} - \Delta V \leq V_0 \\ V_{DS} - \sqrt{V_{DS}^2 + K_2}, & \text{if } \Delta V \leq V_0 \\ & \text{and } V_{DS} - \Delta V > V_0 \\ V_{DS} - \sqrt{V_{DS}^2 + K_3}, & \text{if } \Delta V > V_0 \\ & \text{and } V_{DS} - \Delta V \leq V_0 \\ V_{DS} - \sqrt{V_{DS}^2 + K_4}, & \text{if } \Delta V > V_0 \\ & \text{and } V_{DS} - \Delta V > V_0 \end{cases} \tag{A.6}$$

where the constants K_1 , K_2 , K_3 and K_4 are:

$$K_1 = \frac{E_{\text{initial}} - V_{\text{DS}}Q_{\text{oss}}(V_{\text{DS}})}{C_0} \quad (\text{A.7})$$

$$K_2 = 2K_1 \frac{C_0}{C_0 + C_1} - \frac{(C_0 - C_1)V_0^2 + C_1V_{\text{DS}}^2}{C_0 + C_1} \quad (\text{A.8})$$

$$K_3 = 2K_1 \frac{C_0}{C_0 + C_1} - \frac{C_0(V_{\text{DS}} - V_0)^2 + C_1V_0(2V_{\text{DS}} - V_0)}{C_0 + C_1} \quad (\text{A.9})$$

$$K_4 = K_1 \frac{C_0}{C_1} + V_0^2 + \frac{C_0}{C_1}V_0(V_{\text{DS}} - V_0) - V_{\text{DS}} \left(V_0 + \frac{V_{\text{DS}}}{2} \right) \quad (\text{A.10})$$

The remaining charge necessary to charge output capacitance of the switch that is turning off is:

$$\Delta Q_{S_2} = Q_{\text{oss}}(V_{\text{DS}}) - Q_{\text{oss}}(V_{\text{DS}} - \Delta V) \quad (\text{A.11})$$

Finally, according to [143], dissipated energy during partial ZVS transition (iZVS) is:

$$E_{\text{diss, iZVS}} = E_{\text{oss}}(\Delta V) + \Delta Q_{S_2} V_{\text{DS}} - (E_{\text{oss}}(V_{\text{DS}}) - E_{\text{oss}}(V_{\text{DS}} - \Delta V)) \quad (\text{A.12})$$

Accumulated charge $Q_{\text{oss}}(V_{\text{DS}} - \Delta V)$ is calculated in the same manner as $Q_{\text{oss}}(V_{\text{DS}})$ and accumulated energies $E_{\text{oss}}(\Delta V)$ and $E_{\text{oss}}(V_{\text{DS}} - \Delta V)$ are calculated in the same way as $E_{\text{oss}}(V_{\text{DS}})$.

The model of non-linear C_{OSS} presented here is used in the optimization algorithm from Chapter 4 to calculate the optimal values of the resonant current for starting ZVS transition [denoted as I_{pos} and I_{neg} in Fig. A.2(b) and A.2(d)] according to the following equations [127]:

$$I_{\text{neg}} = -V_{\text{IN, BRC}} \sqrt{\frac{2C_{Q, \text{eq}}}{L_{\text{RES}}}} \quad (\text{A.13})$$

$$I_{\text{pos}} = \begin{cases} V_{C, \text{max}} \sqrt{\frac{2C_{Q, \text{eq}}}{L_{\text{RES}}}}, & \text{for DC side inductor} \\ -I_{\text{neg}}, & \text{for AC side inductor} \end{cases} \quad (\text{A.14})$$

where $C_{Q, \text{eq}}$ is calculated by (A.2) and term $V_{C, \text{max}}$ refers to the peak value of the voltage in the resonant capacitor. The term ‘‘optimal value’’ of the inductor current refers to the minimal value necessary to achieve ZVS. The optimal value for I_{pos} is obtained under the

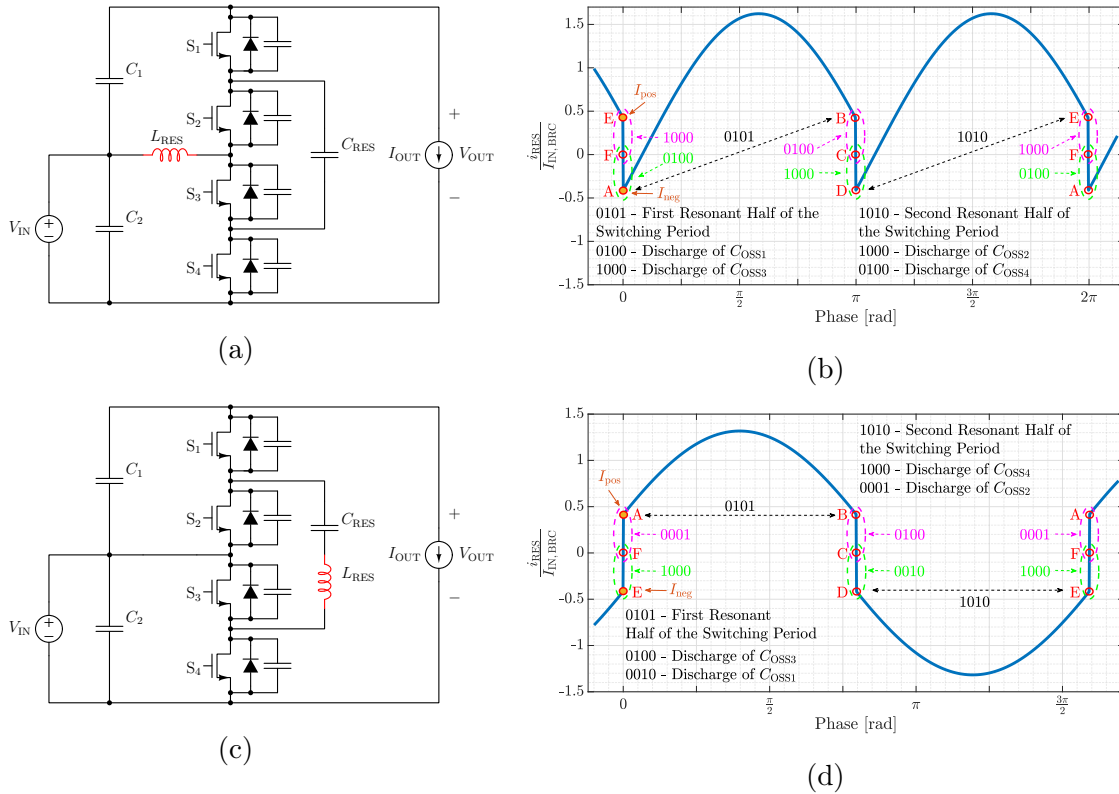


Fig. A.2: BRC stage. DC side inductor (a) schematic and (b) waveform of the inductor current with marked and explained important intervals of the switching period. AC side inductor (c) schematic and (d) waveform of the inductor current with marked and explained important intervals of the switching period.

assumption that the ZVS transition in the corresponding switch has finished in precisely the moment that the resonant current reaches zero, while the optimal value for I_{neg} is obtained under the assumption that the voltage of its counter pair switch reaches zero in the moment when the resonant inductor current reaches I_{neg} [127]. As can be seen from (A.14), the calculation of I_{pos} is different for the DC side and AC side inductors. This is due to the fact that with the AC side inductor, MOSFETs block only half of the output voltage, while in the case of the DC side inductor, voltage blocked by the MOSFETs additionally includes voltage ripple in the resonant capacitor, which can be considerably high in some cases.

The same model, in the similar manner is used to calculate the negative value of the FCML and the two-phase boost inductor current (I_{zvs}) operating in TCM mode with variable switching frequency discussed in Section 3.2 and 4.2.

The common name for I_{zvs} , I_{pos} and I_{neg} is I_{off} from (A.5). More details on the switching sequences and design aspects related to obtaining ZVS transitions in all the analyzed dc/dc topologies can be found in Section 3.2 and 3.3.1. Fig. A.2 and equations

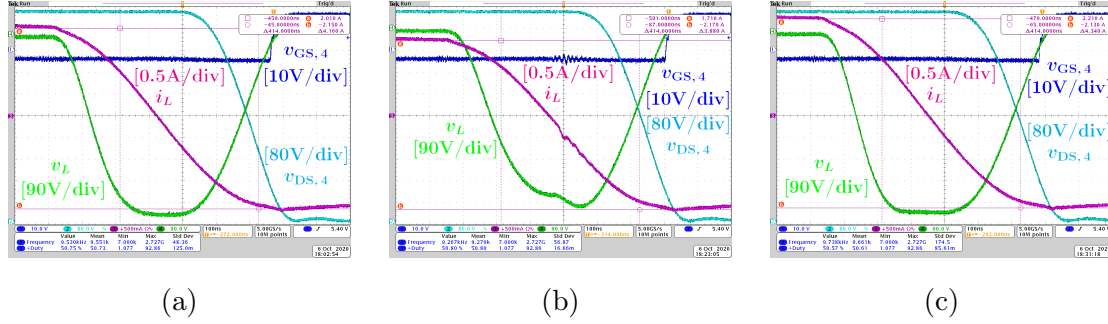


Fig. A.3: Experimental verification of the prediction of the optimal ZVS conditions by the presented simplified model of the non-linear C_{OSS} . Results are presented for the single-phase BRC with the resonant inductor in DC side [see Fig.A.2(a)] and C3M0120090J device (three in parallel). The converter operates under the following conditions: $V_{IN,BRC} = 750\text{ V}$, $V_{OUT,BRC} = 1500\text{ V}$ and $P_{IN,BRC} = 1.7\text{ kW}$. Labels in the figure correspond to the ones in Fig. A.2(a). (a) Full ZVS transition with the optimal values of I_{pos} and I_{neg} ($I_{pos} = 2.01\text{ A}$, $I_{neg} = -2.15\text{ A}$ and $f_{SW} = 9.53\text{ kHz}$). (b) Partial ZVS transition ($I_{pos} = 1.71\text{ A}$, $I_{neg} = -2.17\text{ A}$ and $f_{SW} = 9.27\text{ kHz}$). (c) Full ZVS transition with oversized values of I_{pos} and I_{neg} ($I_{pos} = 2.21\text{ A}$, $I_{neg} = -2.13\text{ A}$ and $f_{SW} = 9.73\text{ kHz}$).

(A.13)-(A.14) are already given in Section 3.3.1, but they are repeated here for sake of clarity of the analysis conducted in this appendix.

A.2 Experimental Validation

A simplified C_{OSS} model is presented and the accuracy of the prediction of "the optimal value" of the inductor current, which is necessary for obtaining ZVS transitions, is verified by the measurements presented in Fig. A.3. Results are given for the single-phase BRC with the resonant inductor in DC side [see Fig. A.2(a)] and C3M0120090J device (three in parallel). The converter is placed in a certain operating point (in this specific case $V_{IN,BRC} = 750\text{ V}$, $V_{OUT,BRC} = 1500\text{ V}$ and $P_{IN,BRC} = 1.7\text{ kW}$) and the resonant and dead times are finely adjusted until the converter changes from the partial ZVS into the full ZVS. This state is considered as "the optimal ZVS transition" and the I_{pos} and I_{neg} in this state are considered "the optimal values". The following cases can be noticed in Fig. A.3:

1. Full ZVS transition with the optimal values of I_{pos} and I_{neg} ($I_{pos} = 2.01\text{ A}$, $I_{neg} = -2.15\text{ A}$ and $f_{SW} = 9.53\text{ kHz}$) in Fig. A.3(a),
2. Partial ZVS transition ($I_{pos} = 1.71\text{ A}$, $I_{neg} = -2.17\text{ A}$ and $f_{SW} = 9.27\text{ kHz}$) in Fig. A.3(b) and
3. Full ZVS transition with oversized values of I_{pos} and I_{neg} ($I_{pos} = 2.21\text{ A}$, $I_{neg} = -2.13\text{ A}$ and $f_{SW} = 9.73\text{ kHz}$) in Fig. A.3(c).

Table A.1: COMPARISON OF THE ESTIMATED AND MEASURED VALUES OF THE CURRENT OF THE RESONANT INDUCTOR THAT ARE NECESSARY FOR FULL ZVS TRANSITIONS.

(a)

Device	C_0	C_1	V_0
C3M0120090J	700 pF	40 pF	70 V
C3M0065090J	1000 pF	60 pF	70 V

(b)

Device	Ind. Pos.	$P_{N,BRC}$	$V_{IN,BRC}$	$V_{C,max}$	L_{RES}	C_{RES}	$C_{Q,eq}$	I_{pos}			I_{neg}		
								Calc.	Meas.	Err.	Calc.	Meas.	Err.
3 x C3M0120090J	DC	1.7 kW	750 V	766 V	74 μ H	4.5 μ F	301 pF	2.20 A	2.00 A	9.09%	-2.15 A	-2.15 A	0.00%
		4.0 kW	750 V	788 V	74 μ H	4.5 μ F	296 pF	2.24 A	2.74 A	22.3%	-2.13 A	-2.23 A	4.69%
	AC	1.7 kW	750 V	750 V	74 μ H	4.5 μ F	305 pF	2.17 A	2.00 A	3.23%	-2.17 A	-2.05 A	5.53%
		4.0 kW	750 V	750 V	74 μ H	4.5 μ F	305 pF	2.17 A	2.08 A	4.15%	-2.17 A	-2.13 A	1.84%
2 x 2 x C3M0065090J	2 DC	1.7 kW	750 V	761 V	74 μ H	2 x 1.5 μ F	586 pF	3.07 A	3.01 A	1.95%	-3.02 A	-2.69 A	10.9%
		4.0 kW	750 V	777 V	74 μ H	2 x 1.5 μ F	579 pF	3.11 A	3.43 A	10.3%	-3.01 A	-2.70 A	10.3%

Current values are calculated according to (A.14) and (A.13).

(a) Approximated parameters of the MOSFET according to the data sheets of the devices [117] and the model described in this appendix.

(b) Comparison of the calculated results with the measured values.

The inductor position labeled as "2 DC" refers to the two-phase interleaved BRC described in Section 3.3.3.

In case of Fig. A.3(c), the full ZVS transition is obtained, but the value of the switching frequency is increased compared to "the optimal conditions". Increased switching frequency leads to the increased switching losses during the devices' turn-off transitions.

The same procedure described in the previous paragraph is applied to the other topological variations of the BRC under different operating conditions with both analyzed 900-V SiC devices in order to obtain the optimal resonant current values for starting ZVS transition and the results of these experiments are compared with the values estimated by the presented model. The comparison is summarized in Table A.1. The biggest relative error of 22.3% is obtained for single-phase BRC with DC side inductor and C3M0120090J device operating at $P_{IN,BRC} = 4$ kW. The rest of the values are estimated with the relative error in range of 10% or less.

It can be concluded that sufficiently high accuracy of prediction of the values of I_{pos} and I_{neg} is achieved with a relatively simple model that can be included in the optimization program without slowing down the calculations. Once again, it is important to emphasize that this model is accurate enough for switching voltage values enough higher than V_0 value. Otherwise, I_{pos} and I_{neg} values would be overestimated.

A.3 Appendix Summary

A simplified C_{OSS} model for the prediction of ZVS conditions in applications where switching voltages are in range of several hundreds of Volts is presented. This model is simple enough to be included in the optimization program without increasing the time consumption of calculations while simultaneously demonstrating high accuracy.

Experimental validation shows a maximal error of 22.3 % in the prediction of “the optimal” values of resonant current necessary for starting ZVS transition. The rest of the errors are in the range of 10 % or less. Starting switching transition with values of resonant current lower than “the optimal” ones leads to the loss of full ZVS and an increase in the temperature (losses) of the circuit components. Conversely, values higher than “the optimal” ones increase the RMS value of the resonant current and switching frequency and thus increase the temperature (losses) of the circuit components.

Static Instability of the Flying Capacitor Voltage in the Three-Level Boost Converter

MULTI-LEVEL converters since their first appearance, [52, 53], represent very popular topologies in both, dc/dc and dc/ac conversion. The multi-level operation, in combination with the effective multiplying of the switching frequency, results in favorable trade offs in terms of decreasing the switching ripples, decreasing the switching frequency, reducing the size of the filter elements, increasing the converter open-loop bandwidth, or increasing the converter efficiency, compared to the two-level topologies [54]. Additionally, in these converters switches' blocking voltage is reduced by factor of $1/(N - 1)$ with N number of levels. This have found very spread usage in the applications where switching voltages are in the range of several hundred of volts such as [55–57] and the work presented in this thesis. In this way, in combination with new classes of 650-V and 900-V WBG devices, very high efficiencies and power densities are achievable. This is already demonstrated in Chapter 4.

However, the main issue found in these topologies is related to the imbalance of the flying capacitor (FC) voltages that can cause overvoltage failure of the semiconductors or reduced converters' lifetime. Parasitic effects and circuit non-idealities that cause imbalance of the FC voltages are summarized in [196]. Natural balancing of the FC voltages and conditions under which it is achievable is investigated in [197–199]. Nevertheless, in most of the cases it is inevitable to use some kind of control of these variables. Works such as [54, 200] propose additional voltage loop for FC voltage. This approach is not very popular since it assumes implementation of additional hardware for FC voltage measurements. The works presented in [201–204] use inherent information of the FC voltage in the valley inductor current to modify control loop and control $v_{C_{\text{fly}}}$ without additional hardware. However, these approaches suffer from the lack of control ability under low-load conditions. The authors of [205] investigate basic stability properties of the three-level flying-capacitor buck converter when operated under current-mode control (CMC). The proposed analysis is developed for both peak CMC (P-CMC)

and valley CMC (V-CMC), and addresses both the static instability of the inductor current and the FC voltage runaway phenomenon. Control methods proposed in [206,207] are based on inherent control of $v_{C_{fly}}$ by controlling inductor current, without additional sensing circuitry and with good performances under all load and duty cycle conditions. Still, none of the previous works deals with FC voltage imbalance issue in the multi-level converters under TCM operating mode with variable switching frequency.

On the other hand, the analysis presented in Chapter 4 shows that achieving ZVS leads to the huge reduction of switching losses in the applications where blocking voltages are in the range 700 V - 800 V. The authors of [55] propose variation of f_{sw} in a certain range and under specific operating conditions in order to extend ZVS operating range. Additionally, experimental results of Chapter 3 show that even partial ZVS operation in this kind of applications can lead to the excessive temperature increase and failure of the switching devices. For this reason, and for the sake of achieving higher efficiency under full operating voltage and load range, the work presented in this thesis assumes TCM operating mode with variable switching frequency (f_{sw}) and constant T_{ON} control.

The main contribution of this appendix is the investigation of the FC voltage imbalance control in the three-level boost converter under TCM operating mode with variable f_{sw} and constant T_{ON} control. The analytical analysis is conducted and the load range in which the natural FC balance is achieved is determined by the presented model. The compensation action is proposed to balance FC voltage in the operating ranges where it is not achieved naturally.

B.1 Variable Switching Frequency Operation in the Three-Level Boost Topology

Investigated three-level boost (TLB) topology is depicted in Fig. B.1. Inductor and FC current together with applied switching sequence, explained processes that occur in each part of the switching period are presented in Fig. B.2 and B.3. The data is displayed for both ranges, $V_{IN} < V_{OUT}/2$ (see Fig. B.2) and $V_{IN} > V_{OUT}/2$ (see Fig. B.3) under steady-state and transient conditions due to a slight perturbation on the FC voltage, $\hat{V}_{C_{fly}}$. All the parts of the switching periods are marked with its switches arrangement and the explanation on the process that happens in each transition. Waveforms marked in red are assumed to be the steady-state ones. Waveforms marked in green are assumed to be the transient ones after the introduction of the small perturbation $\hat{V}_{C_{fly}}$. Circuit schematics with the explanations on the energy flow for each transition during the switching period are also depicted in these figures. Inductor energy is marked in blue, while the energy supplied from the output capacitor is colored in green.

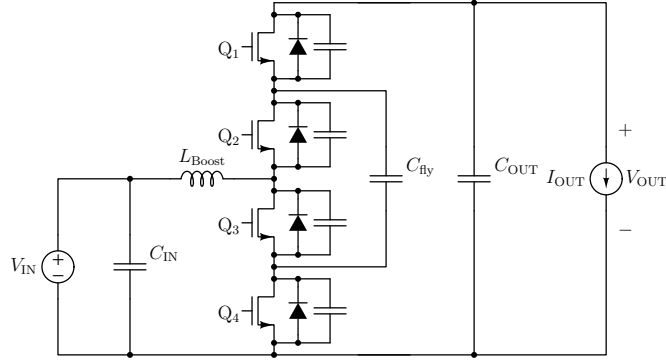


Fig. B.1: Three-level boost converter - schematic.

The analysis in the figures is presented for the loads higher than zero. It is assumed that dead-times duration in the inductor current positive peaks are equal, $t_{dp1} = t_{dp2}$, and also in the inductor current negative peaks, $t_{dn1} = t_{dn2}$. It is not necessary that "positive" and "negative" dead-times are equal between each other. T_{ON} time is dictated by the voltage loop and, at the beginning of the analysis, is assumed to be equal in both halves of the switching period, $T_{ON1} = T_{ON2}$. T_{OFF} times are parts of the switching period between the end of the "positive" ZVS transitions and negative inductor current I_{zvs} that is determined to be sufficient to obtain full ZVS transition under specific switching voltage level (see the discussion in Appendix A). I_{zvs} is fixed for the converter operation and it is determined by the external current detection circuit. This circuit sends a control pulse to the FPGA [142] when inductor current reaches specified negative value. When FPGA detects this pulse from the current detection circuit, it moves to the "negative" ZVS transition.

B.2 Subharmonic Oscillations Under the Variable Switching Frequency Operation

After roughly explaining the operation principle of the control scheme that is applied in this work, several features that mostly differs this operating mode to the constant switching frequency operation are discussed. Firstly, the work presented in [205] analyzes the issue of the subharmonic oscillations under constant f_{sw} operation. The subharmonic oscillations regions for V-CMC and P-CMC are determined considering a perfectly balanced FC voltage, $V_{C_{fly}} = V_{OUT}/2$. It is concluded that, in case of buck converter, inductor-current static stability regions of V-CMC and P-CMC when no compensating ramp is employed are: 1) $(0.25 < M < 0.5) \vee (0.75 < M < 1)$ for V-CMC and 2) $(0 < M < 0.25) \vee (0.5 < M < 0.75)$ for P-CMC, otherwise, compensation ramp is necessary to avoid subharmonic oscillations.

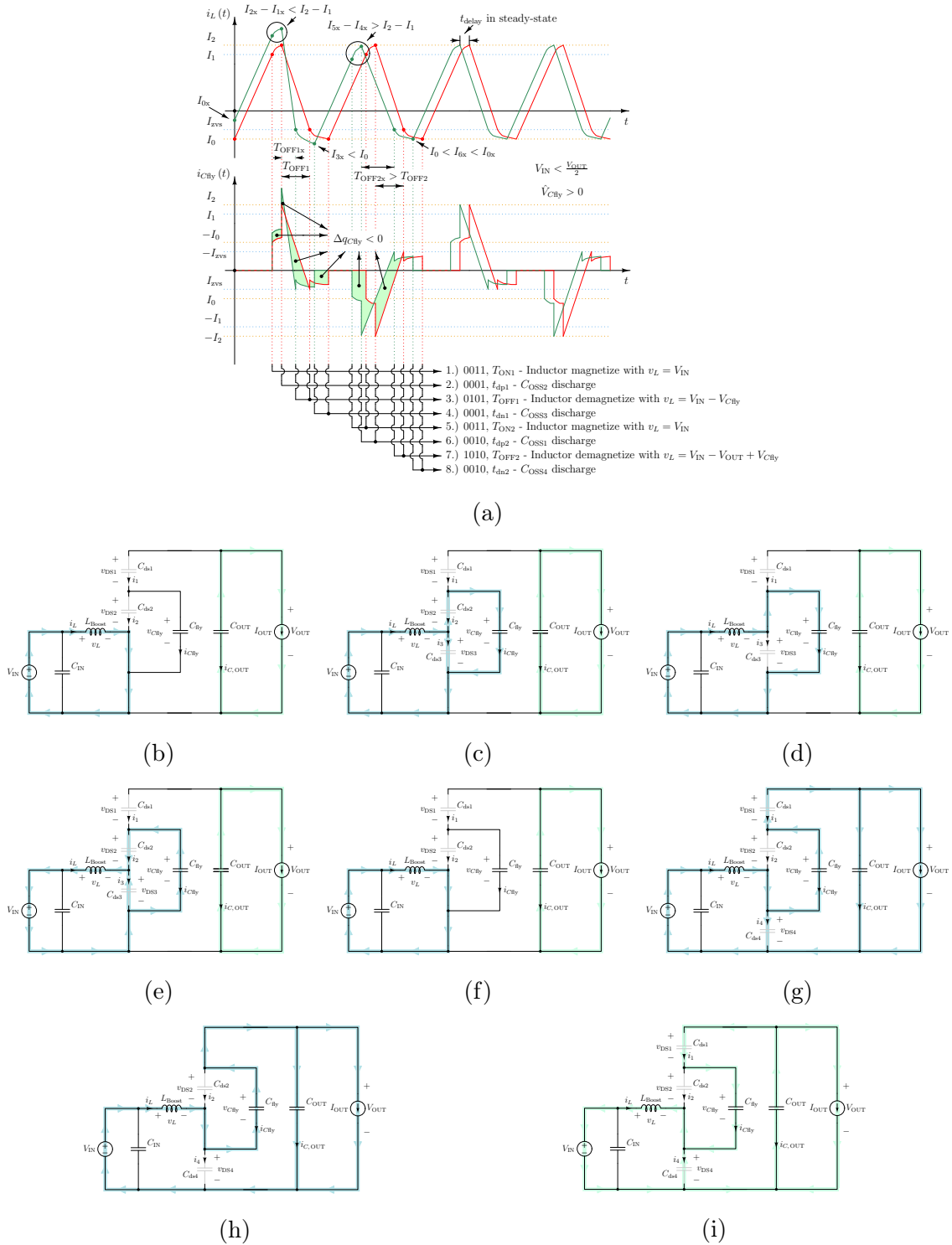


Fig. B.2: (a) Control sequence for variable frequency operation and $V_{IN} < V_{OUT}/2$. Details on the switching transitions: (b) 0011 (T_{ON1}) inductor magnetize with $v_L = V_{IN}$, (c) 0001 (t_{dp1}) C_{OSS2} discharge, (d) 0101 (T_{OFF1}) inductor demagnetize with $v_L = V_{IN} - V_{Cfly}$, (e) 0001 (t_{dn1}) C_{OSS3} discharge, (f) 0011 (T_{ON2}) inductor magnetize with $v_L = V_{IN}$, (g) 0010 (t_{dp2}) C_{OSS1} discharge, (h) 1010 (T_{OFF2}) inductor demagnetize with $v_L = V_{IN} - V_{OUT} + V_{Cfly}$, (i) 0010 (t_{dn2}) C_{OSS4} discharge.

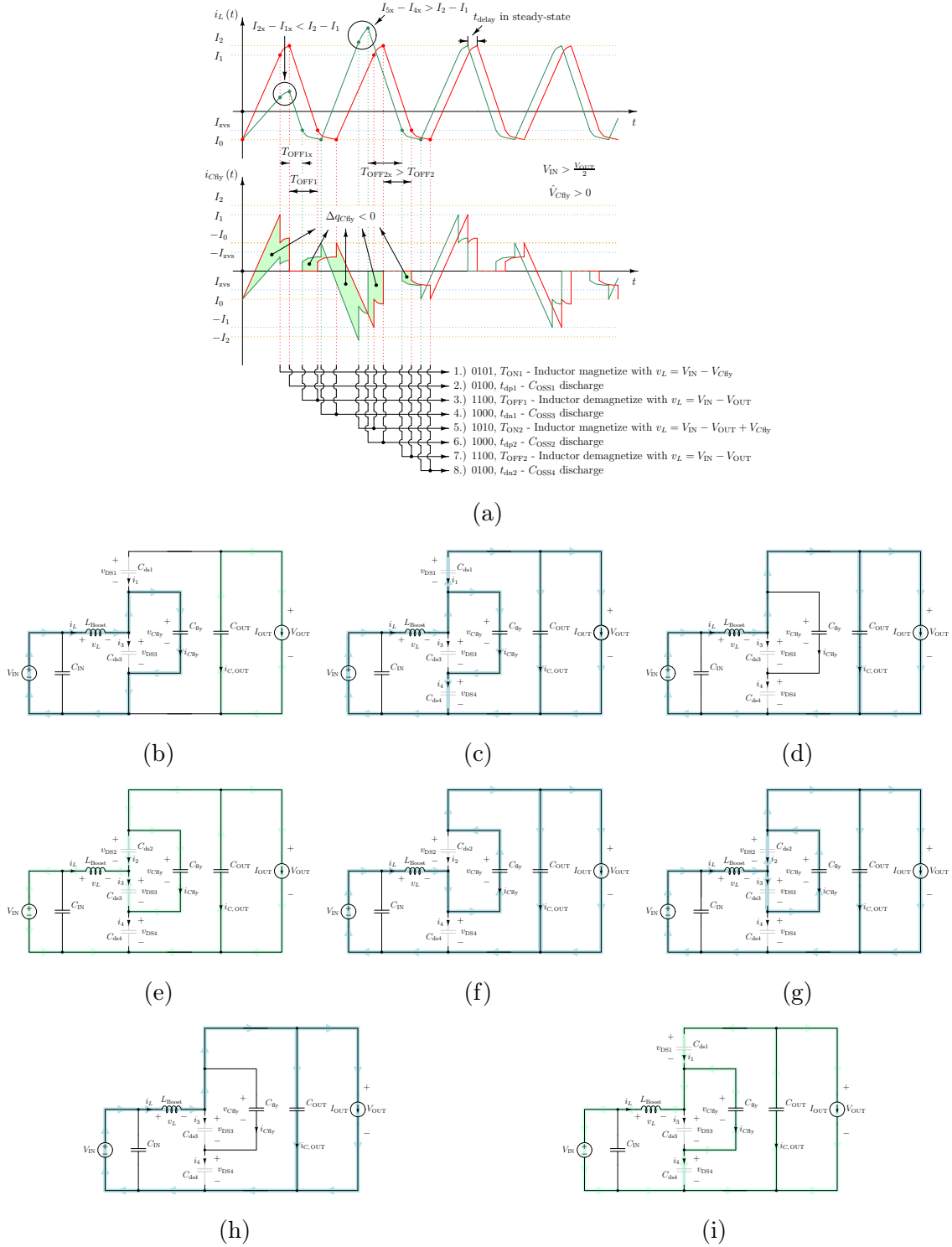


Fig. B.3: (a) Control sequence for variable frequency operation and $V_{IN} > V_{OUT}/2$. Details on the switching transitions: (b) 0101 (T_{ON1}) inductor magnetize with $v_L = V_{IN} - V_{CBy}$, (c) 0100 (t_{dp1}) C_{OSS1} discharge, (d) 1100 (T_{OFF1}) inductor demagnetize with $v_L = V_{IN} - V_{OUT}$, (e) 1000 (t_{dn1}) C_{OSS3} discharge, (f) 1010 (T_{ON2}) inductor magnetize with $v_L = V_{IN} - V_{OUT} + V_{CBy}$, (g) 1000 (t_{dp2}) C_{OSS2} discharge, (h) 1100 (T_{OFF2}) inductor demagnetize with $v_L = V_{IN} - V_{OUT}$, (i) 0100 (t_{dn2}) C_{OSS4} discharge.

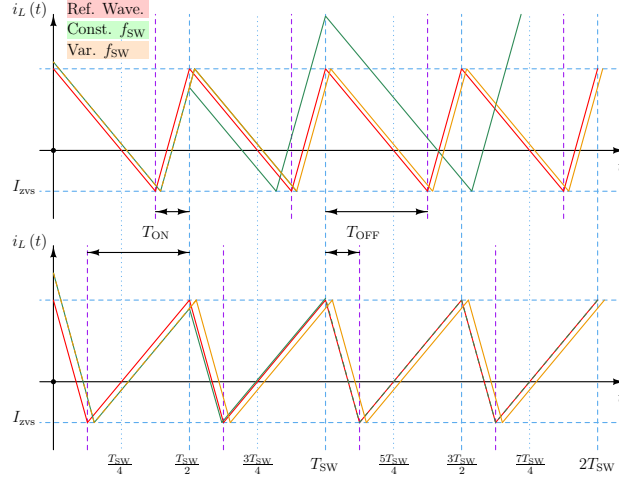


Fig. B.4: Subharmonic oscillations - comparison of the behaviour of the constant and variable switching frequency V-CMC operating modes under the same initial perturbation of the inductor current.

The previous conclusion can be explained in a different way: in case of the V-CMC and constant frequency operation, when the inductor current rise time is higher than the fall time, initial perturbation will decrease in each following switching cycle. On contrary, if the inductor current fall time is higher than the rise time, initial current perturbation will increase and cause static instability of the inductor current. For the P-CMC operating mode, the stability regions are determined in the opposite way.

An example of the comparison of the V-CMC operating mode under the constant and variable switching frequency operation in terms of subharmonic oscillations, under the same assumption of a perfectly balanced FC voltage, $V_{C_{fly}} = V_{OUT}/2$, is presented in Fig. B.4. It is assumed the same referent, *steady-state*, waveform without perturbation (red line in Fig. B.4) for both operating modes. Then, the same perturbation is applied and the behaviour of both operating modes is observed. The constant frequency transient is depicted in green color, while the variable frequency transient is shown in orange. Two ranges of operation are discussed, the inductor current rise time is lower than the fall time ($T_{ON} < T_{OFF}$) and the rise time is higher than the fall time ($T_{ON} > T_{OFF}$). One can notice that for $T_{ON} < T_{OFF}$, initial current perturbation causes the instability in case of constant frequency operation, while for $T_{ON} > T_{OFF}$ the perturbation decreases with each following switching cycle. This perfectly matches with the conclusion drawn in [205]. On the other side, the variable frequency operation in both operating modes converges in the following half of the switching cycle to the initial *steady-state* waveform, with a certain delay compared to the referent waveform. This means that there is no static instability, under the same assumption of a perfectly balanced FC voltage, $V_{C_{fly}} = V_{OUT}/2$, in case of the variable switching frequency operation. This eliminates the need of employing the

artificial ramp in order to solve the mentioned issue that exists in the constant frequency operation.

It is important to notice that the analysis conducted in this section is valid for both, buck and boost operating modes. Analysis in the buck operating modes coincides with the one from [205], just explained in a different way.

B.3 Static Instability of the Flying Capacitor Voltage

By the analysis of the Fig. B.2(a) and B.3(a), one can conclude that in case of equal magnetizing times in both halves of the period, $T_{ON1} = T_{ON2}$, equal "positive" dead-times, $t_{dp1} = t_{dp2}$, and equal "negative" dead-times, $t_{dn1} = t_{dn2}$, FC voltage will always converge to the ideally balanced value, $V_{C_{fly}} = V_{OUT}/2$ [red waveforms in Fig. B.2(a) and B.3(a)]. Additionally, in case of a slight perturbation of the FC voltage, $\hat{V}_{C_{fly}}$, after the each following switching cycle, charge through the C_{fly} , $\Delta q_{C_{fly}}$, will always be of the opposite sign to the $\hat{V}_{C_{fly}}$ [green waveforms in Fig. B.2(a) and B.3(a)]. These conclusions are valid for both operating ranges, $V_{IN} < V_{OUT}/2$ and $V_{IN} > V_{OUT}/2$, under loads higher than zero. Detailed and comprehensive mathematical model that describes the previous analysis is discussed in the continuation of the section.

The work presented in [205] shows that under constant frequency operation, after removing subharmonic oscillations in V-CMC, flying capacitor voltage is always perfectly balanced to the half of the output voltage. The same starting point is selected for the analysis conducted in this article. It is assumed that the flying capacitor voltage has a certain perturbation over the ideal value at the beginning of the switching cycle:

$$V_{C_{fly}} = \frac{V_{OUT}}{2} + \hat{V}_{C_{fly}} \quad (B.1)$$

Due to the simplicity reasons, no dead times are included in the theoretical analysis. Only inductor magnetizing and demagnetizing switching states are taken into account. As will be shown later, this is enough for the conclusions drawn in this work.

Under the assumed flying capacitor voltage and taking V_{IN} , V_{OUT} and I_{IN} as input variables, integral of the inductor current on the switching period is calculated:

$$I_L = \frac{1}{T_{SW}} \int_0^{T_{SW}} i_L(t) dt \quad (B.2)$$

and also the flying capacitor charge on the switching period:

$$\Delta q_{C_{fly}} = \int_0^{T_{SW}} i_{C_{fly}}(t) dt \quad (B.3)$$

Value of the T_{ON} is obtained by solving the equation:

$$I_L = I_{IN} \tag{B.4}$$

Obtained solution for T_{ON} is substituted in (B.3). This is done for both previously discussed operating ranges, $V_{IN} < V_{OUT}/2$ and $V_{IN} > V_{OUT}/2$. Under the assumption of small perturbation $\hat{V}_{C_{fly}} \ll V_{OUT}$ and after linearization, the following expressions are obtained:

$$\Delta q_{C_{fly}} \approx \begin{cases} \frac{-16 \cdot L \cdot I_{IN} \cdot (I_{IN} - I_{zvs})}{(2V_{IN} - V_{OUT})^2} \cdot \hat{V}_{C_{fly}}, & \text{if } V_{IN} < V_{OUT}/2 \\ \frac{-16 \cdot L \cdot (I_{IN} - I_{zvs})^2}{(2V_{IN} - V_{OUT})^2} \cdot \hat{V}_{C_{fly}}, & \text{if } V_{IN} > V_{OUT}/2 \end{cases} \tag{B.5}$$

Only general steps for obtaining (B.5) are presented in the previous paragraphs. Mathematical expressions that are obtained in the mid-steps between analysis of the circuit and integration of the state-variables for different parts of the switching period, are too complex and not of interest to be presented here. However, it is important to mention that Symbolic Math Toolbox of MATLAB is used to define expressions and solve the discussed equations.

By the analysis of (B.5), it can be concluded that for $V_{IN} > V_{OUT}/2$, flying capacitor charge will always be of the opposite sign compared to the applied $\hat{V}_{C_{fly}}$ perturbation. This means, that in this operating range, flying capacitor voltage will always converge to the ideal value of $V_{OUT}/2$. On the other hand, for $V_{IN} < V_{OUT}/2$, $\Delta q_{C_{fly}}$ will be of the opposite sign of the $\hat{V}_{C_{fly}}$ perturbation only if the converter's consumption is higher than zero. In case that the converter operates under no-load conditions, flying capacitor charge will always be zero, no matters how big is the deviation of the $V_{C_{fly}}$ compared to the ideal value of $V_{OUT}/2$. Or in other words, under these operating conditions there is a possibility of static imbalance of the flying capacitor voltage. This behaviour will be confirmed in the section of the experimental results.

The same issue can be detected by the analysis of the waveforms in Fig. B.5 where both operating ranges are depicted, boosting factor is higher than 2 (upper figure) and lower than 2 (bottom figure), under no-load condition. The inductor current for the perfectly balanced flying capacitor voltage is marked in red.

For $V_{IN} > V_{OUT}/2$, charging/discharging of the flying capacitor happens during the rising slope of the inductor current. Rising slope depends on the value of the $V_{C_{fly}}$ and

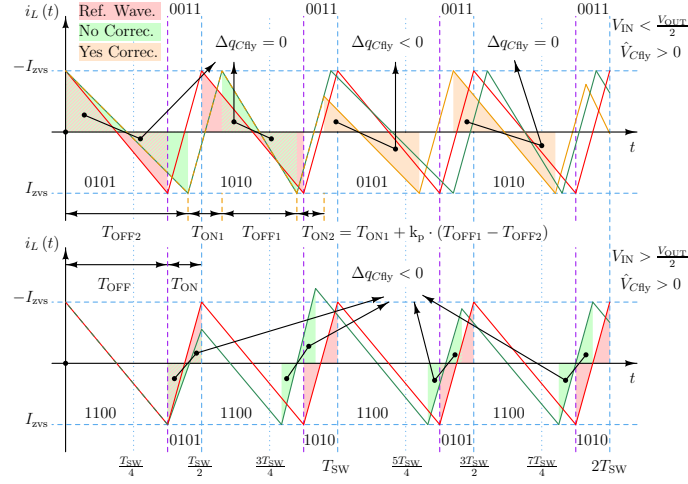


Fig. B.5: Static instability analysis of the flying capacitor voltage under no-load conditions. Switches arrangement for each part of the switching period and T_{ON} correction that stabilizes V_{Cfly} to the half of the output voltage are also depicted.

lasts always for the fixed time, T_{ON} . On the other side, falling slope of the inductor current is always the same, $(V_{IN} - V_{OUT})/L$, and this transition lasts until the current reaches a negative I_{ZVS} value. Under a positive \hat{V}_{Cfly} perturbation, first rising edge decreases (green waveform) and for the same T_{ON} time as in the case of the red one, inductor current reaches lower value than $-I_{ZVS}$. Since in this part of the period $i_{Cfly} = i_L$, the total Δq_{Cfly} is negative. This means that the flying capacitor voltage is already a bit decreased in the first rising time. In the following rising time of the inductor current, the slope is still higher than the ideal one, $(V_{IN} + V_{Cfly} + \hat{V}_{Cfly} - V_{OUT})/L$, and for the same rising time, inductor current will reach a bit higher value than $-I_{ZVS}$. Since, in this part of the switching period $i_{Cfly} = -i_L$, it means that the flying capacitor charge is negative again and the V_{Cfly} is even closer to the ideal value. This process will continue inherently until V_{Cfly} reaches $V_{OUT}/2$.

In case of $V_{IN} < V_{OUT}/2$, charging/discharging of the flying capacitor happens during the falling slope of the inductor current. Rising slope of the inductor current is always the same, V_{IN}/L , and this period always lasts for the time of T_{ON} . Under a positive \hat{V}_{Cfly} perturbation, first falling slope decreases from $(V_{IN} - V_{Cfly})/L$ down to $(V_{IN} - V_{Cfly} - \hat{V}_{Cfly})/L$. This increases the falling time of the inductor current (green waveform in the upper part of Fig. B.5). However, in both cases, red and green waveform, positive and negative area of the falling inductor current slope is always the same. This means that average flying capacitor charge is always zero, even during the falling slope only. The same conclusion can be drawn for the following half of the switching period where the inductor falling slope changes from $(V_{IN} + V_{Cfly} - V_{OUT})/L$ up to $(V_{IN} + V_{Cfly} + \hat{V}_{Cfly} - V_{OUT})/L$ due to the flying capacitor voltage perturbation.

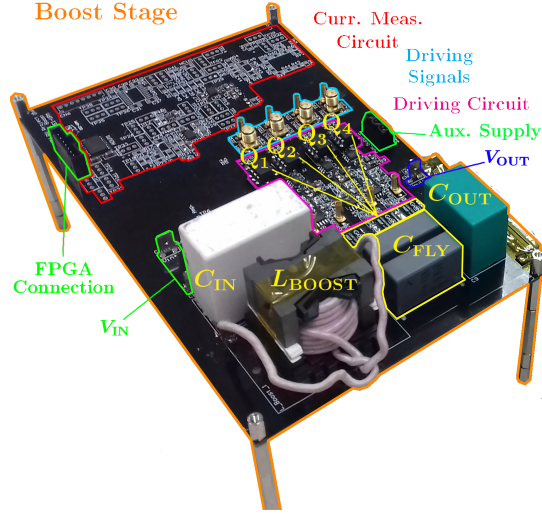


Fig. B.6: Photograph of the prototype. Labels in the prototype correspond to the ones in Fig. B.1.

This means that the average charge of the flying capacitor on the switching period will always be zero, no matter on the deviation of the V_{CFly} from the ideal value. And, once again, in this way, a flying capacitor voltage static instability will appear.

In order to resolve this issue, a very simple manipulation of the data that is already available in the FPGA control board is conducted. Instead of having the same T_{ON} times in both halves of the switching period, the inductor current magnetizing time in the second half of the period is calculated in the following manner:

$$T_{ON2} [k] = T_{ON1} [k] + k_p \cdot (T_{OFF1} [k - 1] - T_{OFF2} [k - 1]) \quad (B.6)$$

where k_p is a positive, real constant. This action is also described in the upper part of Fig. B.5 (orange waveform). One can notice that in the second rising slope of the inductor current, positive peak is decreased compared to the original waveform and in this way, during the following falling slope, a negative flying capacitor charge is obtained and V_{CFly} is closer to the ideal value. With this modification, FC voltage balance is achieved under all operating points. This will be experimentally confirmed in Section B.4.

B.4 Experimental Validation

In order to justify previously described theoretical analysis, experimental prototype is built and tested (see Fig. B.6). Output voltage of the prototype is controlled to $V_{OUT} = 75$ V. Input voltage is swepted from 10 % - 90 % of the output voltage value, while load is changed between 0 W and 25 W.

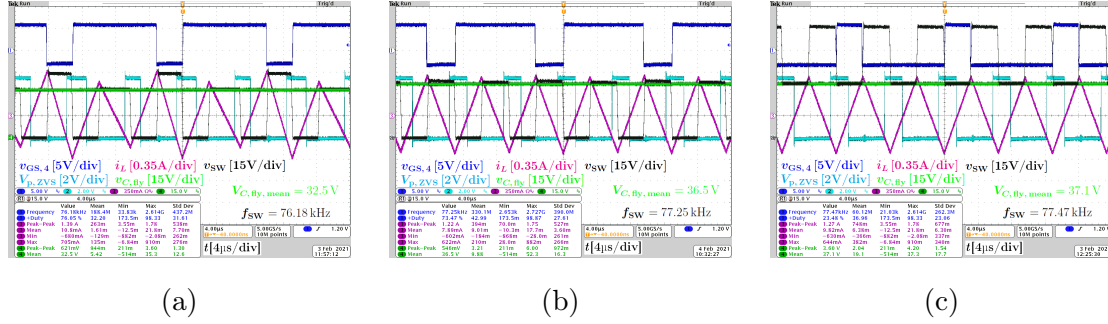


Fig. B.7: Measured waveforms under different input voltages, with and without included T_{ON} correction. (a) Example of the imbalance of the FC voltage under no load and $V_{IN} = V_{OUT}/4$. (b) Example of the FC voltage imbalance correction under no load and $V_{IN} = V_{OUT}/4$. (c) Example of the FC voltage balance without added compensation under no load and $V_{IN} = 3 \cdot V_{OUT}/4$.

Measured waveforms are provided for no load conditions and two input voltage points, $V_{IN}/V_{OUT} = 0.25$ [see Fig. B.7(a) and B.7(b)] and $V_{IN}/V_{OUT} = 0.75$ [see Fig. B.7(c)]. In case of $V_{IN}/V_{OUT} = 0.25$, FC voltage deviates from the ideal value and it is $V_{C_{fl,y}}/V_{OUT} = 0.43$ [see Fig. B.7(a)]. In order to solve this problem, modification that is described by (B.6) is employed and the results are presented in Fig. B.7(b). In this way FC voltage value is improved, $V_{C_{fl,y}}/V_{OUT} = 0.49$. On the other hand, in case of $V_{IN}/V_{OUT} = 0.75$, $V_{C_{fl,y}}$ voltage is well balanced even without included compensation, $V_{C_{fl,y}}/V_{OUT} = 0.495$ [see Fig. B.7(c)].

Beside the waveforms under no load conditions that are presented to illustrate the behaviour of the $V_{C_{fl,y}}$, values of the flying capacitor voltage in steady state under different input voltages are measured and presented in Fig. B.8. Results are provided for case without load and with a certain consumption at the output, in this case 25 W. It can be noticed that in case of $P_{OUT} = 25\text{W}$, flying capacitor voltage is well balanced and its behaviour is approximately constant under the full V_{IN} range (around 49% of V_{OUT}). This small deviation from the ideal value is the consequence of the circuit non-idealities [196]. However, in case of no consumption at the output, flying-capacitor voltage drops down to 43% of the output voltage value for $V_{IN} = V_{OUT}/4$. Previously discussed T_{ON} correction is applied to all the analyzed cases and results are also depicted in Fig. B.7. One can notice that under the all tested operating points, compensation action improves voltage balance of the flying capacitor.

All the previously presented measurements are conducted with balanced dead times adjusted in the FPGA board ($t_{dn1} = t_{dn2} = 15T_{CLK}$ and $t_{dp1} = t_{dp2} = 14T_{CLK}$, with $T_{CLK} = 10\text{ns}$) [142]. Of course, even with adjusted balanced dead times in the control board, there is a certain delay caused by non-idealities of the driving circuitry, noise, etc.

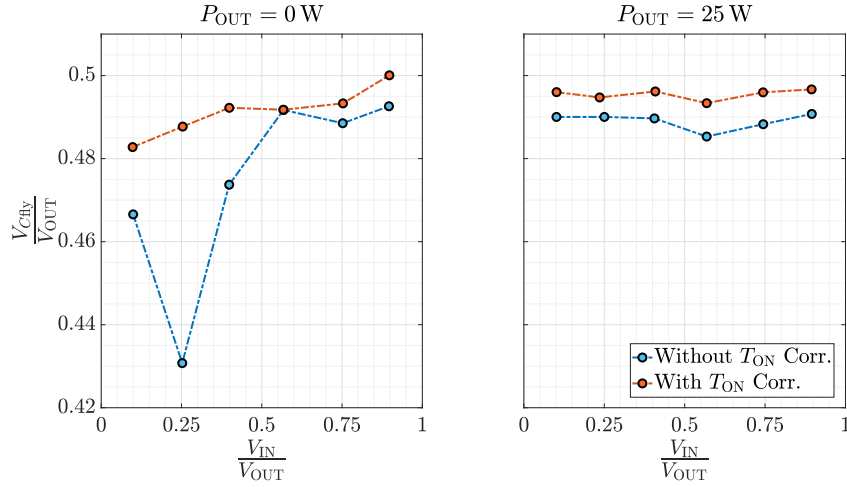


Fig. B.8: Measured flying capacitor voltage value in steady state under different input voltage and load conditions.

These delays are expected to be in the range of one T_{CLK} , but they are not measured here.

However, in order to determine the influence of the unbalanced "positive" dead times between each other and, also, "negative" dead times between each other, the set of measurements is conducted with the adjusted imbalance of the mentioned dead times directly in the FPGA board, apart from the already mentioned one that is caused by the circuit non-idealities. During the measurements and setting the dead times, it was concluded that there is no a significant difference with the measurements from Fig. B.8 for the imbalance in range of one T_{CLK} . So, a bigger step is made and the measurements are proceeded with the adjusted differences of $5T_{CLK}$ between the corresponding dead times. Results of these measurements are depicted in Fig. B.9. Once again, for loads higher than zero, the FC voltage is almost perfectly balanced for the whole input voltage operating range and for the all tested combinations of the dead time imbalance. The same can be concluded for no-load conditions and boosting factor lower than two. On the other side, for $V_{IN} < V_{OUT}/2$ and without output consumption, there is a deviation of the FC voltage from the ideally balanced value, $V_{OUT}/2$, just it is more expressed than in the case of Fig. B.8. This is expected, since the difference between the corresponding dead times is forced to be higher in this set of measurements and the flying capacitor is charged/discharged during these dead times (see schematics of the different transitions during the switching period in Fig. B.2 and B.3). It is interesting to notice that unbalancing the dead times in the opposite direction, also has an impact on the deviation of the FC voltage in the opposite direction, taking $V_{OUT}/2$ as a referent value. It is to say, when $t_{dn1} < t_{dn2}$ the V_{Cfly} is higher than the ideal value, while for the opposite case

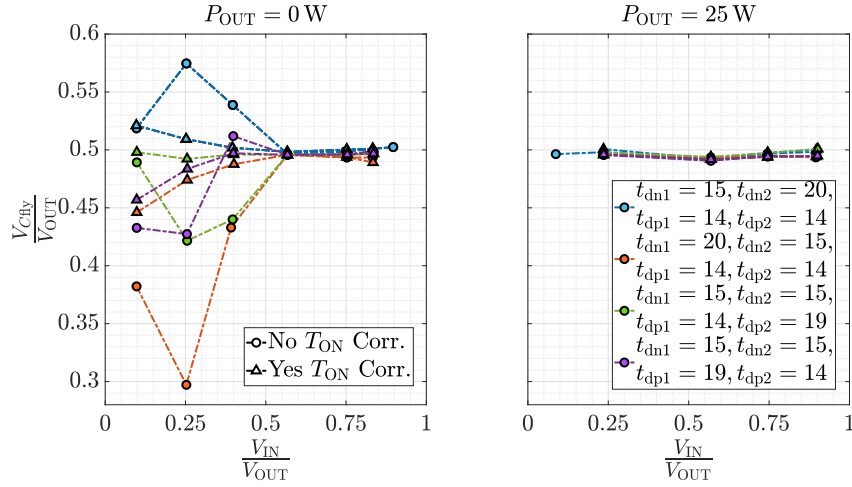


Fig. B.9: Measured flying capacitor voltage value in steady state with unbalanced "positive" and "negative" dead times under different input voltage and load conditions. Duration of the dead times is expressed in the number of the clock cycles of the FPGA board [142], $T_{CLK} = 10$ ns.

it is lower (see Fig. B.9). Nevertheless, the compensation action proposed in the previous section by (B.6) improves V_{Cfly} balance in all the investigated points.

B.5 Appendix Summary

Flying capacitor voltage balance of the three-level boost topology under variable switching frequency, V-CMC and TCM operating mode is investigated in this appendix. It is concluded that, opposite to the case of the constant switching frequency operation, the issue related to the subharmonic oscillations does not exist. This eliminates the need for compensation ramp.

Additionally, it is shown by the detailed mathematical model and graphical explanations that by controlling the negative value of the inductor current, necessary for obtaining ZVS transition in the switches, the flying capacitor voltage always converge to the ideal value of $V_{OUT}/2$, for the full input voltage range, as long as the load is higher than zero. Nevertheless, when the output consumption drops to the zero value, the mathematical model shows that in case for $V_{IN} > V_{OUT}/2$, the flying capacitor voltage will still converge to the ideal balanced value, while for boosting factor higher than 2, it is discovered that the charge balance of the flying capacitor is always zero, no matter on the deviation of V_{Cfly} from the ideal value. This behaviour leads to the static instability of the flying capacitor voltage for $V_{IN} < V_{OUT}/2$ and no-load conditions.

A very simple control modification is proposed to deal with the previously discussed issue. It assumes manipulation of the data already available in the FPGA control board

and recalculation of the T_{ON} time in the second half of the switching period in order to obtain flying capacitor charge of the opposite sign than the $\hat{V}_{C_{fly}}$ perturbation.

All the theoretical analysis presented in this appendix is confirmed by the detailed prototype measurements. The measurements also include the testing of the behaviour of the FC voltage under unbalanced corresponding dead times in the two halves of the switching period. It is concluded the same behaviour and the same stability regions as in the case of balanced dead times with the only difference that in the regions of the static instability of the FC voltage, it is more expressed if the dead times are unbalanced. The proposed control modification improves the balance of the flying capacitor voltage in all the measured operating points.

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Curriculum Vitae

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