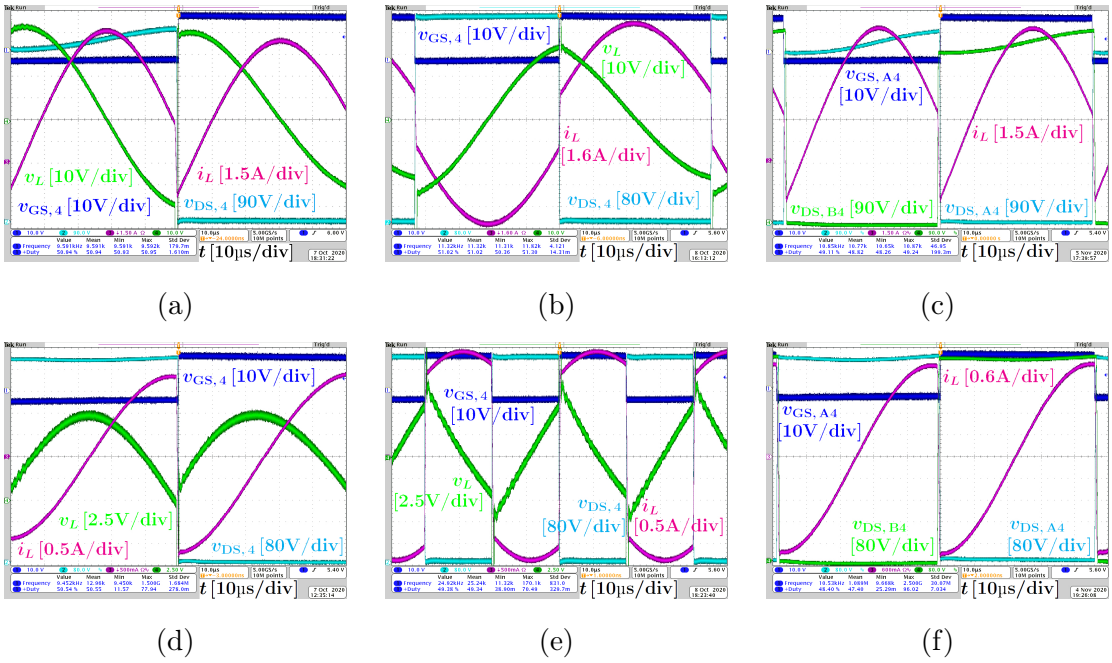


Fig. 3.18: Measured waveforms of all the previously analyzed variants of BRC topology under nominal and minimal operating load. Labels of the waveforms correspond to the ones in Fig. 3.17(a) and 3.17(b). DC side inductor at (a) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (d) $P_{\mathrm{OUT}} = 0\,\mathrm{kW}$. AC side inductor at (b) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (e) $P_{\mathrm{OUT}} = 1.7\,\mathrm{kW}$. DC side inductor interleaved at (c) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (f) $P_{\mathrm{OUT}} = 0\,\mathrm{kW}$.

1) Presented model assumes constant value of the resonant inductor, while the resonant inductor in the prototype is implemented by the use of the MPPT powder core which permeability is very sensitive to the premagnetization, 2) C_{OSS} capacitances are assumed to be constant and calculated by the approximation presented in Appendix A. Thus, the non-linear behaviour of the MOSFET capacitances is partially taken into account by the model, 3) Model proposed in Section 3.3.2 assumes $C_{\mathrm{DC,BUS}} >> C_{\mathrm{RES}}$. Still, dc bus capacitances have a finite value and influence in a certain level frequency of the resonant tank. However, presented model can be considered as appropriate to be included in the design and optimization of the converters with described inductor current shape.

3.6 Chapter Summary

In order to reconcile two contradictory demands, high power density and controllability of dc bus voltage, this chapter proposes a hybrid dc/dc topology that combines a highly efficient, non-controllable step-up RSCC with a controllable, but lower efficient boost topology. In the presented solution, all employed devices have to withstand half of the output voltage; therefore, new classes of 650-V and 900-V WBG devices present

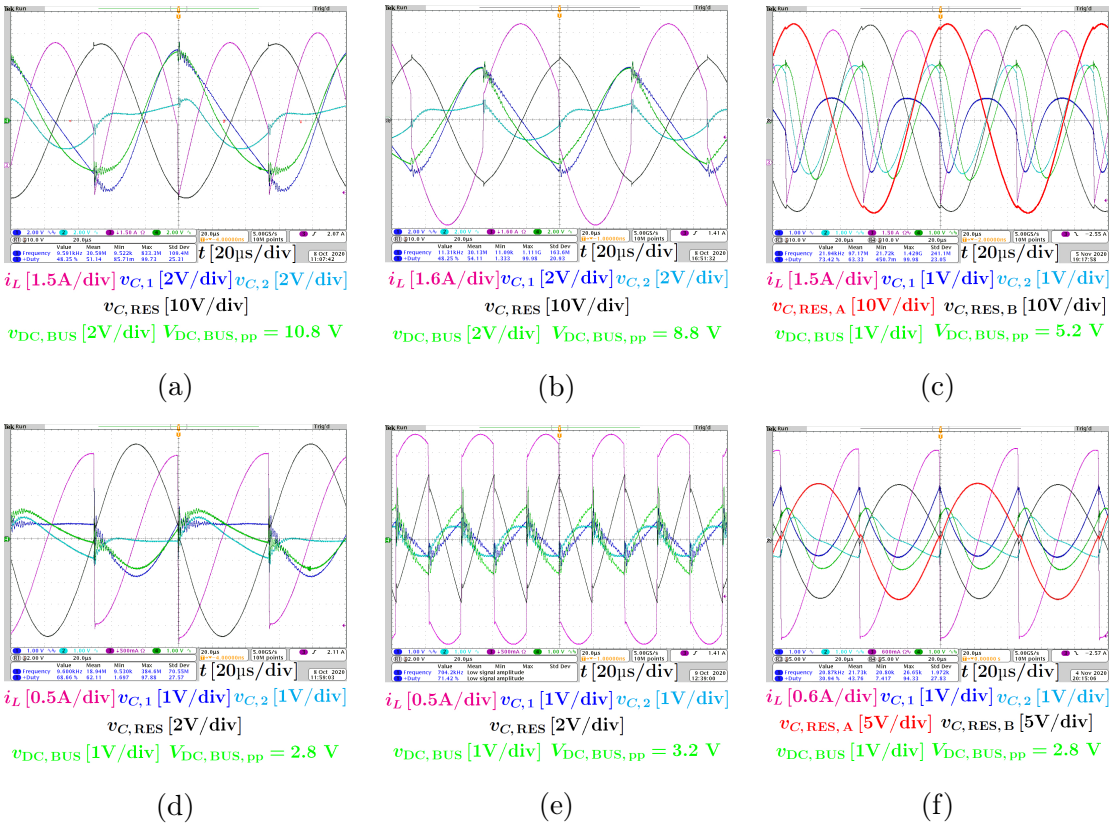
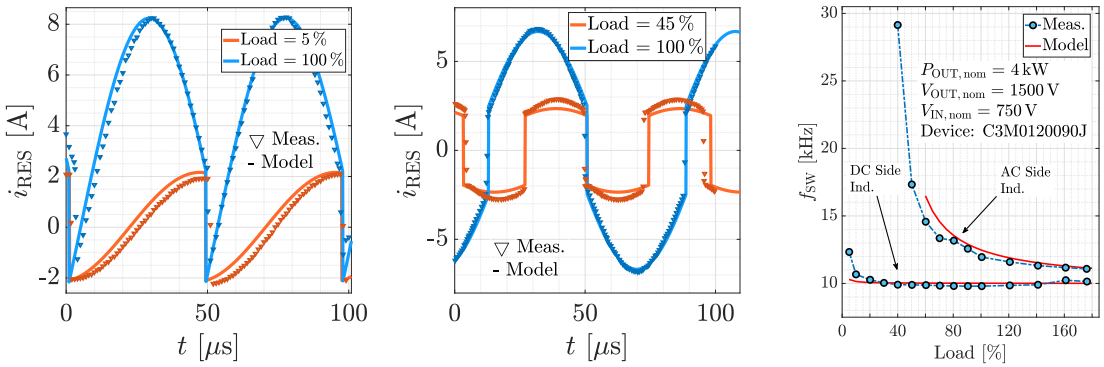


Fig. 3.19: Experimental verification of dc bus voltage ripple reduction by applying interleaving technique in the BRC stage. Waveforms are measured for nominal and minimal operating load, for all investigated BRC variants and nominal input and output voltages, $V_{\mathrm{IN}} = 750\,\mathrm{V}$ and $V_{\mathrm{OUT}} = 1500\,\mathrm{V}$. In order to better see the details of the ripple cancelation, voltage measurements are conducted in ac coupling mode. Inductor current measurements are given in dc coupling mode. Labels of the waveforms correspond to the ones in Fig. 3.17(a) and 3.17(b). DC side inductor at (a) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (d) $P_{\mathrm{OUT}} = 0\,\mathrm{kW}$. AC side inductor at (b) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (e) $P_{\mathrm{OUT}} = 1.7\,\mathrm{kW}$. DC side inductor interleaved at (c) $P_{\mathrm{OUT}} = 4\,\mathrm{kW}$ and (f) $P_{\mathrm{OUT}} = 0\,\mathrm{kW}$.

an excellent option, keeping in mind their superiority over 1200-V Si IGBTs. The benefits of the proposed topology are that it has full ZVS transitions in the complete operating range in terms of the load demand and input voltage and that it is a hybrid topology in which the energy is partially not processed through the resonant converter or the boost converter. The total energy is processed only in the case of extremely low input voltage when it is necessary to provide a constant gain of two, but even in this case, it is processed very efficiently through the presented resonant converter.

In case of boost part, two-phase and three-level boost are combined with two operating modes: 1) Constant switching frequency and 2) TCM operating mode under variable switching frequency. All the analyzed combinations are compared in terms of device's



(a) (b) (c)

Fig. 3.20: Experimental verification of the resonant current model presented in Section 3.3.2. (a) DC side inductor waveforms. (b) AC side inductor waveforms. (c) Comparison of the estimated and measured switching frequency for different loads.

blocking voltage, number and rating of the passive components, input current ripple, etc. In order to obtain full ZVS transitions, TCM is selected over constant frequency operation in the boost stage, despite the fact that constant frequency operation provides better input current ripple cancelation than the TCM mode. The reason for this is the fact that with constant frequency operation, ZVS would be possible only at the nominal operating point. It is experimentally proven that the loss of ZVS would cause failure of MOSFET due to high temperatures. Additionally, PV voltage fluctuation during the day is very frequent, so the loss of ZVS is unacceptable.

Three variations of the resonant stage of the proposed hybrid topology are discussed and compared: 1) Single-phase with the resonant inductor in series with input connection (DC side inductor), 2) Single-phase with the resonant inductor in series with resonant capacitor (AC side inductor) and 3) Two-phase with the single resonant inductor in series with input connection and two switching legs with its own resonant capacitors that are placed in parallel and that operate in the counter phase (DC side inductor interleaved).

Model of the resonant current that covers all the analyzed RSCC variations is explained. This model provides the possibility of the analysis of the resonant topology under different operating conditions and it is very usefull to be applied in some kind of the optimization algorythm that is based on *Euro Efficiency*, rather than the usual optimization in the nominal operating point. Additionally, this model is used here to analyze different parameters of the discussed RSCC variants and to compare them.

It is concluded that the AC side inductor scenario shows the best performances in terms of the RMS and peak values of the resonant current. This means that the highest efficiency and compactness is expected in this case (it will be discussed in more details in the following chapter). On the other side, due to the operating principle and necessity

to start ZVS transitions with a certain value of the inductor current, AC side inductor scenario shows impossibility of operation under low-load conditions due to the exponential increase of the switching frequency with the decrease of the output power. Interleaving technique in the DC side inductor scenario provides the possibility that, keeping the single resonant inductor and splitting resonant capacitor in the two parallel switching legs that operate in the conuter phase, dc bus capacitor volume can be halved reaching at the same time reduction of dc bus voltage ripple by the factor of two.

The previously described theoretical concept of the hybrid, multi-level, partial power processing dc/dc topology is fully experimentally confirmed by building and measuring a 10-kW prototype. All the analysis related to the BRC stage is confirmed by detailed and comprehensive measurements of two prototypes of 4 kW of nominal and 7 kW of maximal power. The details on the prototypes' designs and their optimization are described in the following chapter.

Chapter 4

Full Multivariable Optimization of the Proposed DC/DC Topology

After the analysis of the different variants, particular design aspects and selection of the control strategies for both stages of the proposed hybrid topology, the results of the multivariable optimization are presented in this chapter.

At the very beginning, a short review of 650-V and 900-V WBG devices currently available in the market is provided. These devices are analyzed and compared in terms of conduction and switching losses using the simplified model of C_{OSS} described in Appendix A.

The work presented in [58] is the first work to target 1500-V operation with 650-V class transistors. In order to have better comparison of the proposed dc/dc concept with the state of the art than the brief and general one from Section 3.4, the flying-capacitor multi-level (FCML) topology from [58] is considered for the optimization under the same operating conditions as the examined architecture. It is optimized considering different number of levels and appropriately rated WBG devices and the best solution is selected for the comparison with the full optimized hybrid topology from this thesis.

Optimization algorithm is discussed with all the design aspects, employed loss models, semiconductor devices and passive components. Explained procedure is applied to the all previously discussed variants of the stages of the hybrid topology from Chapter 3. Obtained pareto fronts are combined in the one for the whole hybrid topology. These results are compared to the full optimized FCML topology from [58]. FCML architecture is analyzed for different number of levels. Optimization algorithm includes new classes of 650-V and 900-V WBG devices that are available in the market. In this way, standard multi-level concept is compared with multi-level concept in combination with PPP, employing state of the art semiconductor devices, for use in emerging 1500-V grid-connected PV applications.

The analysis presented in Chapter 2 compares one-stage grid-connected architecture, with two two-stage concepts, already presented in literature and industry - "mini-boost"

and "string-optimizer", in 1000-V and 1500-V PV system for different ac grid voltage levels with respect to energy harvesting during one year period. The mini-boost concept that is presented in [33] and analyzed in Chapter 2 is extended here by including the multi-level topology from [58] and the hybrid topology presented in the previous chapter. Once again, these topologies provide the possibility of use of new classes of 900-V and 650-V wide band-gap (WBG) devices in 1500-V PV systems and are included in the comparison presented in this work with the clear focus on the benefits that could be obtained in terms of increased energy harvesting compared to the standard two-level topologies.

Due to the fact that efficiency over 99 % of the resonant stage of the hybrid topology is expected, it was necessary to find an appropriate losses measurements technique. Different methods for the measurements of the losses of the power converters are compared in [151, 152]. A simple multimeter measurements of the input and output power of the converter would not give a satisfactory results. Calorimetric measurement, [153–156], is time consuming and difficult to implement. The opposition or back-to-back method, [157–159], represents a good compromise between the precision and cost to be conducted. However, this method demands a voltage and current loop to be closed. The authors in [160] propose a back-to-back method in open loop operation. Unfortunately, this method is not applicable to the voltage-fed dc/dc converters. Another contribution of this thesis is the proposed losses measurements technique for the open-loop driven, voltage-fed dc/dc converters.

Previously described theoretical analysis is fully experimentally confirmed by building and measuring a 10-kW prototype of 8.26-kW/kg specific power and 404.6 cm^3 volume occupied only by the power stage components. *Euro efficiency* of 99.48 % in the nominal input/output voltage conditions is achieved. Additionally, all the loss models applied in the optimization algorithm and the energy harvesting calculation program presented in this chapter are confirmed by detailed measurements, thermal calibration and finite element (FEA) thermal simulations of the WBG devices and inductor designs employed in this work.

4.1 Overview of the Commercially Available WBG Devices

Before the discussion on the optimization algorithm and its results conducted in the following sections, it is necessary to make a brief overview of the WBG devices that are commercially available in the market and that could be included in the optimization process. It is already mentioned that in multi-level converters switches' blocking voltage is reduced by factor of $1/(N-1)$ with N number of levels. On the other hand, increasing number of levels leads to the increased number of switches in the inductor current path [58] that leads to the increased conduction losses in semiconductors. So, it is very important

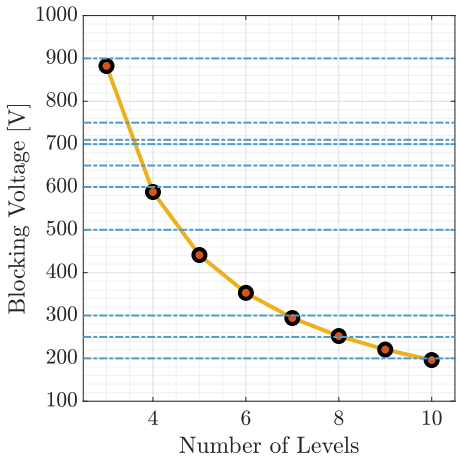
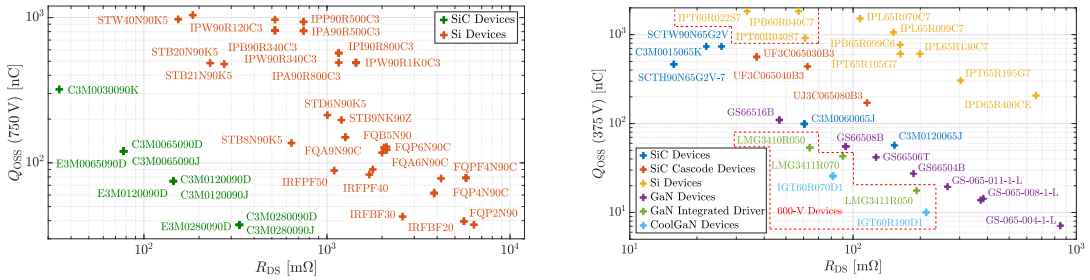


Fig. 4.1: Blocking voltage of the semiconductor devices in FCML topology [58] for different number of levels. It is assumed $V_{\mathrm{DC,\,BUS}} = 1500\,\mathrm{V}$ and 85 % derating is included in the graph. Voltage ratings of commercially available devices (GaN, GaN-on-Si, Si, SiC) between 200 V and 900 V are depicted in dashed blue lines. Data of the commercialy available devices is taken from [161].

that increased number of levels is followed by the appropriate decrease of voltage rating of the commercially available semiconductos.

The authors of [162] conclude that there are no commercially available WBG devices between 200 V and 600 V (GaN-on-Si HEMTs are not available between 200 V and 600 V, while SiC MOSFETs are not available below 650 V). Fig. 4.1 shows blocking voltage of semiconductor devices with increase of number of levels in FCML converter. The curve is obtained under the assumption of $V_{\mathrm{DC,\,BUS}} = 1500\,\mathrm{V}$ and 85 % derating included. Voltage ratings of commercially available devices (GaN, GaN-on-Si, Si, SiC) between 200 V and 900 V are depicted in dashed blue lines. Data of the commercialy available devices is taken from [161]. It is important to mention that for the devices between 200 V and 600 V only N-chanel, 1-chanel, enhancement mode Si devices suitable for the application in this work are considered: $I_{\mathrm{D}} \geqslant 10\,\mathrm{A}$ and $R_{\mathrm{DS}} \leqslant 40\,\mathrm{m\Omega}$. The latter constraint is taken in order to have a Si device with on-resistance less or equal than the overall WBG devices included in the comparison. In this way, a gap of voltage rating of WBG devices between 200 V and 600 V could be overrun and increase of the number of switches in series seen by the inductor current could be compensated by lower R_{DS} devices. One can notice that in the mentioned gap only 300-V and 500-V devices are available. The former ones demand 7 or more levels in FCML to be employed. However, the maximum number of levels considered in this work is 6, as a compromise between the complexity and possible benefits that could be gained. On the other hand, 500-V devices that are found in [161] do not show better conduction characteristics than the analyzed WBG devices and because of this they are not considered in the further comparison.



(a) (b)

Fig. 4.2: R_{DS} versus Q_{OSS} plots for WBG devices that are currently available in the market. Values of Q_{OSS} are calculated accroding to the model of C_{OSS} that is presented in Appendix A. Values of R_{DS} are calculated as the average value between minimal and maximal values of drain-source resistance that are provided by the manufacturers in data sheets of the devices. (a) 900-V devices. Q_{OSS} is calculated for $V_{DS} = 750\,V$. Data for devices from Wolfspeed/Cree (10), Infineon (18), ON Semiconductor (11), Vishay Intertechnology (6) and STMicroelectronics (12) is depicted. (b) 600-V and 650-V devices. Q_{OSS} is calculated for $V_{DS} = 375\,V$. Data for devices from GaN Systems (11), United SiC (4), STMicroenectronics(2), Infineon (12), Texas Instruments (4), Infineon CoolGaN (6), Wolfspeed/Cree (6) is depicted. 600-V devices are marked in dashed red line.

As will be shown in the following sections, the main limiting factor in the design process of the proposed hybrid dc/dc topology in applications with switching voltages of several hundreds of volts is the amount of energy that is necessary to obtain ZVS transitions in all the switches. This energy is influenced by the voltage that is switched and parasitic output capacitance (C_{OSS}) of the semiconductor devices. Relatively high values of the voltages result in a high value of the energy that is necessary for ZVS and thus a high value of the resonant inductor. Finally, this will lead to low switching frequencies. Additionally, conduction losses in the MOSFET devices represent a significant portion of loss breakdown. This phenomenon will be discussed later in detail.

According to the previous discussion, parameters of interest of the analyzed semiconductor devices are drain-source resistance of channel (R_{DS}), output capacitance (C_{OSS}) and parameters related to this capacitance - $Q_{OSS}\,(V_{DS})$ and $E_{OSS}\,(V_{DS})$. Due to the low switching frequencies, in this work, parameters such as input gate capacitance (C_{ISS}), total gate charge (Q_G), Miller capacitance (C_{RSS}), and figure of merit (FoM = $R_{DS}Q_G$), will not be discussed.

A review of the conduction versus switching characteristics of the commercially available semiconductor devices of interest for the application considered in this work is presented in Fig. 4.2. R_{DS} versus Q_{OSS} plot for 900-V devices from Wolfspeed/Cree (10), Infineon (18), ON Semiconductor (11), Vishay Intertechnology (6) and STMicroelectronics (12), that are currently available in the market, is presented in Fig. 4.2(a). Values of Q_{OSS}

Table 4.1: Review of the Characteristics of WBG Devices That Are Considered as the Most Suitable of the Devices Analyzed in Fig. 4.2 for the Application Considered in This Work.

Device	Manufacturer	Technology	R_{DS} [mΩ]	Q_{OSS} [nC]	V_{DS} [V]
C3M0065090J	Wolfspeed/Cree	SiC	77.5	120.2	900
C3M0120090J	Wolfspeed/Cree	SiC	145	74.8	900
C3M0060065J	Wolfspeed/Cree	SiC	60.5	99	650
GS66504B	GaN Systems	GaN	186.5	109.75	650
GS66508B	GaN Systems	GaN	92.75	55.37	650
GS66516B	GaN Systems	GaN	46.75	27.47	650

Values of Q_{OSS} are calculated for $V_{DS} = 750\,V$ in case of 900-V devices and for $V_{DS} = 375\,V$ in case of 600-V and 650-V devices by the approximation that is presented in Appendix A. Values of R_{DS} are calculated as the average value between minimal and maximal values of drain-source resistance that are provided by the manufacturers in data sheets of the devices [115–117]. 900-V devices are highlighted in gray.

are calculated for $V_{DS} = 750\,V$ by the approximation that is presented in Appendix A. Values of R_{DS} are calculated as the average value between minimal and maximal values of drain-source resistance that are provided by the manufacturers in data sheets of the devices. The same data for 600-V and 650-V devices from GaN Systems (11), United SiC (4), STMicroenectronics(2), Infineon (12), Texas Instruments (4), Infineon CoolGaN (6), Wolfspeed/Cree (6) is presented in Fig. 4.2(b). 600-V devices are marked in dashed red line. Q_{OSS} is calculated for $V_{DS} = 375\,V$ in case of 600-V and 650-V devices.

Expected advantage of low Q_{OSS} of SiC and GaN over Si technology can be observed. However, some Si devices show very low R_{DS} values compared to the WBG technologies. Devices that are considered to have low enough R_{DS} have significantly higher values of Q_{OSS} and E_{OSS} that would cause high values of energy that is necessary for obtaining ZVS transitions and because of this are excluded from the optimization process. Devices that are considered in the discussion of the following sections are listed in Table 4.1. More details on these devices can be found in [115–117]. 900-V devices are highlighted in gray.

4.2 Description of the Optimization Algorithm

As mentioned before, the FCML boost topology from [58] is fully optimized and compared with the hybrid topology proposed in this thesis. A general schematic of the FCML topology is depicted in Fig. 4.3(a). For sake of clarity, the schematics of the variants of the boost stage discussed in Section 3.2 are repeated here in Fig. 4.3(b) and 4.3(c). The FCML architecture from Fig. 4.3(a) is considered to operate in TCM mode, under variable switching frequency as discussed in Section 3.2 and Appendix B for the topologies from Fig. 4.3(b) and 4.3(c), respectively. A block diagram of the optimization process of the boost/FCML topology in the nominal operating point is presented in Fig. 4.4. It can be observed that the parameters that influence the shape of the inductor current are swept

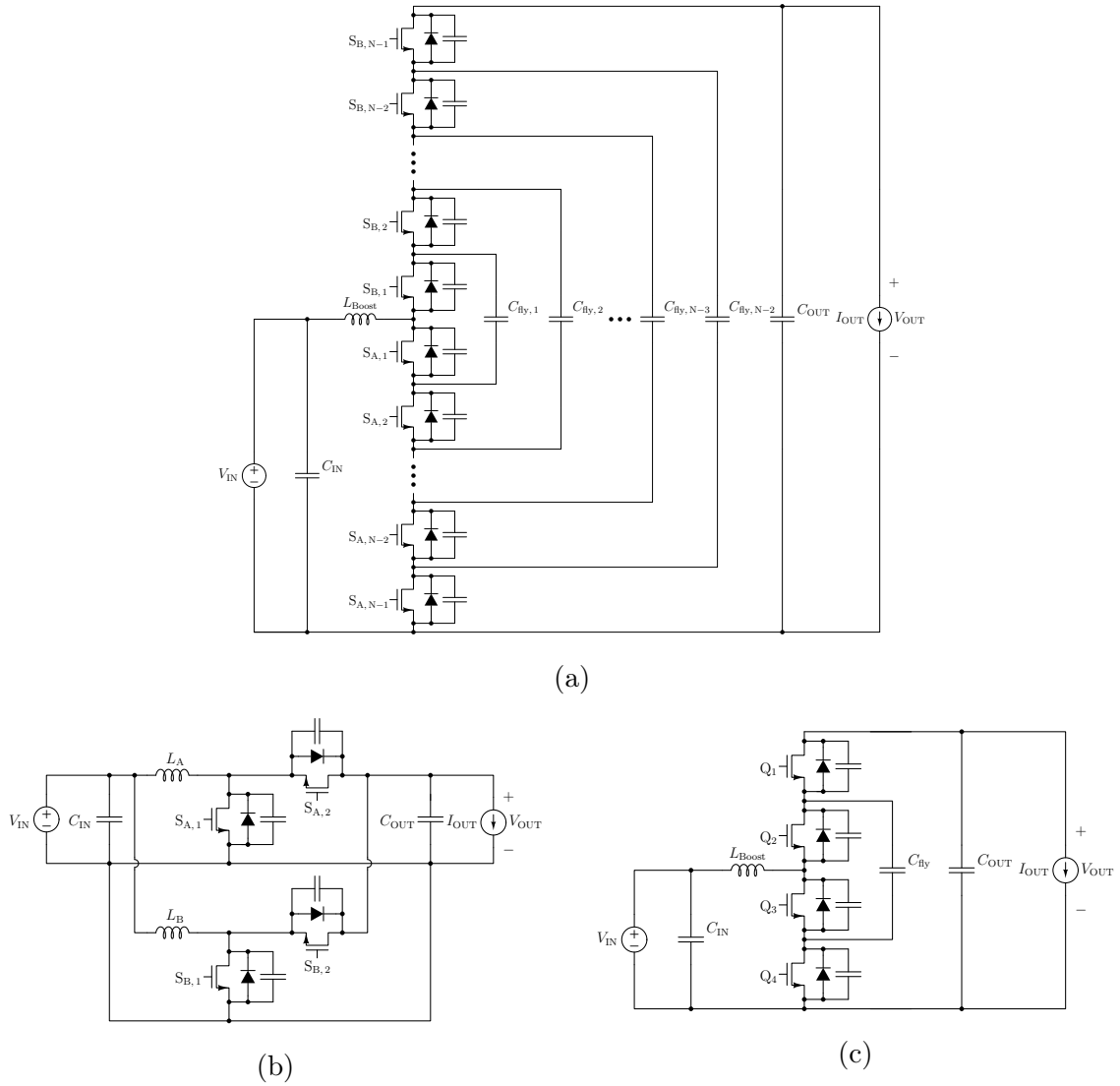


Fig. 4.3: Schematics of the optimized boost topologies. (a) Multi-level dc/dc FCML topology proposed in [58]. Analyzed variants of the boost stage of the hybrid architecture proposed in this thesis: (b) Two-phase boost. (c) Three-level boost.

first. Some of these parameters are GaN/SiC device and the number of devices in parallel. The reason for this is that the negative peak of the inductor current in TCM mode, necessary for obtaining ZVS transitions, influences RMS value as well as the peak value and frequency of the inductor current and thus the design of the rest of the components in the power stage. The optimization algorithm described here includes the following:

1. Appropriately voltage rated WBG devices [115–117],

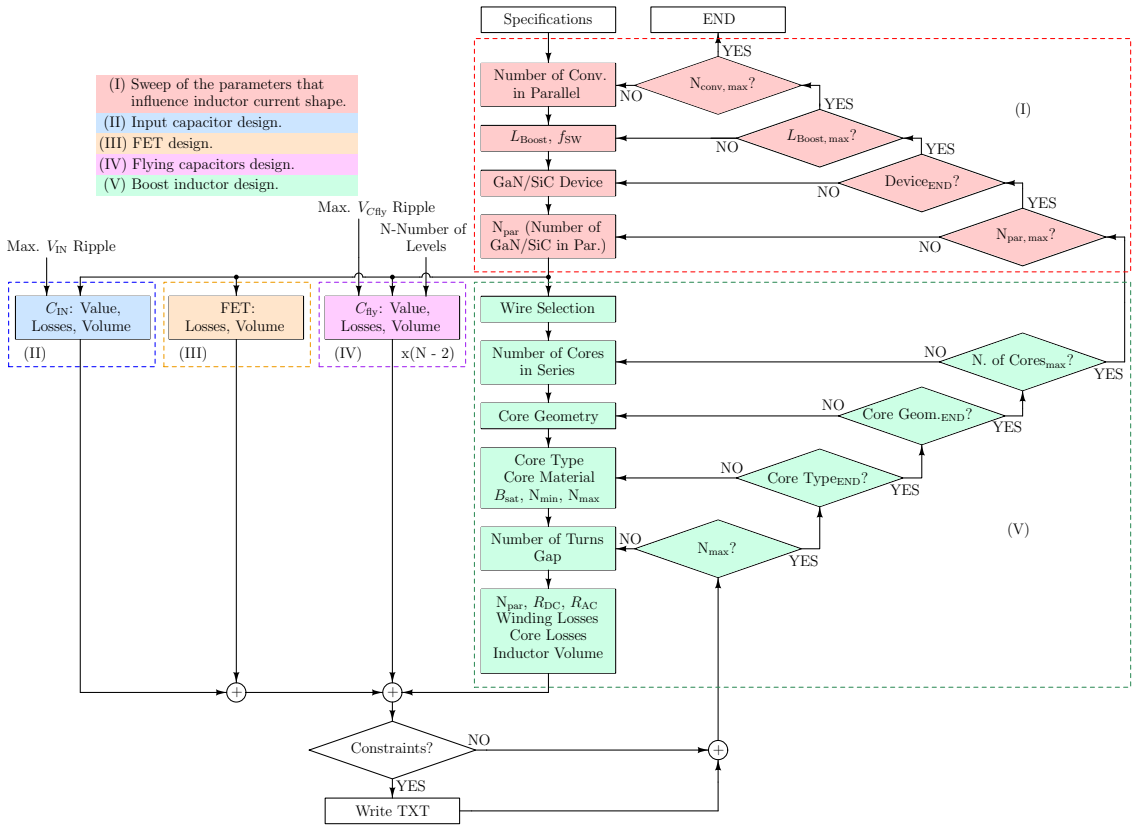


Fig. 4.4: Optimization diagram of the boost/FCML topologies from Fig. 4.3. Optimization is conducted for the nominal operating point (see Table 4.3).

2. Appropriately voltage rated MKP (polypropylene) film capacitors from KEMET [113]. This technology is selected for C_{RES} and dc bus capacitors according to the analysis presented in [146, 163],

3. 89 magnetic corres from Ferroxcube (29 of EE, 4 of EFD, 25 of ETD, 19 of POT, 6 of PQ and 6 of RM) [112],

4. 4 magnetic materials from Ferroxcube (3C90, 3C91, 3C95, 3C96) [112],

5. 31 wire diameters (AWG10-41).

Variations of the resonant stage of the proposed hybrid dc/dc topology are already described in Section 3.3. Once again, for sake of clarity, their schematics are repeated here in Fig. 4.5. As can be concluded from the analysis of the BRC stage conducted in Section 3.3 and ZVS conditions discussed in Appendix A, the number of MOSFETs in parallel per switch can significantly influence the shape and frequency of the current of the resonant inductor and thus the design of the rest of the circuit. Because of this phenomenon, the optimization process cannot be done separately for different parts of

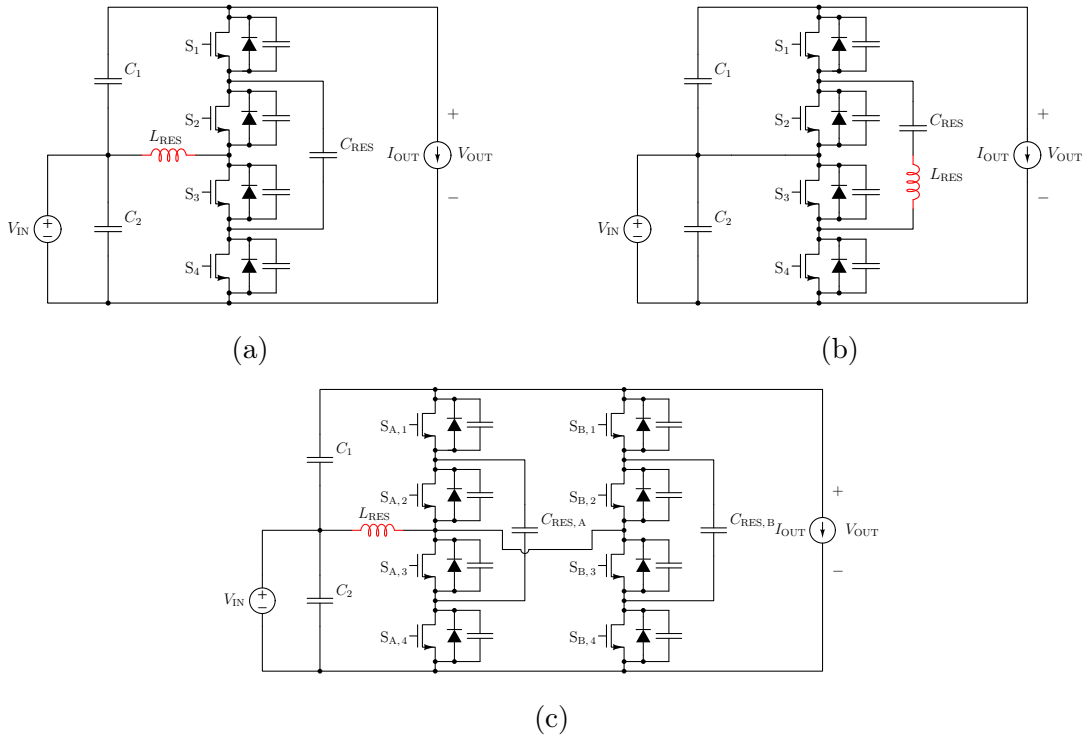


Fig. 4.5: Schematics of the optimized BRC topologies: (a) BRC with the resonant inductor in DC side, (b) BRC with the resonant inductor in AC side and (c) Two-phase interleaved BRC with a single resonant inductor in DC side.

the power stage of BRC, but instead needs to be interleaved. Fig. 4.6 shows the block diagram of the optimization of the BRC stage. Due to the high expected peak of the resonant current and operation with high magnetic flux density, beside the magnetic cores and magnetic materials included in the optimization of the boost stage, in the BRC optimization are additionally included:

1. 33 MPP powder cores from Magnetics [164],
2. MPP60u material from Magnetics [164].

Semiconductor losses are calculated by the model presented in [90]. Inductor core losses are calculated by improved general *Steinmetz* equation (iGSE) which is discussed in [93] and implemented in [94]. For winding losses calculations dc losses and skin effect are considered, [95, 97]. DC bus, flying and resonant capacitor losses are calculated by the two-elements series model that is presented in [98].

During the optimization algorithm some design constraints are introduced in order to discard the solutions that can not withstand the worst case conditions. Appropriately voltage rated WBG device is selected with 85 % derating included. Voltage ripple is included in the calculation of the device's blocking voltage (for example BRC stage with

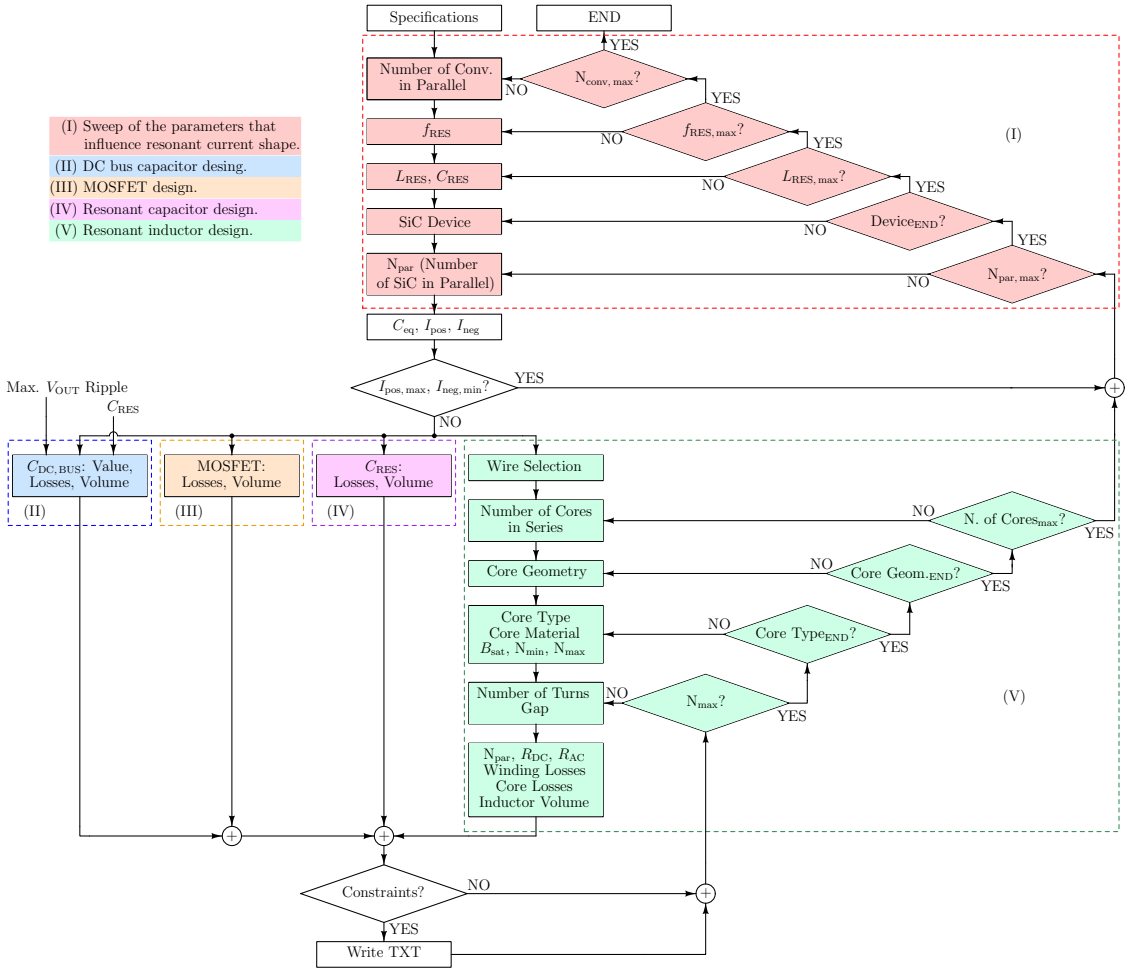


Fig. 4.6: Optimization diagram of the BRC topologies from Fig. 4.5. Optimization is conducted for the nominal operating point (see Table 4.3).

DC side inductor). Since no heat sinks are considered in this work and cooling through the printed circuit board (PCB) surface of the FET devices is assumed, the losses per semiconductor device were limited to a certain value in order to its case temperature does not exceed 120°C under the worst case conditions. The limit value of the losses per device is determined according to the data on the thermal resistance of the device package provided by the manufacturer in the data sheet.

Constraints included in the inductor design are the following: 1) Gap size is limited to the 10 % of the core height in order to limit the losses caused by the proximity effect. 2) Minimal number of turns is selected in order to limit the maximum operating flux density under the worst case conditions to the 75 % of the saturation value provided by the manufacturer. The value for B_{sat} is taken for the maximal operating temperature given in the data sheet. 3) Up to five stacked cores or cores in series are assumed in the inductor design. 4) The wire diameter is selected in order to avoid or reduce the losses

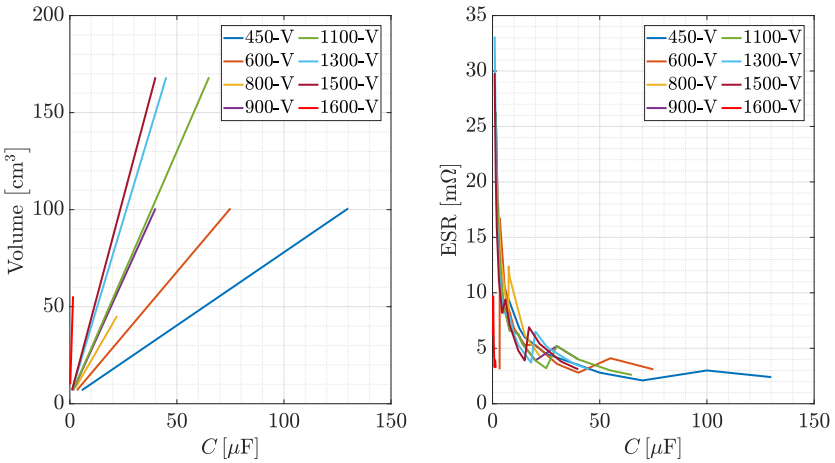


Fig. 4.7: Data sheet parameters of the MKP (polypropylene) film capacitors for different voltage ratings considered in the optimization algorithm discussed in this work [113].

caused by the skin effect. 5) Inductor designs that exceed the temperature of 110°C under the worst case operation are discarded. Diameter of the wire is selected to be lower than the skin depth for copper:

$$d \leqslant \frac{1}{\sqrt{\pi \cdot f_{\text{ind}} \cdot \mu_0 \cdot \sigma}} \tag{4.1}$$

where f_{ind} is the frequency of the inductor current (in some of the analyzed cases it differs from the switching frequency), $\mu_0 = 4\pi \cdot 10^{-7}\,\text{H/m}$ is the magnetic permeability of free space and $\sigma = 58.7\,\text{S/m}$ is the conductivity of the copper. Inductor temperature is calculated according to [83]:

$$T_{L,\,\text{max}} = R_{\text{th}} \cdot (P_{\text{winding}} + P_{\text{core}}) + T_{\text{amb}} \tag{4.2}$$

with assumed ambient temperature of $T_{\text{amb}} = 40\,^{\circ}\text{C}$ and thermal resistance:

$$R_{\text{th}} = \left(53 \cdot \left(V_{\text{eff}}\ \left[\text{cm}^3\right]\right)^{-0.54}\right) \frac{\text{K}}{\text{W}} \tag{4.3}$$

where V_{eff} is effective core volume.

Voltage rating of the employed film capacitors is calculated with the ripple and 90 % derating included. Data sheet parameters of the MKP (polypropylene) film capacitors for different voltage ratings considered in the optimization algorithm discussed in this work are depicted in Fig. 4.7.

4.3 Discussion on the Optimization Results

Results of the full multivariable optimization algorithm explained in the previous section and applied on the topologies discussed in Chapter 3 and [58] are analyzed here.

4.3.1 FCML as a Full Power Processing DC/DC Stage

Results of the full, multivariable optimization of dc/dc stage from Fig. 4.3(a) are presented in Fig. 4.8. Optimization algorithm is conducted for different number of levels, from 3 to 6. Also, it is important to mention that new classes of WBG devices are included in the comparison: two 900-V SiC devices from Wolfspeed/Cree [117], a 650-V SiC device from Wolfspeed/Cree [116] and three 650-V GaN devices from GaN Systems [115]. Together with pareto fronts, loss breakdown of the pareto solutions is also presented. Pareto solutions are arranged from the most compact to the most efficient. Optimization is conducted for the nominal operating conditions (see Table 4.3).

For the three-level FCML it was necessary to employ 900-V devices, while for higher number of levels 650-V voltage rating was sufficient. By the analysis of the loss breakdown from Fig. 4.8 it can be seen that MOSFET conduction losses are dominant in all the cases. This is due to the fact that full ZVS transitions are considered in all the switches. According to this, for all the analyzed number of levels, the device with the lowest R_{DS} shows the best pareto fronts. It is important to emphasize that the values for R_{DS} that are included in the optimization algorithm are calculated as an average value of the minimal and maximal one given by the manufacturers' data sheets and that include variation of the junction temperature and other effects.

Analyzing the loss breakdown for the number of levels where 650-V devices are compared, it can be noticed that SiC technology shows better compromise between conduction and switching losses. It is to say, compared to the best analyzed GaN device from the point of view of R_{DS}, GS66516B, 650-V SiC device, C3M0060065J, shows similar conduction, but much lower switching losses. This is the reason why for every analyzed number of levels higher than three, 650-V SiC device shows better pareto front solutions than its GaN counterparts. Additionally, SiC devices are much easier for practical implementation than the GaNs in the application range considered in this work. It is to say, SiC devices have plenty of commercially available driving circuits, for example [165, 166], that are very robust and show good performances, while for GaN devices it is necessary to design a custom driver. Also, the commercial drivers are much easier and less time consuming to be placed on PCB than the custom ones. On the other hand, the difference in price between commercial driver and sum of the components' cost necessary to build a custom one is negligible. Footprints of the SiC devices are more

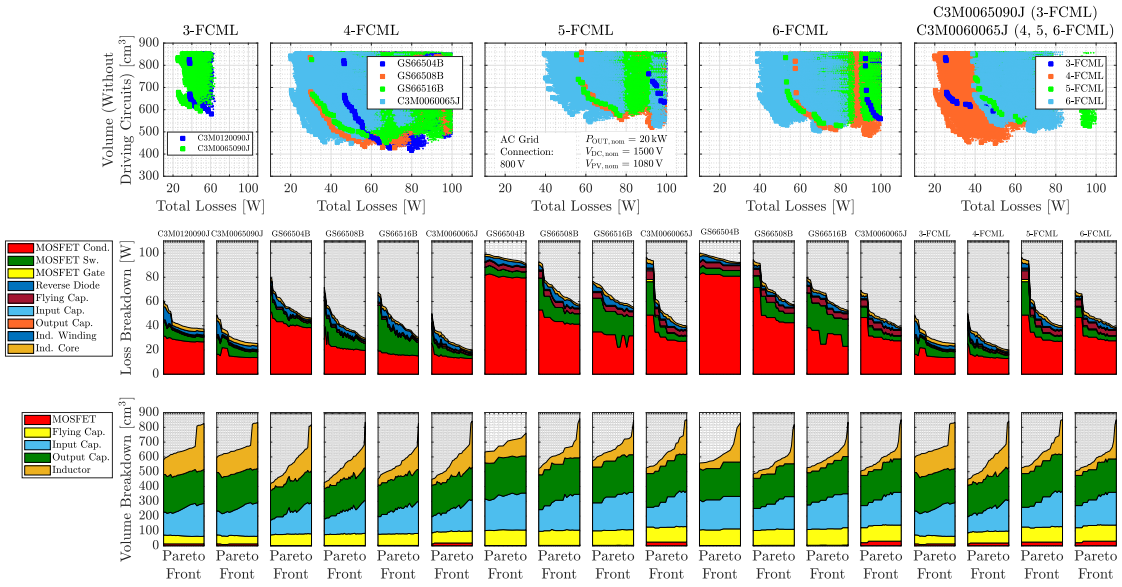


Fig. 4.8: Results of the full, multivariable optimization for the full power processing FCML topology [see Fig. 4.3(a)]. Different number of levels and appropriately voltage rated WBG devices are included in the comparison. Loss and volume breakdown for the pareto front solutions are also depicted. Pareto solutions are arranged from the most compact to the most efficient. Optimization results are provided for nominal operating point (see Table 4.3). The presented results assume that the total input power of 20 kW is processed by two 10-kW converters placed in parallel.

suitable for soldering and placing on PCB. Finally, SiC devices are much more robust than the GaNs in sense of the failures due to the ringing, hard switching conditions, etc.

Dominant conduction losses lead to the very important blocking voltage scaling of the employed devices that is already discussed in Section 4.1. It is to say, the change from 3-FCML to 4-FCML where device rating is changed from 900 V down to 650 V shows improvement in the optimization results (see Fig. 4.8), while for the higher number of levels, 5 and 6, pareto fronts are worse than the one for 4-FCML. The reason for this is already mentioned increase in the number of switches in the inductor current path with increase of number of levels and increase in the dominant conduction losses. On the other side, there is a gap in the voltage rating of the commercially available WBG devices between 200 V and 650 V [162].

From the point of view of volume, the most space is occupied by input and output capacitors. The volume occupied by the passive components decreases passing from 3-FCML to 4-FCML, while for higher number of levels it almost doesn't improve. The reason for this are, once again, dominant conduction losses in combination with gap in the voltage rating of the WBG devices between 200 V and 650 V. This leads to the increase of the conduction losses with increased number of levels. Since in the optimization algorithm the loss per WBG device is limited due to the thermal issues, increased conduction losses

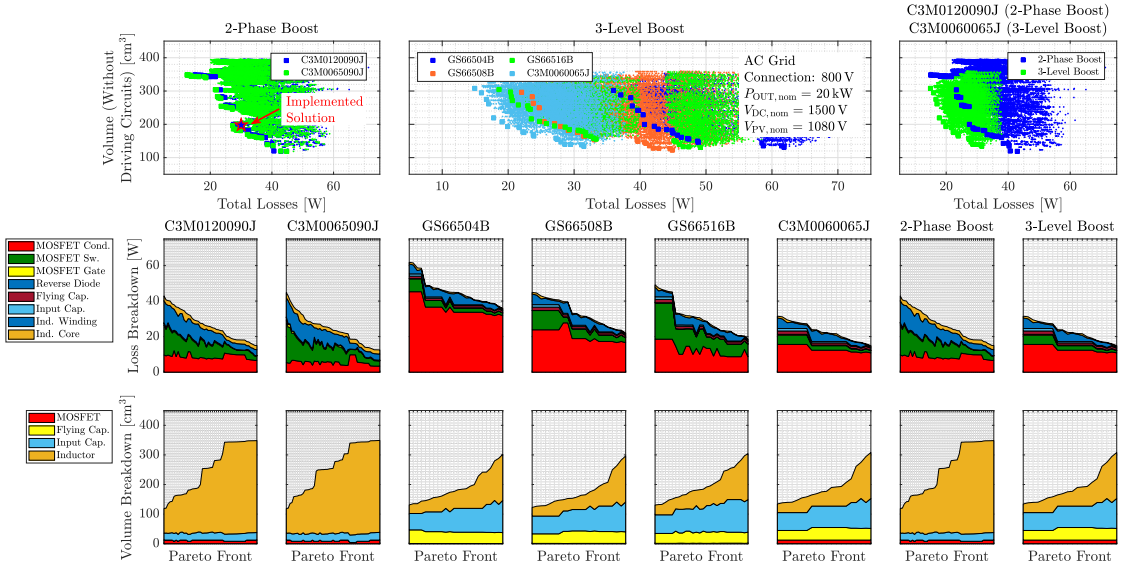


Fig. 4.9: Results of the full, multivariable optimization for the boost stage of the hybrid, multi-level topology presented in Chapter 3. Two-phase boost is compared with three-level boost topology with appropriately voltage rated WBG devices included in the comparison. Loss and volume breakdown for the pareto front solutions are also depicted. Pareto solutions are arranged from the most compact to the most efficient. Optimization results are provided for nominal operating point, see Table 4.3. The presented results assume that the total input power of 20 kW is processed by two 10-kW converters placed in parallel.

leave smaller space for increase of the switching frequency that could contribute to the smaller passive components.

4.3.2 FCML as a Controllable Stage of the Hybrid, Multi-Level Topology

Two possible variants for the controllable boost stage of the hybrid topology from Chapter 3 are considered here: 1) Two-phase interleaved boost employing 900-V SiC devices from Wolfspeed/Cree and 2) Three-level boost that employs 650-V GaN and SiC devices already mentioned. Optimization is conducted in the same manner and for the same operating conditions as explained in Section 4.3.1. Optimization results are presented in Fig. 4.9.

One can notice that in two-phase boost conduction losses are in the range of switching losses, on contrary to the analysis from Section 4.3.1. The reason for this is that the current from PV array is splitted between the phases. Due to this, 120-mΩ and 65-mΩ SiC devices give very similar pareto solutions. From the point of view of volume, most of the volume is occupied by the inductors, because there are two-phases and two separate inductors. Additionally, voltage rating of the input capacitor is halved compared to the topology from Fig. 4.3(a) that is optimized in Section 4.3.1. Also, interleaving technique