

# DC-DC Transformer Multiphase Converter with Transformer Coupling for Two-Stage Architecture

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**Abstract**— This paper presents an analysis of a very high efficiency topology based on a multiphase converter where the coupling among the phases is done by means of transformers. Since energy is not stored in the transformers, it is transferred directly from the input to the output. This topology along with its control strategy, were previously reported in state of the art. Some advantages of the proposed concept are that, thanks to the minimum storage of energy, the transfer rate of the energy is decoupled from switching frequency and can be chosen in order to increase efficiency. The regulation capability of this topology is limited and the topology acts as a dc-dc transformer. In this paper, the proposed topology is analyzed in detail and design guidelines are presented in order to optimize the design of the converter. These guidelines are applied to a specific design in order to build an optimized prototype.

## I. INTRODUCTION

Voltage Regulator Modules are converters dedicated to supply large amounts of energy with very fast slew rates at very low voltages (1.1 V). These converters generally operate under very small duty cycle conditions because the available input voltage is usually 12 V. When running under these conditions the efficiency and overall performance of the converter is degraded. In state of the art, the use of a two-stage architecture [1,2] has been proposed as a way to solve this problem since it enables the use of a lower intermediate voltage. This principle is illustrated in Figure 1. In this way, the converter which is adjacent to the load (Point Of Load converter) is allowed to run under better duty cycle conditions and therefore achieve better efficiency so it can be operated at higher switching frequencies, as in [2] where the POL is operated in the MHz range. When the system is adequately configured, improvements regarding size and efficiency can be achieved [1]. One of the requirements for the adequate configuration of the system is to choose a first stage or pre-regulator with very high efficiency. In this kind of applications, dc-dc transformers become an interesting choice. A dc-dc transformer can be described as a converter whose output voltage is for every instant of time, proportional to the

input voltage; the proportion is given by the ‘transformation ratio’ of the dc-dc converter, which is usually operated under fixed duty cycle conditions; hence, if the input voltage varies, the dc-dc transformer will be unable to adjust the duty cycle in order to compensate for the input voltage variation. In a two-stage architecture, this fine regulation would be accomplished by the POL converter. Two voltage dividers (used as first-stage topologies) based on different technologies are found in the literature. These topologies operate as 2:1 dc-dc transformers. The application of a voltage divider based on switching capacitor technology can be found in [4], while a resonant voltage divider is reported in [3] as a pre-regulator candidate in a two-stage architecture.

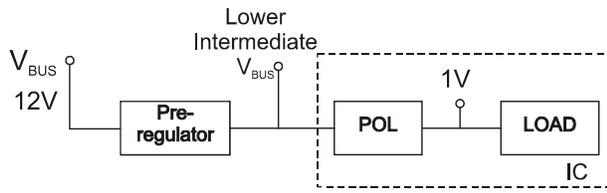
In this paper, a dc-dc transformer with different ‘transformation ratios’ and based on PWM technology is presented. The main characteristic of this multiphase converter is that the magnetic coupling among the phases is done by tight coupled transformers. Hence it is called multiphase converter with transformer coupling. Its operating principle, which was presented in [5] is reviewed in Section II along with a brief review of inductor-coupled multiphase converters. Design guidelines for this kind of converters are given in Section III; these design guidelines are based on a losses model which is also briefly explained. This methodology is applied and validated with two different prototypes. Section IV presents and compares these prototypes. Finally, conclusions are presented in Section V.

## II. PROPOSED CONCEPT AND STATE OF THE ART

The present work focuses on proposing a control strategy that can be applied to a coupled inductor converter. This topology is illustrated in Figure 2b. First of all, Figure 2a. illustrates the operating principle of a coupled inductor converter when  $d < 50\%$ . From this figure, it can be seen that the magnetic structure (represented by an ideal transformer) acts as an energy adder, adding the voltages  $v_A$  and  $v_B$ . The combined waveform resulting at the node  $v_C$  is a pulsating voltage that needs to be filtered by the output inductor

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**Figure 1.** Two-stage architecture enables a lower bus voltage which could allow Point Of Load converter (POL) to operate at higher frequency and reduce its size.

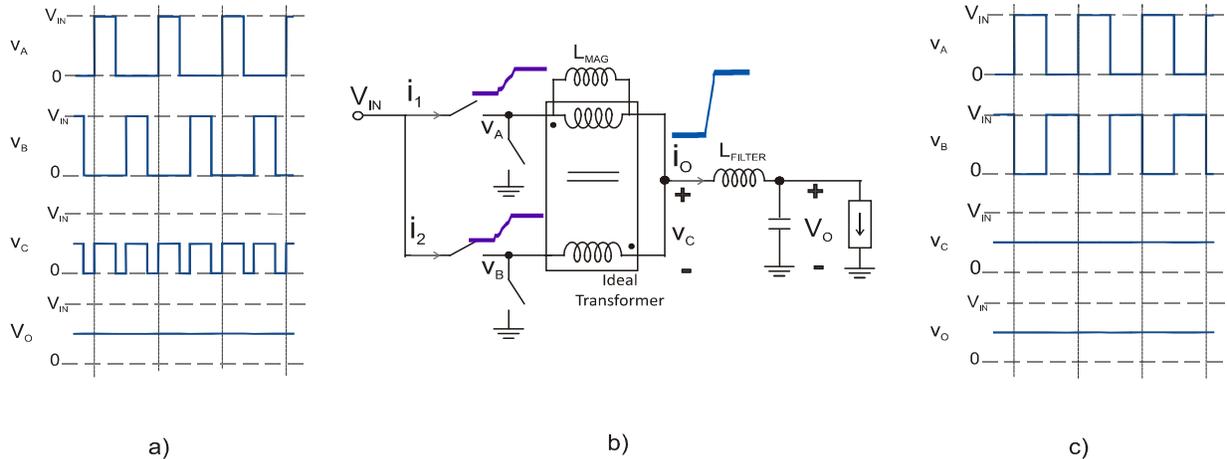
( $L_{\text{FILTER}}$ ) and capacitor. One of the main advantages of coupled-inductor converter is that the inductance seen by the converter during steady state is different from that seen under dynamic conditions [8]. It is desirable that inductance seen under steady state is greater, so smaller phase current ripple can be achieved. However, the values of  $L_{\text{FILTER}}$  and output capacitor should be adequately chosen, along with the operating frequency and magnetizing inductance in order to filter the pulsating voltage and the current ripple at  $v_C$  and also provide the required dynamic response and efficiency.

The main voltage waveforms of the proposed operating principle is illustrated in Figure 2.c; it is based on keeping the sum of the voltages  $v_A$  and  $v_B$  (inputs to the magnetic structure) constant for every instant of time, the voltage in the magnetic structure is given by:

$$v_A - v_C = v_C - v_B \quad (1)$$

if the sum of  $v_A$  and  $v_B$  is constant for every instant of time, the voltage at the node  $v_C$  will be also constant., and equal to:

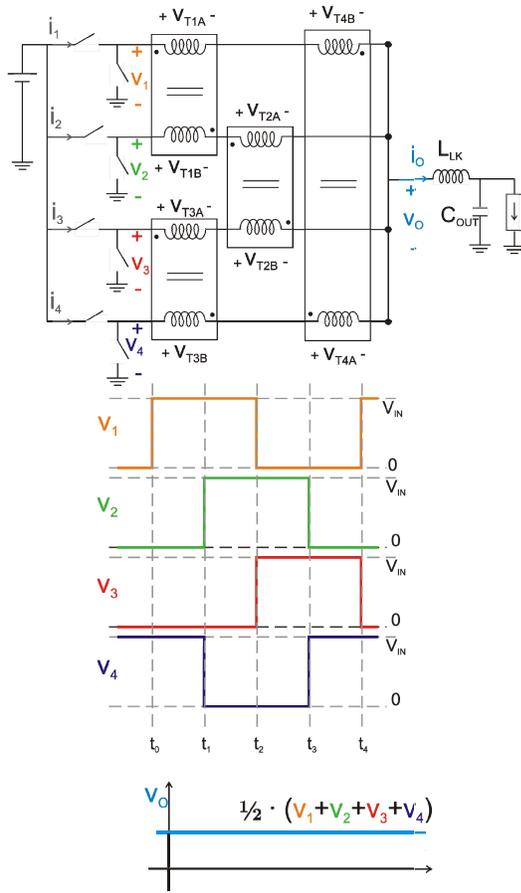
$$v_C = \frac{v_A + v_B}{2} \quad (2)$$



**Figure 2.** a) Operating waveforms for a coupled-inductor multiphase converter for  $d < 50\%$ . b) Magnetic structure in a coupled multiphase converter can be represented by an ideal transformer (plus  $L_{\text{MAG}}$  and leakage inductance); in an ideal transformer a change in the output current is seen immediately at the input of the transformer and distributed equally among the input phases. c) Proposed control strategy achieves that  $v_C = v_O$ ,  $v_C$  is constant for every instant of time. Since there is no pulsating voltage to filter at  $v_C$ ,  $L_{\text{FILTER}}$  is no longer necessary and can be minimized to its minimum ( $L_{\text{LK}}$  inherent to the construction of the transformer). Coupling between the phases is done by a tightly coupled transformer.

seen that  $v_C = v_O$  at any instant of time, hence the output inductance ( $L_{\text{FILTER}}$ ) can be reduced or theoretically eliminated from the converter, minimizing the energy storage in the converter. In this way, tightly coupled transformers can be used instead of coupled inductors. This implies that a converter working under the proposed concept can only operate at certain duty cycles; as in the example, the operating waveforms shown are those corresponding to  $d = 50\%$ . If the value of  $L_{\text{FILTER}}$  can be represented only by the leakage inductance inherent to the construction of a very tight coupled transformer, the energy will not be stored as it is in coupled inductors, but it will be transferred directly from the input to the output through the transformers that couple the phases. Designing a converter with a minimum value of  $L_{\text{FILTER}}$  can provide certain advantages regarding dynamic response and efficiency.

For instance, if  $L_{\text{FILTER}}$  is minimized, the predominant dynamic under a load step is that of the transformer. The response of the transformer to a load step is also illustrated in Figure 2.b. When a load step occurs at the common point of the transformer, it is immediately seen at the input, and equally distributed among the phases carrying  $i_1$  and  $i_2$ . A step in the load will be seen almost immediately at the input, since the element that opposes to the current change (filter inductance) has been reduced to its minimum. This can be done by using an adequate interleaving technique while placing the windings in the transformer. With the proposed control technique and the converter designed to operate with minimum storage of energy, the transfer of the energy under a load step is independent from the switching frequency, and  $f_{\text{SW}}$  can be chosen to minimize losses instead of the accomplishment of a specific dynamic response. It has been said before, that this converter has limited regulation capability and it behaves as a DC-DC transformer. However, if more phases are added to the magnetic structure, more duty cycles where the proposed control strategy is achieved become



**Figure 3.** Schematic of proposed topology and main operating waveforms. Coupling between phases is done by means of tightly coupled transformers

available; then it is possible to achieve different values of output voltage and the topology behaves as a DC-DC transformer with multiple conversion ratios.

When the concept is extended to multiple phases, the duty cycles where the control strategy is achieved are related to the number of phases and are given by:  $d = k/n$ , where  $n$  is the number of phases;  $k$  is an integer which represents the number of cells that are simultaneously transferring energy from the input and the range of its values is comprised from 0 to  $n - 1$ . For example, in a four-phase converter ( $n = 4$ ), three different levels of output voltage would be available, those corresponding to duty cycles of 25%, 50% and 75%, when  $k$  equals 1, 2 and 3 respectively. A schematic of a four-phase topology is illustrated in Figure 3, along with the operating waveforms that corresponds to  $d=50\%$ . It can be seen that the switching cycle has been divided into four periods ( $t_0$  to  $t_4$ ). For every instant of time, there are two phases which are simultaneously connected to  $V_{IN}$ .

At  $t_0-t_1$ , the value of the voltages  $v_1$  and  $v_4$  is equal to  $V_{IN}$ , while the other phases are connected to ground. At  $t_1-t_2$ ,  $v_1$  and  $v_2$  equal  $V_{IN}$ . In the same way, the other phases connect consecutively to  $V_{IN}$  for the other instants of time, as

can be seen in Figure 3. The voltages of the transformers can then be found by the following equations:

$$v_{T1A} = \frac{3}{4}v_1 + \frac{1}{4}v_3 + \frac{1}{2}v_4 - \frac{3}{2}v_O \quad (3)$$

$$v_{T2A} = -\frac{1}{4}v_1 - \frac{3}{4}v_3 - \frac{1}{2}v_4 + \frac{3}{2}v_O \quad (4)$$

$$v_{T3A} = -\frac{1}{4}v_1 + \frac{1}{4}v_3 + \frac{1}{2}v_4 + \frac{1}{2}v_O \quad (5)$$

$$v_{T4A} = -\frac{1}{4}v_1 + \frac{1}{4}v_3 - \frac{1}{2}v_4 + \frac{1}{2}v_O \quad (6)$$

and the output voltage equals:

$$v_O = \frac{v_1 + v_2 + v_3 + v_4}{4} \quad (7)$$

for every instant of time.

Based on the assumption of the constant input – constant output voltage, the proposed topology can be represented with the model shown in Figure 4, where the magnetic structure is represented by dependent current and voltage sources. The input and output impedance are represented in this model since they have a significant impact on the dynamic response. It is important to point out, that the  $L_{LEAKAGE}$  stands for the equivalent leakage inductance of the transformers.

There are many strategies to couple the phases using discrete transformers, the one shown in Figure 3 is used in order to build the prototype covered in section IV.

### III. DESIGN GUIDELINES AND LOSSES MODEL

In a converter operating with minimum storage of energy, the dynamic response is decoupled from the switching frequency, so the criteria for choosing  $f_{SW}$  is independent from the dynamic response. The values of  $L_{MAG}$  (magnetic core) and  $f_{SW}$  can be chosen in order to minimize the losses. However, size optimization should also be taken into account. For a fixed value of  $L_{MAG}$ , a  $f_{SW}$  value at which the losses are minimized exists; aiming to find this point, along with the optimum MOSFETs, a design methodology was developed. This methodology helps to find the appropriate losses and size. The process starts with some given specifications ( $V_{IN}$ ,  $V_{OUT}$ ,  $I_{OUT}$ , current ripple, etc.) and the objective is to find the optimum combination of size and losses by evaluating different combinations of transformer configurations (turns, core size and material), MOSFETs and switching frequencies. The proposed methodology is based on a losses model that was verified using a preliminary prototype.

This losses model was implemented taking into account conduction losses, switching losses (6) and circulating energy losses. The validation of this model is shown in Figure 6, where measurements for different loads at a frequency of 100 kHz are compared with the theoretical calculation of the losses; It is desirable that this model works in a wide range of frequencies and loads.

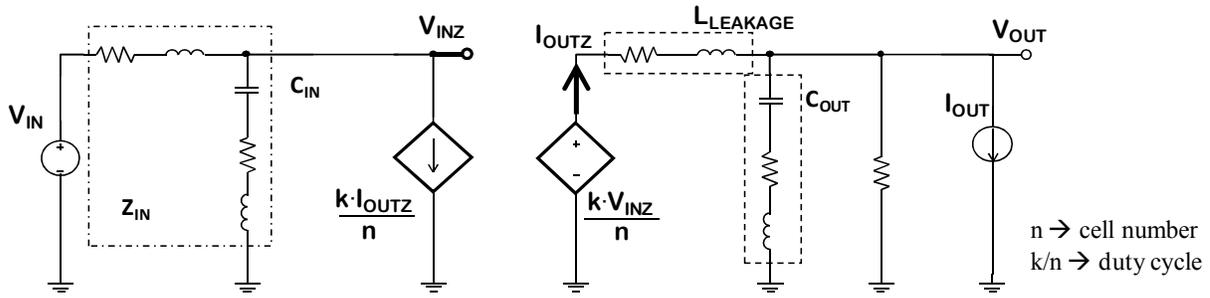


Figure 4. Model of the proposed topology. The magnetic structure is modeled as a current and voltage dependent sources.

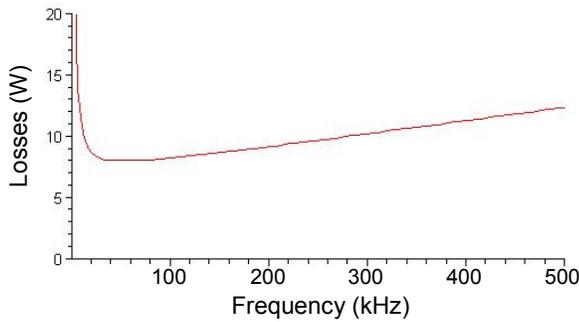


Figure 5. Losses for maximum load ( $I_{OUT}=30A$ ) over a wide range of frequencies.

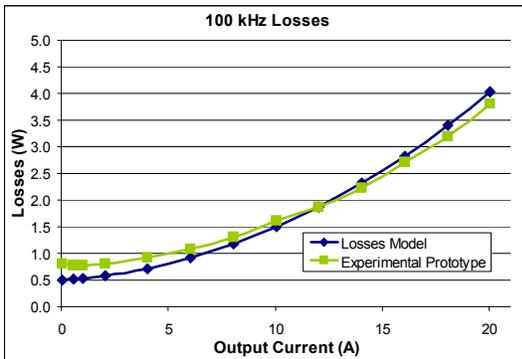


Figure 6. Losses measurements and model prediction for different loads at 100kHz frequency

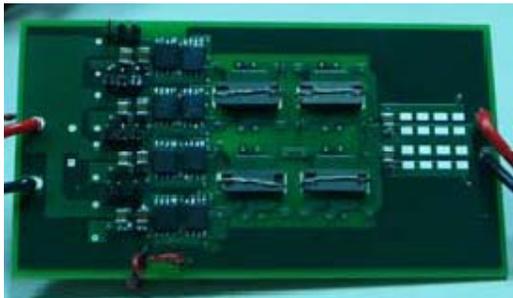


Figure 7. Picture of the implemented prototype. The magnetic structure is comprised of four pairs of E/14/3.5/5 cores

The losses taken into account are the following:

1) Conduction losses. These power losses include losses due to average current and circulating energy losses. Conduction losses account for losses in the  $R_{DSon}$  of MOSFETs, in the DC windings of the transformer and an estimation of the parasitic resistance of the PCB:

$$PR_{Dson} = n \cdot (RonHI) \cdot d \cdot \int_0^f i_n^2 dt + n \cdot (RonRS) \cdot (1-d) \cdot \int_0^f i_n^2 dt$$

$$PR_{PCB} = (R_{PCB}) \cdot I_{out}^2$$

$$PR_{DC\_TRANSFORMER} = n \cdot RDC \cdot \left( \frac{I_{out}}{n} \right)^2$$

2) Switching losses. These losses are calculated by implementing the model proposed in [6] where, given a MOSFET model which includes the parasitic inductance of the PCB, apart from the parasite capacitances ( $C_{ISS}$ ,  $C_{OSS}$ ,  $C_{RSS}$ ); in this paper, expressions for the  $V_{DS}$  and  $I_{DS}$  of the

MOSFET are derived, making it possible to calculate the losses due to ON and OFF MOSFET transitions.

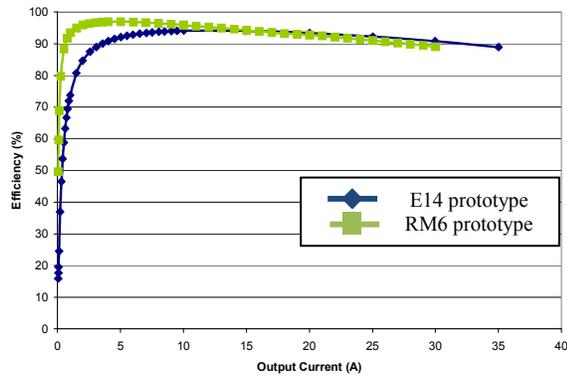
3) Circulating energy losses. These include losses in the magnetic core and losses due to the AC resistance in the windings of the transformer. The core losses are calculated by Steinmetz equation:

$$Pv = k \cdot f_{SW}^\alpha \cdot B^\beta$$

in order to calculate losses due to AC resistance of the transformer windings, (which gains importance when operating at high frequency), an AC resistance model has been obtained from PEmag. With this model, the AC resistances at different frequencies can be calculated, and use them in the formula:

$$PR_{AC} = n \cdot (RMS_1^2 \cdot RAC_1 + RMS_2^2 \cdot RAC_2 + \dots + RMS_n^2 \cdot RAC_n)$$

Figure 5 shows the prediction of the losses using this model for an output current of 30 A within a wide range of operating frequencies. From this curve, the frequency for less losses for a given  $L_{MAG}$  at  $I_{OUT}=30A$  can be chosen.



**Figure 8.** At frequency of 100 kHz, the efficiency of the prototype is higher than 90% for a wide load range: from 3 A to 30 A.

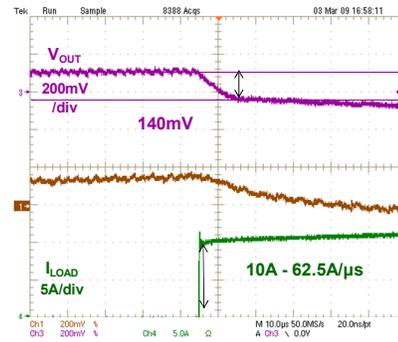
#### IV. DESIGN OF A FOUR-PHASE PROTOTYPE APPLYING PROPOSED METHODOLOGY

Based on the proposed minimum energy storage concept, two four-phase converters were implemented in order to verify the concept. The design specifications for both converters are:  $V_{IN}=12V$ ,  $V_{OUT}=3V$ ,  $I_{OUT}=30A$  and  $I_{RIPPLE}<5\% \cdot I_{OUT}$ . The main difference between these two prototypes is that they were designed with different criteria. The first of them was designed prioritizing the reduction of the switching losses, this is mainly reflected in an increased efficiency at medium and light load. Operating frequency of this prototype is around 40 kHz and the size of the transformers employed to couple the phases are RM6 and the magnetizing inductance is  $100\mu H$ . In the design of the second prototype, the proposed design methodology is applied with the aim of optimizing the size and power losses. The size of the cores, resulting from the application of the methodology is E14 ( $L_{MAG}=10\mu H$ ). This prototype is operated at 100 kHz. In order to develop this solution, the following design guidelines, based on proposed design methodology, were followed:

1. The number of phases was selected in agreement with the required conversion ratio. For this case  $V_{IN}/V_{OUT}=4$ . Any multiple of 4 can achieve the desired conversion ratio. Four would be the minimum number of phases at which the desired conversion ratio can be achieved, when  $k=1$  (since  $d=k/n$ ,  $d=25\%$ ); for simplicity, four phases have been selected.

2. When size of the prototype is a main constraint, the core can be chosen in function of its size as the next step. Assuming that the turns of the transformer are integrated into the PCB, maximum number of turns fitting into the window area of the core is determined when a PCB technology is chosen, hence determining the maximum magnetizing inductance and the minimum operating frequency that accomplishes the specified current ripple. In this case, planar E14 cores are chosen.

3. At this point (with initial  $L_{MAG}$ ,  $f_{SW}$ , and current ripple determined), a preliminary losses evaluation can be done taking into account the losses in the transformer (DC and circulating energy losses). Since full load output power is known, acceptable losses in the transformer can be considered



**Figure 9.** For a 10 A load step (60 A/ $\mu s$ ) only twenty 22 $\mu F$  capacitors are needed to maintain the voltage deviation within 5% of  $V_{OUT}$ .

to be less than 5% of total output power at full load. In order to achieve this losses level, turns number should be decreased and more windings can be paralleled, thus reducing DC losses. After this, it is interesting to return to step 2 in order to choose a different core size and evaluate different configurations for the transformer.

4. When a set of acceptable transformer designs has been done, the next step is to evaluate different MOSFETs with this set of transformers. The evaluation of different MOSFETs has to be carried out based on a losses model explained above. After selecting the less power losses combination for  $L_{MAG}$ ,  $f_{SW}$  different set of MOSFETs can be evaluated. After choosing the right MOSFETs for the selected operating frequency, a prototype can be build. The prototype with E14 cores is shown in Figure 7. The turns of the transformer are integrated into de PCB and in this case, a 12 layer PCB was chosen for the implementation of the prototype. Its efficiency is shown in Figure 8 along with the efficiency of the prototype built with RM6 cores. The size of RM6 prototype is greater than that of the optimized E14 prototype (effective volume for RM6 is  $1090mm^3$  while for E14 is  $300mm^3$ ). Although at heavy load, the efficiency for both prototypes is very similar, the peak efficiency for RM6 cores is higher than that for E14: 96.9% and 94 % respectively.

For both prototypes, efficiency is high in a wide load of ranges, for E14 prototype efficiency is greater than 90% for 3A to 30 A, while for RM6, this range goes from 1 A to 25 A. When using the RM6 prototype with  $V_{IN}=12V$  and  $V_{OUT}=6V$ , the measured efficiency is 98% from 4 A to 6 A (24 W to 36 W). Figure 9 shows output voltage deviation (when a load step occurs) for the topology built with E14 cores: the output voltage deviation for  $V_{OUT}=3V$  is shown in this figure ( $\Delta V_{OUT}=140mV$ ). This is due to the drop in the equivalent series resistance of the converter at 10 A (for this prototype, measured  $R_{SERIES}$  equals 10 m $\Omega$  approx.). It is important to point out, that this voltage drop cannot be compensated since the prototype can only operate with duty cycles of 25%, 50% and 75%. The slew rate of the applied load step is 60A/ $\mu s$ . This response is achieved with only 20 MLC Capacitors of 22 $\mu F$  at the output and a 470 $\mu F$ -Oscon at the input.

## V. CONCLUSIONS

The proposed topology, which can be considered as multiphase converter with transformer coupling, is controlled with a constant-input, constant-output control strategy, which allows a direct transfer of energy from the input to the output. Since stored energy is minimized in the converter, the dynamic response of the topology is decoupled from the operating frequency and this parameter can be chosen in order to optimize losses or size of the converter. It is important to point out, that due to the lack of energy storage in the proposed topology, there are only certain duty cycles where the converter can be operated and these points correspond to the duty cycles where the proposed control strategy is achieved.

The proposed design methodology is based on a losses model. With this model, different transformer configurations (size, turns) can be evaluated in order to determine the less power losses operating frequency. This methodology is applied to optimize the design of a prototype, and its optimum frequency is around 100 kHz with small cores (E14). Since switching frequency is kept in a low value (100 kHz) switching losses can be reduced and the obtained efficiency is high in a wide load range ( $>90\%$  for 3 A to 30 A) and a peak efficiency of 94% was measured. When using bigger cores (RM6) higher efficiency can be achieved: peak efficiency of  $\approx 97\%$  and the range where  $\eta > 90\%$  is from 1A to 25 A. This efficiency can be achieved while maintaining a fast dynamic response thus allowing a small size of the output capacitor. The high efficiency presented by this topology enables its use as a first stage, in two-stage architectures, where the converter in the second stage (the converter placed close to the load), can benefit from a lower input voltage. Regulation capability of this topology is limited, but if multiple-phases are considered, output voltage can be changed among different values and the topology can be considered as a DC-DC transformer with multiple ratios.

## REFERENCES

- [1] Julu Sun, Ming Xu, Yucheng Ying and Fred C. Lee. "High Power Density, High Efficiency system Two-stage Power Architecture for Laptop Computers". Power Electronics Specialists Conference, 2006. 37th IEEE pages 1-7. June 2006
- [2] Yuancheng Ren, Ming Xu, Kaiwei Yao, Yu Meng and F.C. Lee. "Two-stage approach for 12 V VR". Power Electronics, IEEE Transactions on, Nov. 2004
- [3] K. I. Hwu, and Y. T. Yau, "A Simple Resonant Voltage Divider", Applied Power Electronics Conference and Exposition, 2009. APEC 2009
- [4] Ming Xu, Julu Sun, and Fred C. Lee, "Voltage Divider and its Application in the Two-stage Power Architecture", Applied Power Electronics Conference and Exposition, 2006. APEC 2006
- [5] M.C.Gonzalez, L.Laguna, P.Alou, O.Garcia, J.A.Cobos and H.Visairo, "New control strategy for energy conversion based on coupled magnetic structures", Power Electronics Specialists Conference, 2008. PESC 2008. IEEE
- [6] Yuancheng Ren, Ming Xu, Jinghai Zhou, and Fred C. Lee, "Analytical Loss Model of Power MOSFET", IEEE Transactions on Power Electronics, Vol. 21, No. 2, March 2006
- [7] P.Zumel, O.Garcia, J.A.Cobos, J. Uceda, "Tight magnetic coupling in multiphase interleaved converters based on simple transformers", Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE pp: 385- 391
- [8] Pit-Leong, Peng Xu, Bo Yang, F.C. Lee "Performance Improvements of Interleaving VRMs with Coupling Inductors" IEEE Transactions on Power Electronics, Vol.16 July 2001