Design and implementation in a DSP of a digital double voltage/current loop for a power inverter for an aircraft application

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Abstract—In this paper is presented a method of control of a power inverter with a DSP. The control is based on two PWMs that controlled a full bridge. Being an application for avionics, a slow branch has a frequency of 400Hz. In order to have precision in the final waveform, the fast branch of the full bridge is 40 kHz, what prevents a calculation time of 25µs for the computation for all the system. In addition, a communication protocol has been implemented to be able to put the inverters in a parallel mode and in three phase mode.

Keywords-component; Digital Signal Processor ; Control Loop design ; Comunication protocol ; Inverter 400Hz ;

I. INTRODUCTION

In the airplane, having a alternative current is important for the motor, equipment, etc. The power inverters is used in photovoltaic applications [1] or in airplane ones [2]. Because of the size of the magnetic component, the frequency is 400Hz. The critical systems must have an Uninterruptible Power Supply (UPS). Low switching frequency and high output voltage fundamental frequency will result in a low control bandwidth [3]. The controller gain at the fundamental frequency is limited when traditional PI or PID controllers are adopted in a low bandwidth control system, so the system has high steady state error and slow dynamics response [4]. Moreover, the delay induced by the processes of sampling, computing and PWM have bad impact on transient and steady state performance of the system in digital control.

In the state-of-the-art, the UPS is usually controlled by a DSP with a 50Hz (or 60Hz) frequency signal [5]-[7]. As it can be seen in Figure 1, S1 and S4 is going to form a branch (the slow one) and S3 and S4 is going to form another branch(the fast one). An elevated modulation in frequency (proportion between the frequencies of the two branches of the complete bridge) is necessary to have a high precision. So if a sinusoidal voltage of 50Hz is wanted and if a slow branch/fast branch topology is used, the fast branch will have a frequency of 5 kHz so the period will be 200us. This time is used to calculate the next duty cycle .The higher the period, the easier the implementation of the control and/or the protections.

Traditionally, the analogical control method uses a PWM. But there are a number of drawbacks found in an analog system, for example, temperature drifts and susceptibility to ElectroMagnetic Interference (EMI). A natural technique of PWM generation is to compare a sinusoidal waveform with a triangular signal. When a circuit is affected with an EMI noise or with the temperature, it can cause problems in the MOSFETs commutation of the.

Another possibility to control a full bridge for the generation of a sinusoidal signal is with a microprocessor and a generator of signal PWM helped by an Analog to Digital Converter (ADC). The particularity of the DSP (Digital Signal Processor) is that they have all the peripherals in one chip. Thus, with the data of the ADC and with the digital reference and the previous data of the duty cycle, the next pulse width can be calculated.

II.- CONTROL OF THE PWM IN CURRENT MODE AND VOLTAGE MODE

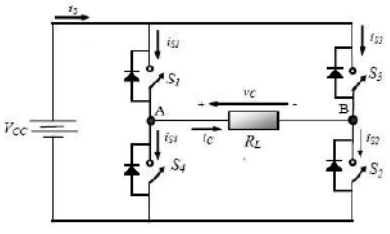

Figure 1: Full Bridge of the single-phase inverter

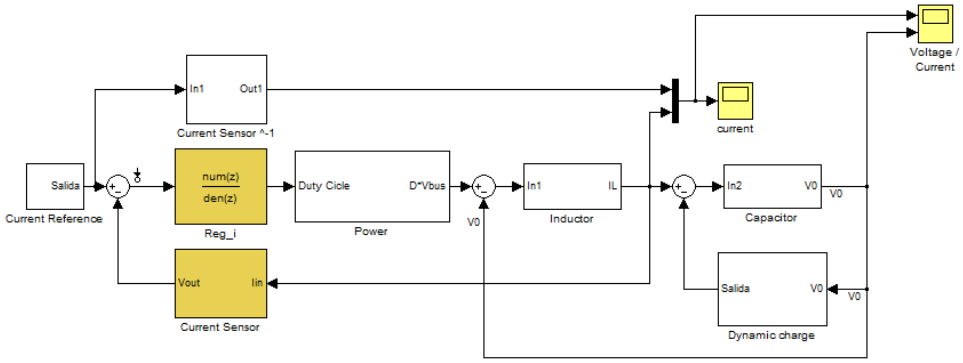

Figure 2: Model of the current mode control

As it can be seen in Figure 1, the inverter has a continuous bus of Vcc=200V. The amplitude of the voltage is directly proportional to the control of the pulse width of the PWM. Before the output filter (LC), the voltage can vary between - V0 and +V0. In this section, we study the current control mode (Figure 2).

Figure 2 is a model of the system using steady state equation. "Current Reference" is going to generate the sinusoidal reference for the system. The block "Reg_i" is the current reference. The input of this block is the current error between the reference and the measurement. "Power" Is a model of the power supply. Typically, it multiply the duty cycle by the voltage bus. then, the current in the inductor is calculated by the equation 1. At the end, the output voltage is calculated by equation 2.

$$I_L(t) = \frac{1}{L}\int (D(t) * V_{Bus} - V_O(t))dt \qquad (1)$$

$$V_O(t) = \frac{1}{C}\int \left(I_L(t) - \frac{V_O(t)}{R}\right)dt \qquad (2)$$

This control is made with a 4 order regulator that it is a PID plus a pair of complex conjugate zeros with an important gain at 400Hz. It has had to implement this gain to clear the phase angle that could exist between the reference and the current. Indeed, the system has a slow branch. A phase angle takes place due to the exit filter and the load. If the load changes, the phase angle between the reference and the exit current also changes and produces problems in the crossing by zero. Then, the design must clear the phase angle. The complex pole in 400Hz that has been put in the regulator gives enough gain to clear the phase angle [6]. The regulator has been designed to regulate the current so the voltage is sinusoidal at 400Hz for any load. Figure 4 represents the waveform of the current and the voltage for 3 different loads and the Bode diagram of the regulator can be seen on Figure 3.

In figure 4 is possible to see the output voltage (above) and the current in the inductor. The system is controlling in current mode, so the current in the inductor must follow the reference.

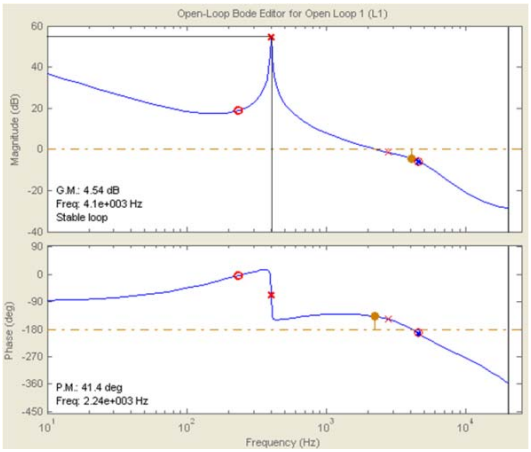

Figure 3: Bode diagram of the current loop.

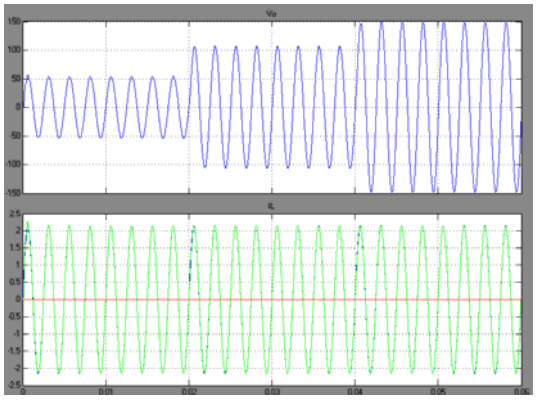

Figure 4: Control of the inverter in current mode.

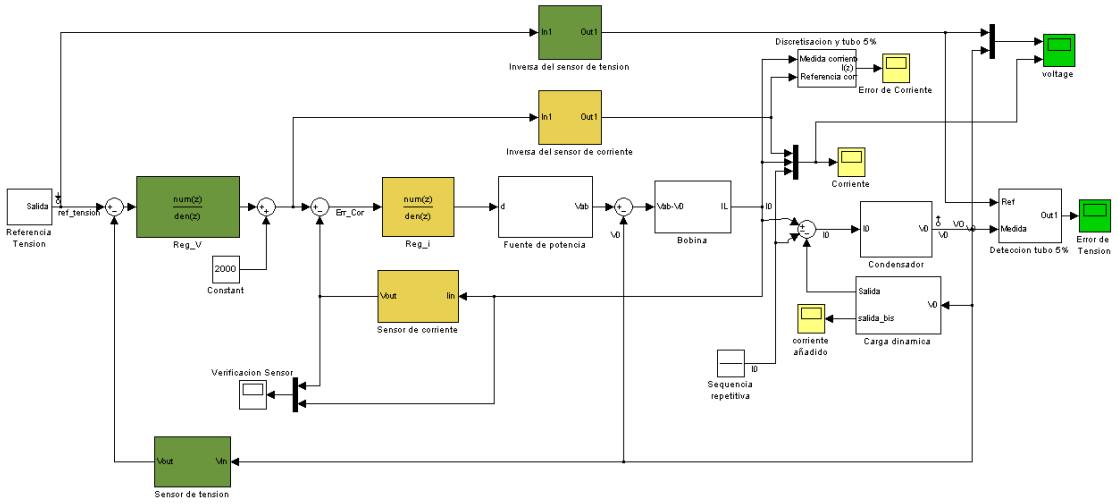

Figure 5: Model of the voltage control.

It is possible to appreciate that the current does not change while the output voltage goes from 50V to 150V.

The regulation of the output voltage is based on the same design than the current regulation. That is, a 3 order regulator with a double pole at 400Hz to avoid the phase angle between the output voltage and the reference. The difference between the current control and the voltage control is that the current reference is given by the voltage regulator. In figure 5, the complete system modeled in Matlab Simulink® can be seen.

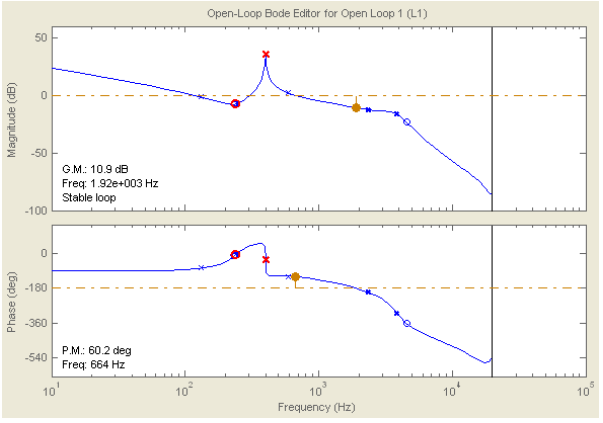

Figure 6: Control of the inverter in voltage mode.

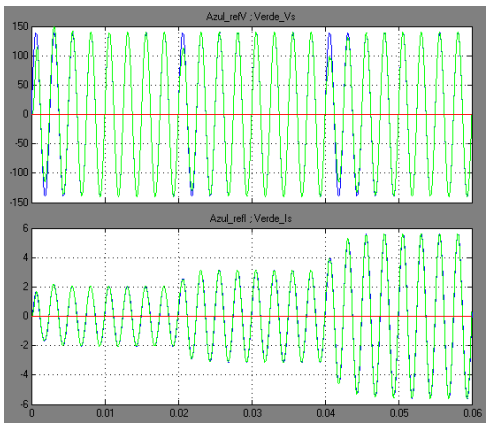

Figure 7: Control of the inverter in voltage mode.

Figure 6 represent the bode diagram of the voltage loop. It can be seen an important gain margin at 400Hz (50dB) to avoid the phase problem.

Figure 7 shows previous results. The system has been tested with 3 different loads to verify that the output voltage does not change meanwhile the current takes the value provides by the voltage loop.

The advantage of having a double control (current and voltage) is the robustness and the possibility of putting the inverters in parallel with a system of master/slave, where the slave is current controlled so that it doesn't interfere with the voltage regulation (master) in the load.

The proposed system is done in Matlab Simulink ®. The coefficients of the regulators are decimal. Then, it is possible to implement it in a DSP in two ways. First it is using decimal numbers (float).

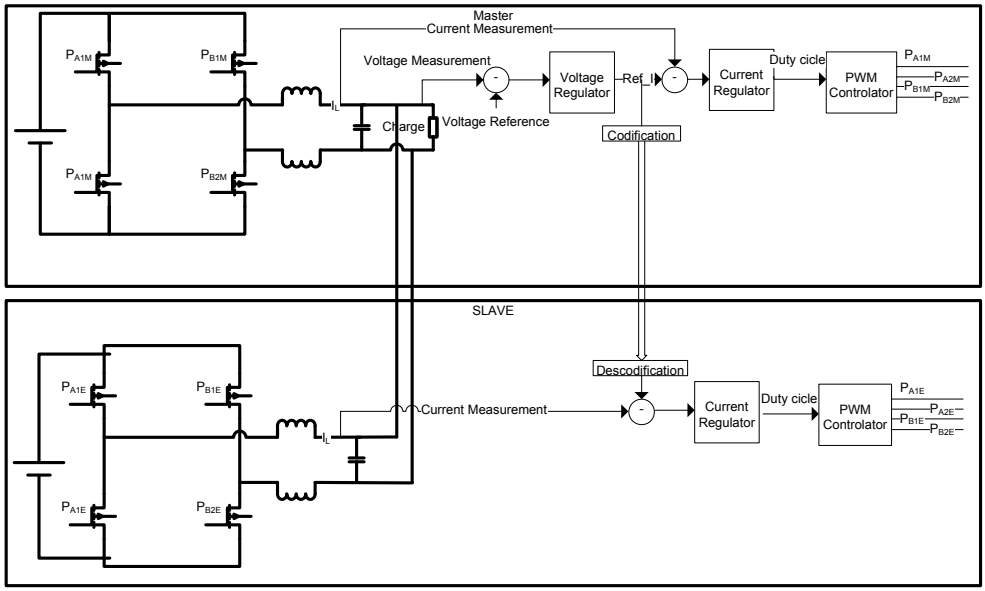

Figure 8: Scheme of the parallel inverters

The fixed point DSP can calculate using this type of numbers, but they are very slow. Using floating point numbers, the current loop is executed in 22µs when the maximum time of computation is 25µs (period of commutation of 40 kHz). Then it is preferred to use a DSP with a floating point unit, but it is an expensive solution. The second possibility is to optimize the code using a library of floating point calculation that translates floating point numbers in fixed point numbers using an approximation number, encoding them with N bits ($1 < N < 31$) of resolution. The IQmath library of Texas Instrument [8] is a collection of much optimized mathematical functions that are used in the fixed point DSP, so the DSP 320F2808 simulates a calculation unit with floating point on a calculation unit in fixed point. Using this library, it has been possible to optimize the time of computation of the current loop from 22µs to 7.5µs

III. COMMUNICATION SYSTEM OF THE POWER INVERTER

The inverter presented here has a power of 350VA. If more power is wanted, the inverter can be put in parallel, having a master who controls the voltage and the current. The slave only gives power, so there isn't voltage control in the slave board; it receives the current reference from the master via a parallel connection between both boards. Figure 8 represents the system.

In this figure, the master can be seen (above) which has a current and voltage regulator. At the end of the voltage regulator, the current reference is encoded and submitted to the slave. This reference can be decoded and used to calculate its duty cycle with its current regulator. So, the slave does not need a voltage regulator.

The communication system encodes the current reference with 10 bits. The Master interrupts the slave DSP that receives the current reference on 10 GPIOs (General Purpose Input Output) and it decodes it. Once decoded, the slave sends a reception confirmation to the master, by means of interruption, to indicate that the communication has succeeded. In addition of it is being very robust to the outer noise because it is sent digitally, it is encoded and it is sent in a maximum delay of 2µs.

In Figure 9, it can be seen the low branch at 400Hz(yellow) of the system, the fast branch at 40kHz (red), the sinusoidal current measurement (green) and the communication system (Digital1). It can be seen the 10 bits plus the start bit (D10). So, the current reference, that is calculated by the voltage regulator, is codified every commutation cycle to be sent to the slave board.

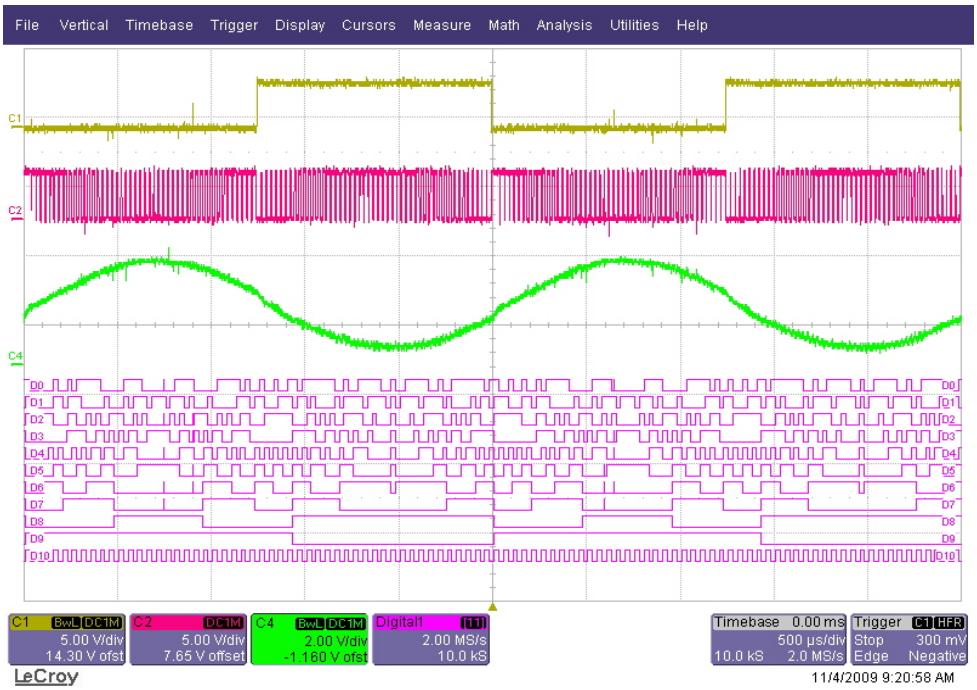

Figure. 9: Communication system

IV. PROGRAMMING OF DSP TMS320F2808

The program begins by a boot of its registries. The PWM must be formed with a frequency of 40 kHz, the GPIOs must be defined as inputs or outputs, depending of its use, the WatchDog also have a boot, etc. When the system is ready to start, the interrupt signal of the PWM is allowed. In this way, an interruption takes place and starts the analog to digital conversion. While a counter for the slow branch control is increased, the conversion of the data is made.

When the data is ready, the ADC interrupts the system and the data treatment starts. The system has to check if the 0V reference of the ADC and the 0V of the system are the same. If it is not truth, 20 values are taken in a sleepy state, these values are added and they are divided by 20 so that the ground reference is known.

The data is filtered with a digital average filter. The current reference is calculated thanks to the voltage regulator. Then, the current reference is encoded with 10 bits and it is transmitted to the slave. The duty cycle is calculated with the current reference and the measured current. So, the PWM registries are updated with the new value of the duty cycle, multiplying it with the maximum pulse width. Finally, the duty cycle is reflected in the PWM.

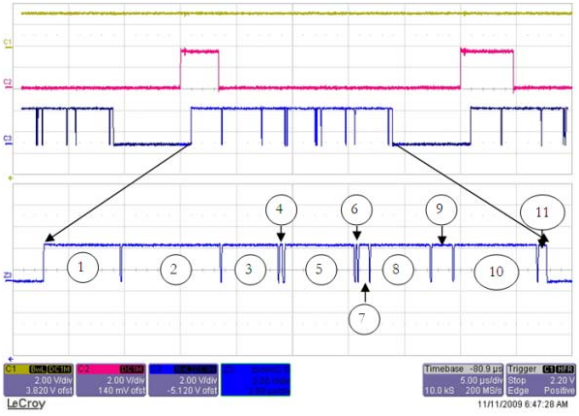

Figure. 10: Time of computation

In figure 10, the computation time of the system presented here can be seen.

Table I : Parameter of the digital controller

Number	Description	Time (µs)
1	Digital filter (mean value)	2.73
2	Voltage regulator	3.53
3	Current reference encoding	2
4	Displacement current error table	0.120
5	Displacement of the previous duty cycle table	2.48
6	Calculation of the new current error	0.6
7	Calculation of the current	0.365

	regulator numerator	
8	Calculation of the current regulator denominator	2.14
9	Program of data storage (only for tests)	0.775
10	PWM Controller	2.96
11	Registry updater	0.305
Total		17.98

V. Experimental Results

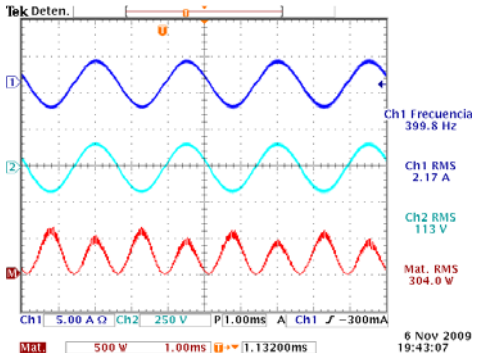

Figure 11a experimental Results

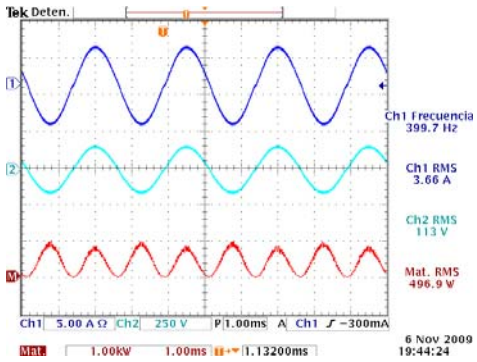

Figure 11b experimental Results

In figure 11a-b, the operation of the system with 2 different loads can be seen. Thus, it is possible to see that the voltage is 113VEFF at 400Hz while the current can be 2.17AEFF or 3.66AEFF. With an output power of 350VA, it has an efficiency of 96% with 2% of total harmonic distortion. The fluctuation of the power is due to an offset on the current probe.

VI. Conclusion

This article presents an implementation of a double voltage/current loop control for an onboard UPS airplane system. The TMS320F2808 from Texas Instruments has been used for the control of this inverter with a slow branch (400Hz) /fast branch (40kHz) topology. The implementation of a PWM digital control improves the efficiency of the inverter as opposed to an analog solution because of the simplicity to synchronize the slow branch and the fast branch, so it reduce the commutation loose in the MOSFETs. A pair of complex conjugate zeros at the frequency of the slow branch commutation (400Hz) has been implemented in the current regulator and in the voltage one, giving much gain at this frequency in order to reduce to the maximum phase angle between the measurement and the reference. A parallel system has been implemented with a master/slave topology for increasing the power delivered to the load. The master controls the output voltage and generates the current reference. Thanks to the digital system communication, the slave and the master have the same current reference and so it can increase the delivered power. The whole system, allows having a sinusoidal signal at the frequency of 400Hz, voltage and current controlled, with a maximum power of 350VA (with a single converter), an efficiency of 96% and 2% of total harmonic distortion.

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VII. Apendix

Table II: Parameters of the PWM Inverter

Parameter	Value	Unit
Filter inductor, L	2*720	μH
Filter capacitor, C	1	μF
Rated load resistance	30-200	Ω
Dc-link Voltage	200	V
Rated output voltage	115	V_{EFF}
Switching frequency	40	kHz