

Figure 47: CV comparison between all LIG MSCs with MoS<sub>2</sub> at different conditions

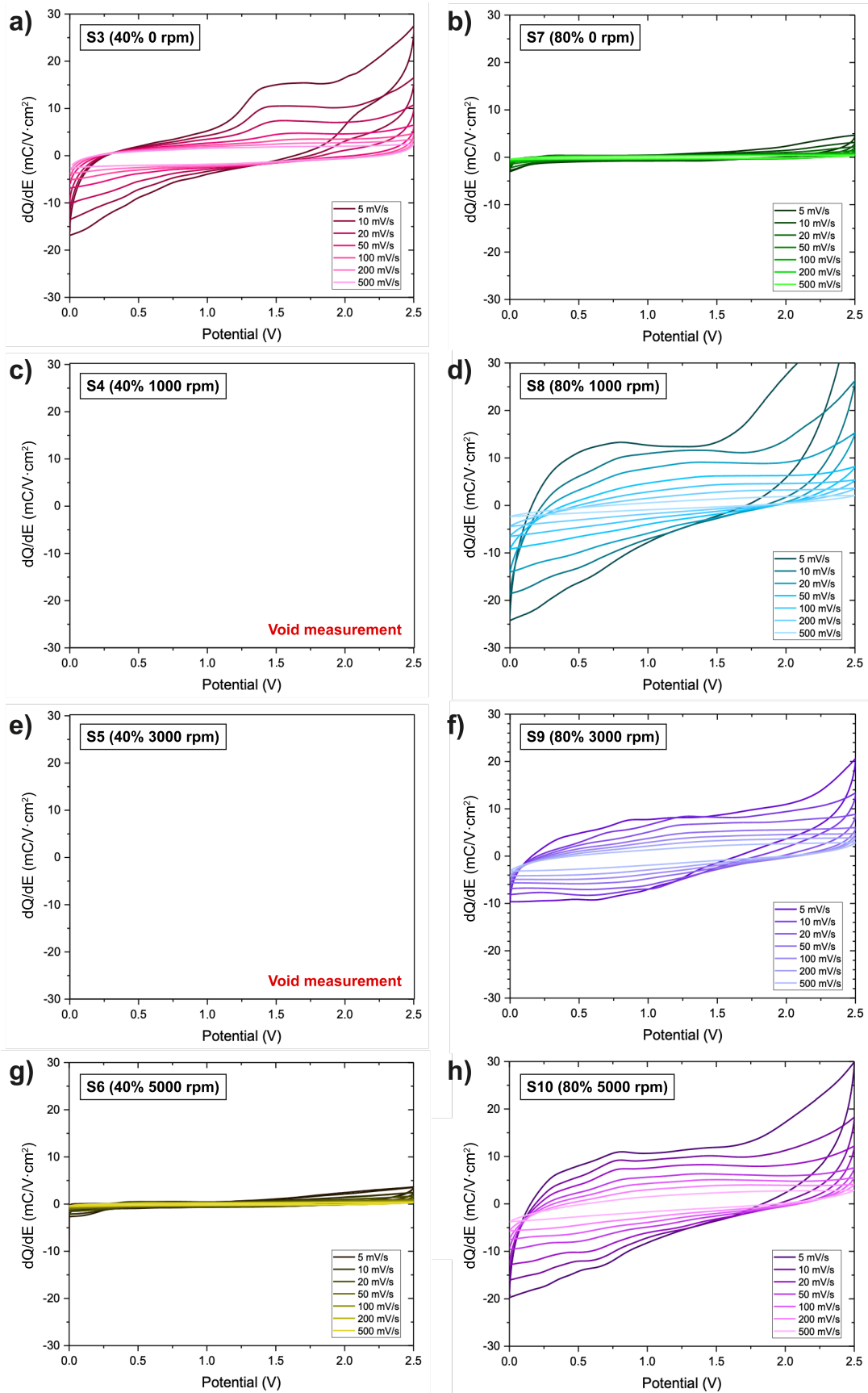
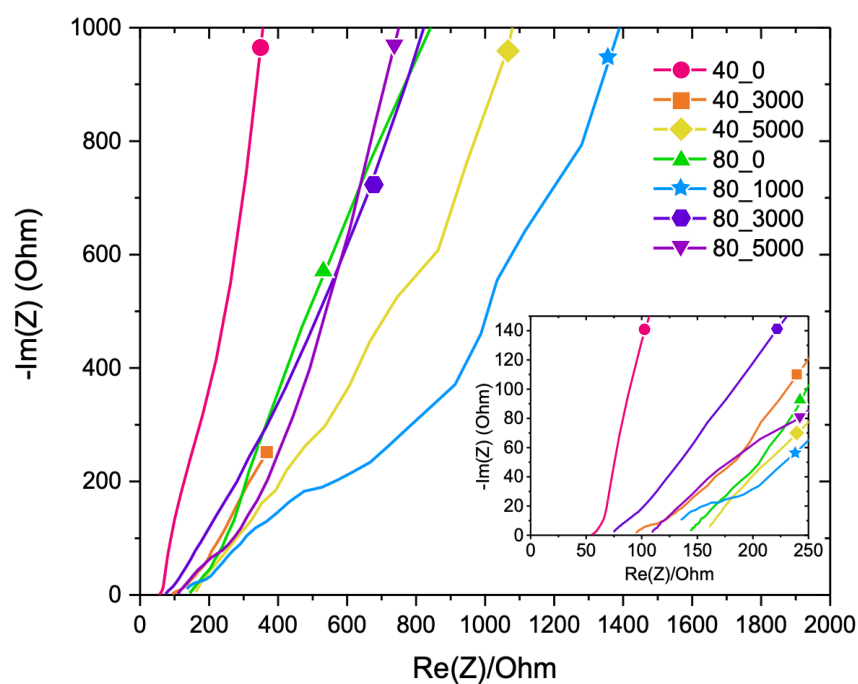


Figure 48:  $dQ/dE$  CV comparison between all LIG MSCs with  $\text{MoS}_2$  at different conditions.

In Figure 47 and Figure 48, the CV and  $dQ/dE$  measurements of all eight samples are shown at the same scale. A few observations can be made directly. Devices 80\_0 and 40\_5000 show a very small current in comparison to the other devices, only comparable to devices S1 and S2 made in December. All eight samples, S3 to S10, were made under the same conditions, so this low performance could be attributed to damaging of the LIG substrate during manual handling, or to a bad contact during sample fabrication. This variation makes it complicated to extract conclusions in the 80% EtOH series. For the 40% series, samples 40\_3000 and 40\_5000 could not be plotted due to inconsistencies during measurement.

The Electrochemical Impedance Spectroscopy data (see Figure 49) shows a big variability in the measured impedance between all samples, which also translates to the measured  $R_s$  parameter for each device. This parameter, as explained before, is extracted as the cross with the x-axis of the Nyquist plot, so an inset with a zoomed region of the graph is placed alongside the full one.

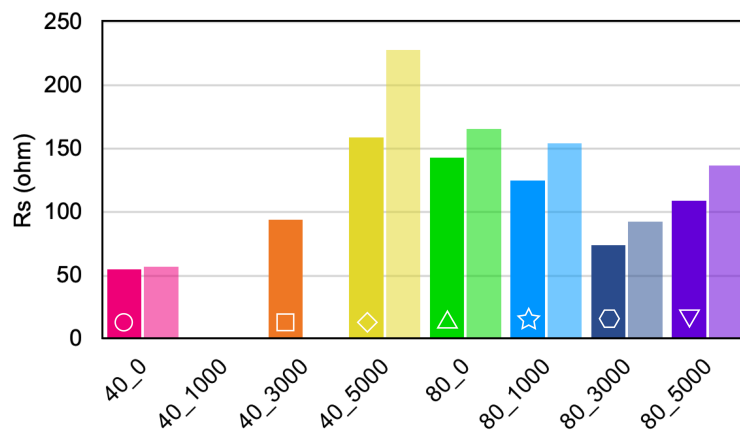


**Figure 49:** Electrochemical Impedance Spectroscopy data of all samples. Inset: zoomed region to visualize clearly the cross with the x-axis.

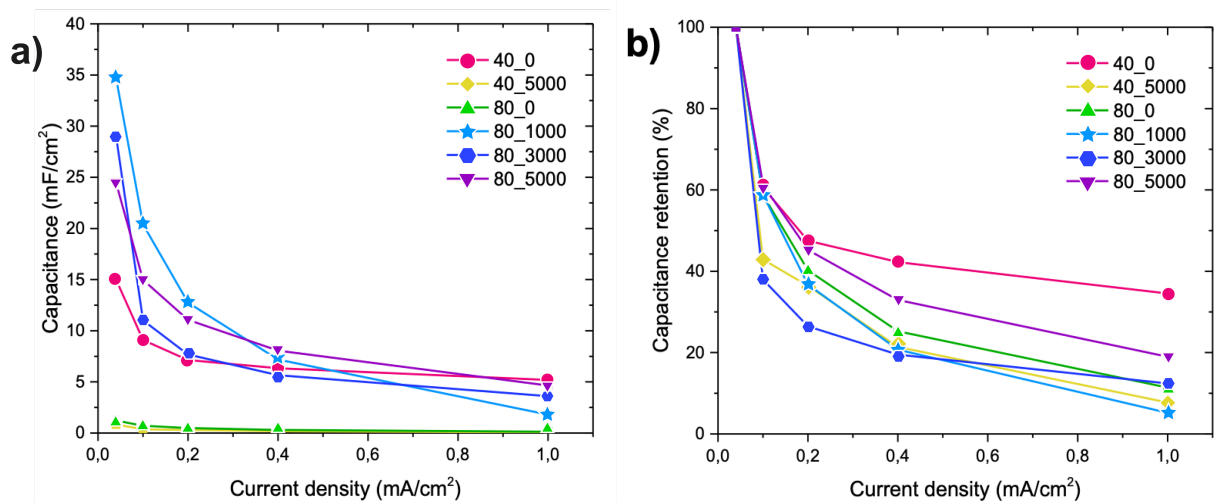
Furthermore, the results were confirmed by extracting the ERS value from the galvanostatic charge-discharge characterization, using equation 2.4, plotted in Figure 50. Both measurements show the same trend, and the difference between them is easily explained, as the solid columns' data are extracted from the EIS measurement, this represents the electrode resistance. On the other hand, the more transparent columns

represent the ESR value extracted from GCD measurements, which represents more resistance factors, including the electrolyte and its interfaces. In any case, both measurements show similar results, as 40\_0 (S3) is the lowest resistive device, while 40\_5000 (S6) is the highest.

By further analysis of the GCD data, using a custom python code, the areal capacitance for each device can be extracted. This data is plotted in Figure 51 showing the capacitance variation with the current density. In Figure 51b, the capacitance data is normalized by the highest capacitance value for each sample.



**Figure 50:** Series resistance values plot for all MoS<sub>2</sub> LIG devices. In solid, the Rs values extracted from EIS measurements. Transparent columns (right) represent the equivalent series resistance (ESR) extracted from galvanostatic charge-discharge measurements.

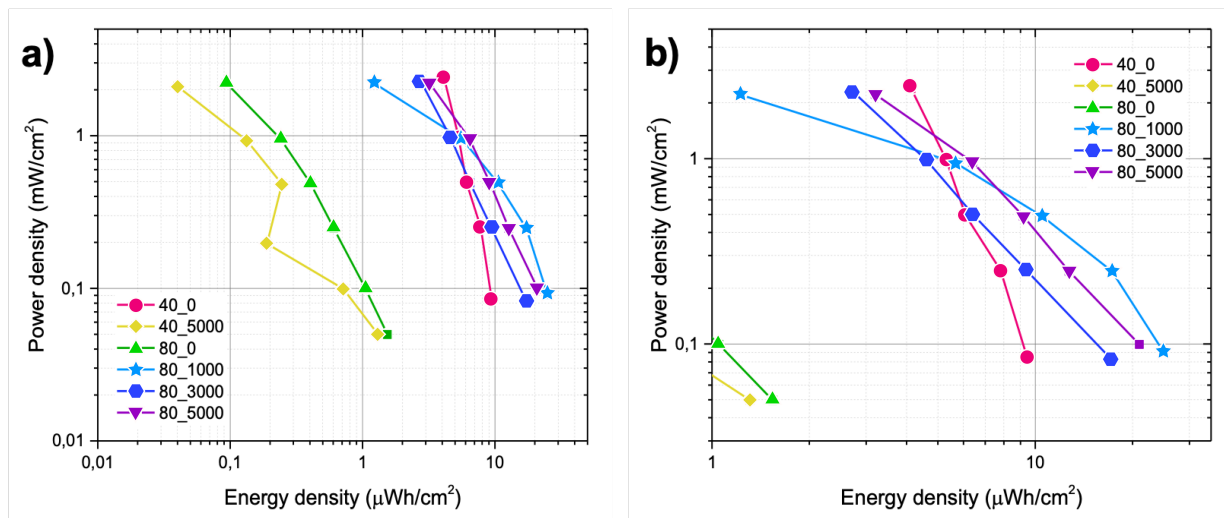


**Figure 51:** Comparison of the capacitance of the MoS<sub>2</sub> LIG microsupercapacitors. (a) Areal capacitance vs current density for all devices. Calculated from GCD measurements using a custom python code. (b) Plot showing the capacitance retention with increasing current density. Capacitance values from GCD, normalized by the capacitance at 0.04 mA/cm<sup>2</sup> for each sample.

For the six devices that could be fully characterized, we observe that the samples having the lowest series resistance are the ones that keep better the capacitance at high current densities, such as 40\_0 (the “flattest”) and to a lesser extent 80\_3000 and 80\_5000. Regarding the best performance at low current densities, we get promising results, with 80\_1000 showing capacitances of almost 35 mF/cm<sup>2</sup> at 0.04 mA/cm<sup>2</sup>, although its higher resistance is responsible for the quicker drop of the capacitance at high currents.

To better observe this behaviour, Figure 51b shows the same data, normalized for each device to the capacitance at 0.04 mA/cm<sup>2</sup> (100%) to analyze the capacitance retention with increasing current density. It can be observed that 40\_0, the less resistive sample, is the one that shows the highest retention, of around 40% at 1 mA/cm<sup>2</sup>. 80\_3000 shows an abnormally high capacitance at the lowest current, which falls towards a lower value, which is kept for high currents as expected, as its resistance is also very low. 80\_5000 is the best sample overall, with a high capacitance value at low currents and a decent capacitance retention at 1mA/cm<sup>2</sup>.

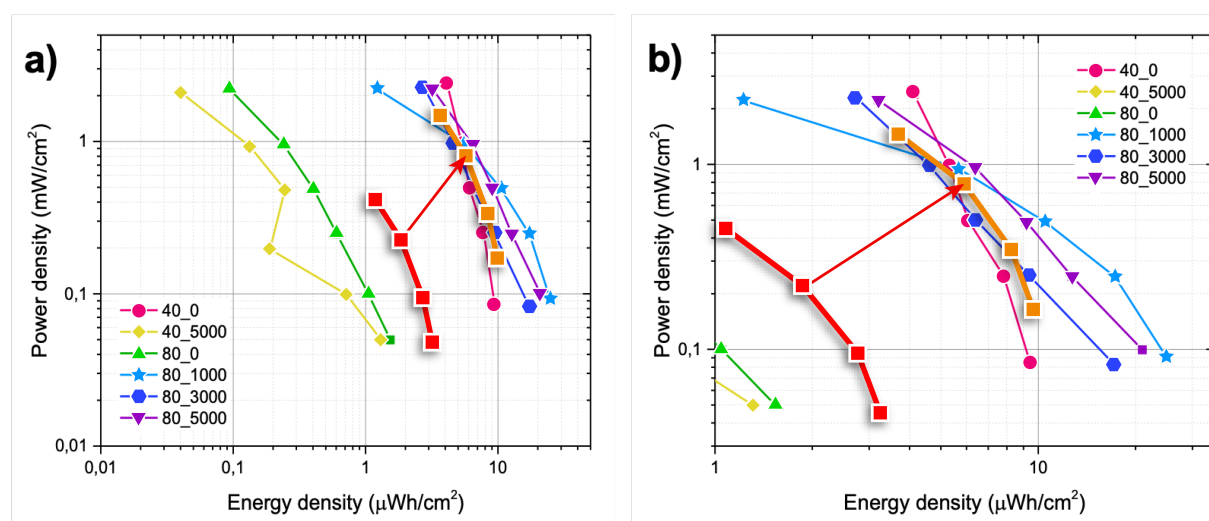
The most used comparison plot to study supercapacitors is the Ragone plot, where the measured devices are compared in terms of its areal energy density and areal power density. Figure 52 shows this plot for the six samples that could be fully characterized. In this plot, we observe similar results to those in Figure 51a. Samples 40\_5000 and 80\_0 are out of range, with much worse performance than the rest. For the other four samples, the same trends can be seen, with 40\_0 having the best energy density at high powers, and the worst at low powers. 80\_5000 is again showing a good overall performance, with good energy density at both extremes of the plot.



**Figure 52:** Ragone plot of the MoS<sub>2</sub> LIG MSCs. (a) Ragone plot of the measured devices. (b) Zoomed region showing only the best four devices.

The energy densities range between 10 and 25  $\mu\text{Wh}/\text{cm}^2$  for low current densities of 0.04  $\text{mA}/\text{cm}^2$  or 0.1  $\text{mW}/\text{cm}^2$ , and between 1.22 and 4.13  $\mu\text{Wh}/\text{cm}^2$  for a maximum power density of 2.25  $\text{mW}/\text{cm}^2$ , at a current of 1  $\text{mA}/\text{cm}^2$ .

It is interesting to contextualize these values with other LIG devices, in order to clarify if the use of  $\text{MoS}_2$  and its oxides brings any real improvement. To do this, future work is needed as the amount of samples that could be measured has been very limited. However, a theoretical approximation can be performed. This comparison is made against the best device presented in section 4.2.2, S-2.0-45, which Ragone plot is replicated in red circles in Figure 53a.



**Figure 53:** Theoretical comparison of LIG MSCs hypothetically measured in ionic liquid, with the  $\text{MoS}_2$  LIG MSCs fabricated. (a) Ragone plot of the devices complemented with  $\text{MoS}_2$ , together with two extra devices. In red circles, S-2.0-45 taken from section 4.1, and in orange triangles the same data, theoretically translated to take into account the change in conditions. (b) Same plot, zoomed to show better the region of interest.

To make this theoretical translation of the values, a rude first approximation be made using equations 2.3 and 2.4, presented in section 2. The energy density, according to equation 2.3, depends on the capacitance of the device, and on the square of the voltage window. For the voltage window, an increase from 1 V to 2.5 V would yield an energy density increase of 6.25x. However, the capacitance is theoretically reduced, some studies suggest that due to the difference in ion size, higher viscosity and lower conductivity of the electrolyte, capacitance can be expected to be approximately reduced by half, 0.5x [198]. In the same way, power density can be expected to increase the same factor than the energy density.

By applying these conversion factors, the energy density and power density data of S-2.0-45 could be modified, to show a tentative performance if the sample was measured

in ionic liquid electrolyte on an extended voltage window. This result shows the potential improvement that compositing with molybdenum oxides bring, taken into account the many unknowns that this study still has. The energy density can reach values that more than double the expected ones for bare LIG, while the power density is slightly improved as well.

However, this rude approximation does not consider the change in properties brought by the use of a different LIG material, double pass with high laser power. Furthermore, more experiments are needed in order to extract more conclusions, as only one device has been fabricated for each MoS<sub>2</sub> condition, and many samples offered resistivities that exceeded the acceptable values in order to fabricate reliable devices. More samples need to be fabricated, in the same way that was performed in section 4.1, to ensure that the device show similar performances at the same conditions. This work will be continued in the near future by fabricating more samples in order to extract stronger conclusions.



## 5. Graphene in silicon solar cells

### 5.1. Graphene as transparent electrode

Graphene is a recent alternative material to be used as transparent electrodes in a variety of applications due to the combination of its unique properties: high transparency, of more than 97.7% for one monolayer of material [199], high carrier mobility, high conductivity and extraordinary mechanical properties, including its ability to bend and stretch. Traditionally, most transparent electrodes are made from transparent conductive oxides, such as indium tin oxide (ITO) and others, and they have several challenges. First of all, its mechanical properties are limiting its applications, as ITO and similar materials are very brittle, and cannot be stretched or bended. Furthermore, there are supply chain issues regarding materials such as indium, a scarce rare earth for which reserves are expected to last only 20 more years.

The rise of new applications, such as bendable and foldable screens, and the explosion in photovoltaic cell technology adoption worldwide must be sufficient motivators to explore other materials. For now, flexible displays are already in the market, while not in large numbers as their price is not competitive yet. These displays currently use as transparent electrode a metallic nanowire mesh, typically made from silver, but also gold, which provides the required conductivity and offers mechanical flexibility.

However, since the discovery of graphene, this material has been called to replace ITO and other materials as a transparent electrode. In the meanwhile, many challenges still need to be solved.

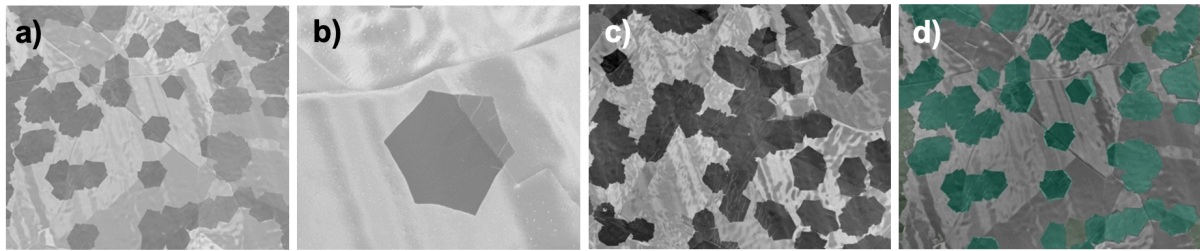
#### 5.1.1. CVD graphene growth and transfer

Large area growth of monolayer graphene continuous films has to be done through chemical vapor deposition. As explained in depth in section 3.1.1, a thin film of pure copper is placed inside the CVD reactor chamber, and given enough temperature and carbon-containing gaseous precursors, such as  $\text{CH}_4$ , after some minutes the gas molecules crack, in some systems helped by a plasma, and leaves the solid carbon on the surface. Thanks to the high surface temperature of the copper, the carbon can arrange forming crystals of graphene, which after some minutes have covered the entire surface.

In order to separate the graphene film from the copper, chemical etching must be performed. At ISOM a patented automated system is used [174], [175]. After being coated with a thin layer of protective PMMA, the copper/graphene film is placed on an ammonium peroxydisulfate (APS) solution. This chemical slowly etches the copper, and after some time and a thorough cleaning, a graphene/PMMA film is left floating in deionized water. The target substrate to which this graphene layer is to be transferred, can then be placed underneath, submerged in the liquid, and by slowly removing the water, the transfer process is finished. This versatile process can be used to transfer graphene monolayers on any arbitrary surface, with high yield and avoiding manual operation and contamination.

Monolayer graphene has been grown using different CVD recipes. Apart from the continuous monolayer growth, which is ideal for general applications, it is quite difficult to fully characterize the crystalline properties of the graphene film once the growth has been completed. Therefore, for some samples, the growth was stopped earlier, including only the nucleation stage of the graphene grains and allowing them to grow only partially. Together with a post-treatment in hot  $\text{H}_2\text{O}_2$  to oxidize the graphene/copper films, the samples could be inspected by SEM with high contrast. Hexagonal graphene grains can be seen, and important data such as the nucleation density, the lateral growth speed or the grain size could be extracted by careful image analysis, using a custom program created previously by the group.

As seen in Figure 54, the  $\text{H}_2\text{O}_2$  treatment helps to distinguish the almost transparent graphene grains from the copper background, as the areas covered by the graphene are protected from oxidation. In Figure 54b, a single crystalline graphene grain with its classic hexagonal shape is shown. The mentioned analysis program first adds more contrast to the image by means of a digital filter, and finally differentiates and classifies those areas (as shown in Figure 54d) in order to perform the required statistics. For the samples used in this work, the average grain size after 5 min of growth was 30  $\mu\text{m}$  in diameter, with a radial growth speed for each grain of around 3  $\mu\text{m}$  per min. The nucleation density was measured to be  $\sim 50000$  grains/ $\text{cm}^2$ , assuring the coalescence of the grains after around 8 min of CVD growth. To ensure a complete coverage of the graphene monolayer, the growth for the final graphene samples was maintained for 20 min.



**Figure 54:** SEM images of the graphene grains after a partial CVD growth and image analysis pipeline. (a) Low magnification. (b) High magnification on a single grain. (c) Pre-processing of the SEM image to increase contrast. (d) SEM image analysis result, from which the growth parameters are extracted.

### 5.1.2. Graphene field effect transistors

Given that the transparency of the fabricated graphene is given only by its number of layers, the most important parameter left to measure for this intended application is its resistance. For thin films, the concept of sheet resistance emerges, and there are many ways of characterising it. Taking advantage of previous processes developed by the group, the full electrical characterization of the fabricated graphene has been realized using graphene transistors. Graphene transistors, or GFETs, are a special type of transistor in which the channel through which the current passes is a graphene monolayer.

In a regular transistor, the current through the channel is modulated by the presence of a gate, which can be controlled using smaller currents than the ones passing between source and drain. A transistor can act as an amplifier, or just modulate one signal using a different one, and is the base of electronic technology nowadays. Standard semiconductor materials are widely used to fabricate transistors, silicon being the most common choice by far. Thanks to its semiconducting nature, silicon shows a different level of conductivity depending on the available carriers in its crystal structure, and by forcing the inclusion of different elements into the bulk of the material (doping), new carriers can be made available, electrons for n-type, and holes for p-type silicon.

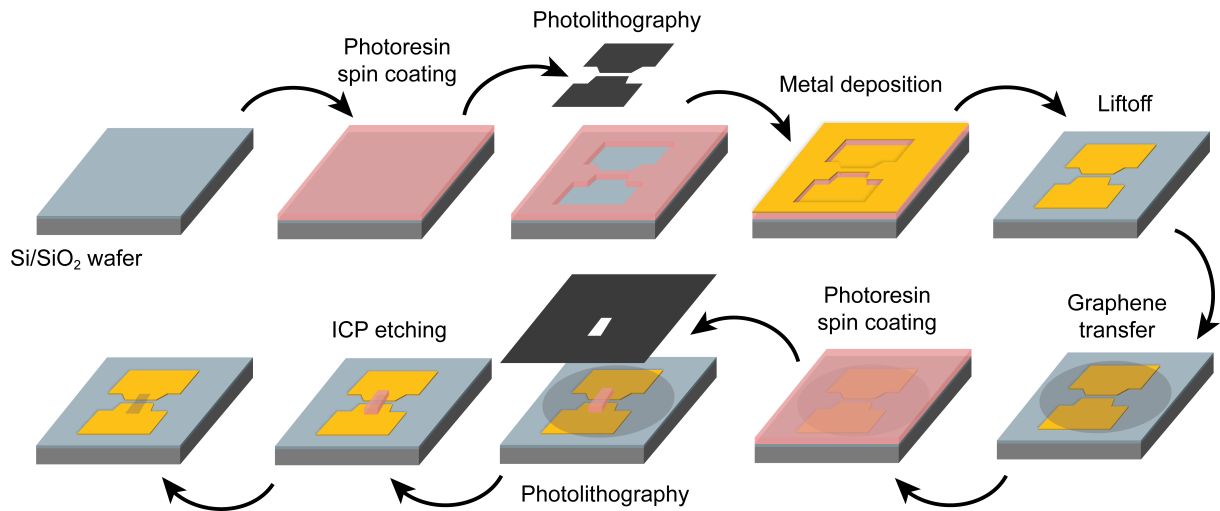
With silicon, a number of transistor architectures have been proposed over the years, and many others are still being proposed, as the miniaturization scaling of these devices keeps going on, fuelled by the huge demand for faster and more energy efficient electronics. The first one was the bipolar junction transistor, formed by two p-n junctions very close together, which was followed by the current complementary MOS (CMOS) transistor technology, based on metal-oxide-semiconductor (MOS)

junctions. These CMOS devices are based on the concept of the field effect transistor or FET, from which graphene transistors were proposed. In a FET, the distribution of charge carriers in the channel are modulated by a gate, which is isolated by an oxide layer, typically  $\text{SiO}_2$ .

GFETs are based on the same concept, where the graphene monolayer is deposited typically on a  $\text{SiO}_2/\text{Si}$  substrate. In this case, the graphene monolayer acts as the channel, so the source to drain current does not travel through the silicon film. The modulation of the channel is performed through the  $\text{SiO}_2$  insulated gate, placed below the graphene layer. This device is capable of a much higher cut-off frequency than standard silicon FETs, and the two-dimensional nature of graphene made it ideal to fabricate sensing devices. However, the structure is also ideal to characterise electrically the graphene, as the modulation of its conductivity by a gate voltage allows to extract magnitudes such as the position of the Fermi level of the graphene and the unintentional doping it achieved during processing, as well as its conductivity, sheet resistance and other basic parameters.

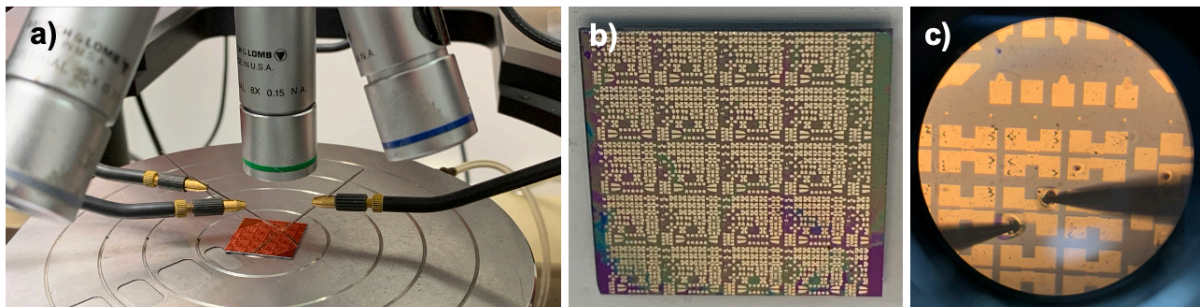
It's fabrication process is also rather simple and is schematically shown in Figure 55. One metallization and lift-off step is enough to define metallic contacts on a  $\text{Si}/\text{SiO}_2$  wafer, and graphene can be conformally transferred on top. An extra lithography step is required to define the graphene channels, which are isolated using inductive coupled plasma etching using oxygen. After removing the ICP resist protecting layer, in order to homogenize the properties of the graphene layer, an annealing step is required. The annealing is performed at  $280^\circ\text{C}$  in a tubular oven, in the presence of a nidron (non-flammable mix of hydrogen in nitrogen) flow, at ambient pressure. Through this step, the possible residues attached to the graphene are reduced, and the transferred monolayer gets more conformally attached to the substrate below.

The small dimensions of such devices allow to fabricate many of them on a single die, which is useful to perform statistical data analysis on the measurements, to smooth the high variability intrinsic to 2D materials. Furthermore, the exposed graphene layer on top of the transistor structure allows to continuously characterize the device as the following process steps are performed, such as chemical doping of the graphene layer or device encapsulation.



**Figure 55:** Schematic drawing of GFET transistor microfabrication process.

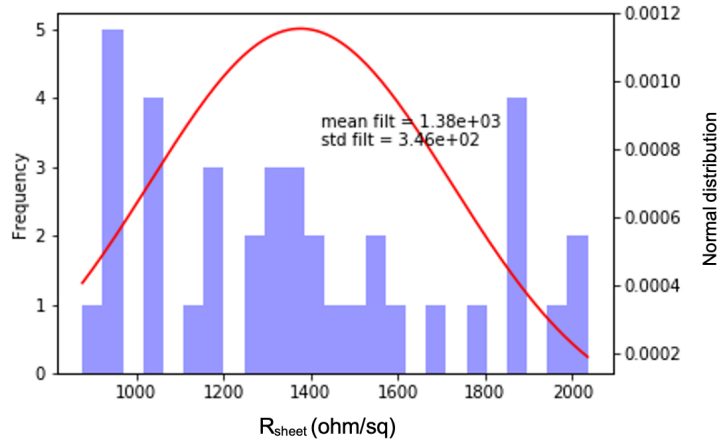
GFET characterization is performed through standard 3 terminal measurements using a probe station and a semiconductor analyzer (Figure 56a), which monitors the source-drain current with a variable gate voltage. During the measurement the gate current is monitored to avoid short-circuits indicative of device breakage. The IV data, taken from a set of GFET devices with different channel lengths, allows to extract the required parameters, which are analyzed using a custom python program previously developed in the group.



**Figure 56:** GFET transistors and measurement set-up. (a) Probe station measurement setup, using three terminals. (b) Final silicon die with many GFET devices (c) Close-up of the GFET being measured, through the optical microscope.

To characterize the deposited graphene layer, a photolithography mask was designed. This mask contains a matrix of patterns, each with 16 GFETs of different dimensions, with channel length ranging from 10 to 50  $\mu\text{m}$ . In a 20x20 mm silicon die, over 20 regions can be fitted, including over 100 transistors, as seen in Figure 56b. This high density of devices was designed to be very flexible, allowing to distinguish, for example, spatial variabilities such as the electrical properties of the edge and the center

of the transferred graphene monolayer, which can have different growth parameters. For the characterization performed in this experiment, between 30 and 60 GFETs for each silicon die were measured, as seen in Figure 57, more than enough to characterize the electronic quality of the graphene monolayer.



**Figure 57:** Histogram of electrical measurements for sample S275-3. (30 GFETs), no extra processing steps. In blue columns, the frequency of  $R_{sheet}$  measurements; in red, the normal distribution.

### 5.1.3. Graphene doping with $AuCl_3$

As mentioned in section 2.4.4, chemical doping is one of the key strategies to improve the electrical properties of graphene. Graphene presents an extremely high carrier mobility, due to its unique electronic band structure and crystal quality. However, the density of carriers at the Fermi level gets close to zero, making it highly resistive at that non-biased level. Therefore, the macroscopic properties of graphene regarding its conductivity have limited its application in many fields.

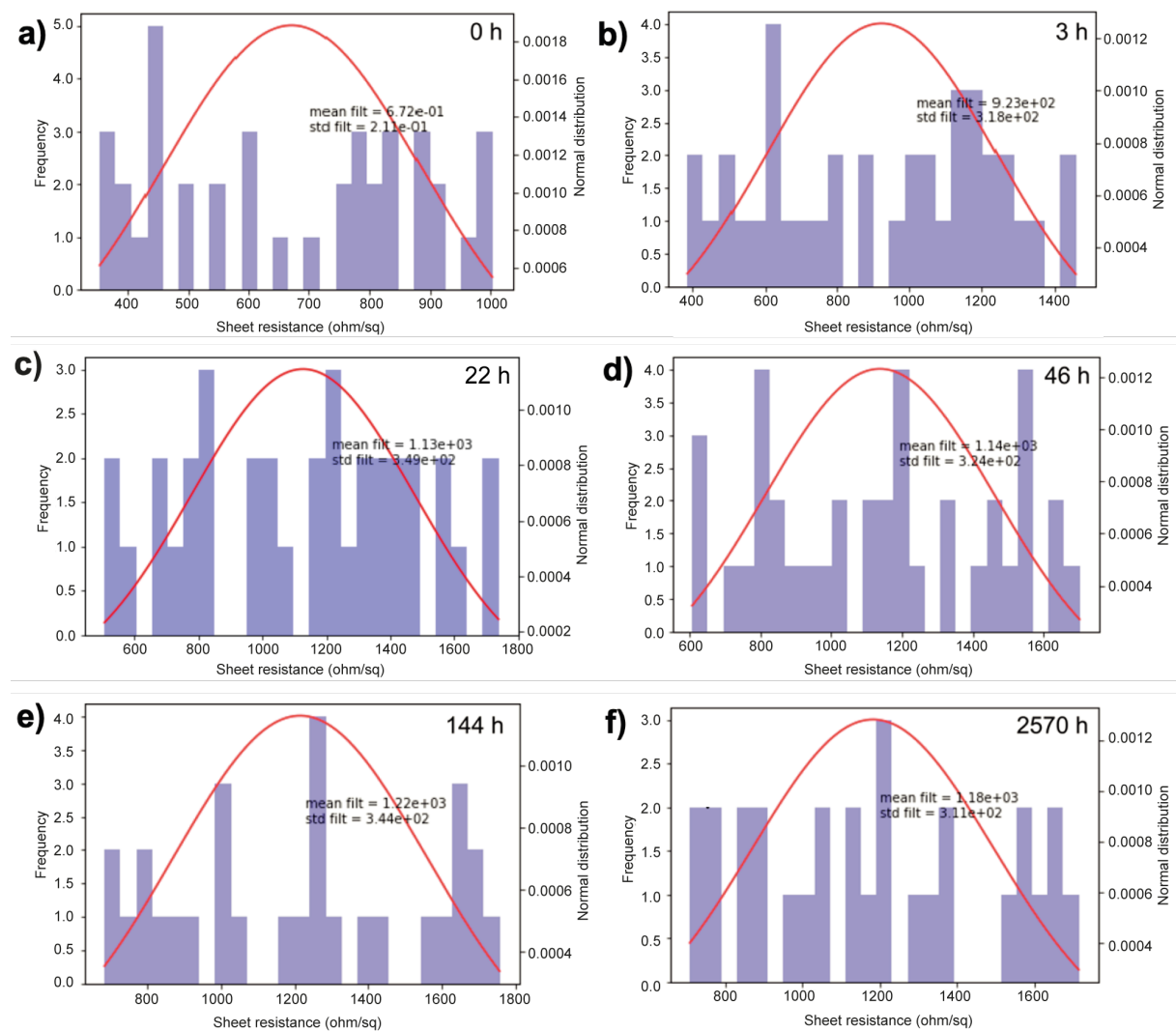
Graphene's sheet resistance is governed by two parameters, the carrier mobility ( $\mu$ ) and the carrier concentration ( $n$ ) by the following expression, where  $\mu$  is expressed in  $cm^2/Vs$ , and  $n$  in  $cm^{-2}$ :

$$R_{sheet} = \frac{1}{q \cdot \mu \cdot n} \quad (5.1)$$

In previous sections, the many possible dopants of graphene have been mentioned, from chemicals in vapor form, to metallic nanoparticles. Here in this study,  $AuCl_3$  nanoparticles have been used. The use of gold chloride nanoparticle as a dopant for graphene was proposed by Kim et al. [200], who achieved a 77% reduction in sheet resistance, up to 150  $\Omega/sq$  for monolayer graphene, by spin coating  $AuCl_3$  dissolved

in nitromethane, a very volatile solvent. The objective of this work was to deepen the knowledge of the group in graphene technology, adapting a proven method for graphene doping and study its degradation over time. Adding to this, the ultimate goal was to propose strategies to lock the doping particles on the graphene and avoid, or at least delay, its degradation.

For the characterization of the graphene doping and its degradation, the electrical characteristics of several doped graphene transistors were measured with time to observe any changes. The measurements were made in 30 devices, every few h at the beginning, and every few days later. The different measurements of the unprotected doped transistors are shown in Figure 58.



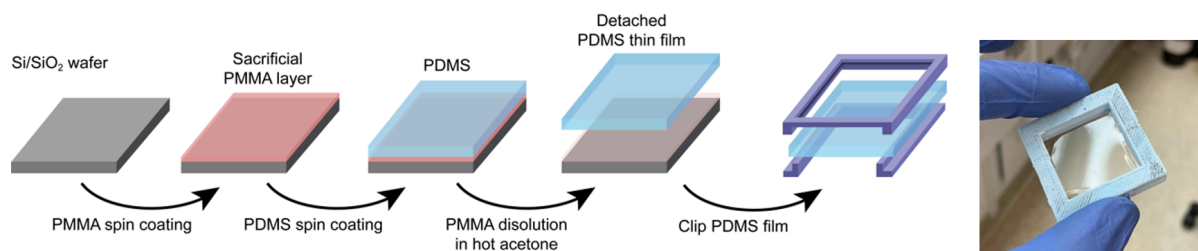
**Figure 58:** Sheet resistance histograms for sample "A" (S275-3) doped and unprotected. (a-f) Histograms showing the sheet resistance evolution with time of the graphene transistors, from 0 h to 2570 h.

Sample S275-3 (A), doped and left unprotected, shows a great improvement right after doping, with the sheet resistance going down from the original 1380 ohm/sq (Figure 57) to 672  $\Omega$ /sq immediately after. It took less than one day to bring the sheet resistance over 1000 ohm/sq, and after 22 h, the measured value was 1130  $\Omega$ /sq. After 6 days, or 144 hours, 1220  $\Omega$ /sq, the value was still slightly below the undoped one, and it kept the small improvement for 100 more days, the last measurement being 1180  $\Omega$ /sq after 2570 h.

#### 5.1.4. Doping encapsulation with PDMS thin films

It is clear that doping graphene with Au nanoparticles is beneficial for the sheet resistance, although the improvement fades quickly with time. However, it is necessary to protect the doped device with a layer which could trap those particles and isolate them from the degrading agents in the atmosphere, which for most dopants is humidity.

The proposed encapsulation technique to protect the doping without degrading its optical and electrical properties was the coverage with polydimethylsiloxane (PDMS), a silicone-based transparent polymer. Using PDMS, two strategies were tested. First, the direct spin-coating of the doped graphene transistors, baking and setting the PDMS on the chip. As this strategy was expected to interfere to some extent with the applied doping, a second strategy was developed, consisting on the fabrication of free-standing PDMS thin films using a lift-off method, as described in Figure 59. The dry PDMS thin film was then placed on top of the doped graphene transistors, and conformally attached to the substrate using light vacuum.



**Figure 59:** Schematic drawing of the PDMS thin film fabrication process, and picture of the final fabricated PDMS thin film.

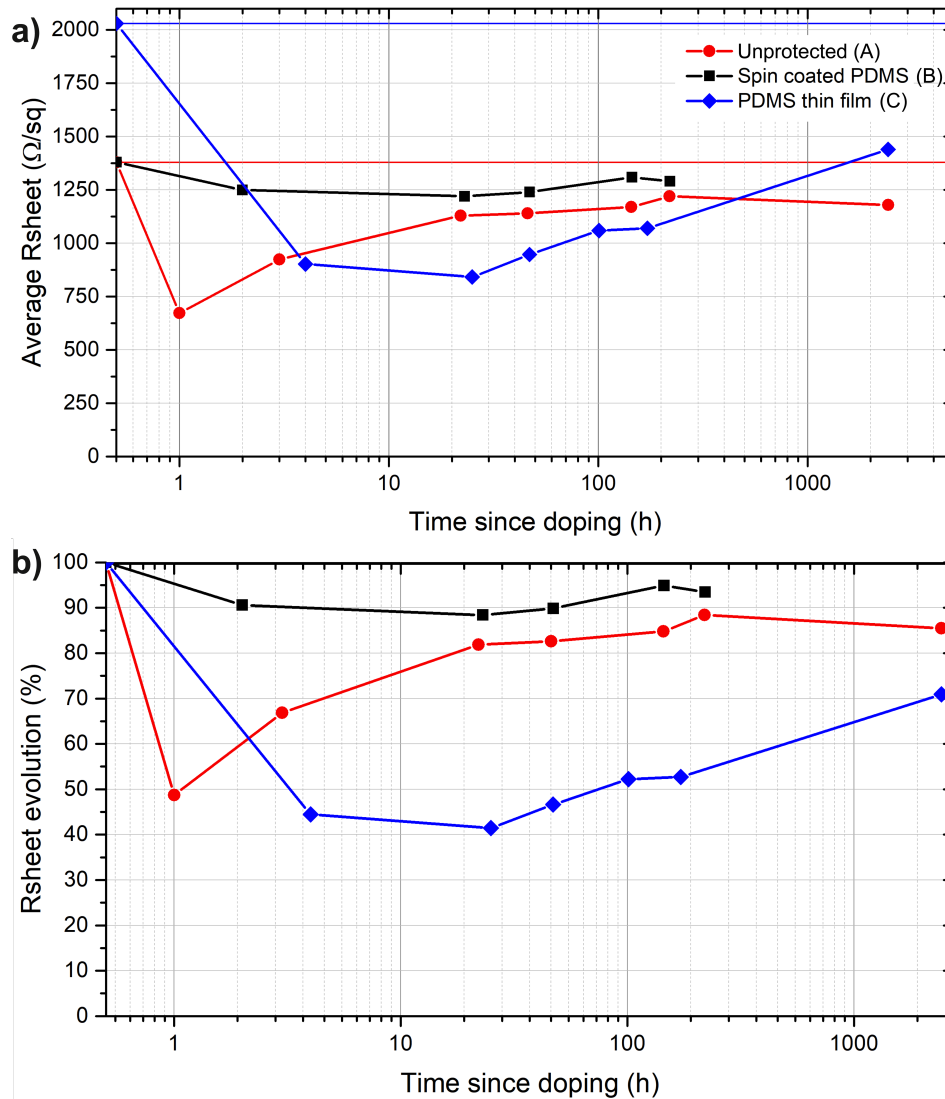
All three samples, the unprotected (sample A), the protected with spin-coated PDMS (sample B) and the protected with thin-film PDMS (sample C) were fabricated and measured over a span of 100 days, the last measurement being taken around 2500 h after the doping. The same measurements as the ones shown in Figure 58 were

performed for samples B and C, and the sheet resistance results are plotted in Figure 60 for clarity. Figure 60a shows the raw average values of the sheet resistance, and Figure 60b shows the same values normalized by the initial undoped  $R_{\text{sheet}}$  value for each sample. In both cases, lower is better.

Sample A and B are both part of the same graphene transfer piece, labelled S275-3, while sample C used graphene S275-4, part of the same S275 growth, but transferred as a different piece, at a different time. The as-transferred  $R_{\text{sheet}}$  value, post-annealing, for samples A and B is 1380  $\Omega/\text{sq}$ , while for sample C, the value was much higher at 2030  $\Omega/\text{sq}$ . After this measurement, samples were doped using the same 10 mmol  $\text{AuCl}_3$  solution and protected accordingly.

The blue diamond symbols represent sample A, with a marked reduction in  $R_{\text{sheet}}$  right after the doping, of around 50% of the original value. However, the doping particles get degraded over time and after 20 h, the resistance value increases up to around 85% for the rest of the experiment. For the protected samples, the trends are slightly different. Sample B did not show any relevant reduction in the sheet resistance, with values of around 90% of the original one. This can hint to a removal of the doping particles by the same protecting layer, as the PDMS layer was spin-coated in its liquid form, partly removing the Au nanoparticles in the process, or reducing its effect.

However, sample C, protected with a dry PDMS thin film, shows much better results. 4 h after doping, the sheet resistance was still of 900  $\Omega/\text{sq}$ , 44% of the original value. Furthermore, this low resistance level is kept for the first hours, as at 25 h, the measured value was the minimum of the series at 841  $\Omega/\text{sq}$  or 41%. For the next measurements, the values increase slightly, but to percentages of around 50%, much better than the other two samples. The last measurement, after 2500 h, shows an increase of the sheet resistance up to 1440  $\Omega/\text{sq}$  or 71%, still considerably better than samples A and B.



**Figure 60:** Graphene sheet resistance evolution with time, for three doped samples, all with 10 mmol  $\text{AuCl}_3$  spin coated. Sample A (red, circles) was exposed to air, not protected. Sample B (black, squares) was protected with spin coated PDMS. Sample C (blue, diamonds) was protected with a transferred PDMS thin film. (a) Absolute  $R_{\text{sheet}}$  values, averaged. Colored horizontal lines mark the initial  $R_{\text{sheet}}$  values for A, B and C samples. (b)  $R_{\text{sheet}}$  values expressed normalized by the initial value for each sample before doping.

A last comment must be made, as these experiments were heavily affected by the lockdown caused by the COVID-19 pandemic. The large gap between the two last measurements, at around 150 h and 2500 h is explained by the inability of accessing the labs between these times. After the access to the labs was re-established, the samples were measured one last time. However, the limited access to the equipment and time restrictions, made it difficult to continue with the series of measurements or to fabricate new samples, leaving the experiment without strong conclusions. However, these results, as well as the PDMS thin film strategy, which is very

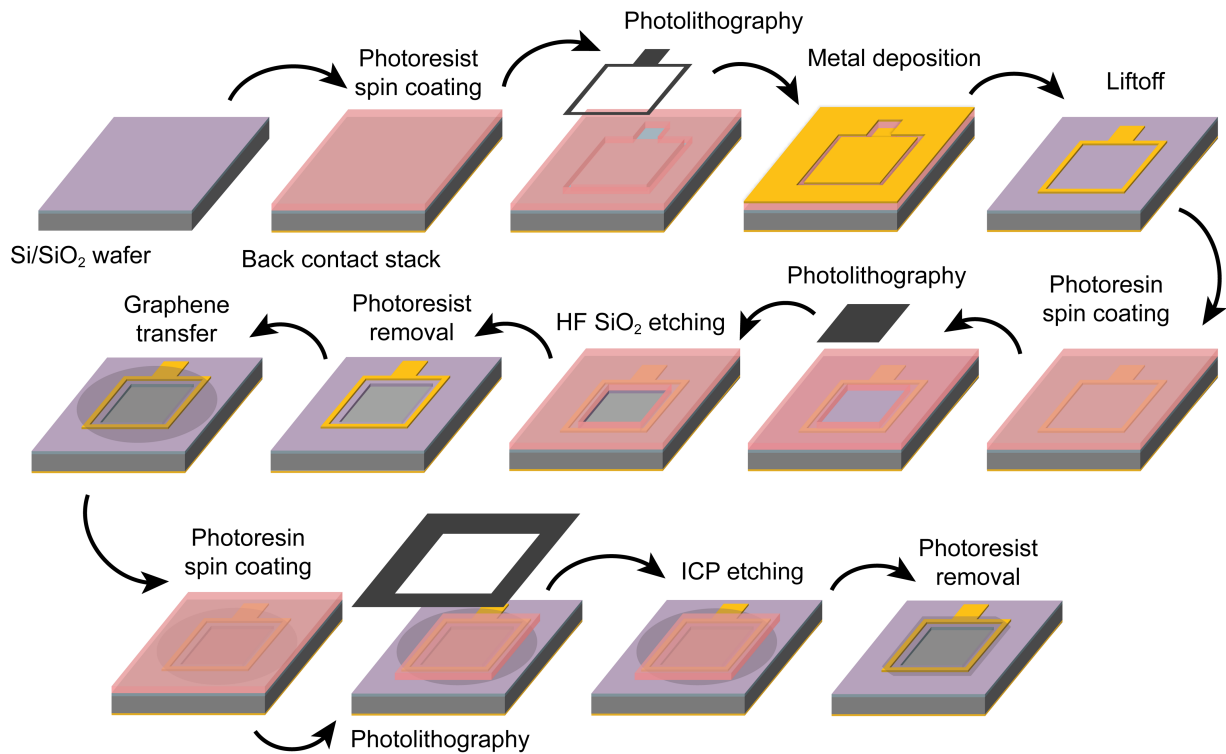
promising once fully optimized, will serve as base work for a future PhD research focused on graphene for transparent electrodes and solar cells, which is currently underway.

## 5.2. First Schottky solar cells

In order to explore new applications of graphene, a small line of work was set up to fabricate graphene/silicon Schottky solar cells using the expertise that the group had in both microfabrication and graphene technology. These devices would serve as a benchmark to test the effect of the different graphene processing steps in the performance of solar cell devices, and are integrated within the DIGRAFEN and REGRAP-2D projects. This study has been realized thanks to a close collaboration with CIEMAT, jointly processing and characterizing the devices.

Schottky solar cells (SSC) have been introduced in section 2.4.4. To quickly introduce these devices, they consist of a graphene layer deposited on top of a silicon window, forming a diode, a Schottky junction. A top contact shaped as a ring access the graphene layer, and a back contact is placed on the back side of the silicon wafer. Many elements affect the performance of these devices, the most critical ones being the quality and electrical properties of the graphene layer, and the interface between graphene and silicon.

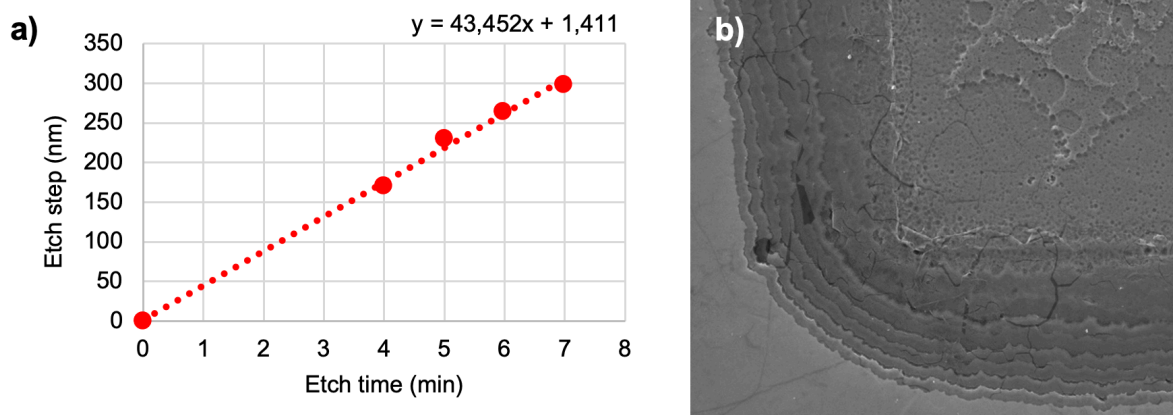
The general fabrication process for graphene/silicon SSCs is outlined in Figure 61, starting with a Si/SiO<sub>2</sub> wafer. First, the back contact is deposited, and the rest of the processing steps will keep to the front side. The front contact is then deposited through photolithography and lift-off, and a second lithography step defines the area for the silicon window. The window was opened using buffered hydrofluoric acid (BHF), a mixture of HF and NH<sub>4</sub>F in 1:10 ratio, to etch the SiO<sub>2</sub> layer. After that, the graphene layer is transferred on top of the window and metallic ring, immersing the sample in DIW as part of the transfer process. The time between the etching and the graphene transfer step was monitored, to fix the amount of native SiO<sub>2</sub> that grows on the etched window. The process leaves a very thin layer of SiO<sub>2</sub> on top of the opened silicon window. It is unavoidably grown natively by oxygen and water exposure, between the BHF etching and the graphene transfer. Once the graphene has been transferred, the graphene is patterned by photolithography and ICP etching. However, for the devices presented in this work, this step could not be completed due to equipment limitations, so the devices were isolated manually using a diamond tip.



**Figure 61:** Schematic drawing of the main processing steps for the fabrication of a graphene/silicon Schottky solar cell.

To gain some insight on the process' most critical steps, some initial studies were made on silicon oxide etching using BHF. The etching process is rather simple, immersing the wafer in the solution, moving slowly the sample to increase the access fresh BHF is enough. After some minutes, a clear change in the hydrophobicity of the opened window marks the completion of the etching process. This step was characterized using several dummy samples etched for different durations and measuring the step size with a profilometer. The SiO<sub>2</sub> thickness of the used wafers was 300 nm, and after 7 min, the silicon underneath was reached, as seen in Figure 62.

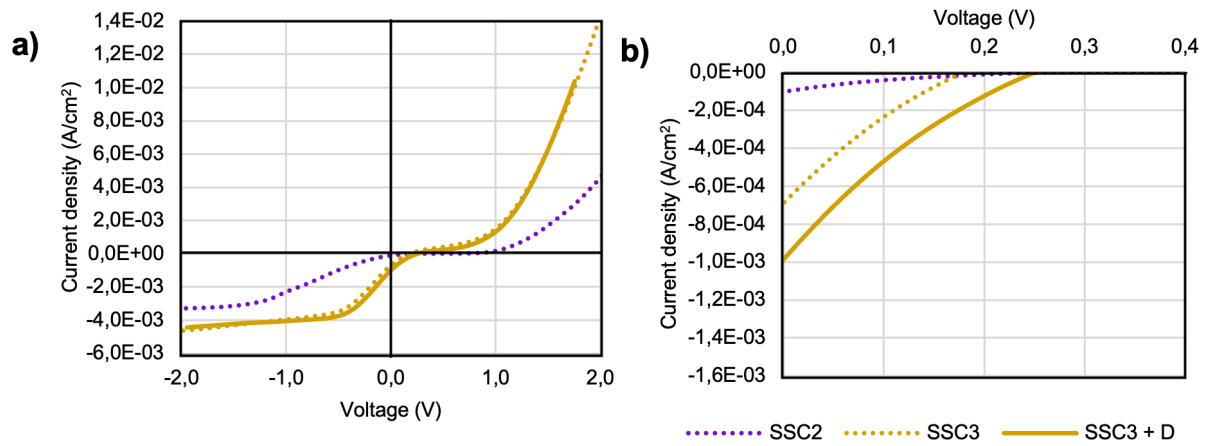
The etch rate was measured to be linear, around 43.5 nm/min, and once it was known, the first prototypes were produced. The first prototype, SSC1, failed, not producing the required diode in dark. For this device, the selected back contact was a Cr/Au stack, and the silicon wafer used had a rough, not polished back side, which was not standard for solar cell manufacturing. A second device, SSC2 was fabricated using the same back contact and silicon wafer, and its I-V characteristics under illumination were measured successfully and plotted in purple in Figure 63. With a  $J_{SC}$  of 84  $\mu\text{A}/\text{cm}^2$ , a  $V_{OC}$  of 0.285 and a fill factor of 0.15, the efficiency is almost negligible, pointing at wrong material choices or mistakes during processing.



**Figure 62:** (a) Thickness of the SiO<sub>2</sub> etched step with time. (b) SEM image of the etched edge of SSC2.

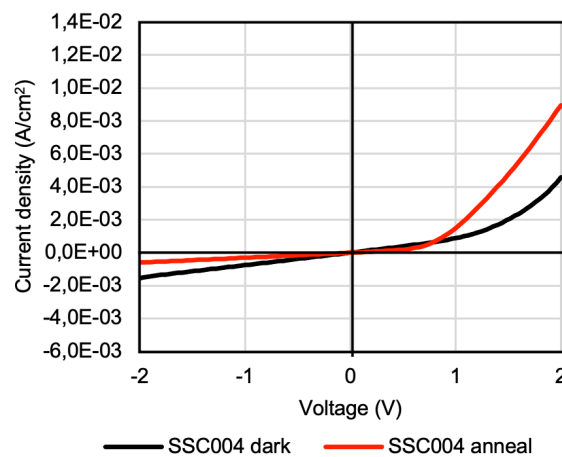
In order to achieve better performances, the back contact was modified. With the help of CIEMAT photovoltaics unit, a standard back-contact stack for silicon wafers was used, consisting of a thin layer of intrinsic amorphous silicon (a-Si), followed by a layer of n-type a-Si and finished with two metal layers of titanium to promote adhesion and gold for good electrical connexion. The rough n-type silicon wafer was kept, so the modification of the back-contact alone, improved greatly the behaviour of SSC3 as can be seen in Figure 63. In yellow (dotted line), the I-V curves under illumination of the as-fabricated SSC3 is shown, with an efficiency of 0.26% thanks to the improved  $J_{SC}$  up to 0.7 mA/cm<sup>2</sup>, although the  $V_{OC}$  is slightly reduced. The yellow line corresponds to the same sample, once it has been doped and protected with a thin PDMS film as explained in the previous section. Both  $J_{SC}$  and  $V_{OC}$  are clearly improved by the doping, reaching an efficiency of 0.475%.

However, the shape of the I-V curve is far from what is expected for a solar cell. This feature, which can be described as an S-shaped curve, has been previously described for many types of solar cells, where a mismatch between the absorber layer and the charge extraction layers is found. This means that the back contact stack needs to be further optimized, but the main issue lays in the graphene layer characteristics and doping level. Following these strategies, the S-shape can be fully mitigated [201]. Specifically, for Schottky solar cells, the shape can be corrected by a combination of annealing and doping [202].



**Figure 63:** I-V characterization under 1.5AM illumination of samples SSC2, SSC3 and SSC3 after doping. (a) I-V curve from -2 to 2 V. (b) Zoomed region from 0 to 0.4 V.

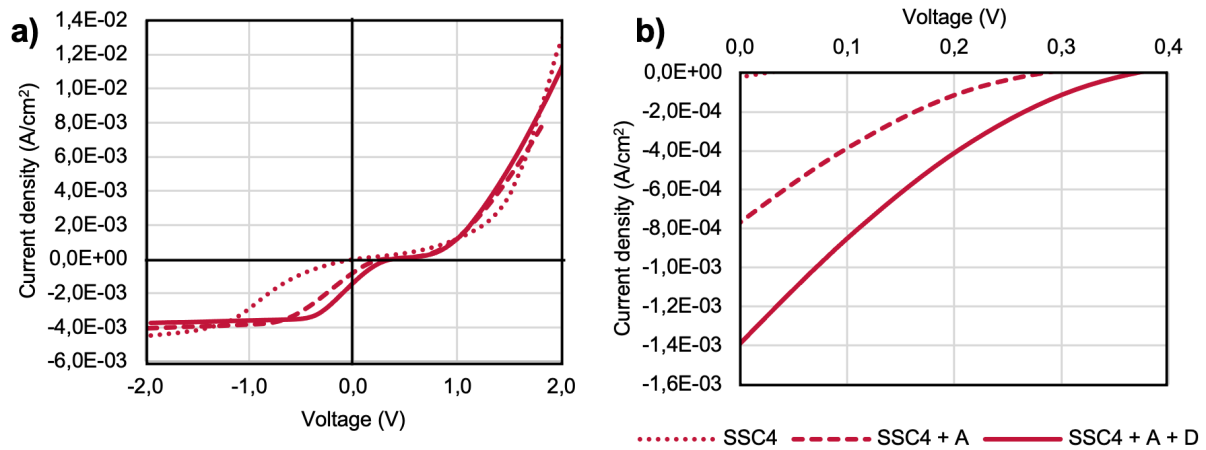
In Figure 64, the dark I-V characteristics of SSC4 are shown. SSC4 is a similar device as SSC3, using the same back contact stack and similar graphene, but applying an annealing step before the doping. Figure 64 shows in dashes the as-fabricated dark characteristics of the solar cell, and in dots the same device after being annealed for 2 min at 400°C in forming gas. The improvement of the dashed line is clear, with a much flatter shape at negative voltages, showing a promising diode behaviour before doping.



**Figure 64:** I-V characterization in dark of sample SSC4, before and after annealing.

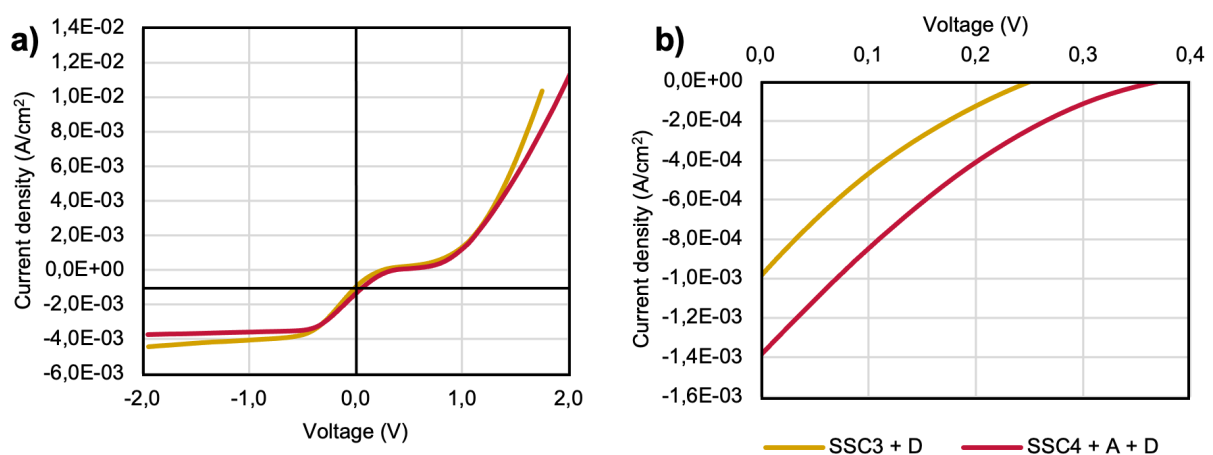
SSC4 was then doped using the same AuCl<sub>3</sub> recipe, and protected using a PDMS thin film. The I-V characteristics of all the stages of SSC4 are shown in Figure 65. The improvement achieved by the doping is noticeable, even more as the first measurement of SSC4 before annealing or doping barely produced any current. Once the sample as annealed, the characteristics improved to 0.77 mA/cm<sup>2</sup> and 0.29 V of J<sub>SC</sub>

and  $V_{OC}$  respectively, with a fill factor of 0.178 and an efficiency of 0.4%, similar to the value the doped SSC3 sample achieved. By doping, the characteristics improved even more, pushing both  $J_{SC}$  and  $V_{OC}$  to 1.39 mA/cm<sup>2</sup> and 0.378 V. This sample, while keeping the same fill factor of 0.178, reached an efficiency of 0.94%.



**Figure 65:** I-V characterization under AM1.5G illumination of samples SSC4, SSC4 after annealing and SSC 4 after annealing and doping. (a) I-V curve from -2 to 2 V. (b) Zoomed region from 0 to 0.4 V.

To finish the comparison, SCC3 and SSC4, both fabricated using the same materials and process, and both after doping, have been plotted in Figure 66. The difference between them is that SSC4 was annealed before doping. While the annealing step did not change abruptly the shape of the curve, it can be considered as a step in the right direction.



**Figure 66:** I-V characterization under AM1.5G illumination of samples SSC3 after doping and SSC4 after annealing and doping. I-V curve from -2 to 2 V. (b) Zoomed region from 0 to 0.4 V

ID	$J_{sc}$ (mA/cm <sup>2</sup> )	$V_{oc}$ (V)	FF	$\eta$	$R_{sheet}$ ( $\Omega/sq$ )	Info
SSC1	-	-	-	-	-	No diode
SSC2	0,08442	0,285	0.15	0.037%	-	BC: Cr/Au
SSC3	0,6994	0,182	0.206	0.26%	-	BC: a-Si (i) / a-Si (n) + Ti/Au
SSC3 + doping	0,9979	0,257	0.185	0.475%	-	BC: a-Si (i) / a-Si (n) + Ti/Au D: AuCl <sub>3</sub> 10mM NPs
SSC4	0,023	0,024	~ 0	~ 0 %	1360	BC: a-Si (i) / a-Si (n) + Ti/Au
SSC4 + annealing	0,77	0,29	0,178	0.40%	1250	BC: a-Si (i) / a-Si (n) + Ti/Au A: 400°C, 10 min in nidron
SSC4 + annealing + doping	1,39475	0,378	0,178	0,94%	977	BC: a-Si (i) / a-Si (n) + Ti/Au A: 400°C, 10 min in nidron D: AuCl <sub>3</sub> 10mM NPs

**Table 3:** Summary of electrical properties of the fabricated Schottky Solar Cells. BC: back contact; D: doping; A: annealing.

## 6. Conclusions and future work

In this thesis, two main areas of work have been considered. On one hand, the use of graphenic materials for energy storage in supercapacitors, specifically through the fabrication of laser induced graphene microsupercapacitors, complemented with pseudocapacitive elements. And on the other hand, the use of monolayer graphene in solar cells, studying its potential as a transparent electrode and integrated in graphene/silicon Schottky solar cells. For the first project, the results were successfully published in scientific journals, and for the latter one, the exploratory nature of the projects yielded promising results which served as a base for future projects within the group.

Regarding the energy storage area, the results have been published in several research papers. These include the evaluation of the main trends in the supercapacitor research field, identifying laser writing as a very promising technique to fabricate microsupercapacitors. In that study it was also shown that complementing those supercapacitors with metallic and bimetallic oxides and sulfides was the best approach to increase its energy density without compromising its power. Furthermore, the development of microsupercapacitors opens new applications as power sources on flexible and wearable electronics.

From there, laser writing technique was applied in the lab to fabricate laser induced graphene, which was optimized for its use in microsupercapacitors. Laser writing is proposed as a fast, flexible and accessible technique to fabricate high-quality, thin-film, 3D graphene networks. In that study, interdigitated microsupercapacitors with a capacitance of over 22 mF/cm<sup>2</sup> were fabricated, through thorough study of the material quality and microstructure of the LIG used. The performance of the fabricated devices, in capacitance, but also in energy and power density, is among the highest for a pure-carbon, EDLC supercapacitor made from LIG. Furthermore, higher voltage configurations using the optimized LIG material were produced, measured, and finally integrated with the electronics developed at CIEMAT.

Finally, during an international research stay, the addition of pseudocapacitive nanoparticles to the microsupercapacitors was tested, using MoS<sub>2</sub> nanoflakes to produce nanosized molybdenum oxides through laser irradiation. MoO<sub>2</sub> nanoparticles were produced on top of the LIG microsupercapacitors, which were measured using an ionic liquid electrolyte in an oxygen and humidity free atmosphere. This addition

increased the capacitance up to 35 mF/cm<sup>2</sup> at 0,04 mA/cm<sup>2</sup> and the energy density up to 25 μWh/cm<sup>2</sup> at the same current. These values are better than what could be expected theoretically by measuring the best bare LIG microsupercapacitor in ionic liquid. The study yielded promising results, which will guide future experiments.

Regarding the second area of this thesis, a first topic was dedicated to advancing general graphene technology. Chemical doping of graphene and its protection for better durability was studied, using AuCl<sub>3</sub> nanoparticles, which was confirmed to effectively dope the graphene, reaching improvements of the sheet resistance of more than 60%. An approach for protecting the doping using thin films of PDMS was tested, which partially kept the doping activity for more than 100 days. That technology was later applied to the fabrication of Schottky solar cells, which after several prototypes and the optimization of the most critical processing steps, an efficiency of 1% was reached. While the efficiency can still be improved, mostly through the optimization of the graphene quality and the doping, the establishment and validation of the processing steps serves as a starting point for future iterations.

## **6.1. Future prospects for graphene in energy storage**

One of the main topics worth to keep investigating after this thesis is the continued optimization of LIG material fabricated on flexible substrates. The LIG shown in this work as all fabricated on flexible polyimide films, which are strongly attached to solid glass support plates. This allowed for easy manipulation and less sample-to-sample variability; however it eliminated one of the main advantages of LIG, its flexibility. The mechanical properties of the substrate material and its effect on the electrochemical properties of the microsupercapacitors, including the effect of the electrolyte as structural support, are already being investigated. Two master thesis have been devoted to this topic at the ISOM-UPM laboratory, testing different methods to transfer the LIG material to other substrates such as PDMS, which are not only flexible, but also stretchable. With this, devices such as strain or bending sensors have been developed.

Another interesting topic is the fabrication of more compact microsupercapacitor stacks for higher voltage applications. Exploiting the use of thin polyimide substrates and avoiding the use of thicker support structures, high voltage stacks can be made in a much more compact way, allowing to increase the current rating of the fabricated devices. It is also possible to explore the use of larger polyimide substrates to connect in parallel the devices in an integrated way using LIG as well.

As a continuation of the work in complementing the LIG material with pseudocapacitive elements, a priority would be to finish the MoS<sub>2</sub> experiment to obtain stronger conclusions, fabricating more samples to account for sample variability and molybdenum mass loading. Understanding the role of the size and shape of the precursor MoS<sub>2</sub> nanoparticles in the transformed molybdenum oxides and their redox pseudocapacitance is an interesting topic. In the same area, other nanostructured pseudocapacitive materials can also be proposed to complement graphene supercapacitors.

Finally, a topic which was proposed before, is to explore the potential of LIG to fabricate other devices such as heaters or sensors, which could be integrated in the same polymer substrate for flexible and wearable electronics.

## **6.2. Future prospects for graphene for solar cells**

In the area of solar cells and transparent electrodes based on graphene, a first topic would be the exploration of different dopants for improving the electrical properties of graphene and its applications as a transparent electrode. These dopants should be effective, have good stability in ambient conditions and not interfere with graphene's optical properties. Silver nanowires are one of the most promising ones, bridging the graphene grains and adding a flexible network improving conductivity and doping the graphene. This experiment has already started at the group.

If still the dopants need to be protected, the development of a protection strategy using multi-layered polymeric films is expected to improve the actual level of protection. This way, the thin films would block even better the oxygen and humidity, using as a base the PDMS thin film process presented in this thesis. On top of that, a different strategy would be to nanostructure the encapsulating PDMS film, using nanoimprint lithography or other techniques. This way the protecting layers would become multifunctional, acting as an antireflective coating too and improving the solar cell characteristics.

Within the topic of Schottky solar cells, the use of other 2D materials such as MoS<sub>2</sub> as an interlayer between the graphene and the silicon is to be explored, benefiting the charge separation and avoiding recombination by passivating the interface. Furthermore, a modification of the automatic graphene transfer process can be proposed so it works faster at depositing two graphene layers. On a different approach, as the transfer process now is based on the immersion of the target substrate,

dopants that can survive the process are needed. If this cannot be established, a dry transfer process of the graphene layers can be proposed.

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solar cells," *J Mater Chem A Mater*, vol. 5, no. 35, pp. 18716–18724, 2017, doi: 10.1039/C7TA05481E.

## Annexes

### A. Publications

- Velasco, Y. K. Ryu, A. Boscá, A. Ladrón-de-Guevara, E. Hunt, J. Zuo, J. Pedrós, F. Calle and J. Martínez, "Recent trends in graphene supercapacitors: From large area to microsupercapacitors," *Sustain Energy Fuels*, vol. 5, no. 5, pp. 1235–1254, 2021.
  - Selected as front cover for volume 5, issue 5 (2021)
  - Highly cited article certificate from the Royal Society of Chemistry (top 5% in 2022)
- Velasco, Y. K. Ryu, A. Hamada, A. de Andrés, F. Calle and J. Martínez, "Laser-induced graphene microsupercapacitors: structure, quality and performance" *Nanomaterials*, vol. 13, no. 5, pp. 788, 2023.
- M. Belén Gómez-Mancebo, R. Fernández-Martínez, A. Ruiz-Perona, V. Rubio, P. Bastante, F. García-Pérez, F. Borlaf, M. Sánchez, A. Hamada, A. Velasco, Y. K. Ryu, F. Calle, L. J. Bonales, A. J. Quejido, J. Martínez and I. Rucandio, "Comparison of Thermal and Laser-Reduced Graphene Oxide Production for Energy Storage Applications" *Nanomaterials*, vol. 13, no. 8, pp 1391, 2023.
- H. Bukovska, F. García-Perez, N. Brea, L. J. Bonales, A. Velasco, M. A. Clavero, J. Martínez, A. J. Quejido, I. Rucandio and M.B. Gómez-Mancebo, "Evaluation and Optimization of Tour Method for Synthesis of Graphite Oxide with High Specific Surface Area" *C*, vol. 9, no. 3, pp. 65, 2023.
  - Selected as front cover of Volume 9, Issue 3 (2023)

#### Future publications

- Hamada, Y. K. Ryu, A. Velasco, M. B. Gómez-Mancebo, F. Calle and J. Martinez. "Double Pass Effect on Laser Induced Graphene Microsupercapacitors" Manuscript to be submitted to *Applied Surface Science*. (under preparation)
- Martínez, Y. K. Ryu, S. Tarancón, E. Tejada, A. Hamada, A. Velasco and J. Martínez. "Laser Induced Graphene Strain Sensors for Body Movement Monitoring" Manuscript submitted to *ACS Omega*.

## B. Scientific conferences

- Spanish conference of Electron Devices, CDE 2021, Sevilla (online format). Poster presentation “Towards a hybrid Graphene device for green energy”.
- Spanish conference of Electron Devices, CDE 2023, Valencia. Oral presentation “Exploring recent trends in graphene supercapacitors”
- Graphene conference, 2023, Manchester, UK. Poster presentation “Laser-Induced Graphene Microsupercapacitors: exploring its structure, quality and performance”

## C. Final degree projects

- Elijah L. Hunt, “Laser Induced Graphene Micro-supercapacitors: The Effectiveness of Electrolytes for Energy Storage”. Master thesis for the completion of the Master in Materials Engineering (ETSICCP, UPM) directed by Dr. Javier Martínez and Andrés Velasco.
- Manuel Guillermo Altava Sanz “Diseño e implementación de un banco de medias conectado e interoperable basado en Arduino” Bachelor thesis for the completion of the “Grado en Ingeniería de Tecnologías y Servicios de la Comunicación” (ETSIT, UPM) directed by Andrés Velasco and endorsed by Dr. Alberto Boscá.

## D. Research projects

- Dispositivos de Grafeno para la mejora de las energías renovables, DIGRAFEN. MINECO (in col. with CIEMAT), 2018-2020. ENE2017-88065-C2-2-R
- Graphenic and 2D materials for Solar Cells and Renewable Energy Storage Devices, REGRAP-2D. MICINN (in col. with CIEMAT), 2021-2024. PID2020-114234RB-C21
- New 2D materials: Characterization, properties and applications, NMAT-2D. CM P2018/NMT-4511 (in col. with LabCOA - IMDEA Nano, Department of Condensed Matter Physics - UAM, CSIC ICMN, FIDAMC). 2019-2023.

- Plan complementario Materiales Avanzados: 2D Materials. MICIN y CM, 2022-25.

## E. Divuligation activities

- Semana de la Ciencia 2020. Presentación “El grafeno y su papel en los retos energéticos del futuro” (online).
- XI Noche Europea de los Investigadores 2020: Compromiso #UPM2030: tecnología para alcanzar los ODS. Presentación “El grafeno y su papel en los retos energéticos del futuro” (online).
- Semana de la Ciencia 2021. Actividad presencial “Masterchef Sostenible ¡Crea una fuente de energía verde gracias al grafeno!”.
- XII Noche Europea de los Investigadores 2021: Tecnología en acción para un mundo más verde y sostenible. Actividad presencial “Masterchef Sostenible ¡Crea una fuente de energía verde gracias al grafeno!”.
- Día Internacional de la mujer y la niña en la ciencia 2022. “From Argelia to Madrid: our PhD travel discovering graphene for a sustainable world”.
- XI Feria Madrid es Ciencia 2022. “Grafeno para un mundo más sostenible”.
- #UPMday 2022 como parte del equipo del ISOM-UPM.
- Ateneo de Madrid, ciclo de conferencias de la Sección de Medio Ambiente, 2022. “Nanotecnología para la sociedad. Energía con grafeno: verde, eficiente y barata”.
- XII Noche Europea de los Investigadores 2022: Tecnología en acción para un mundo más verde y sostenible. Actividad presencial “Masterchef Sostenible ¡Crea una fuente de energía verde gracias al grafeno!”.
- Semana de la Ciencia 2022. Actividad presencial “Masterchef sostenible DELUXE: energía verde con grafeno...y ahora: flexible!”.
- Noche Europea de los Investigadores 2023. “Diálogo, Kahoot y taller sobre nanotecnología y futuro: energía sostenible y estructuras cuánticas”.
- Semana de la Ciencia 2023. “Diálogo, Kahoot y taller sobre nanotecnología y futuro: energía sostenible y estructuras cuánticas”.