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Preliminary Results of a 65-nm CMOS Free-running Oscillator Emitter With Tunable Radiation from 280 GHz to 292 GHz

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***Abstract*—We report on a submillimeter-wave radiating source integrated in 65-nm CMOS technology. The source is based on a free-running differential oscillator which radiates the second harmonic of the oscillation frequency through an on-chip integrated folded-slot antenna. The chip was wire-bonded and combined with a silicon lens for backside radiation. Preliminary measurements yield tunable radiation frequency from 280.1 GHz to 291.6 GHz, with peak radiated power of -8.2 dBm for one of the measured samples. Great repeatability is observed between different samples in terms of the oscillation frequency.**

I. INTRODUCTION

TERAHERTZ technology has seen great promise in applications such as radar, spectroscopy, imaging, and communications [1]. Nevertheless, there is still a lack of affordable room-temperature sources for effective signal generation. With the increasing miniaturization of silicon transistors, their cutoff frequency (f_T) now surpasses the millimeter-wave regime. Thus, it has become realistic to build terahertz and millimeter-wave circuits implemented in CMOS or other high-yield mainstream silicon technologies [2]. Moreover, since the cutoff wavelength ($\lambda_T = c/f_T$) of integrated silicon transistors is now smaller than the size of the dies, distributed passive structures and antennas can be combined in the same die as high-frequency transistors, thus avoiding lossy electrical interfaces at high-frequency [2].

The following text reports on the electromagnetic design of a 300 GHz on-chip radiator implemented in 65-nm CMOS technology from TSMC foundry. Since the maximum oscillation frequency of the used technology is below the target frequency, the desired radiation arises from the second harmonic of the oscillation frequency. Hence, the main challenge is to achieve efficient radiation of this harmonic component out of the chip without affecting fundamental oscillation activity.

II. ELECTROMAGNETIC DESIGN

Fig. 1a depicts the proposed CMOS radiation source consisting of a pair of separate self-feeding oscillators coupled differentially by a central slotline. The used oscillator topology has been previously demonstrated in SiGe BiCMOS technology showing state-of-the-art performance in terms of output radiation [3],[4]. For this topology, it has been shown that harmonic radiation is maximum if (a) optimum complex voltage gain is achieved between gate and drain, (b) gate and drain are isolated for the second harmonic, and (c) second harmonic radiation occurs near the transistors [4].

The NMOS transistors in Fig. 1a were chosen with 14 fingers each, 1.22 um width per finger, and channel length of 60 nm. The positive feedback path to achieve close-to-optimum complex gain has total electrical length of 81° at 150 GHz and it is realized using a 56 Ω microstrip line. The central slotline ensures that both fundamental oscillation signals (at f_0) couple differentially (Fig. 1b). Thus, the second harmonic signals (at $2 \cdot f_0$) generate in common mode and cannot propagate through the central slotline (Fig. 1c) [3]. The second harmonic drain content gets radiated from the upper slotline, which is bent in the shape of a folded slot antenna that resonates approximately at $2 \cdot f_0$. The dipole is slightly offset from the antenna center for improved matching. This antenna directs most power towards the substrate, but it requires an additional dielectric lens to suppress substrate-wave propagation [2],[5].

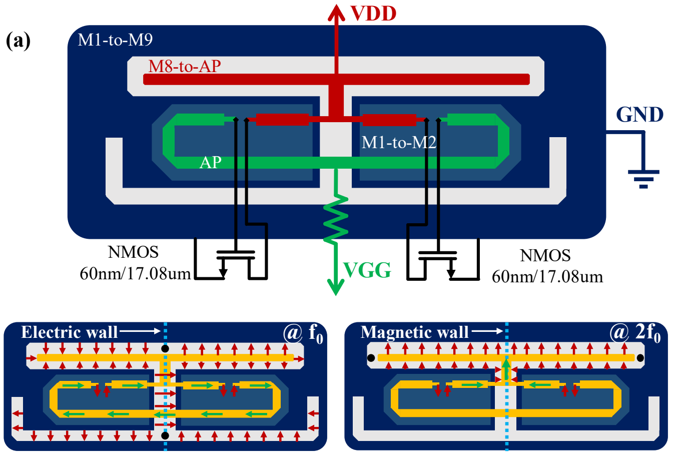

Fig. 1. Topology and operation principle of the emitter: (a) layout of the proposed emitter with details on the transistor connections and the used metal layers (M1 to M9, and AP) of the CMOS stack, (b) electric field (red arrows) and current (green arrows) propagation through the proposed emitter at the oscillation frequency (f_0), and (c) at the second harmonic ($2 \cdot f_0$ = radiation frequency). Black dots indicate virtual nulls of electric field.

Nonlinear transistor behavior was simulated from the standard transistor models provided by TSMC foundry, while the high-frequency performance of the passive electromagnetic structures was simulated using the finite element method embedded in Ansys HFSS 3D electromagnetic solver. To account for substrate-wave reduction by the lens, in simulation, the structure was placed in between air-silicon semi-infinite spaces [5]. Joint optimization of passives and transistors was carried out at the Keysight ADS environment.

Simulated radiation frequency and power at second harmonic are depicted in Fig. 2. The shown power accounts for radiation efficiency loss inside the silicon substrate of the chip, and the ~30% power reflected at the lens-to-air interface of a hyper-hemispherical silicon lens attached to the backside of the chip [5]. The emitter is expected to achieve output power from the lens of -26 dBm at 300 GHz.

It is worth mentioning that the proposed emitter is fully compliant with all design rules of the used CMOS technology. To enforce metal density rules, most distributed passives of the system are built as slot structures (*e.g.*, slotline, slot antenna), with all available metal layers of the process shunted to form

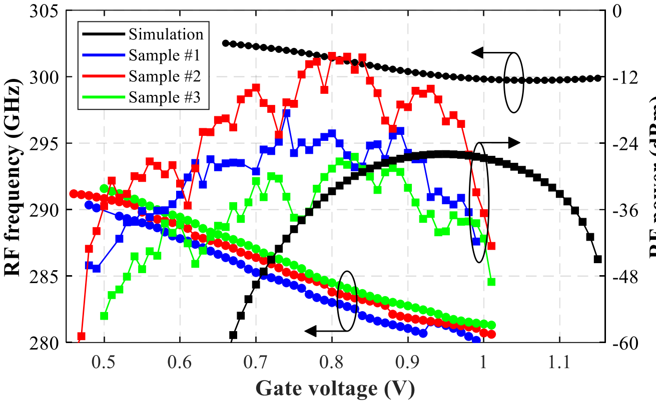

Fig. 2. Measured and simulated radiated power and frequency at $2 \cdot f_0$, as a function of gate voltage, for several samples of the CMOS-integrated emitter prototype. Drain voltage is fixed at 1.2 V. The measured power values are integrated in an 8 MHz resolution bandwidth, and the losses of the measurement system are de-embedded. Simulated data points are not post-fitted in any manner.

the common electromagnetic ground plane of the circuit (Fig. 1a). DC biasing is applied through the symmetry plane of the structure to avoid disturbance of fundamental frequency operation (note the electric wall in Fig. 1b).

III. PRELIMINARY MEASUREMENTS

The chips were wire-bonded to a custom PCB and backed by a hyper-hemispherical silicon lens for characterization. The optical measurement setup is shown in Fig. 3: we used two TPX lenses in telescope configuration for focusing the beam onto the phase center of a WR3.4 horn. The radiofrequency (RF) signals were downconverted using a subharmonic mixer (SHM) from RPG and they were read at intermediate frequency (IF) in a spectrum analyzer. Due to the low power radiated from the prototypes at $2 \cdot f_0$, the power measurements were also acquired with the spectrum analyzer. All the measurements presented in the following are corrected by calibrated attenuation of the TPX lenses, the horn, the SHM, and the IF cables.

Fig. 2 shows the measured frequency tuning capabilities of the proposed design for three different die samples. It is easy to observe that the operation biasing point of the oscillators has shifted, which shall be considered to adjust the model of following prototypes. One may observe that the frequency response is quite linear, with great chip-to-chip repeatability. The maximum measured frequency is 291.6 GHz, which is only 3.6% offset from the peak radiation frequency in simulation. The lock frequency range extends beyond 10 GHz for all the shown samples, which is wider than expected from simulation.

Fig. 2 also shows the measured power at $2 \cdot f_0$. Due to the calibration procedure of the setup, there are some uncertainties in the absolute power values shown in the plot. Still, sample-to-sample results are fully comparable. The peak measured power is achieved at a gate voltage close to 0.8 V for all the samples, in contrast to the 0.95 V optimum bias in simulation. In terms of the output power at second harmonic, the differences between samples are greater than 10 dB at some tuning voltage values. This large variation might originate from the delicate manual procedure used to assemble each sample. Sample #2 presents the highest measured RF power of -8.2 dBm. For this sample, the DC-to-$2 \cdot f_0$ conversion efficiency reaches 1.04%.

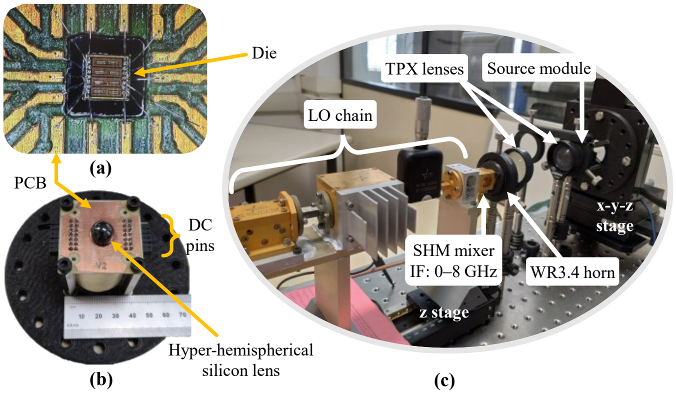

Fig. 3. Measurement setup: (a) through-microscope photograph of a die sample wire-bonded to the PCB, (b) photograph of the backside of the PCB attached to a hyper-hemispherical silicon lens, and (c) photograph of the optical setup used to characterize the emitters. The subharmonic mixer (SHM) uses a local oscillator (LO) frequency of (RF+IF)/2.

IV. CONCLUSION

We have presented the preliminary results of a CMOS-integrated source based on a pair of differentially coupled oscillators. The proposed prototype circuit is fully compliant with all design rules of industrial silicon fabrication technology. Several emitter samples of the same circuit have been characterized and the preliminary results show great repeatability between samples in terms of frequency, but not in terms of output radiated power. The samples deliver stable oscillation from 280.1 GHz to 291.6 GHz. The peak measured power is -8.2 dBm for one of the samples, which is 5.5 dB lower than reported state-of-the-art of unitary free-running oscillators built using this technology [6].

These initial results shall be further analyzed to correct the models used in the design stage, with special focus on the reason why peak oscillation activity occurs at a different biasing point than in simulation. Future work will address on-chip and off-chip synchronization strategies of several emitters to build a high-power radiating array of coupled oscillators.

V. ACKNOWLEDGEMENT

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