A Highly Power- and Area-Efficient PMU for Cell-Size Autonomous Microsystems

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***Abstract*— Power Management Units (PMU) are present in most electronic devices today. However, for power and area constrained applications, their design becomes a real challenge, especially when cell-sized autonomous microsystems are targeted. This paper presents an LDO regulator and a voltage reference, which are usually a must in any PMU, for autonomous microsystems fabricated in 65 nm CMOS technology. This PMU has been designed to minimize quiescent power and area, consuming a minimum power of 15.6 nW and occupying only 391 μm^2, while being able to deliver up to 40 μA to the load. No significant degradation was observed, as the measured line regulation is 0.173%/V, the temperature coefficient is 128.4 ppm/°C over a very wide temperature range going from 0 °C up to 120 °C, and the PSR at low frequencies is −67.1 dB.**

***Index Terms*— LDO, voltage reference, PMU, low power, low area.**

I. Introduction

With the growing need for wireless sensing nodes for applications such as the Internet of Things (IoT), *Smart Dust* [1] has gained considerable interest in recent years [2], [3], [4]. It has emerged as a very promising branch of research that attempts to take advantage of a drastic size and power reduction to enable the development of very tiny autonomous microsystems. These ultra-small electronic particles are conceived to be able to enter spaces currently inaccessible to electronics and enable new applications. For example, they would be small enough to interact with individual biological cells, potentially be carried by the wind, or be embedded into quotidian things like paint and thread to make fabrics that would be useful for creating large sensing networks on almost any surface. Some remarkable progress has already been made in this area. For instance, the study in [5] presented an autonomous microsystem designed for implantation in the human eye to detect glaucoma. Another work [6] developed an electronic microparticle to record neural activity in animals *in vivo* while causing minimal tissue damage.

These microsystems are typically powered by ambient energy through an energy harvester. Since the collected energy is extremely small for such small device volumes, a power-limited design is required. At the same time, the energy supplied by the harvester tends to fluctuate considerably, depending not only on the environmental conditions but also on the operating point of the circuit, making it impossible to feed this energy directly to the electronics' core. Instead, a power management unit (PMU) is always required. The PMU is the subsystem responsible for managing the power coming from any available power source to make it stable and usable for the core circuit. Its complexity in autonomous microsystems varies with the application needs, but low-dropout regulators (LDOs) and voltage references are always required to produce stable voltages and currents.

If the intended application involves a temperature-changing environment, the need for a temperature-compensated design over a wide temperature range is added to this area- and power-constrained scenario. As a result, the design becomes challenging as there are not too many PMUs that meet these requirements with solvency. Most of the temperature-compensated designs use bandgap references, which consume too much area and power for the restricted budget mentioned above. Some CMOS-only voltage references provide excellent results regarding temperature variation and power requirements [7], [8], [9]. However, when cell-sized microsystems are aimed, they are still far from satisfying the area constraint, as they still require the addition of a regulator to supply power.

In our target scenario, the second generation of *SynCells* [4], both area and power are extremely limited. The *SynCells* are autonomous microsystems developed at MIT to demonstrate microscale sensing capabilities. The second generation of *SynCells* consists of two GaN solar cells for energy harvesting, a MoS_2 based sensor, a GaN LED for optical communication and a CMOS *Si*-chip that regulates the power generated by the solar cells and drives the LED. In this way, the information captured by the sensor is transmitted to the outside world through light pulses of varying frequency generated by a voltage-controlled oscillator (VCO). This microsystem imposes the following requirements on the PMU:

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- The CMOS *Si*-chip must integrate several building blocks, such as a PMU, a VCO and an LED driver, on a $50 \times 50\ \mu m^2$ die. Therefore, ultra-low area designs are required.
- The design needs to be stable with temperature as it will be used in environments ranging from *in vitro* to outdoor applications [10].
- The MoS_2 based sensor is the component of the microsystem that draws the most power from the PMU. The rest of the system has a power consumption that can be neglected in comparison. This chemical sensor has a nominal resistance of approximately 5 MΩ and it is expected to experience a $\sim$100$\times$ decrease in its resistance after chemical exposure. Consequently, the PMU must be able to deliver at least $\sim$20 μW of regulated power.
- The PMU must deliver power to the load with high efficiency, which leads to low-quiescent current designs.
- The sensor takes a few minutes to complete the conductivity change after chemical exposure, and several hours to return to its initial state. This causes smooth load changes in the PMU allowing this design to have more relaxed transient response requirements.
- The VCO of the system operates within the range of 30 to 80 Hz. Therefore, achieving a good power supply rejection (PSR) in the PMU at low frequencies is desirable.

In this work we present a PMU composed of an LDO regulator and a voltage reference with ultra-low die area and quiescent power consumption, without any significant degradation in important features such as the line regulation, the temperature coefficient (TC), or the power supply rejection (PSR), making this design very suitable for autonomous microsystems applications. To the best of our knowledge, there is no other work that simultaneously addresses the design of a regulator and a voltage reference with such reduced area and power requirements.

The paper is organized as follows. First, Section II presents an overall description of the proposed PMU. Then, section III provides further design considerations. It starts with an explanation of the temperature compensation of the voltage reference, which is done in III-A. Section III concludes with a more detailed description of the regulator design in III-B. Finally, the experimental results are presented and discussed in section IV, and some conclusions are drawn in Section V.

II. Proposed Structure

Most PMUs include a voltage reference and an LDO that follow a connection scheme similar to that shown in Fig. 1a. In this structure, the reference voltage is generated by an independent section, V_{ref}, and is used to establish the value of the output voltage. However, we propose a structure in which the voltage reference is embedded in the feedback loop of the regulator around the error amplifier (EA), as shown in Fig. 1b, with the purposes detailed next.

The main upside of this alternative is that the voltage reference takes advantage of the regulator's open loop gain through the feedback loop, to enhance parameters such as the line regulation or the PSR, while, at the same time, the LDO can deliver regulated power to the core of the microsystem.

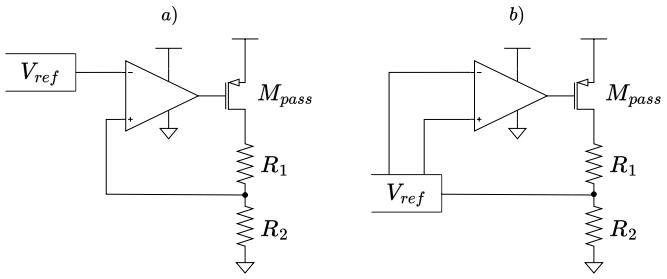

Fig. 1. Conceptual scheme of a) a typical LDO with a voltage reference, b) an LDO with a voltage reference integrated into its feedback loop.

As a result, the die area of the PMU is significantly optimized. In fact, this design occupies an area of the same order of the smallest reported voltage references [7], [11], [12], to generate not only a bias voltage but also a stable voltage supply to power the core of the microsystem. Unlike this design, none of the smallest voltage references reported to date can act as a power supply even for low-current demanding systems.

To implement this structure, the first step is to find an invariant potential from which to build the reference. The bandgap potential, based on BJT junctions, is one of the most common solutions. However, BJTs fabricated in CMOS processes generally lack accuracy and require relatively high bias currents, compared to MOS transistors, to avoid large process variations [13], [14]. At the same time, most bandgaps references, and especially recent efforts to achieve low power designs [15], [16], include large resistors. Consequently, there is a very difficult variability-power-area trade-off that makes their use for tiny autonomous microsystems really difficult, as they usually end up requiring too much area and power [17] for what these microsystems can afford.

A widely employed alternative to address the above issues is the threshold voltage potential [12], which provides good supply insensitivity and a well-documented response to the temperature [18], [19], [20]. Additionally, unlike bandgap references, it allows a relatively easy way to generate low-voltage designs, which is beneficial for our target application. For all of these reasons, the voltage reference of this work was set to rely on the threshold potential.

The simplified schematic of the proposed PMU is shown in Fig. 2. The voltage reference block is based on the threshold voltage difference between an HVT MOSFET (M_1) and a regular MOSFET (M_2). This reference can be realized with as few as four transistors, making it very suitable for area-constrained applications. To explain the voltage reference principle of operation, let's first point out that the transistors $M_{3,4}$ work as current sources with the same bias voltage, so they both supply the same current to transistors M_1 and M_2. On the other hand, the regulator, due to its high open-loop gain and negative feedback, equals the voltages at the sources of both M_1 and M_2. Consequently, in order for these two transistors to draw the same current, the output stage of the LDO is forced, through the feedback network, to apply a voltage at the gate of M_2, V_{ref}, that compensates for the difference in threshold voltages between M_1 and M_2. Finally, the output voltage generated by the proposed circuit can

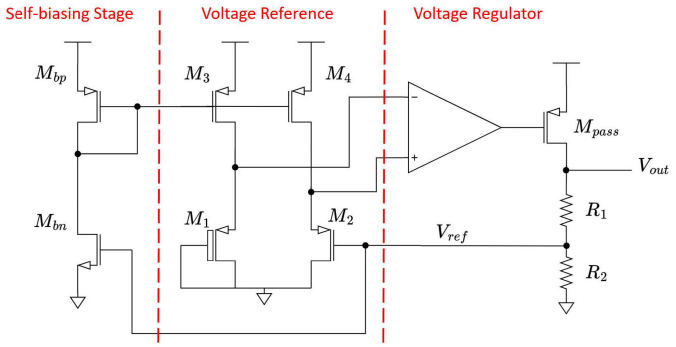

Fig. 2. PMU simplified schematic.

be expressed by:

$$V_{out} = V_{ref}\frac{R_1 + R_2}{R_2} \tag{1}$$

At the same time, to make this design low power, every transistor is set to work in the deep subthreshold regime where the drain current of a transistor is governed by:

$$I_{DS} = I_0\frac{W}{L}e^{\frac{q(V_{GS}-V_{TH})}{nK_bT}} \tag{2}$$

where I_0 is the scale current, V_{TH} is the threshold voltage, n is a fitting parameter, q is the the electron charge, K_b is the Boltzmann constant, and T the temperature. Current I_0 is described by the following equation:

$$I_0 = \mu\sqrt{\frac{q\varepsilon_{s_i}N}{2\phi_s}}(\frac{K_bT}{q})^2 \tag{3}$$

where N is the doping concentration, ϕ_s represents the surface potential and ε_{s_i} is the relative electrical permittivity of the silicon.

Assuming the negative feedback is strong enough, we can equal the currents flowing through transistors M_1 and M_2, I_{DS1} and I_{DS2}, as well as voltages V_{S1} and V_{S2}, and resolve the equation for V_{G2} (V_{ref}) giving as a result:

$$V_{ref} = \frac{n_2}{n_1}|V_{TH1}| - |V_{TH2}| - \frac{n_2K_bT}{q}ln\frac{I_{01}W_1L_2}{I_{02}W_2L_1} + V_S(1-\frac{n_2}{n_1}) \tag{4}$$

where the voltage V_S can be obtained from (2):

$$V_S = |V_{TH1}| + \frac{n_1K_bT}{q}ln\frac{I_{DS}}{I_{01}} \tag{5}$$

It can be observed that the voltage V_S introduces a dependency on the bias current I_{DS}. However, since n_1 and n_2 are very similar in (4), the dependency is small.

Note that for simplicity, no second-order effects were included in the equations, although they were considered in the design. In particular, the cascoding technique was used in the current sources of the voltage reference, as will be shown later, to attenuate the channel length modulation effect. Otherwise, the regulation of the supply voltage, among other parameters, would suffer a significant degradation. For the same reason, the entire design is self-biased to reduce the supply sensitivity of the circuit as much as possible. This not only results in a significant improvement in line regulation and the PSR at low frequencies, but also saves significant die area by eliminating the need of additional biasing or startup circuitry to achieve a stable operating point.

III. Design Considerations

A. Temperature Compensation

Developing a temperature-stable design becomes crucial when considering outdoor applications or any other scenario where there is significant temperature variation. Since it is implicit in the nature of transistors to vary their operating conditions with the temperature, preventive measures must be taken into account in the design. There are two conventional approaches, as explained in [21], to perform a temperature-compensated design. The first method is to add two terms with complementary temperature coefficients. The second method is based on multiplying two terms with complementary temperature coefficients. In this work, both methods are used because in view of the nature of (4).

To simplify the explanation of the temperature behavior of the voltage reference let's first assume that the slope parameters of the transistors M_1 and M_2 in Fig. 2 are equal, i.e., $n_1 = n_2 = n$, which in reality, for the technology and the transistors used in this case, does not carry a significant error as long as weak inversion saturation ($V_{DS} \geq 4\frac{K_bT}{q}$) is granted [22]. In this case then (4) is simplified as follows:

$$V_{ref} = |V_{TH1}| - |V_{TH2}| + Q \tag{6}$$

where:

$$Q = -\frac{nK_bT}{q}ln\frac{I_{01}W_1L_2}{I_{02}W_2L_1} \tag{7}$$

It is well known that the threshold voltage has a significant negative temperature coefficient [18]. According to the BSIM 4.5 simulation model, the behavior of the threshold voltage versus temperature is modeled by the following equation:

$$V_{TH} = V_{TH0} + K\left(\frac{T}{T_0} - 1\right) \tag{8}$$

where V_{TH0} is the threshold voltage at the nominal temperature T_0 and K is the temperature coefficient for the threshold voltage. Consequently, if V_{TH1} and V_{TH2} are subtracted, as in (6), their temperature dependence relies only on the difference of the temperature coefficients:

$$\frac{\partial(V_{TH1} - V_{TH2})}{\partial T} = \frac{K_1 - K_2}{T_0} \tag{9}$$

Since these two coefficients K_1 and K_2, are very similar to each other, some temperature compensation is already provided, as shown by the blue line in Fig. 3 extracted from simulations.

A major improvement in the temperature compensation can be achieved by carefully designing the remaining term in (6), Q. The expression of Q can be split into the product of $-\frac{nK_bT}{q}$, which is clearly a CTAT term with a fixed slope, and $ln\frac{I_{01}W_1L_2}{I_{02}W_2L_1}$, which shows a PTAT behavior with a variable slope. The reason behind this PTAT response is a more pronounced degradation in the mobility of transistor M_2 relative to that of

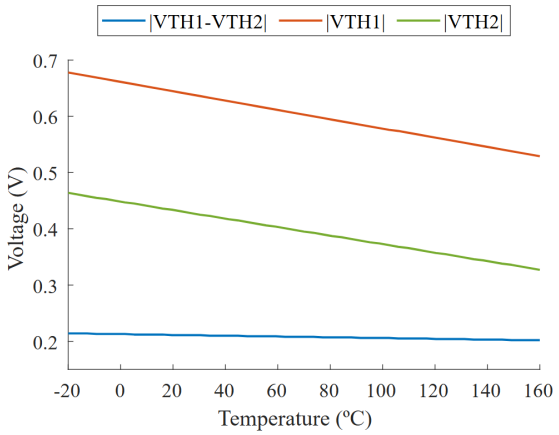

Fig. 3. Simulation of the threshold voltages behavior vs. temperature.

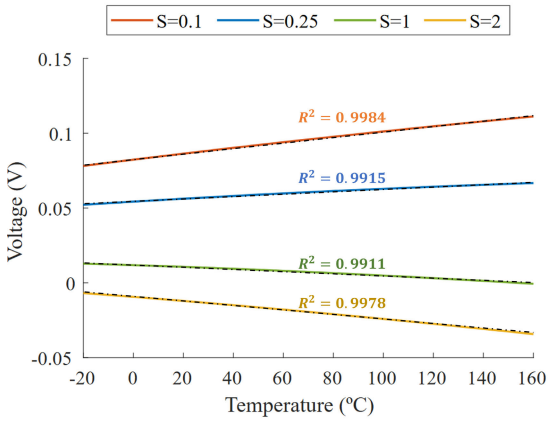

Fig. 4. Q vs. temperature for different values of S.

M_1 in the I_{02} and I_{01} terms with increasing temperature. Since the PTAT term is adjustable, it can be set to a value where the overall slope of Q cancels to some degree the temperature coefficient provided by the threshold voltage difference.

As mentioned before, I_0 is modeled by (3), where the carrier mobility μ, the thermal voltage $\frac{K_bT}{q}$ and the surface potential ϕ_s, which is modeled by (10), are the only temperature-dependent terms. However, when dividing $\frac{I_{01}}{I_{02}}$, the dependence of the surface potential temperature and the thermal voltages cancel each other out, and the only temperature contribution comes from the mobility ratios $\frac{\mu_1}{\mu_2}$.

$$\phi_s = \frac{K_bT}{q} ln \frac{N}{n_i} \tag{10}$$

In a first-order approach, the temperature behavior of the mobility can be modeled by:

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^m \tag{11}$$

If we combine (3) and (11), the expression in (7) can be rewritten as:

$$Q = -\frac{nK_bT}{q} ln \left(S \frac{\mu_{01}(\frac{T}{T_0})^{m_1}}{\mu_{02}(\frac{T}{T_0})^{m_2}} \sqrt{\frac{N_1}{N_2}} \right) \tag{12}$$

where S is the ratio of the geometries of the transistors M_1 and M_2:

$$S = \frac{W_1L_2}{W_2L_1} \tag{13}$$

The parameter Q is plotted against temperature in Fig. 4 for different values of S. Depending on whether the result of the logarithm is negative or positive, as a result of the selected S value, Q can have either a PTAT or a CTAT behavior respectively. As can be observed, Q has a quasi-linear behavior ($R^2 > 0.99$), and consequently (12) can be approximated by the first two terms of its Taylor series centered at T_0 (eq. 14):

$$Q \simeq \frac{-nK_bT_0}{q} ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) - \frac{nK_b(T-T_0)}{q} \left(ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) + m_1 - m_2 \right) \tag{14}$$

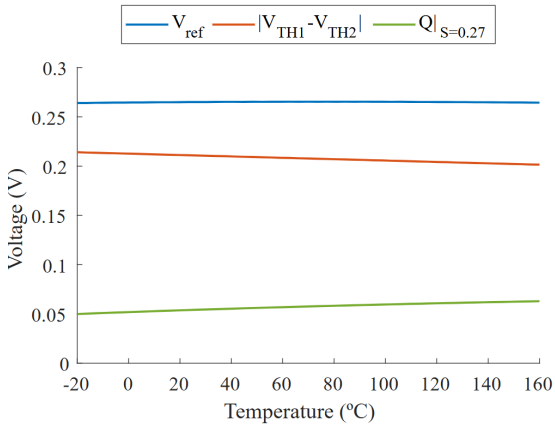

Fig. 5. Theoretical representation of the temperature compensation of the design.

whose slope is given by (15):

$$\frac{\partial Q}{\partial T} \simeq -\frac{nK_b}{q} \left(ln \left(S \sqrt{\frac{N_1}{N_2}} \frac{\mu_{01}}{\mu_{02}} \right) + m_1 - m_2 \right) \tag{15}$$

The value of $\frac{\partial Q}{\partial T}$ can be set by the geometries of S of the transistors M_1 and M_2, as shown in Fig. 4. When S is chosen such that $\frac{\partial Q}{\partial T}|_{T0} = |\frac{K_1-K_2}{T_0}|$ the temperature effect at T_0 is canceled and a significant improvement in the overall temperature compensation is achieved over the whole temperature range of this design. Note that every single term in (15) other than S, which is the design variable, is either a known constant or a simulation parameter that can be obtained from the model given by the technology. Fig. 5 shows the theoretical temperature compensation that can be achieved following the mathematical development explained above.

It is also important to mention that since the mechanism available to tune the temperature compensation of this structure is based on pondering the $\frac{\mu_{01}}{\mu_{02}}$ ratio, it is essential to mitigate as much as possible the layout dependent effects that can affect the mobility ratio, such as the mechanical stress introduced by the shallow trench isolations (STI) next to M_1 and M_2. To reduce this effect their diffusions were extended to move the STIs away from the channels. This layout measure, unlike the option of adding a dummy transistor

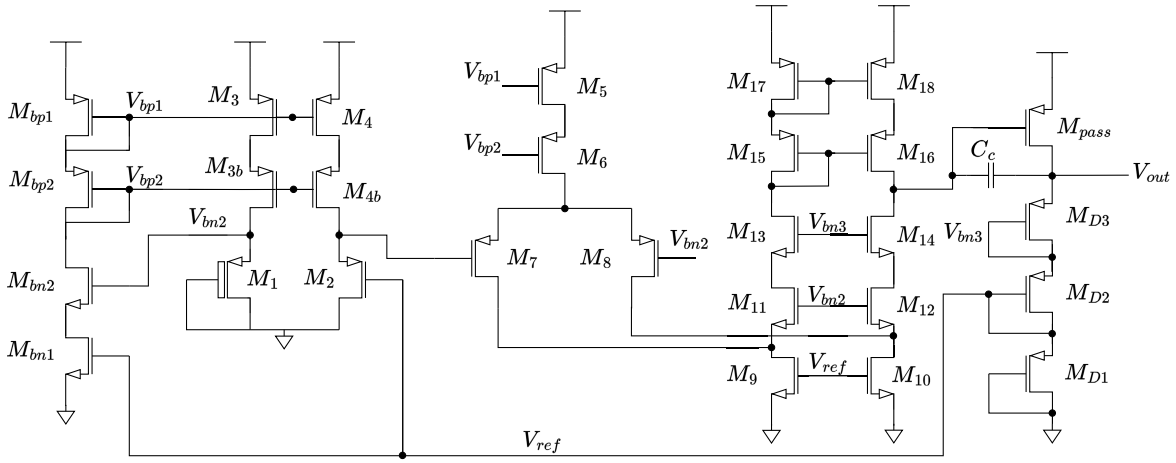

Fig. 6. Complete schematic of the proposed PMU.

on each side, increases the drain and source capacitance to the bulk. However, it requires less area for similar stress mitigation. At the same time, large transistor sizes were used for M_1 and M_2, which also helped to reduce the compression of the channel.

Finally, if the consideration $n_1 = n_2$ is not assumed, a second iteration for S around the previously obtained value is needed to account for the slight deviation introduced in the temperature behavior. The theoretical value of S calculated from 6 to obtain the best temperature compensation was 0.27, and after the second iteration, the value was moved up to 0.275, meaning that the simplified model given by 6 is accurate enough to obtain a first estimate with an error of less than 2% to the final value, while at the same time greatly simplifying the calculation.

B. Regulator Design

The dropout voltage of the regulator, V_{DO}, defined as the minimum voltage drop of the output voltage with respect to the supply voltage, is well known to be larger for an NMOS approach ($V_{DO} = (V_{GS} + V_{DS,sat})$), than for the PMOS counterpart ($V_{DO} = V_{DS,sat}$). This voltage drop translates directly into dissipated power that is not delivered to the load. Since the energy harvesters used in this sort of microsystem, such as photovoltaic cells, are very weak power supplies, it is very important to make the most of the energy collected. In addition, a PMOS output stage, unlike the NMOS version, adds some gain to the overall open-loop gain of the regulator which is also beneficial for parameters like the line regulation. For these reasons, a PMOS transistor was chosen as the pass device in this design. However, unlike most of the typical LDOs, the size of the pass transistor did not have to be large because autonomous microsystems typically handle relatively low currents, in the order of a few tens of pA to hundreds of μA. As a result, a significant area reduction is achieved.

A folded cascode topology was chosen for the error amplifier (EA). It is very suitable for low-voltage designs and provides high gain and only one dominant pole, which simplifies the full design of the frequency compensation and requires less area for the compensation capacitor. The complete schematic is shown in Fig. 6.

The current mirror in the EA is made with PMOS transistors because it has been demonstrated that the noise present in the supply voltage is completely replicated at the gate of the PMOS pass transistor [23]. This measure results in a PSR improvement since the gate noise of the PMOS pass device is equal to the noise present at its source and cancels it out at the output of the regulator.

Regarding the regulator stability, for capacitorless-LDOs with Miller frequency compensation, the non-dominant pole is set by the output stage, whose frequency location depends on the load current ($p_2 \simeq g_{m,pass}/C_L$). In fact, for lighter load currents the non-dominant pole shifts to lower frequencies, thus reducing the phase margin. Since the design is focused on low output currents, special attention was paid to the stability of the regulator. The Miller compensation was employed to take advantage of the output stage gain to reduce the capacitor size while ensuring that the non-dominant pole is always placed at higher frequencies than the unity gain frequency ($UGF \simeq g_{m,in}/C_c$). Fig. 7 shows the Bode diagram of the proposed PMU at different I_{load} values. A minimum phase margin of 48° is guaranteed for a worst-case scenario of $I_{load} = 0$ A.

The feedback network is implemented by PMOS transistors in their own n-well in diode configuration working in the deep sub-threshold regime to reduce their static power dissipation. At the same time, these diodes make the regulator react smoother in transitions from high to low load currents. As the output voltage increases in the transient state, the diodes' impedance decreases exponentially providing a better sinking capability.

Load regulation, understood as the voltage variation in the output node after a load change happens, is another important parameter for regulators in general. However, there is a trade-off between the quiescent current drawn by the pass transistor and the load regulation itself. As clarified in (16), the load regulation depends on the pass device transconductance, which

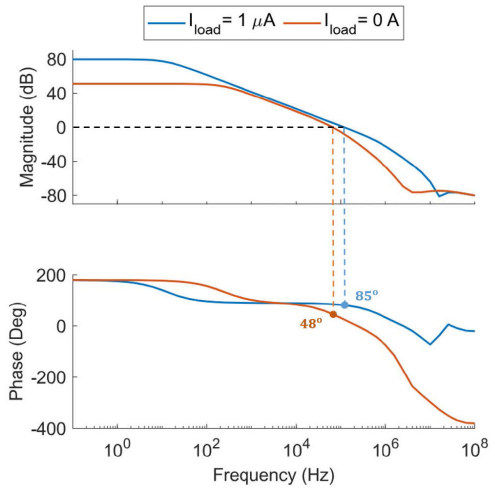

Fig. 7. Simulated Bode diagram of the proposed PMU at $I_{load} = 0$ A and $I_{load} = 1\ \mu A$.

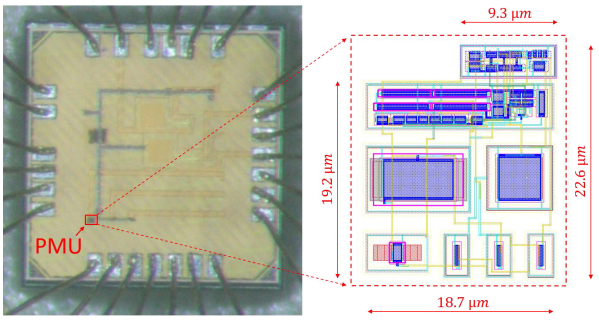

Fig. 8. $1 \times 1\ mm^2$ chip photograph and layout capture.

increases with its biasing current:

$$\frac{\Delta V_{out}}{\Delta I_{out}} = -\frac{1}{\beta A_v g_{m,pass}} \tag{16}$$

where β is the feedback factor and A_v is the regulator open loop gain.

In the context of autonomous microsystems, it is more important to keep the quiescent consumption under relatively low limits than to achieve outstanding load regulation, since large load currents and large load variations are not frequent. For this reason, the load regulation of this design, as well as the load regulation of some related works [24], [25], cannot be compared to the typical LDO load regulation, nor can they be expressed within the same scale.

IV. Simulation and Measurement Results

The chip photograph is shown in Fig. 8 with the proposed PMU highlighted in red. This design occupies a total area of only 391 μm^2, making it one of the smallest voltage references reported in the literature. This work is compared to the smallest reported voltage references in the state-of-the-art. It is worth noting, however, that unlike the other references in this list, this circuit can also deliver a certain amount of regulated power, further emphasizing the area optimization of this design.

Measurements were performed using an Agilent 4156C Precision Semiconductor Parameter Analyzer, a VöTSCH

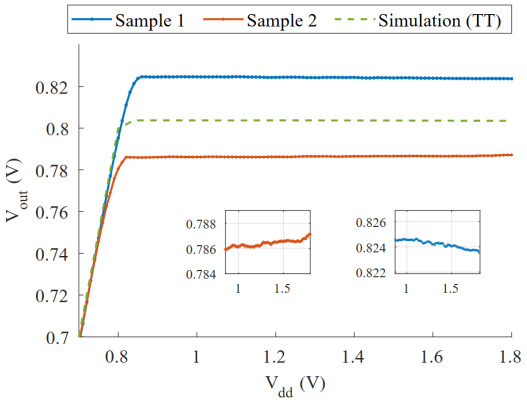

Fig. 9. Measured supply dependency of V_{out}.

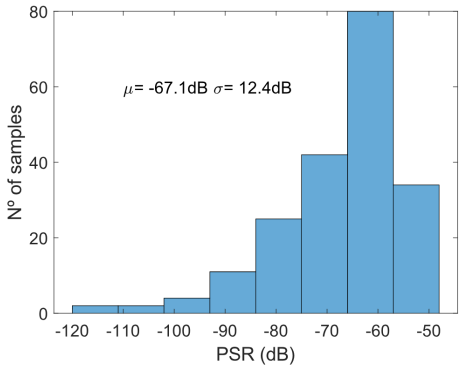

Fig. 10. Monte Carlo simulation of the proposed PMU's PSR at 1 Hz.

VCL 4010 Temperature Chamber, and a Keysight MSO9104A Mixed Signal Oscilloscope.

The supply dependence of this circuit was measured in 16 samples. The average line regulation between 0.85 V and 1.85 V was found to be 0.173%/V, which is slightly higher than the expected mean of 0.109%/V from a 200-run Monte Carlo simulation. The best and worst measured results were 0.025%/V and 0.832%/V, respectively. Figure 9 illustrates the supply dependency of V_{out} in two measured samples compared to the typical simulation case simulation (0.02%/V).

The Monte Carlo simulation of the PSR @1 Hz, with both process and mismatch variations enabled, is shown in Fig. 10. The average value obtained is -67.1 dB, which also demonstrates this design's good supply dependency at low frequencies.

On the other hand, we focused on ensuring that the regulator had low temperature drift over a wide temperature range. Temperature compensation was an important aspect of the design. Fig. 11 shows the typical case simulation of the temperature behavior at $I_{load} = 4nA$ and $I_{load} = 4\mu A$. The regulator demonstrated an outstanding temperature coefficient (TC) of 55 ppm/°C (between -10°C to 125°C) for the first case and 40 ppm/°C (between -30°C to 125°C) for the second case. We also checked how process variations affect this parameter through a 200-run Monte Carlo simulation, where the average temperature coefficient obtained was 139 ppm/°C, with a standard deviation of 56.1 ppm/°C from -20°C to 125°C. Measurements of the temperature behavior of 5 samples are

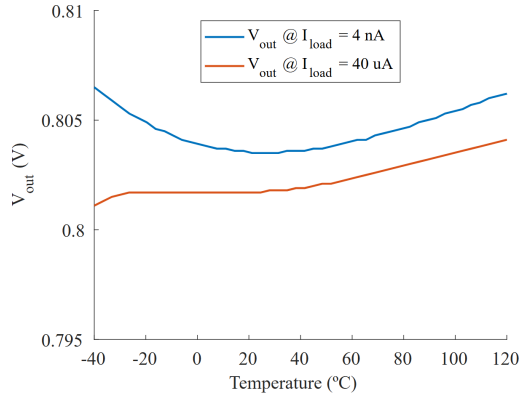

Fig. 11. Temperature behavior simulation of the LDO from -40°C to 125°C at $I_{load} = 4nA$ and $I_{load} = 40\mu A$.

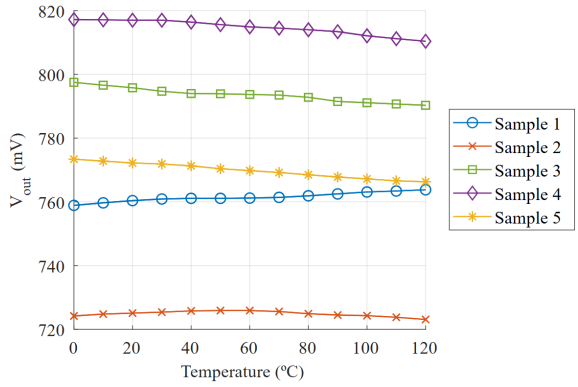

Fig. 12. Temperature behavior of 5 samples measured from 0°C to 120°C.

shown in Fig. 12. The average measured TC was 128.4 ppm/°C from 0 to 120 °C, with a best case of 96.5 ppm/°C and a worst case of 163.8 ppm/°C. At the same time, it is worth mentioning that, unlike this work, all the temperature coefficients reported in Table I would worsen when used alongside a linear regulator due mainly to the offset drift of the regulator with temperature. This effect is exemplified in [7] where the typical case TC simulated rises from 40 ppm/°C to 91 ppm/°C after including an LDO in the system [26].

In terms of power efficiency, this PMU can supply regulated power up to around 32 μW (40 μA @0.8 V) under high-efficiency performance. The regulator requires a drop-out voltage of 250 mV to supply the maximum load current, which meets the low drop-out standards of the topology. The average measured quiescent current is 18.4 nA, which constitutes less than 0.05% of the 40 μA that can be delivered to the load. Only about 1.5 nA (from simulations) of this quiescent current is used for the voltage reference, while the rest is distributed among the self-biasing stage and the different branches of the LDO as shown in Fig. 13. Although the overall quiescent current can be reduced below 1 nA, it was a design decision not to do so. Minimizing the quiescent current would make the transient response too slow, even for the very relaxed response times of most autonomous microsystems. Biasing in the pA range usually results in settling times on the order of tens of ms [25].

Fig. 14 shows the measured load regulation of two samples. Both silicon prototypes were supplied with 250 mV more

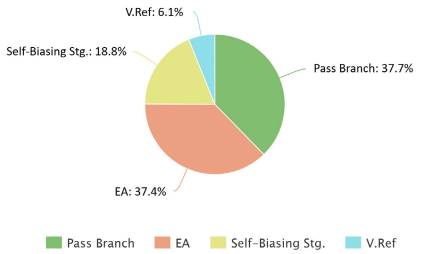

Fig. 13. Simulated breakdown of the proposed PMU's power consumption.

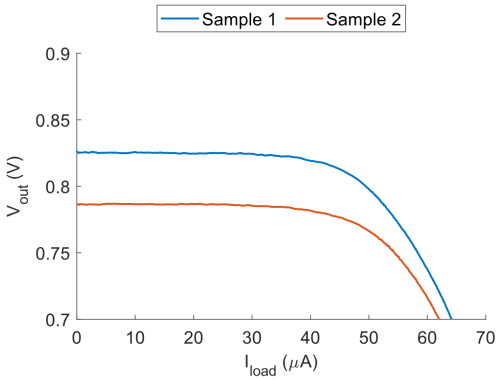

Fig. 14. Measured load regulation at $V_{dd} = V_{out} + 250mV$.

than their nominal output value. The average load regulation measured from 16 samples is 0.0381 $mV/\mu A$. As explained before, the load regulation of this tiny PMU cannot be compared or expressed on the same scale as the traditional LDOs because the significantly smaller size chosen for the pass transistor in this design reduces the output transconductance and consequently worsens the load regulation as well.

The voltage reference present in this PMU outputs a typical case simulated value of 267.7 mV. Since the feedback factor chosen for the LDO is 1/3, the output of the LDO is set around 800 mV. A 200-run Monte Carlo simulation was performed and the results are displayed in Fig. 15. The simulation showed that the average voltage reference value is 271 mV, with a standard deviation of 26 mV. Measurements were made only at the output of the LDO, as it was a design decision not to make the voltage reference output accessible to avoid the measurement setup affecting the operation point of the circuit. The measured LDO output voltage from 16 samples was 777.9 mV with a standard deviation of 65.7 mV ($\sigma/\mu = 8.45\%$).

This relatively high process variation is attributed to the use of different transistor types on the one hand, and the use of a self-biased structure on the other. Although the self-biased structure introduces some process variation, it is advantageous as it improves supply regulation significantly. It also eliminates the need for an additional stable biasing circuit, saving space, which is crucial for this design.

On the other hand, using different types of transistors also introduces some process variation. Most researchers address this issue by including a trimming stage. This approach is also applicable to this structure. However, this technique is not suitable for autonomous microsystems. Firstly, it comes with a

TABLE I
COMPARISON OF RESULTS AGAINST ULTRA-LOW AREA VOLTAGE REFERENCES RELATED WORKS

	This Work	[11]	[7]†	[12]	[30]	[9]	$[31]_a$	$[31]_b$	[8]	[32]
Technology (nm)	65	65	40	130	65	180	65	180	180	130
Area (μm^2)	391	104	480	665	840	900	900	1425	2500	3000
V_{dd} (V)	0.85-1.85	0.4-1.2	1.5-2.5	0.3-1.2	0.5-1.8	≥0.25	0.5-2.5	0.5-3.6	1.4-3.6	≥1.1
V_{out} (mV)	777.9	342.8	570	26	257.5	118.1	327.2	326.8	1250	800
σ/μ (%)	8.45	4.9	7	3.4	0.3	1.1	0.85	0.8	0.8	5
Min. Power (nW)	15.6*	0.00042	151	0.04	0.0143	0.113	0.24	0.006	0.033	27.5
Line reg. (%/V)	0.173	0.47	5-8	0.188	0.02	0.3	0.33	0.044	0.31	2
PSR (dB)	-67.1†	-	-70†	-67.3†	-	-65	-40	-49	-41	-
	@1 Hz	-	@ 915 MHz	@100 Hz	-	@100 Hz	@100 Hz	@100 Hz	@100 Hz	-
TC (ppm/ºC)	128.4	252.2	40	208	99.2	73.5	89.1-118.2	54-176	8-53	100
Temp. Range (ºC)	0∼120	-40∼60	-55∼125	-25∼125	0∼100	-40∼140	-20∼80	-20∼80	0∼100	-40∼85
Loading capability	40 μA	No	No	No	No	No	No	No	No	No

* The PMU average measured power consumption is 15.6 nW @$V_{dd,min}$. However, according to simulations, the voltage reference block only requires around 1.3 nW from the total.
† Simulated result.

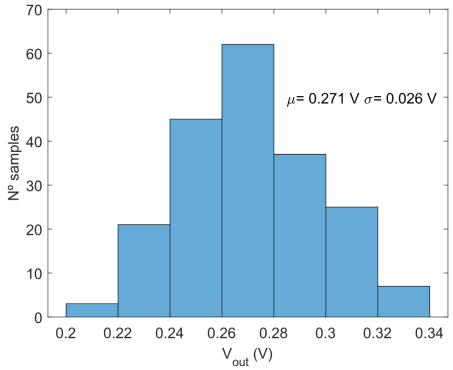

Fig. 15. Monte Carlo simulation of the voltage reference.

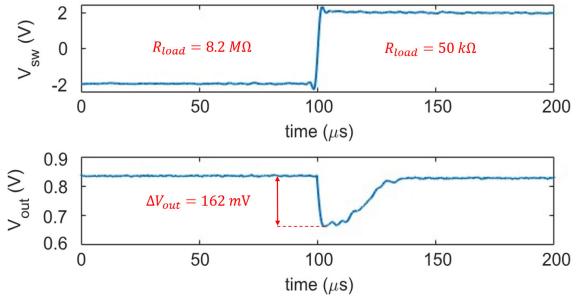

Fig. 16. Loading transient response of the PMU from $R_{load} = 8.2\ M\Omega$ to $R_{load} = 50\ k\Omega$ in 1 μs.

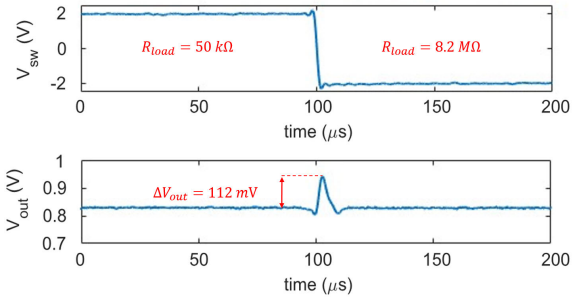

Fig. 17. Unloading transient response of the PMU from $R_{load} = 50\ k\Omega$ to $R_{load} = 8.2\ M\Omega$ in 1 μs.

significant area penalty. Secondly, post-fabrication calibration is not trivial in these very tiny microsystems.

Besides, due to their constrained area and power characteristics, most autonomous microsystems are usually designed to allow for even larger variations. For example, the microsystem presented in [27] allows for a variation of the core voltage going from 1.8 V to 0.3 V and uses a sub-nW clock [28] with an inaccuracy of $\sigma/\mu = 31.4\%$.

The transient response to a load change is shown in Fig. 16 and Fig. 17. In this measurement, a resistive load is switched from $R_{load} = 8.2\ M\Omega$ to $R_{load} = 50\ k\Omega$ at the output of the regulator. The switch was implemented with an external transistor driven by a pulse generator's signal (V_{SW}), whose edge time was configured to 1 μs. This is equivalent to a load current step from $I_{load} = 0.1\ \mu A$ to $I_{load} = 16.5\ \mu A$. First, the good stability of the regulator is demonstrated as there is no ripple at the output voltage during the transient response. Second, the maximum overshoot (162 mV) and undershoot (112 mV) remain within reasonable limits. The response times of the proposed PMU for the described loading and unloading transitions are 29 μs and 13 μs respectively.

Finally, Table I collects and summarizes the performance of the proposed PMU against only the smallest voltage references found in the literature. In addition, Table II compares this work to LDOs with similar target load currents and low quiescent currents.

Low quiescent power LDOs, as mentioned earlier, tend to have a slower transient response (T_R) because the currents available to charge/discharge internal nodes are very limited unless adaptive biasing is applied [29]. The regulators listed in Table II have different speeds and quiescent consumption depending on their target applications. Therefore, to facilitate comparison, we have included the widely used figure of merit FOM_t in Table II. This figure of merit, defined as 17, relates the response time of the LDO, T_R, the quiescent current, I_Q, and the load current step that the regulator has been proven

TABLE II
COMPARISON OF RESULTS AGAINST VOLTAGE REGULATORS RELATED WORKS

	This Work	[24]†	[33]	[34]	[25]	[35]	[26]†	[29]†
Reg. Topology	LDO	LDO	DLDO	DLDO	LDO	LDO	LDO	LDO
Technology (nm)	65	-	65	65	180	180	40	65
Area (μm^2)	391	-	42000	48000	15000	4310	6700	200000
V_{dd} (V)	0.85-1.85	$\geq$1.4	$\geq$0.5	0.5-1	0.7-2.5	$\geq$0.6	1.3-2	$\geq$1
Dropout V. (mV)	250	200	50	100	300	100	200	200
Min. Power (nW)	15.6	8.4	1350	0.373	0.679	3.5	1110.2	5
Line reg. ($\%/V$)	0.173	0.0025	0.688	-	-	0.636	5.7	0.5
PSR (dB)	-67.1†	-67†	-	-	-	-22.5	-28.5†	-
	@1 Hz	@1 Hz	-	-	-	@10 Hz	@915 MHz	-
Loading capability (μA)	40	10	200	270	500	750	1000	50000
Loading per area ($\mu A/\mu m^2$)	102.3 e-3	-	4.8 e-3	5.6 e-3	33.3 e-3	174.0 e-3	149.2 e-3	250 e-3
FOM_t (ns)	33.7	113.4	9450‡	0.13	13192	1.286	640‡	1.4‡

† Simulated result.
‡ Estimated from the transient response.

to withstand, ΔI_{load}.

$$FOM_t = T_R \frac{I_Q}{\Delta I_{load}} \tag{17}$$

In view of the FOM_t results in Table II, the proposed PMU is not slow in relation to its quiescent current consumption and the load current that can deliver.

It is important to note that, unlike our design, the works collected in the first table lack of any kind of loading capability, while those in the second table, except for [26], do not include the voltage reference block in their design. The LDO presented in [26] incorporates the voltage reference described in [7], and perfectly illustrates the area overhead required for an unbuffered voltage reference to have some loading capability. To compare [7] to our work we can take into account the loading capability per area of the reported in [26] to estimate the extra area that [7] would need to drive a 40 μA load, the same load as the proposed PMU in this work. Indeed, the area needed by [7] would increase from 480 μm^2 to 750 μm^2, which is almost twice the area used in our design. With the proposed PMU, we integrate in the same circuit the missing characteristic of each of the two groups collected in both tables, while achieving the second smallest area reported in the literature.

V. CONCLUSION

A power management unit for cell-sized autonomous microsystems implemented with a 65 nm technology has been presented. It integrates a voltage reference and a low-dropout regulator in a compact area of 391 μm^2. The reduced size of this PMU makes it one of the smallest reported in the literature, which is a key feature when targeting cell-sized systems. This design can efficiently supply up to 40 μA to the load while only drawing a quiescent current of 18.4 nA. It has also demonstrated good stability with respect to temperature and supply voltage. These features make this PMU suitable for a wide range of applications, including those with limited power sources, varying temperatures, or tight spaces. Consequently, the proposed circuit shows an excellent compromise for most *Smart Dust* applications.

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