UNIVERSIDAD POLITÉCNICA DE MADRID
ESCUELA TECNICA SUPERIOR DE INGENIEROS DE TELECOMUNICACION

MANUFACTURING AND FIELD PERFORMANCE OF PHOTOVOLTAIC MODULES BASED ON UNCONVENTIONAL SILICON SUBSTRATES

DOCTORAL THESIS

Submitted for the degree of Doctor by:

Ismael Guerrero Arias
Ingeniero Industrial

Madrid, 2024

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Doctoral Degree in Photovoltaic Solar Energy

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The hardest thing to understand in the world is the income tax

Albert Einstein

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Abstract

The main challenge solar photovoltaics has been facing during the last decades has been its cost therefore photovoltaics science development has been mainly focused on that. All aspects impacting the levelized cost of electricity (LCOE) have been deeply analyzed and different fields of study have been created in the scientific community to do that, the modules manufacturing being the main one. On the journey to reduce the cost of solar modules several materials and manufacturing methods have been explored in all the segments of the value chain being Crystaline Silicon the clear winner that represents today the vast majority of the modules manufactured.

In this work we focus on the manufacturing of the substrate of the crystalline silicon modules analyzing different materials and crystal growing technologies with the objective to compare not only their manufacturing process and results but also the performance in the field.

The main cost of a crystalline silicon module is the materials, and polysilicon is by far the most expensive one and has been the biggest headache of the industry for decades with several manufacturing processes being widely used and studied. The predominant technology comes from the microelectronics industry, the Siemens process, and although other technologies are accepted by the industry like the fluidized bed reactor (FBR), its complexity made it less used. One alternative specifically for solar photovoltaics comes from accepting that the level of purity of the silicon material required for solar cells is not that of manufacturing microchips and therefore a purification of metallurgical grade silicon to a lower level might be good enough. This way the so called Upgraded Metallurgical Grade (UMG) silicon appears into scene, where instead of using a complex chemical process to purify the material a much simpler one based on matellurgical methods could obtain a good enough material for the production of solar cells. This last technology for being simple and specifically designed for solar photovoltaics is the one explored in this work, where we study both the quality and yield of the manufactured wafers and we also deploy modules manufactured with this material on the field and analyze their performance versus modules manufactured with polysilicon of the traditional Siemens process. This study contains data of the first year of the modules in the field.

After the materials of the modules, the cell manufacturing and the efficiency obtained are the main cost components, being the efficiency the most relevant parameter of indirect impact over cost for affecting the whole installation including the balance of systems, the interconnection cost, land usage and every single component of the solar plant. A module that has less efficiency than another implies that for the same power more modules need to be deployed, therefore more land is required, more racking or trackers, more cable, etc. A technology, no matter how cheap it is, incapable of providing high enough levels of efficiency will just not be capable to compete. This take us to the next aspect of the silicon material that we analyze in this work, the growing method that will define the characteristics of the wafers that will be used to manufacture the future solar cells with a very important impact on the efficiency of the future module.

There are two main technologies that evolved over the last decades until today, mono crystalline silicon and multi crystalline silicon. For many years multi crystalline was slightly more predominant than mono crystalline but this turned and today almost all market is mono crystalline based. Manufacturing multi crystalline wafers is simpler and therefore cheaper with significantly lower energy consumption during the manufacturing process but mono crystalline based cells offer higher efficiencies. When the efficiency gap between both technologies has widened enough, the interest for multi crystalline silicon disappeared. There is one technology of growing wafers that was explored on the way, that consisted of using the manufacturing process of multi crystalline wafers but to produce mono crystalline wafers instead and obtained promising results although it has been almost abandoned by the industry as the multi crystalline route has been fading away. The technology was so early on its development that no consensus has been reached when assigning it a name yet, this way you can find scientific work naming it pseudo mono wafers, quasi mono wafers, mono casting wafers, mono crystalline cast wafers, mono like wafers, etc.

We challenge in this work the fact that this technology has suffered the same destiny as multi crystalline silicon wafers too early and that should still be considered as a manufacturing alternative for the solar industry to produce mono crystalline wafers since it is cheaper to produce, and the efficiency gap could not justify the extra cost of the traditional mono crystalline route. In this document we will refer to this technology as cast-mono (CM) wafers and we will analyze different aspects of the manufacturing process including the manufacturing yield and we will study also the field performance of modules based on this substrate. For doing

that we manufactured modules based on cast-mono wafers that we put in the field for three years and compared its performance with multi crystalline and mono crystalline modules. We also simulated the three systems and analyzed how valid the results obtained with software commonly used in the industry for yield and production prediction are for this type of modules.

We found out that modules based on upgraded metallurgical silicon have a very similar performance than those modules manufactured using polysilicon. Although those modules are both multi crystalline. There is research about mono crystalline ingots manufactured from upgraded metallurgical silicon, but we have not found any data of mono crystalline modules made out of upgraded metallurgical silicon probably because the level of impurities is too high making it unviable. Anyway, it has been published that at cell level the performance of upgraded metallurgical silicon cells is very similar of that of poly silicon ones when the technology used is the cast-mono, reporting small differences in efficiency with the latest cell technology.

On the other hand, cast-mono technology has been reported to have achieved efficiencies equivalent to the top efficiencies seeing today and therefore could perfectly be a technology able to compete. We show in this work the origin of the defects that generate low quality wafers when the manufacturing process of this technology is not under control and how to control it. We analyze the mechanical strength of the wafers produced and compare it with multi crystalline and mono crystalline wafers, showing that the mechanical properties of cast-mono wafers are very similar as that of mono wafers for wafers of low dislocations density. If the dislocation density is higher the mechanical strength has a higher risk of being compromised. Therefore, we conclude that in order to obtain good quality cast-mono wafers, both from the chemical and mechanical point of view, low dislocations densities are required and that is possible using the right manufacturing parameters. Finally, we manufactured modules with the three wafers technologies and we deployed them in the field proving that cast-mono modules obtained similar or better results than the other technologies. As a conclusion, we can say that this technology is still valid and deserves to be taken into consideration even in today's environment of high efficiencies.

Resumen

El principal reto al que la tecnología solar fotovoltaica se ha enfrentado durante las últimas décadas ha sido su alto coste y gran parte del desarrollo científico ha estado enfocado a este asunto. Cualquier aspecto que impacte en el coste energético nivelado de una instalación (LCOE por sus siglas en inglés) se ha analizado en profundidad por la comunidad científica creando distintos campos de investigación, siendo la fabricación de módulos el más relevante. En el camino para reducir el coste de fabricación de los módulos solares se han explorado distintos materiales y distintos métodos de fabricación en todos los segmentos de la cadena de valor, siendo el Silicio cristalino el material que se erige como claro ganador y en el que se basan la gran mayoría de los módulos fabricados en la actualidad.

En este trabajo nos centramos en la fabricación del substrato de los módulos de Silicio cristalino analizando distintos materiales y tecnologías de crecimiento del cristal con el objetivo de comparar no solo el proceso de fabricación sino también el comportamiento en campo de los módulos fabricados con diferentes materiales y distintas tecnologías de crecimiento del cristal que conforma el substrato.

El principal coste de un módulo cristalino son los materiales, y el polisilicio es con diferencia el más caro y ha sido el mayor quebradero de cabeza de la industria durante décadas; distintos procesos de fabricación han sido ampliamente empleados y estudiados. La tecnología predominante procede de la industria microelectrónica, el proceso Siemens, y a pesar de que hay otras tecnologías aceptadas por la industria como el reactor de lecho fluidizado (FBR por sus siglas en inglés), su complejidad ha hecho que se utilice menos. Una alternativa específica para la industria solar fotovoltaica surge al aceptar que los niveles de pureza del material de silicio requeridos para la fabricación de células solares no son los mismos que para la fabricación de micro chips y, por tanto, la purificación del silicio metalúrgico en un nivel inferior podría ser suficientemente bueno. De esta forma el silicio metalúrgico mejorado o de grado solar aparece en escena, donde en lugar de usar un complejo proceso químico para purificar el material, uno mucho más sencillo basado en métodos metalúrgicos podría obtener un material suficientemente bueno para la fabricación de células solares. Esta última tecnología por ser sencilla y específicamente diseñada para la industria solar fotovoltaica es la que se explora en esta tesis donde estudiamos tanto la calidad como el rendimiento de las obleas fabricadas a partir de este material. También ponemos módulos fabricados con este material en campo y analizamos su

rendimiento comparado con módulos fabricados con polisilicio del proceso Siemens tradicional después de un año en campo.

Después de los materiales que componen los módulos, la fabricación de células y la eficiencia obtenida son los principales componentes del coste, siendo la eficiencia el parámetro con impacto indirecto sobre el coste más relevante, afectando a toda la instalación incluyendo el balance de sistemas, los costes de interconexión, el empleo de terreno y todos y cada uno de los componentes de una planta solar. Un módulo que tenga menos eficiencia que otro implica que para conseguir la misma potencia de planta necesitamos más módulos en campo, por lo tanto, necesitaremos más terreno, más estructuras o seguidores, más cableado, etc. Una tecnología, no importa como de barata sea, incapaz de proporcionar niveles de eficiencia suficientemente elevados simplemente no será capaz de competir. Esto nos lleva al siguiente aspecto del material de silicio que analizaremos en este trabajo, el método de crecimiento que definirá las características de las obleas que serán usadas para fabricar las futuras células solares.

Hay dos tecnologías principales que evolucionan a lo largo de las últimas décadas hasta hoy, el silicio mono cristalino y el silicio multi cristalino. Durante muchos años el multi cristalino fue ligeramente predominante sobre el mono cristalino, pero esto se ha dado la vuelta y hoy casi todo el mercado está basado en el silicio mono cristalino. Fabricar obleas multi cristalinas es más sencillo y por lo tanto más barato, con un consumo energético significativamente menor durante el proceso de fabricación, pero las células basadas en mono cristalino ofrecen mayores eficiencias. Cuando la diferencia en la eficiencia entre ambas tecnologías se ha hecho suficientemente grande el interés por el silicio multi cristalino ha desaparecido. Hay una tecnología de crecimiento de obleas que fue explorada por el camino, que consistía en usar el proceso de fabricación de obleas multi cristalinas, pero para producir obleas mono cristalinas en su lugar y obtuvo resultados prometedores aunque ha sido abandonada por la industria cuando el proceso multi cristalino ha sido abandonado. La tecnología estaba en un momento tan temprano en su desarrollo que no se alcanzó consenso para asignarle un nombre aún, de esta forma podemos encontrar trabajos científicos que la llaman obleas pseudo mono, obleas mono cast, obleas mono cristalinas cast, obleas mono like, etc.

En este trabajo retamos el hecho de que esta tecnología haya sufrido el mismo destino que las obleas multi cristalinas demasiado pronto y defendemos que debería aún considerarse como una alternativa de fabricación de obleas mono

cristalinas para la industria solar. En este documento nos referiremos a esta tecnología como obleas cast-mono (CM) y analizaremos diferentes aspectos de su proceso de fabricación incluyendo el rendimiento de fabricación, estudiando también el comportamiento en campo de módulos fabricados con este substrato. Para ello fabricamos módulos basados en obleas cast-mono que ponemos en campo durante tres años y comparamos su comportamiento con módulos multi cristalinos y mono cristalinos. También simulamos los tres sistemas y analizamos como de fiable es para este tipo de módulos el software de simulación más empleado industrialmente para predecir la eficiencia y producción de un sistema fotovoltaico.

Encontramos que los módulos basados en silicio metalúrgico de grado solar tienen un rendimiento muy similar a aquellos fabricados usando polisilicio, aunque ambos módulos son multi cristalinos. Hay investigaciones sobre lingotes mono cristalinos fabricados a partir de silicio metalúrgico grado solar pero no hemos encontrados datos sobre módulos mono cristalinos fabricados a partir de silicio metalúrgico grado solar, probablemente porque el nivel de impurezas es demasiado elevado y lo hace inviable. Se ha publicado que a nivel de célula el rendimiento de células de silicio metalúrgico grado solar es muy similar a las de polisilicio cuando la tecnología empleada para la fabricación de las obleas es la del cast-mono, reportándose pequeñas diferencias de eficiencia con la última tecnología de célula. Por lo tanto, parece que esta tecnología merece mayor exploración como hemos demostrado para módulos multi cristalinos.

Por otro lado, hay publicaciones reportando que la tecnología cast-mono ha alcanzado eficiencias equivalentes a las máximas eficiencias alcanzadas hoy y por lo tanto podría ser una tecnología perfectamente capaz de competir en el entorno de alta eficiencia de la actualidad. En este trabajo mostramos el origen de los defectos que generan obleas de baja calidad cuando el proceso de fabricación con esta tecnología no es debidamente controlado y como evitarlo. Analizamos la resistencia mecánica de las obleas producidas y la comparamos con las de obleas multi cristalinas y mono cristalinas, encontrando que las propiedades mecánicas de las obleas cast-mono son muy similares a las de las obleas mono cristalinas para obleas con bajas densidades de dislocaciones, si la densidad de dislocaciones es mayor la resistencia mecánica tiene mayor riesgo de verse comprometida. Por lo tanto, concluimos que para obtener obleas cast-mono de buena calidad, tanto desde el punto de vista químico como mecánico, se requieren obleas con densidades de dislocación bajas, lo cual se puede lograr usando los parámetros de fabricación adecuados. Finalmente, fabricamos módulos con las tres tecnologías de obleas que

se instalan en campo, y los resultados que obtenemos demuestran que esta tecnología es aún válida y que merece que se tenga en cuenta incluso en el entorno de altas eficiencias que tenemos hoy en día.

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Abbreviations and Acronyms

AM	Air mass
a-Si	Amorphous silicon
ATM	Atmosphere
B	Boron
Cdf	Cumulative distribution function
CdTe	Cadmiun Telluride
CIGS	$Cu(InGa)Se_2$
CM-Si	Cast-mono silicon
c-Si	Crystalline silicon
CZ	Czochralski
DS	Directional solidification
DWS	Diamond wire sawing
FBR	Fluidized bed reactor
FE	Finite elements
[Fei]	Interstitial iron concentration
FF	Fill factor
FLBT	Four line bending test
G	Irradiance
GB	Grain boundaries
G-T-E	Irradiance, temperature, efficiency
GWp	Gigawatt Peak
HEM	Heat exchange method
HJT	Heterojunction Technology
ID	Inner diameter
IR	Infra red
I_{sc}	Short circuit current
I-V	Current vs voltage
LBIC	Laser beam induced current
LCOE	Levelized cost of electricity
LID	Light induced degradation
MBE/AV	Mean bias error over absolute value
mc-Si	Multi crystalline silicon
MG-Si	Metallurgical grade silicon
mono-Si	Mono crystalline silicon
MWp	Megawatt Peak
MWSS	Multi wire sawing system
P	Phosporus
PDG	Phosphorus diffusion gettering
PEG	Polyethylene glycol
PERC	Passivated Emitter Rear Contact
PL	Photoluminescence
POA	Pyrometer of array
PR	Performance ratio

PRSTC	Performance ratio standard testing conditions
PSC	Perovskite Solar Cell
PV	Photovoltaics
P-V	Power vs voltage
PVSyst	Name of a software employed in simulation
QM	Quasi mono crystalline
QSSPC	Quasi steady-state photoconductance
RMSE	Root mean square error
SEM	Scanning Electron Microscope
SiCN	Silicon carbon nitride
SRH	Shockley-Read-Hall recombination
STC	Standard testing conditions: 1000 W/m^2 , 25 ^0C, 1.5 ATM
Tbulk	Minority carriers lifetime measured in the bulk material (bricks)
TCS	Trichlorosilane
Teff	Minority carriers lifetime measured in wafers surface
TET	Tetrachlorosilane
TOPCon	Tunnel Oxide Passivated Contact
TTV	Total thickness variation
UMG	Upgraded metallurgical grade
UPM	Universidad Politécnica de Madrid
V_{oc}	Open circuit voltage
µPCD	Microwave photoconductance decay

1. Introduction

Many different technologies and materials have been explored to manufacture solar modules. We can make the following high-level classification to group the different technologies and materials:

- Crystalline Silicon (c-Si) modules, classified in three main groups based on the wafers used: mono crystalline (mono-Si), muti crystalline (multi-Si) and ribbon silicon.
- Thin film modules, a minority of the market almost disappeared but for one manufacturer, classified mainly based on its materials as follows: amorphous Silicon (a-Si), Cadmium Telluride (CdTe) and $Cu(InGa)Se_2$ (CIGS).

There are many other technologies that have been explored but have not progressed enough to be considered.

Solar cells remain the main focus of research, and many different technological evolutions are happening. The latest cells technologies most employed have been the Passivated Emitter Rear Contact (PERC) and nowadays the Tunnel Oxide Passivated Contact (TOPCon) technology is the predominant in the market. Hetero-junction cells are the next step (HJT) where a-Si is used to include an extra layer providing higher efficiency. Recently a combination of organic-inorganic components is the fastest advancing technology based on Perovskite (PSC).

There are many factors that make a technology prevail, the main ones being the cost of producing the modules, the efficiency, that affects the whole system, and the robustness of the technology that allows manufacturers to guarantee enough lifetime of the modules without significant degradation overtime. At the end what is important is that the new technology reduces the LCOE of the previous one to become the dominant player. This way cost and efficiency are the main parameters and lifetime a must.

There are other characteristics that are essential nowadays such as using materials that are abundantly available and that are environmentally friendly, allowing for the module materials to be recycled.

In 2023 c-Si represented more than 97% [1] of the market with around 500 GWp manufactured. There are several factors that made c-Si modules to enjoy the market share they enjoy today: First of all there is tremendous knowledge about silicon materials and manufacturing technologies inherited from the microelectronics industry, which allowed the fastest development of silicon-based technology for solar. Secondly, a semiconductor should have a bandgap between about 1 and 2 eV to be a good absorber of solar energy, the bandgap in Silicon is 1.1 eV what makes it perfect for collecting energy from the sun as shown in figure 1.1 from the important publication of Shockley and Queisser (SQ) about the efficiency upper limit of a solar cell [2].

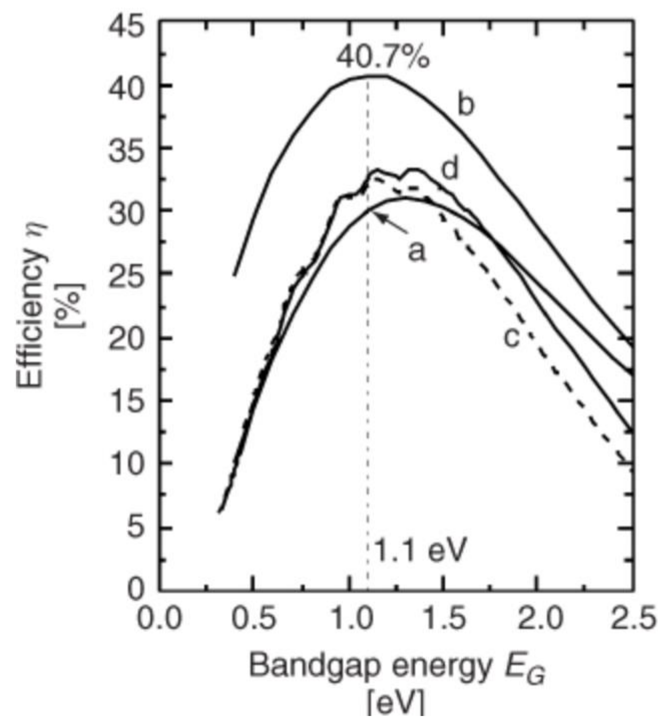


Figure 1-1: SQ efficiency limit for an ideal solar cell versus bandgap energy for unconcentrated black body illumination, for full concentrated illumination and for illumination under the terrestrial sun spectrum: (a) unconcentrated 6000 K black body radiation (1595.9 W/m^2); (b) full concentrated 6000 K black body radiation (7349.0 × 104 W/m^2); (c) unconcentrated AM1.5-Direct [3] (767.2 Wm^{-2}); (d) AM1.5 Global [3] (962.5 W/m^2). Reproduced from [4].

Silicon is also abundant, the second most abundant element in Earth after Oxygen, clean, environmentally friendly and a c-Si based module is possible to recycle above 97% today. Silicon based cells and modules are very stable, and manufacturers today offer guarantees above 40 years of life with small degradations.

The main disadvantages of Silicon are that is brittle and therefore has mechanical limitations, and that it has optical limitations Both make Silicon to require relatively thick cells (although new cells technologies such as TOPCon use 140 microns wafers and HJT is expected to reach 100 microns). This means electrons have to travel distances equivalent to the cell thickness to be extracted by the contacts and recombination (electrons moving from the conduction band back to the valence band) will be a key efficiency factor. To minimize recombination in this thickness distance, a material of high chemical purity and with minimum imperfections is required so that the electron can have high mobility. Impurities and imperfections can absorb the extra energy of the conduction band electrons eliminating the free electron and sending it back to its natural state of energy on the valence band, reducing the efficiency of capturing the energy from the sunlight and reducing the overall efficiency of the module.

Therefore, wafers with high chemical purity and low imperfections are required to obtain good c-Si cells and modules.

1.1. Thesis Outline

Most of the market of solar modules nowadays is based on the mono crystalline silicon technology. The value chain of the manufacturing of silicon modules starts with quartz as raw material of the MG-Si process, then MG-Si is purified producing either UMG-Si or polysilicon. Due to the dramatic drop in price today only polysilicon is used as raw material to produce wafers and almost only Cz wafers are produced. Figure 1.2 shows the main steps of the value chain from quartz to produce the silicon wafers that will be used as substrate to manufacture the solar cells and modules.

As we will describe in more detail, on the way to develop the current process, cheaper and less energy intensive technologies have been abandoned, this way UMG-Si material is not used anymore and the cast-mono process to produce wafers has been abandoned too in favor of the Cz one.

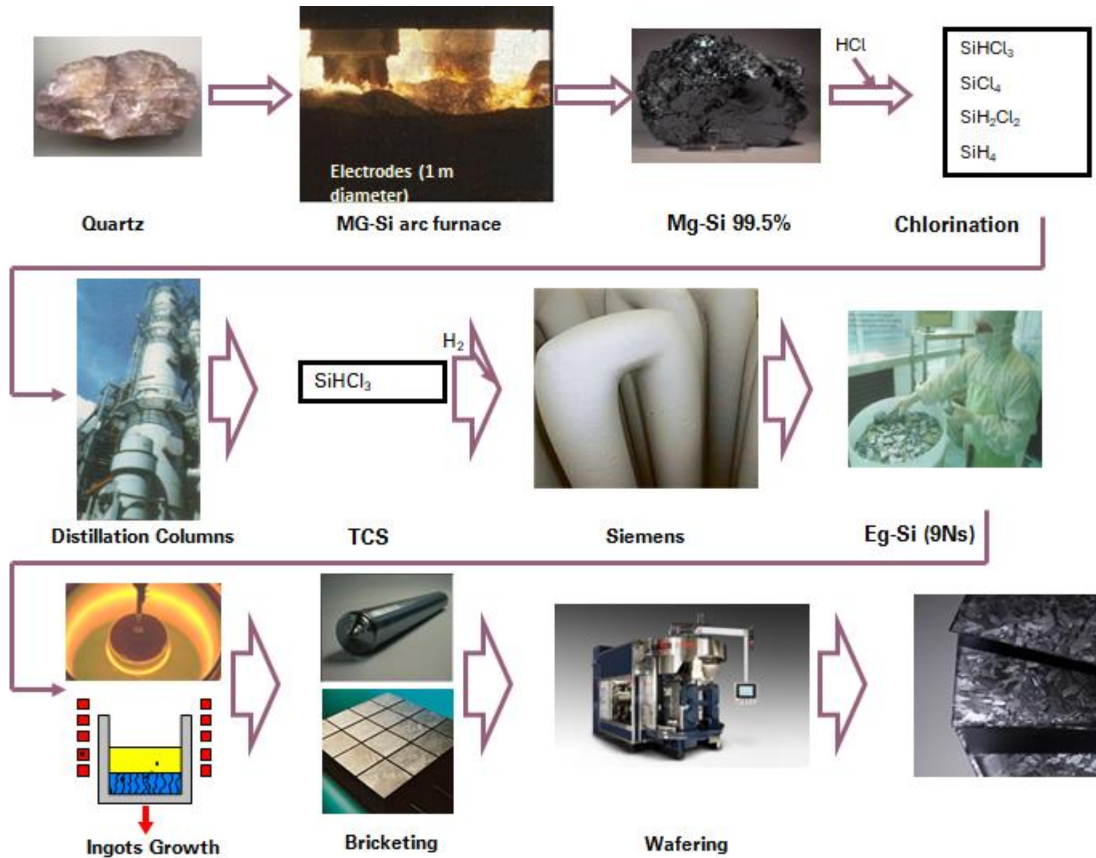


Figure 1-2: Value chain of wafer production.

During years it has been discussed what the specification of the solar material should look like, several of them described in table 1.1 [5]. This PhD explores these alternatives that were left behind, the UMG-Si material and the cast-mono wafers production process. To do that, we investigated the manufacturing of ingots and wafers using UMG-Si, manufactured modules with them and test them in the field comparing its performance with that of multi crystalline silicon modules produced with polysilicon.

Table 1-1: Chemistry specification for solar silicon. Data from [7].

	Feedstock A	Feedstock B	Feedstock C
B	0.05	0.45	1.5
P	0.1(a)	0.6	4(a)
Al	0.05(a)	5(a)	5(a)
Fe	0.05	5	All four Fe, Cu, Ni, Cr: 5
Cu	0.01	1	
Ni	0.01	1	
Cr	0.05	1	
Ti (*)	0.005	0.05	0.05
Na	0.01(a)	0.01(a)	All Na, K: 0.01(a)
K	0.01(a)	0.01(a)	
Zn		2	
Ca			
C	5	30 (multi) 1 (mono)	

On the cast-mono wafers process front, we do something similar although here, since the crystalline structure is quite different and cast-mono wafers might have higher dislocations densities than the Cz wafers, we start analyzing deeply the wafering process with multi wires saw, making a study on the wire wear and on the mechanical strength of cast-mono (CM-Si), multi crystalline (mc-Si) and Cz-Si wafers. We manufactured also modules using CM-Si wafers and we put them in the field for 3 years, collecting a significant amount of data and making a comparison of the performance of modules based on the three wafers technologies. We also made a simulation using commercial software to predict the production of solar systems and we compared the accuracy obtained with that of a mc-Si modules system.

This way in Chapter 3 we describe experiments where we incorporate different levels of UMG-Si into the feedstock to produce mc-Si wafers and report the results we obtained on manufacturing yield, the usable length of the ingots and the quality of the ingots, showing that the level of inclusions increases significantly with the use of UMG-Si and the as cut wafers lifetime is higher due to highly compensated ingots. We also describe the performance on the field of mc-Si modules produced from UMG-Si wafers compared with mc-Si modules from polysilicon after one year of measurements.

Chapter 4 describes in detail the wiring saw process and studies broken and unbroken wire features, in order to better understand why breakages are produced. The properties of CM-Si wafers, based on low and high crystal defect densities, have been studied also in this chapter from a mechanical point of view, comparing their strength with that of both Cz-Si mono crystalline and typical multi crystalline materials.

On Chapter 5 the manufacturing process of CM-Si wafers is deeply analyzed, describing the usable length of the bricks, the dislocations propagation and how to minimize them, and the effect of recycling the seed. Also, the performance data of three years on the field of modules based on CM-Si, mc-Si and CZ-Si wafers is shared and compared with PVsyst simulations.

Finally, Chapter 6 summarizes this PhD conclusions and suggests future works to keep on further investigating both technologies. Both technologies require less energy and are significantly cheaper to produce than polysilicon and Cz-Si, but might struggle to compete in a high efficiency environment. The field performance, though, suggests that are very valid technologies that deserve further exploration.

2. Silicon material and silicon wafers manufacturing

2.1. Polysilicon and UMG manufacturing process

Silicon (Si) is the second member of group IVA in the periodic system of elements (figure 2.1). It never occurs free in nature, but in combination with oxygen, forming oxides and silicates.

IIIA	IVA	VA
B	C	N
Al	Si	P
Ga	Ge	As
In	Sn	Sb
Ti	Pb	Bi

Figure 2-1: Groups IIIA, IVA and VA of the periodic table.

As indicated before, it is a semiconductor with a bandgap of 1.12 eV at 25°C. At atmospheric pressure, silicon crystallizes into a diamond cubic structure. Under some circumstances, slow-growing faces of silicon are {111} but in epitaxial films and polysilicon deposition {111} is the fastest growth direction. Vapor deposition below 500°C results in amorphous silicon. If reheated above this temperature, crystallization will occur. Like water, silicon expands when solidifying.

Impurities incorporated in the silicon lattice during the crystal growth ionize at low temperatures, providing either free electrons or holes. Elements from group IIIA and VA have a similar atomic size as Si and impurities from those elements are common to substitute Si atoms in the crystal. Impurities from group VA have one more valence electron than Si and therefore when they replace a Si atom in the atomic lattice they supply electrons and are called n-dopants or donors. On the opposite, elements from group IIIA have one less valence electron and when they substitute a Si atom they supply holes and are called p-dopants or acceptors. The elements around Si in the periodic table are the ones with atoms of similar size to Silicon (figure 2.2) and of those Phosphorus and Boron, for its easier manipulation,

are the ones most used to control the semiconductor properties (doping levels) of the silicon material.

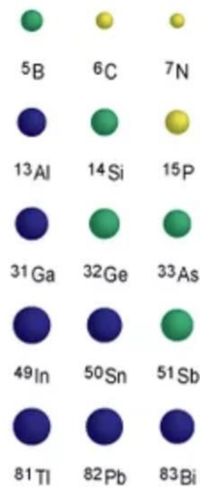


Figure 2-2: Periodic table showing the relative sizes of the elements based on atomic radius data (relative to the largest element Cesium).

When manufacturing silicon materials, impurities are usually expressed in their weight concentration or ratio to the host material, depending on the order of magnitude we usually use ppm(w) or ppb(w). In semiconductor physics it is also expressed in atom concentration as ppm(a) or ppb(a), and taking into account that the silicon crystal has $5x10^{22}$ atoms per cm^3, a related unit is atoms/cm^3. Another frequent way to account for the impact of the impurities concentration in solar technology is the minority-carrier lifetime. This is the average time that it takes to a free electron to recombine with a hole and is in a first approximation inversely proportional to the impurity concentration. Solar cells require at least 100 μs to give reasonable efficiency, and this minimum level increases as solar cells become more efficient. Therefore, the level of impurities in the material should be such that we obtain a minority-carrier lifetime above that one.

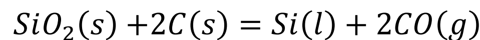
Not all impurities affect the material equally. High-purity silicon crystals with metal content less than 10 ppb(w) may have minority-carrier lifetime values as high as 10000 μs. A typical commercial specification of a solar wafer when it comes to its chemical and semiconductor properties is provided in table 2.1.

Table 2-1: Commercial wafer specification. Data provided by DCWafers.

	Multi-crystalline	**Mono-crystalline**
Electrical properties		
Conduction Type	P	P
Doped	Boron	Boron
Specific resistivity	0.5 ~ 3.0 ohm cm	3.0 ~ 6.0 ohm cm
Minority carrier lifetime (μ-PCD, as cut wafer level)	≥ 1.0 μs	≥ 1.5 μs
Chemical properties		
Carbon concentration [Cs]	Max. $1x10^{18}$ atoms/cm^3	Max. $5x10^{17}$ atoms/cm^3
Oxygen concentration, [Oi]	Max. $8x10^{17}$ atoms/cm^3	Max. $9x10^{17}$ atoms/cm^3

Carbon and oxygen are very stable when combined with silicon and are a major source of impurities, in fact when in contact with oxygen silicon immediately oxides forming a 100 angstrom silica layer. Oxygen reaction with boron overtime is one of the main factors of modules degradation.

The most common mineral in the crust of Earth is quartz which has a composition of 99,9% of SiO_2 and is the starting material of silicon manufacturing. The first purification process of silicon is the production of the so-called metallurgical grade silicon, where quartz is combined with carbon to produce silicon and carbon monoxide following the overall reaction:



$$SiO_2(s) + 2C(s) = Si(l) + 2CO(g)$$

Figure 2.3 illustrates a typical metallurgical silicon (MG-Si) production site where quartz and coal, selected based on its characteristics to achieve high product quality, optimize furnace performance and minimize the environmental impact, are heated using an electrical arc created between carbon electrodes and the ground. The products obtained are liquid silicon metal collected at the bottom of the furnace, and carbon monoxide CO(g), that is further oxidized to carbon dioxide CO_2 (g) in open furnaces and released into the atmosphere. There are many other competing and side reactions taking place that we will not mention, but that the reader could explore further in the reference provided [6].

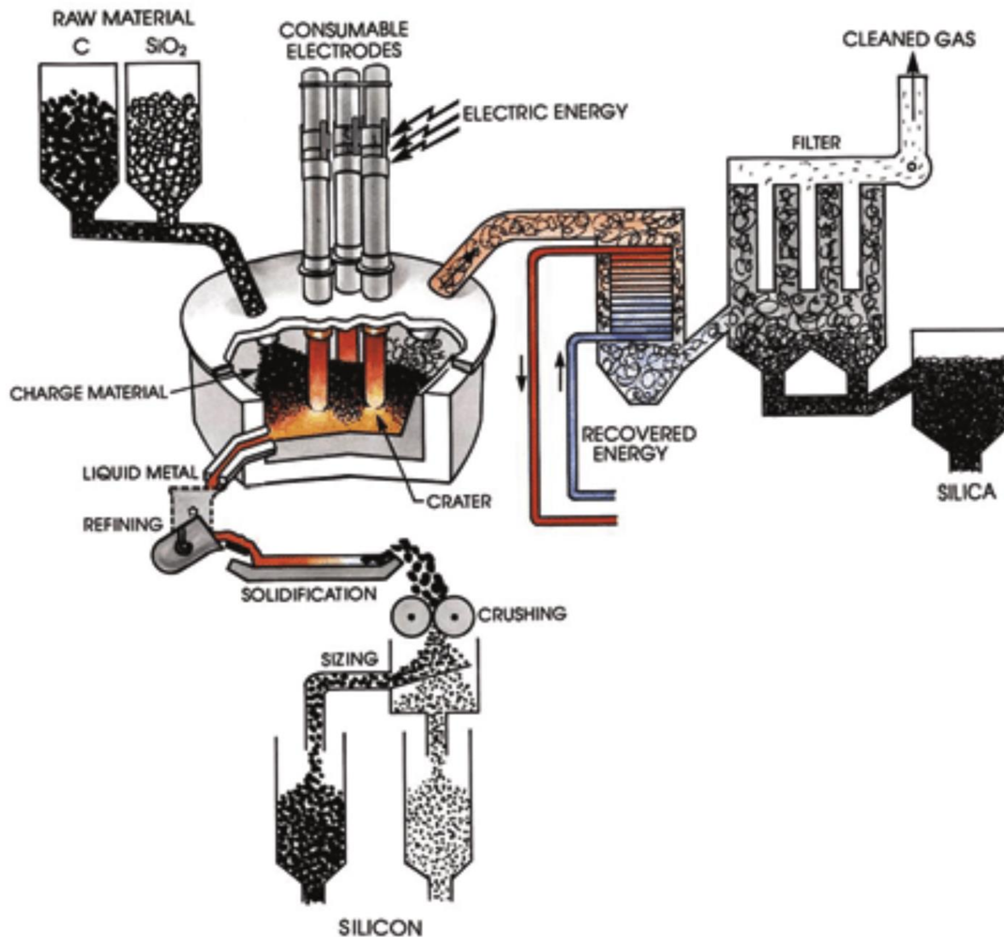


Figure 2-3: Typical metallurgical silicon production site process. Reproduced from [6].

After refining, solidification and crushing, the result is a solid silicon material with a purity between 96 to 98.5% of Si. This material needs to be further purified to be suitable to manufacture solar wafers.

Before going to the solar application, most of the silicon produced was to manufacture microchips for the microelectronic industry where the level of impurities allowed are in the ppt(a) and ppb(a) range. This hyper pure silicon material is what we call polysilicon as mentioned before, and the process most employed to manufacture polysilicon is the Siemens process.

2.1.1. Siemens process

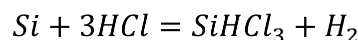
In order to achieve semiconductor properties in the silicon crystals ultra-high purity is required, this is achieved by creating a volatile silicon product that can be purified using fractional distillation. Once the product is highly purified the solid Silicon is obtained through a chemical vapor deposition.

To obtain the volatile silicon external reactants are required and several by products are obtained, that will need to be treated in order to be environmentally respectful.

This way the process to obtain polysilicon includes the following main steps (flow chart in figure 2.4):

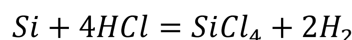
1. Produce volatile silicon
2. Purify the volatile silicon
3. Decomposition to elemental silicon
4. By-products treatment/recycling

The Siemens process is based on the use of Trichlorosilane (TCS) as the volatile silicon product, selected due to its high deposition rate, low boiling point (31.8 ^{0}C) and high volatility in comparison to Boron and Phosphorus, making it easier to reduce their content to the ppb level. The starting material of the process is MG-Si, that is introduced in a fluidized-bed reactor (FBR) where it reacts with Hydrochloric acid (HCl) to produce the TCS following the main reaction:



$$Si + 3HCl = SiHCl_3 + H_2$$

This step removes most impurities but we are still far from the level of purity required. The second step consists of a fractional distillation of TCS where a by-product, tetrachlorosilane (TET), is also produced due to the following compete reaction:



$$Si + 4HCl = SiCl_4 + 2H_2$$

In the first fraction of the distillation process low boiling point or heavier impurities are separated and in the second fraction the components lighter than TCS or volatiles are the focus.

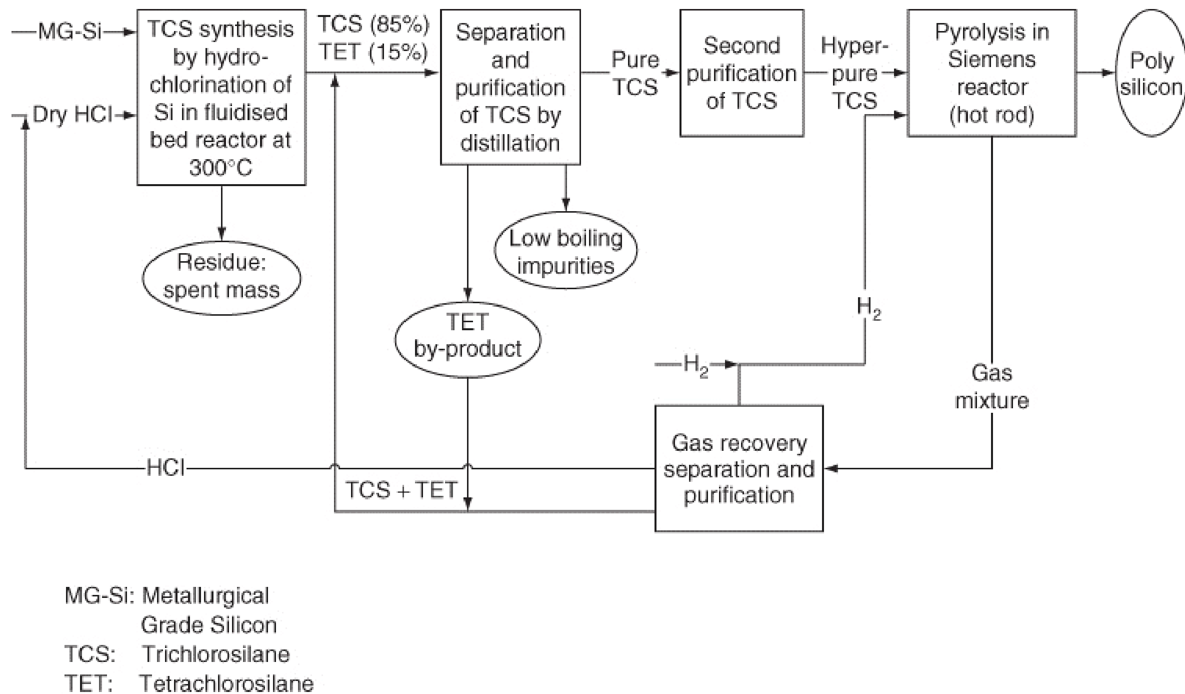
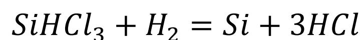


Figure 2-4: Schematic flow chart of the Siemens process. Reproduced from [7].

High purity TCS vapor is diluted with high purity hydrogen and introduced in a deposition reactor (figure 2.5) where it is broken down via the reaction:



$$SiHCl_3 + H_2 = Si + 3HCl$$

Silicon atoms from the vapor are deposited in a silicon starting seed consisting on electrically heated silicon rods at 1100 ^{0}C. This chemical vapor deposition process (CVD) produces thick rods of highly pure silicon that is our desired and final product. They are removed from the reactor and broken into solid polysilicon pieces as shown in figure 2.6.

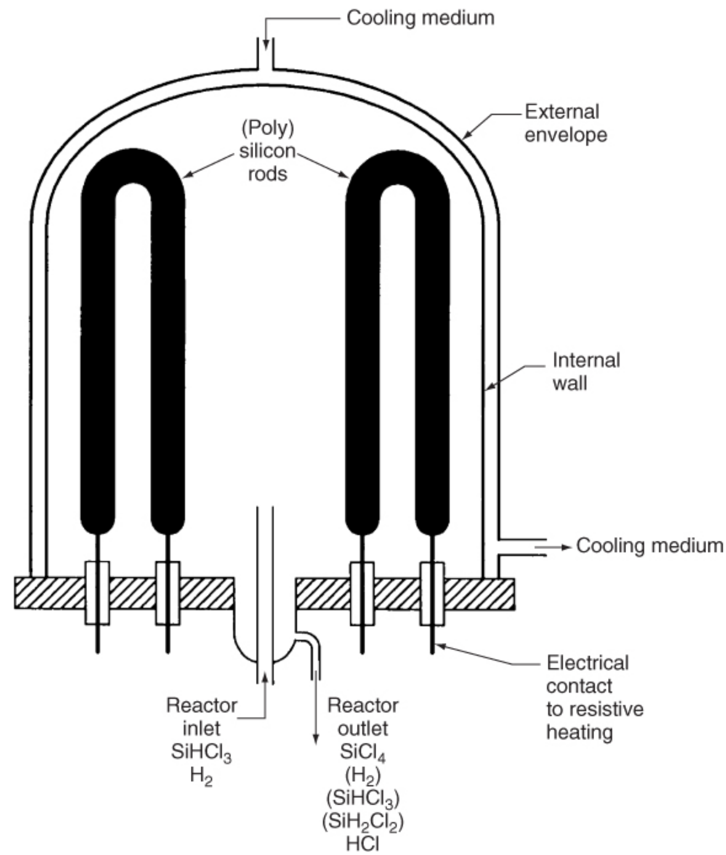


Figure 2-5: Schematic flow chart of the Siemens process. Reproduced from [7].

Figure 2-6: (a) Picture of a Siemens Reactor. (b) As grown polysilicon rods. (c) Final polysilicon chunks. Reproduced from [75].

Several processes have been developed as alternatives to the Siemens one to produce polysilicon being the most successful the Komatsu process based on Monosilanes instead of TCS and the Fluidized Bed Reactor (FBR) based on Silane. Both of them overcome some of the disadvantages of the Siemens process and both bring new issues too mainly regarding the purity of the material obtained. Today most of the industry employs the Siemens process, being the FBR process used too but much less due mainly to proprietary rights.

2.1.2. UMG manufacturing process

Traditionally, the silicon employed in the production of multi crystalline solar cells was originated mostly from waste obtained from the microelectronics industry.

However, considering the differences in silicon specification requirements for microelectronics and photovoltaics (PV), and the costs involved in the process, special emphasis has been given to the search for more economical routes for the production of PV silicon [8].

To manufacture polysilicon is 20 times more expensive than manufacturing MG-Si [7]. The purification process is complicated and very intense in energy consumption. High purity material is required to manufacture semiconductors for the microelectronics industry, we usually call it 9Ns silicon (purity of 99,9999999%) but for solar applications the purity required is not as high.

Thus, other sources must be investigated, including lower quality silicon obtained by purification of metallurgical silicon [9]. The metallurgical route for photovoltaic silicon production is one of the most promising ways of reducing silicon costs.

Starting as well from MG-Si but instead of using a complex chemical process as the one used to manufacture polysilicon, metallurgical processes are used to produce a material with good enough quality to produce solar cells, this material is what we call upgraded metallurgical grade (UMG) silicon and it has a purity level of 5 to 6 Ns (99,999%).

The minimum purity required by the solar industry is shown in table 2.2:

Table 2-2: Specification of chemical impurities in lowest-grade silicon for the solar industry. Table from [7].

Impurity	Specification
Fe, Al, Ca, Ti, metallic impurities	Less than 0.1 ppm(w) each
C	Less than 4 ppm(w)
O	Less than 5 ppm(w)
B	Less than 0.3 ppm(w)
P	Less than 0.1 ppm(w)

The composition of the main impurities of polysilicon used for the semiconductor industry or electronic grade silicon (EG-Si) are shown in table 2.3 together with the typical polysilicon employed in the solar industry. As we can see, the level of impurities using polysilicon as feedstock are much lower than the ones the solar industry admits to make good solar wafers. As a result, the manufacturers of wafers have been using different recipes of feedstock material mixing materials of different qualities using as less polysilicon as possible due to its high cost.

Table 2-3: Impurity limits for solar grade polysilicon (SG-Si) and electronic grade polysilicon (EG-Si). Table from [7].

Impurity	SG-Si	EG-Si
Tota metallic impurities (ppm(w))	<0.05	<0.001
Donor/phosphorous (ppm(a))	<0.005	<0.0005
Acceptor/boron (ppm(a))	<0.0005	<0.0001
Carbon (ppm(w))	<5	<0.1
Oxygen (ppm(w))	<5	<1

The UMG process is based on the segregation coefficient of the different impurities present in the silicon to remove most of the impurities but for B and P that have high segregation coefficients, as we will explain shortly. Starting from MG-Si and after cleaning it, the material is melted in contact with a slag-forming compound to reduce its B content through oxidation. In case of boron the basic principle of slag purification is the oxidation of boron at the Si/Slag interface, followed by the dissolution of the oxidized boron in the slag phase. This B removal step could also be done with plasma refining or gas refining following the same principle of oxidation of boron to gaseous compounds at high temperature, and volatilization of said compounds to the atmosphere. For the removal of P, vacuum refining is

effective thanks to P volatility. From a thermodynamics point of view, the principle of an effective removal of impurities from a liquid metal under vacuum at elevated temperature is the difference of the respective vapor pressure between the metal to be refined and the impurities. According to this approximation, dissolved impurities with higher vapor pressure than silicon are expected to evaporate away. After the slagging to reduce the B content in the material and the vacuum purification to reduce the P, the material is introduced in a directional solidification (DS) furnace where it is melted in an inert atmosphere (to avoid oxygen to be introduced in the melting silicon and also to minimize fire risks) and slowly solidified forming an ingot. Based on their segregation coefficients, different elements will have more appetite to stay in the liquid or solid phase this way impurities which appetite to stay in the liquid phase is high will not be present on the solid material and increase its concentration in the liquid one therefore being pushed to the top of the solid material, obtaining a material of different concentration of impurities along the ingot as shown in figure 2.7.

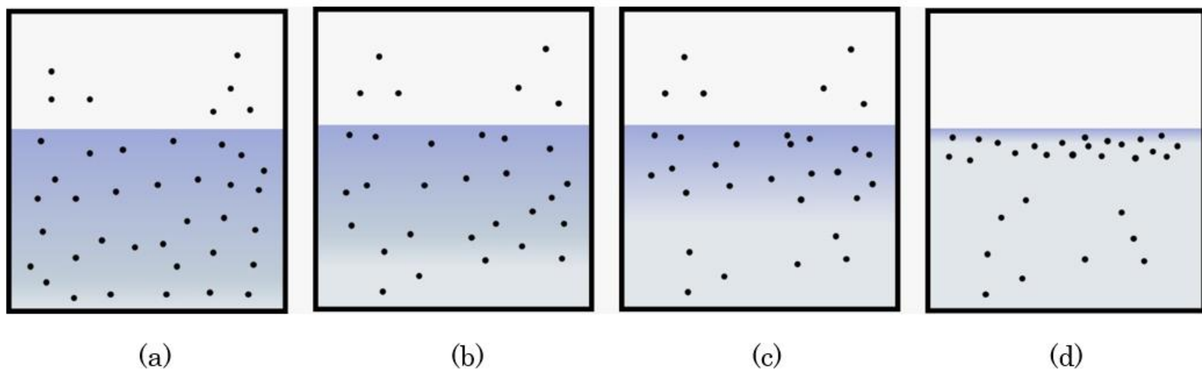


Figure 2-7: Schematic representation of the concentration of a low segregation coefficient component during the solidification process: (a) mainly liquid and starting solidification, same concentration of the component, (b) solid start to grow and small amounts of component staying in the solid (bottom) (c) less liquid than solid and component concentration high in the liquid, (d) almost all solid and high concentration of the component at the top of the solid.

When cooling a melt of composition X_0, it starts to solidify at its melting point T_0. At a lower temperature therefore (T_1) a fraction has solidified. At equilibrium the fractional compositions of the solid and liquid are X_s and X_l, respectively. The equilibrium distribution coefficient k_0 (also called segregation coefficient) at T_1 is defined as the ratio of the equilibrium solid and liquid compositions:

$$k_0 = \frac{X_S}{X_l}$$

A component with k_0 of 1 will have the same appetite to stay in the liquid as in the solid, if k_0 is bigger than 1 it will prefer to stay in the solid and if smaller than 1 the opposite, therefore a component with a k_0 very small will be subject to a high purification using this method, as represented in figure 2.7.

Table 2.4 shows the segregation coefficient of the main impurities at silicon melting point. Assuming that the interface solid-liquid is in equilibrium, meaning perfectly flat, of uniform composition and no diffusion the solidification equation of a component in an ingot of length L would be:

$$X_S(z) = k_0 X_0 \left(1 - \frac{z}{L}\right)^{k_0 - 1}$$

In practice the interface is not in equilibrium, as there is diffusion of different elements as well as convection and other effects that vary depending of the configuration of the furnace, the process, the solidification speed, the composition of the silicon feedstock, etc. Different models are built for each configuration to obtained a more precise solidification equation.

Table 2-4: Segregation coefficients of main impurities at silicon melting point at atmospheric pressure. Table from [7].

Element	k_0	Element	k_0
B	0.75	Ti	3.6×10^{-4}
Al	0.002	Cr	1.1×10^{-5}
Ga	0.008	Mn	1×10^{-5}
N	7×10^{-4}	Fe	8×10^{-6}
P	0.35	Co	8×10^{-6}
As	0.3	Ni	8×10^{-6}
C	0.07	Cu	4×10^{-4}
O	0.85	Zn	1×10^{-5}

This way, starting from MG-Si we can obtain a material after a direct solidification cycle that removes a significant amount of impurities with a simple process and that has a quality that is still not as good as the solar industry traditionally required but it is getting closer (table 2.5).

Table 2-5: Impurities in UMG-Si after one directional solidification. Table from [7].

Impurity	Upgraded silicon metal after one-directional solidification
Tota metallic impurities (ppm(w))	<1
Donor/phosphorous (ppm(a))	<5
Acceptor/boron (ppm(a))	<5
Carbon (ppm(w))	<50
Oxygen (ppm(w))	<100

The process can be further refined by removing more impurities through more DS cycles. There are processes applying chemical leaching, etc. The most common one uses a second step after one DS cycle to remove low segregation coefficient impurities, such as most metals and Phosphorus, where a remelting process in an Argon atmosphere is done using an electric arc furnace. The segregation of metallic impurities and phosphorus into the melt purifies the silicon to contain less than 500 ppm. This is known as UMG-2 material that again could be further purified using plasma or other techniques.

2.2. Silicon Wafers manufacturing

The two main aspects to control during the manufacturing of wafers are the impurities in the material and the quality of the crystal.

Not all impurities have the same effect, neither from the chemical or the mechanical point of view, both affecting the future behavior of the material. It is important therefore to differentiate between impurities in solid solutions and those existing as precipitates. The negative effect of impurities on solar cell efficiency present as solid solution may to a large extent be reduced by gettering [10]. Impurities in precipitates at grain boundaries and dislocations show less effect of

gettering and may act as impurity sources, leaking into the grains during heat treatments.

In order to control the level of dopant properly we need elements of group IIIA and VA of the periodic table to have concentrations on the material several order of magnitude below the dopant we will use, otherwise significant amounts of material will not be usable as it will turn from p-type to n-type. High levels of Boron make the future cells more inclined to suffer light induced degradation (LID) as it does the Oxygen content [11]. High level of carbon impurities might combine with silicon, producing SiC that if precipitate would produce significant issues during the sawing process due to its hardness. Transition metals are in general minority lifetime killers and should be carefully controlled.

The quality of the crystal itself is also very important to obtain the best possible efficiency as the density of dislocations influences the lifetime of the minority carriers and the future mechanical properties of the wafers. The main classification of silicon wafers attends to the mechanical property of the material and the quality of the crystal produced, thus we can manufacture mono crystalline or multi crystalline materials.

2.2.1. Mono crystalline silicon

The wafers manufacturing process acts as a purification step itself, since it melts the feedstock and grows it slowly into a crystal, so that the segregation coefficients come into play again making the material purer. In a mono crystalline silicon process the goal is to have at the end a material formed by just one crystal, getting rid of high density dislocations and of grain boundary recombination that decreases the minority carrier lifetimes.

There are several ways to manufacture mono crystalline silicon, the most extended by far is the Czochralski (Cz) method. The float zone (FZ) method is widely used in the microelectronics industry too, but not in solar. In FZ the silicon is melted without the use of a crucible but instead using a radio frequency field, this way the level of impurities of oxygen and carbon are minimized since the silicon is not contaminated from the crucible as it happens in the Cz method.

The Cz process (schematic in figure 2.8) consists of a chamber in which feedstock material, that is, polysilicon (or residues from previous growing process, as we will

see later) is melted in a crucible and a seed crystal is dipped into the melt as shown in figure 2.9. Then the seed is slowly withdrawn vertically to the melt surface, whereby the liquid crystallizes at the seed.

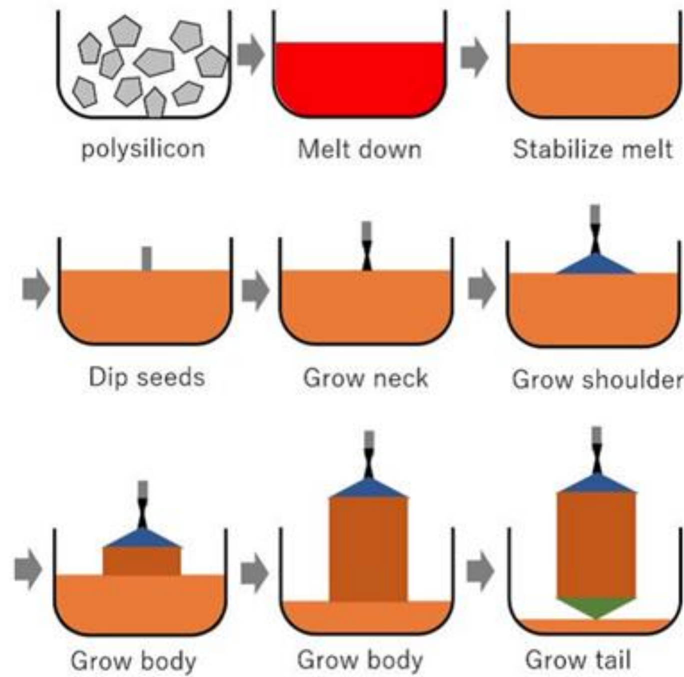


Figure 2-8: Schematic of the Cz process. Reproduced from [78].

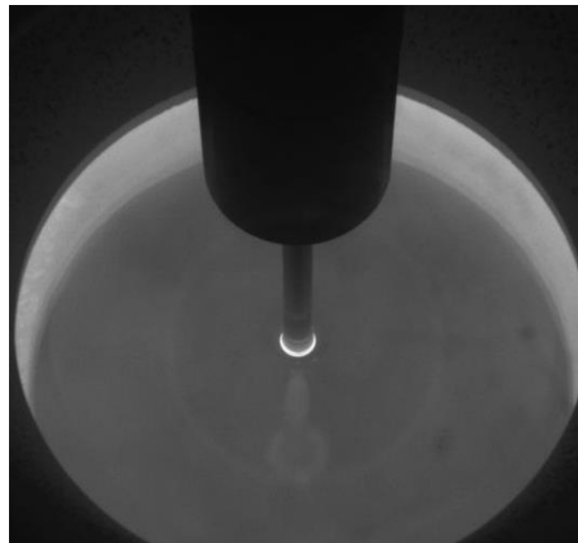


Figure 2-9: Seed dipping. Reproduced from [7].

In order to minimize the oxygen content, the process is done under an argon inert gas stream. After the silicon is completely molten, the temperature of the melt is stabilized to achieve the required temperature to lower the seed into the melt without melting the seed itself. The temperature must be chosen so that the seed is not growing in diameter (melt too cold) or decreasing in diameter (melt too hot). In PV the seed is usually <100>-oriented, is mono crystalline and is pulled upwards to grow a 'crystal neck'. Since dislocations propagate on [111] planes that are oblique in an <100>-oriented crystal, the dislocations grow out of the crystal neck after a couple of centimeters so that the rest of the crystal grows dislocation-free, even if the growth was started from a dislocated seed. The dislocation-free state of the grown crystal manifests itself in the development of 'ridges' on the crystal surface as shown in figure 2.10. If this state is achieved, the diameter of the crystal can be enlarged by slower pulling until it reaches the desired value. The transition region from the seed node to the cylindrical part of the crystal has more or less the shape of a cone and is therefore called the 'seed cone' (figure 2.11).

Figure 2-10: Ridges in the crystal surface of a dislocation-free ingot. Reproduced from [78].

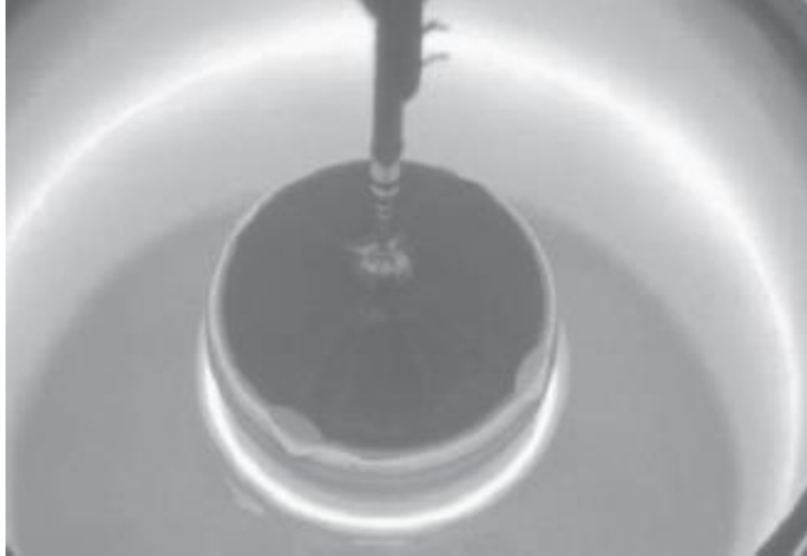


Figure 2-11: Growth of the seed cone. Reproduced from [7].

Shortly before the desired diameter is reached, the pulling velocity is raised to the specific value at which the crystal grows with the required diameter. Owing to the seed rotation, the crystal cross-section is mostly circular. In general, the pulling velocity during the growth of the cylindrical part is not kept constant but is reduced towards the bottom end of the crystal. This is mainly caused by the increasing heat radiation from the crucible wall as the melt level sinks. The heat removal of the crystallization thus becomes more difficult, and more time is needed to grow a certain length of the crystal. Standard pull speeds in the body range from 0.5 to 1.2 mm/min. The diameter of the crystal in PV typically reaches today between 200 and 300 mm [12]. A final mono crystalline ingot can be seen in figure 2.12.

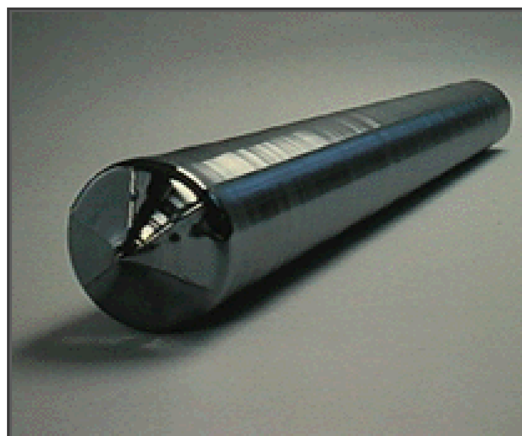


Figure 2-12: Mono crystalline ingot. Reproduced from [78].

To complete the crystal growth free of dislocations, the crystal diameter has to be reduced gradually to a small size, whereby an end cone develops. For this purpose, the pulling speed is raised and the crystal diameter is decreased. If the diameter is small enough, the crystal can be separated from the melt without a dislocation forming in the cylindrical part of the crystal. The withdrawal of the crystal from the residual melt can be done with a rather high velocity, but not too fast, because thermal shock would cause plastic deformation called 'slip' in the lower part of the crystal. The final crystal length is dependent on the crucible charge and varies between 200 and 400 cm [13].

Nowadays, the seed crystals used for Cz crystal growth are usually dislocation-free. However, each time the seed crystal is dipped into the melt, dislocations are generated by the temperature shock and by surface tension effects between the melt and the crystal. Normally these dislocations are propagated, or move into the growing crystal, particularly if the crystals have large diameters. The movement of dislocations is affected by cooling strain and faulty crystal growth.

After losing the dislocation-free state, the crystal continues to grow with a high density of dislocations that are usually arranged irregularly. With crystal diameters above 30 mm, the mono crystalline, but dislocated, growth is not stable and in most cases changes to poly crystalline growth because of the tendency of a Si crystal to form twins in the presence of strain and dislocations. These twins also multiply and form higher-order twins and thus rapidly form a polycrystal. This fine-grained poly-Si material is not usable for solar cell production. Known causes for the generation of the critical first dislocation are either solid particles in the melt that move to the solidification front, gas bubbles that are trapped at the solidification front, impurities that exceed the solubility limit in the melt, vibrations of crystals and melt, thermal shocks or a too high cooling strain.

The growth of the seed cone is the most critical stage in the pulling of the Cz crystal. For productivity reasons, very flat seed cones are preferable since the time needed to make the cone is not productive. However, the probability of introducing dislocations in the seed cone is lowest for tapered cones, although this means an increase in the pulling time by 15–25% for the same body length and additional loss in usable material. The loss of time and material gets worse for larger ingot diameters.

Owing to the reaction between the liquid Si and the quartz crucible, the crucible is of considerable importance to the growth. The silica of the crucible supplies considerable amounts of oxygen to the melt and, owing to the high purity of the silica, only small amounts of other impurities. However, the crucible tends to dissolve after a long time so that the risk for particles in the melt from the crucible is increased with increased pulling time. The oxygen of the melt adds up to 10^{18} oxygen atoms/cm^3 to the growing crystal, whereas carbon is usually $<10^{17}$/cm^3 and has only little impact on the solar cell performance. Oxygen effects such as thermal donors and precipitates can be well controlled in Cz cell processing.

Cz crystals can be grown from a wide variety of differently shaped and doped feedstock material. This enables the PV industry to buy cost-effective feedstock silicon with sufficient quality, even on spot markets. Since the feedstock is molten in a crucible, the shape, the grain size and the resistivity of the different feedstock materials can be mixed for the required specifications, although a given feedstock alone would fail. However, special care must be taken to avoid any macroscopic particles (SiO_2, SiC) that would not be dissolved in the melt, especially when pot scrap material is used.

The Cz process itself acts as a quality control step since proper crystallization, that is, dislocation-free growth of an ingot, can only take place in a well-defined process window. The homogeneity of a well-grown solar grade Cz ingot for PV application is excellent with respect to the bandwidth of electronic and structural properties, whereas mc-Si block casting produces specifications with higher variances in most parameters. Cell processes with Cz-Si can therefore use high-efficiency processes with smaller process windows that require well-defined starting material.

Cz technology is mature and cost-effective. Equipment (figure 2.13) and processes for semi-automated growing of crystals are commercially available so that several Cz pullers can be run by a single operator. Thanks to the robust construction of the machines, many Cz growers more than 20 years of age are still in production.

Figure 2-13: Commercial Cz puller. Reproduced from PVA Crystal Systems.

The fact that the ingot can be pulled in a defined <100> orientation is a big economic advantage since the solar cell process can use this crystallographic property to homogeneously texture solar cells with a very cost-effective wet chemical etching step. By anisotropic etching, a surface structure with random pyramids is built that couples the incoming light very effectively into the solar cell. This effect, together with the usually higher diffusion length of Cz crystals gives rise to the increased efficiency of Cz-Si solar cells compared with similarly processed mc-Si cells.

There exists a high potential for increasing the net pulling speed, that is, the productivity of a puller by a clever design of the hot zone, by sophisticated recharging concepts of Si in the hot crucible and by tuning the growth recipe to the optimum pull speed. For instance, most of the Cz growers nowadays already have a recharging system in their pullers so that we can grow longer ingots using the same crucible [76].

This is possible since the PV specifications are strongly reduced in the number of required parameters in contrast to microelectronic material. A PV specification 'simply' focuses on the maximum productivity, a minority-carrier diffusion length of the material that should exceed the cell thickness and a usually p-type doping that leads to a specific resistivity between 0.3 and 10 Ω cm, depending on the fabricated solar cell type.

One of the main disadvantages of Cz crystallization of silicon is the fact that square cells are best suited to build a highly efficient solar module, whereas Cz ingots have a round cross-section. In order to use both the crystal and the module area in the best manner, the ingots are usually cut into a pseudo-square cross-section before they are cut into wafers. Additionally, the tops and tails of the ingots cannot be used for wafer production since it is where the impurities concentrate. The cropped and slapped materials, that is, tops and tails and so on, are then fed back into the growth process again as feedstock.

The industry is shifting dopant from Boron to Gallium, the absence of boron in Czochralski-grown (Cz-Si) silicon relaxes the constraints for oxygen incorporation by avoiding the formation of Boron–Oxygen defects and hence light-induced degradation. Recent studies [79] reported significant advantages of Gallium doped wafers with the PERC cell technology also applicable to the latest TOPCon technology. It is important to mention that recently the industry is starting to see a shift towards N-type silicon, doped with phosphorus that also presents degradation advantages and higher minority carriers lifetime, resulting potentially in higher efficiencies.

2.2.2. Multi crystalline silicon

Multi crystalline silicon offers advantages over mono crystalline silicon with respect to manufacturing costs and feedstock tolerance at, however, reduced efficiencies. Another inherent advantage of multi crystalline silicon is the rectangular or square wafer shape, yielding a better utilization of the module area in comparison to the mostly round or pseudo-square mono crystalline wafers. The efficiencies of multi crystalline silicon solar cells are affected by recombination-active impurity atoms and extended defects such as grain boundaries and dislocations. A key issue in achieving high solar cell efficiencies is a perfect temperature profile of both ingot fabrication and solar cell processing in order to

control the number and the electrical activity of extended defects. Moreover, the implementation of hydrogen-passivation steps in solar cell processing turned out to be of particular importance for multi crystalline silicon. With the introduction of modern hydrogen-passivation steps by silicon nitride layer deposition, the efficiencies of industrial multi crystalline silicon solar cells were boosted to the 14–15% efficiency range and consequently market shares were continuously shifted towards multi crystalline silicon as the standard material of photovoltaics the last decades. Nowadays, these industrial efficiencies reached 22%, but the cost of polysilicon drop so dramatically that the difference of efficiency of 24% of today's mono crystalline modules makes it the most used technology with multi crystalline practically disappearing.

2.2.2.1. Ingot manufacturing

The main technology utilized in the manufacturing of multi crystalline ingots is the Bridgman process (figure 2.14) where the feedstock is introduced in a quartz crucible and melted inside a furnace in an argon atmosphere. To minimize the impurities from the crucible into the melt a silicon nitride (Si_3N_4) coating is usually applied to the crucible that prevents the silicon to stick to the walls of the crucible. Crystallization starts at the bottom of the crucible by reducing the temperature below the melting point (1410°C) of silicon, the temperature reduction is achieved by simply lowering the liquid silicon containing crucible out of the hot area of the crystallization furnace, or the opposite, elevating the hot area out of the standing crucible. After solidification starts in the bottom region, the crystallization front, that is, the liquid–solid interphase, moves in a vertical direction upwards through the crystallization crucible. This so-called directional solidification (DS) results in a columnar crystal growth and consequently adjacent wafers fabricated out of the ingots show nearly identical defect structures (grain boundaries and dislocations).

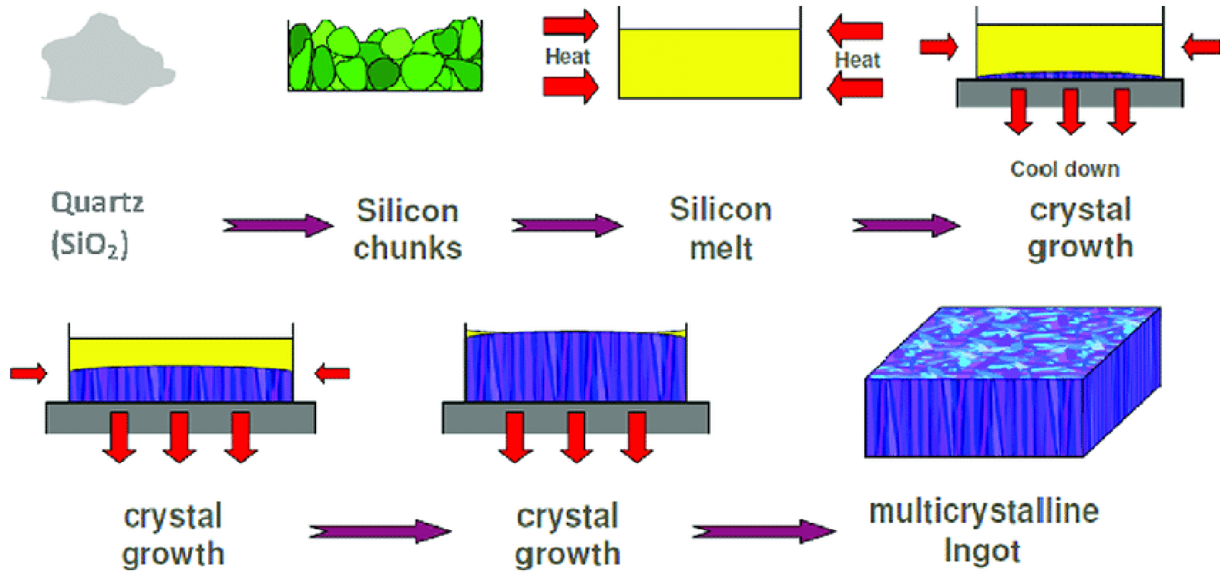


Figure 2-14: Schematic of a Bridgman process. Reproduced from [77].

Common crystallization speeds used for the Bridgman technology are in a range of about 1.5 cm/h (corresponding to a weight of approximately 25 kg/h for large ingots). With regard to the increase in crystallization speed, that is, productivity, mainly cooling of the already crystallized fraction of the ingot has to be taken into account. Too high process speeds cause large thermal gradients within the solidified silicon that may result in cracks or even destruction of the ingot.

Figure 2-15: DSS commercial equipment. Reproduced from DCWafers.

Robust automatic equipment is used in the commercial manufacturing process as shown in figure 2.15. The final product (figure 2.16) is multi crystalline silicon, a boron-doped p-type material with a specific electrical resistivity of about 1.5 Ω cm,

which corresponds to a boron concentration of about $1 \times 10^{16}/cm^3$. The specific resistivity is adjusted in a way such that optimal solar cell performance is guaranteed. Naturally, the boron concentration can be varied according to the requirements of specific solar cell processes. Specific resistivities in a range of 0.1–5 Ω cm have been used for solar cell fabrication so far. The boron concentration is normally adjusted by adding a choice of different boron sources to the silicon raw material prior to the melting of the silicon: the equivalent amount of B_2O_3; the equivalent amount of boron powder; or the equivalent amount of heavily doped Cz-grown silicon.

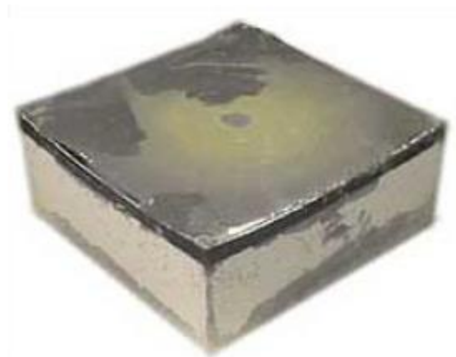


Figure 2-16: Multi crystalline ingot. Reproduced from DCWafers.

Thanks to the segregation coefficient, the dopant content profile will not be the same along the whole ingot height and so will be the resistivity. A key factor of the production to have a high yield is to control the dopant to compensate this effect and make sure that the most length of the ingot is within the required resistivity range.

The main impurities will come from the crucible and from the melted feedstock itself, as well as from the graphite heaters and will be purified based on their segregation coefficients as mentioned before so that a component with a low k_0 will be highly purified and otherwise will not. This way the main impurities of concern are oxygen, carbon and metals. Boron and our dopants are compensated during the doping process and have good segregation coefficients. Oxygen has a $k_0 > 1$ what means that the content at the lower part of the ingot will be higher than in the top parts. Oxygen is not electrically active but it is related to the light induced degradation (LID) of the modules and its content should be under control and the lowest possible. Carbon on the other hand can combine with Si and precipitate

creating needles of high hardness that can affect the slicing process into wafers and also create short circuits in the pn-junction of the solar cells, what we call shunt cells. Metals affect heavily the lifetime of multi crystalline silicon wafers but can be heavily reduced thanks to the low segregation coefficient of most of them and are one of the components that determines the growing speed, to ensure that they are properly purified.

The use of gallium as a dopant in multi crystalline cast silicon wafers has been proven to suppress the light-induced degradation of effective lifetimes [79] but one of the issues for the Ga-doped Si ingots is the very low segregation coefficient of 0.008, which introduces great variation on the ingot resistivity and the yield of the ingot. There have been several studies of compensation engineering [80] using gallium co-doping, also called tri-doping. This doping amins to minimize the resistivity range throughout the ingot and increases the yield considerably when casting ingots based on compensated silicon feedstock, however, with this method the concentration of impurities on the top of ingot is too high, which will affect reuse of those silicon materials.

2.2.2.2. Crystal defects

The main crystal defects in multi crystalline silicon are grain boundaries and dislocations. Concerning the attainable efficiencies of solar cells, not only the concentration of these defects but also their electrical activity is considered crucial.

With respect to the grain boundaries and the grain size, basically smaller grains are observed at the beginning of the crystallization process in the ingot bottom part. With increasing block height, individual grains prevail at the expense of surrounding grains and thus give rise to an increase in the mean grain size. This increase of grain size, however, depends on the crystallization speed. A higher crystallization speed also means higher temperature gradients and thus an increased probability for the formation of crystal seeds in the melt that in turn lead to a limitation of the grain size.

Grain boundaries and dislocations, if electrically charged, effectively attract minority charge carriers and consequently represent highly active recombination centers for photogenerated charge carriers. The electrical activity of grain boundaries and dislocations is determined by their impurity decoration (specifically by transition metals) and strongly increases with higher impurity concentrations.

Moreover, it was discovered that the shape of the crystallization front during solidification also has considerable influence on the grain boundary activity [14]. Preserving a strictly planar solidification front clearly leads to a reduced grain boundary activity. Also, because in modern high-throughput production processes a nearly perfectly planar solidification front is maintained throughout the crystallization process, grain boundaries show only weak electrical activities and therefore are generally considered as less important for solar cell efficiencies.

Crystal dislocations, however, turned out to be the most efficiency-relevant defects in multi crystalline silicon for solar cells. The dislocation density that is experimentally accessible by counting micrometer-sized etch pits after appropriate chemical etching steps shows a nearly perfect correlation to the wafer lifetime and diffusion length that are closely linked to solar cell performance. Dislocations are induced and multiplied by thermal stress that originates from temperature inhomogeneities during crystallization and cooling of the ingot. The reduction of these temperature variations while maintaining high process speed is therefore considered one of the most important issues for the further improvement of multi crystalline silicon.

An optimal process scenario for the production of multi crystalline silicon from both the crystal defect and the productivity point of view starts with a small crystallization speed and minimal temperature gradients in order to secure a low-defect-density bottom region of the ingot. After that, crystallization speed should be largely increased for productivity reasons while keeping the solidification front planar and thermal gradients within the solidified silicon low.

2.2.3. Cast-mono silicon

Mono crystalline silicon crystals can be grown in casting furnaces introducing a mono crystalline silicon seed at the bottom of the crucible. This is not trivial, it requires a very precise temperature control during the melting phase on such way that the feedstock gets fully melted and the seed is not melted but remains solid. The start of the growing process will initiate from the seed material and will be epitaxial, being the temperature control very precise not only to control very well the temperature gradient but also to minimize convection in the fluid, vibrations or any other kind of disturbances to the growth process, especially in the initial stages. Any disturbance would create dislocations that in the case of casting unlike

the CZ method will not grow diagonal and disappear but instead will grow in the <100> plane to the seed and will propagate along the whole ingot length.

The parts of the melt in contact with the crucible, the sides, will always grow multi crystalline, but the melt not in touch with the crucible can grow as a mono crystal as reported in many articles (figures 2.17 and 2.18) [15].

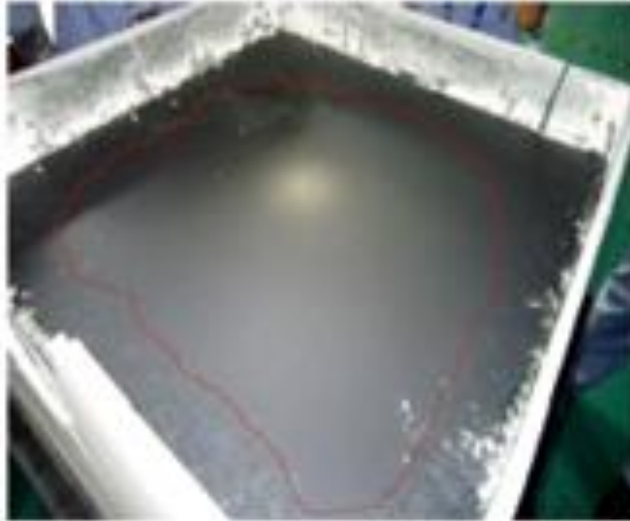


Figure 2-17: Cast-mono ingot, the red line marks the mono portion and the laterals multi crystalline. Reproduced from DCWafers.

This way when the ingot is cut into bricks, we can see that the bricks on the sides that were in touch with the crucibles have multi crystals and the inner ones far from the crucible are mono crystals along its length.

Figure 2-18: Bricks from different parts of an ingot showing a transversal cut. Red lines showing the multi crystalline due to the contact to the crucible walls. Reproduced from DCWafers.

Depending on the size and the number of seeds, the crystallization speed and process control the portion of the ingot that is a mono crystal will be different.

Figure 2-19: Several mono seeds charged in a crucible. Reproduced from DCWafers.

Even though a wafer might look a mono crystal its performance could be more similar to a multi crystalline one if the level of dislocations is very high, so the process focuses not only on producing a single crystal but one with very similar properties to a Cz one and with the same level of impurities and dislocations.

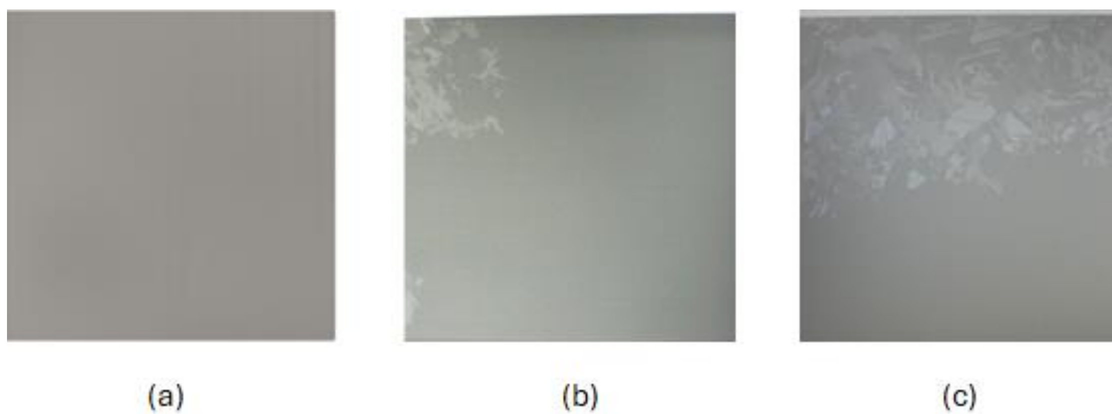


Figure 2-20: (a) cast-mono wafer (b) wafer with a small portion of multi crystals (c) wafers 50% mono crystalline and 50% multi crystalline. Reproduced from DCWafers.

Wafers with very similar properties as Cz ones can be manufactured using the cast-mono process [16] with a seed (figure 2.19), as shown in the pictures of wafers produced following this process in figure 2.20.

2.2.4. Wafering

The ingots produced by Cz and casting process are first cut into bricks. In this process the top and bottoms of the ingots are removed and recycled to go back into the growing furnaces as part of the feedstock after some purification or cleaning, especially in the case of the casting process where the bottoms and sides are in contact with the crucible.

This process of cutting into bricks is slightly different in a Cz ingot than in a casting one due to the shape of the ingot. In a Cz one the brick is converted into a pseudo square (they could also be cut full square recycling more material on the slabs and reducing the productivity, something that is done when polysilicon cost is low) while in the casting process the bricks are grown already squared and this step is not needed.

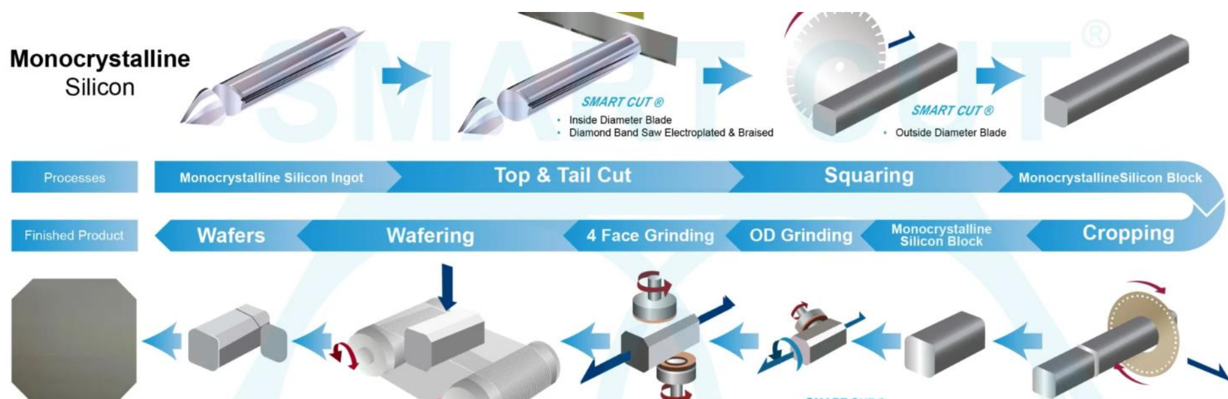


Figure 2-21: Schematic wafering process of Cz ingots. Reproduced from UKAM industrial superhard tools.

Instead in a casting brick the edges are chamfered so that there are low chances of chipping the corners of the future wafers.

A typical wafer size today is 210 mm. square and this is therefore the typical size of the bricks.

At the beginning of the PV industry, the available sawing technology of the microelectronic industry was used. The ingots were mainly cut by inner diameter

(ID) saws. This technology is, however, relatively slow and not economical for mass production [17]. It was therefore gradually replaced by the multi-wire slicing technology [18]. The process schematics can be seen in figure 2.21 for Cz wafers and on figure 2.23 for casting wafers.

2.3. MWSS fundamentals

The principle of the multi wire technology is depicted in Figure 2.22. A single wire is fed from a supply spool through a pulley and tension control unit to the two to four wire guides that are grooved with a decreasing pitch due to the wire degradation during the cut making the wire thinner. Multiple strands of a wire net (known as web) are formed by winding the wire on the wire guides through the 1000–1200 parallel grooves. A take-up spool collects the used wire. The wire is pulled by the torque exerted by the main drive and slave as shown in the figure. The tension on the wire is maintained by the feedback control unit at a prescribed value. The silicon column on the holder is pushed against the moving wire web and sliced into hundreds of wafers at the same time. Wafers for photovoltaic applications are mainly cut by a wire that is moving in one direction, whereas wafers for the microelectronic industry are cut by oscillating wires. Cutting in one direction allows higher wire speeds between 5 and 20 m/s, but yields less planar surfaces. Smoother and more even surfaces are obtained by oscillating sawing. Depending on the cutting speed (the so-called table speed, or speed at which silicon bricks move through the wires, an average of 0.3 mm/min), the wires have a length between 250 and 550 km in order to cut up to four columns in one run. The wire material is usually stainless steel.

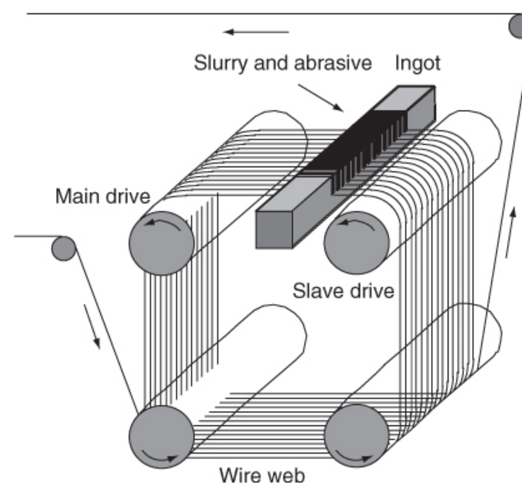


Figure 2-22: Schematic diagram describing the principle of the wire sawing [7].

Cutting is achieved by an abrasive slurry, which is supplied through nozzles over the wire web and carried by the wire into the sawing channel. The slurry consists of a suspension of hard grinding particles. Silicon carbide (SiC) is the most commonly used abrasive. SiC is very expensive and accounts for 25–35% of the total slicing cost. The volume fraction of solid SiC particles can vary between 20 and 60%, and the mean grain size between 5 and 15 µm. For polishing smaller grains sizes below 1 µm are used. The main purpose of the slurry is to transport the abrasive particles to the sawing channels and to the crystal surface. It also has to keep the particles apart and must prevent their agglomeration. The entry of the slurry is a result of the interaction between the wire and the highly viscous slurry. Usually, only a small amount of slurry enters the cutting zone. The two important factors here are the viscosity and the wire speed, but to understand the fluid mechanical problems is not trivial and still subject to continuous research looking for improvements [19].

Most of the commercial slurries are based on polyethylene glycol (PEG) as the carrying fluid and SiC as the abrasive element. The properties of the slurry are critical for a good quality cut and parameters such as granulometry distribution, humidity and viscosity are closely monitored by most of the wafer manufacturers. Both SiC and PEG are recycled up to 80% nowadays through different technologies, this being very important both from an economic and environmental point of view since very large quantities of slurry are used on every cut.

Material is continuously removed through the interaction of the SiC particles below the moving wire and the silicon surface. The abrasive action of SiC depends on many factors such as wire speed, force between wire and crystal, solid fraction of SiC in the suspension, viscosity of the suspension, size distribution and shape of the SiC particles. The viscosity of the slurry depends on the temperature and the solid fraction of particles. Since temperature rises as a result of the cutting process, the suspension has to be actively cooled and the temperature controlled during sawing. The viscosity of the slurry also changes because of the continuous abrasion of silicon and iron from the wire. This gradually degrades the abrasive action and the slurry has to be replaced or mixed with new slurry after some time.

The kerf loss and surface quality are determined by the wire diameter, the SiC particle size distribution and the wire transverse vibrations. The amplitude of vibration is mainly sensitive to the wire tension, but it also depends on the

damping effect of the slurry. Increasing the tension will reduce the amplitude of vibration, hence the kerf loss [20]. Typical wire diameters are 120 to 140 µm. With the mean size of active particles of 5 to 15 µm, this yields kerf losses around 150–200 µm per wafer.

The main issues related to the multi-wire sawing technology are the kerf loss, the expensive slurry consumption, the wafer breakage rates and the challenge to move to wafers below 180 µm thick.

The advantages are the higher throughput of about 8000–10000 wafers per day and per machine, a smaller kerf loss (material loss during the cutting process mainly related to the thickness of the cutting element) of 100–180 µm and almost no restrictions on the size of the ingots. Currently, wafers between 180 and 220 µm are usually cut using MWSS, but a wafer thickness down to about 100 µm can be achieved by the technique in the laboratory [19] and production of wafers as thin as 80 µm by multi-wire sawing has been reported [21], although the mechanical damage created by this technique makes the manipulation of these wafers very challenging and the next steps of the PV value chain would need to adapt their lines to minimize breakage rate.

The sawing process depends on several variable parameters that will be described in depth in chapter 4, which makes it difficult to optimize the process in view of throughput, material losses, reduction of supply materials and wafer quality. Basic knowledge about the microscopic details of the sawing process is required in order to slice crystals in a controlled way.

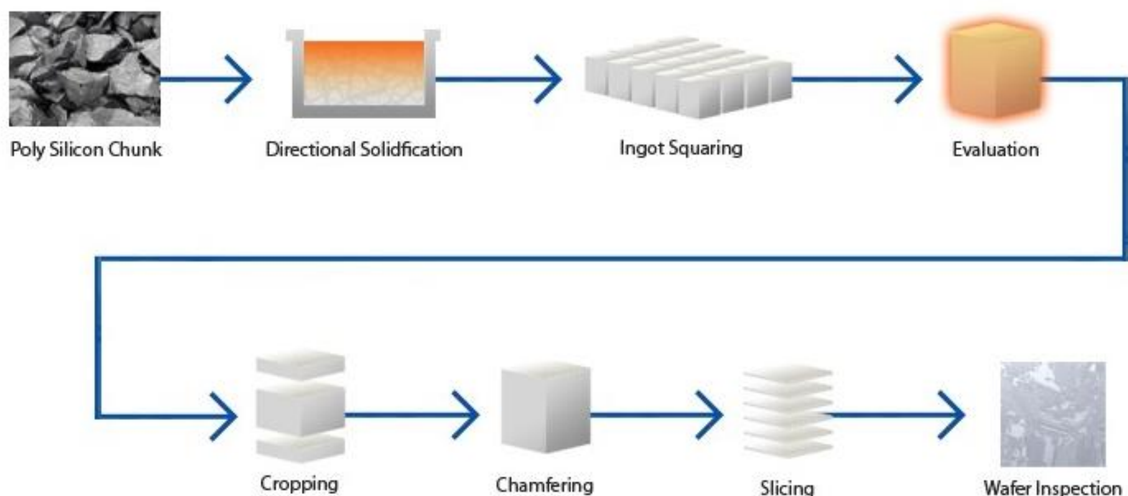


Figure 2-23: Schematic wafering process of casting ingots. Reproduced from Danen technologies.

Wafers thickness of 140 µm are the current standard thanks to the change from the MWSS to the diamond wire sawing (DWS), a fixed abrasive cutting technique that involves bonding and electroplating diamond particles onto a stainless-steel wire [22, 23] and where the PEG slurry is substituted with a water-based cutting fluid. Unlike the three-body material removal mode used in MWSS, DWS utilizes a two-body material removal mode between the diamond particles fixed on the steel wire and the material being cut. The abrasive grains do not roll, and the cutting efficiency can reach several times that of the three-body material removal mode.

DWS offers several advantages including smaller kerf loss, reduced wafer cost, and greater environmental friendliness.

2.3.1. Other technologies

There are many other ways to produce wafers beyond the ones named here but little by little they have been fading away. All of them pursue the same goal, minimize the cost by reducing the energy requirements of the process, increasing the throughput of equipment and minimize the kerf loss during the slicing process. The ribbon technologies were the most employed and had a time were they seemed to have a very high chance of succeed when polysilicon prices were very high. In the ribbon processes the kerf loss is minimal since the silicon is grown directly in wafer shaper instead of ingots and therefore the wafering process is minimal.

3. Wafer manufacturing and outdoor performance of UMG-Si modules

In this chapter we will evaluate the influence of the introduction of UMG silicon from three different suppliers and blended in different ratios with polysilicon in p-type multi crystalline silicon ingots for wafer production. To this purpose, five 430kg ingots were grown by directional solidification with UMG silicon percentages in compositions varying from 10 to 100%. Additionally, an extra ingot per each UMG ingot was grown as Reference, in the same conditions but UMG-Si was substituted by polysilicon. Each ingot was sectioned in 25 bricks, and each brick sliced into 156mm square wafers.

As we described, the metallurgical route is less effective at removing especially boron and phosphorus due to their high segregation coefficients, consequently there is often high and similar amount of both in such materials. This kind of materials is commonly called compensated silicon and its use in wafer production implies an increase of the phosphorous concentration with respect to the use of polysilicon.

Resistivity control in ingots using compensated silicon is difficult due to the different solid to liquid segregation coefficients of B and P, which produce a strongly varying resistivity along the mc-Si as we have seen before. Therefore, an important question for such purification techniques is the accepted level of compensation in order to grow an ingot with a rather homogeneous resistivity profile.

In order to evaluate the resulting quality, several parameters were analyzed (lifetime, resistivity, inclusions…), so that the effects on wafer quality and the influence on the yield can be reported.

3.1. Ingots and wafers manufactured using UMG-Si

As already mentioned, three different UMG-Si materials were tested, each one from a different supplier. The three materials will be referenced as A, B and C. Table 3.1 shows the boron and phosphorous concentration in each of these materials. These values were provided by the supplier together with the material.

Table 3-1: B and P contents of UMG material from different suppliers

	UMG-A	UMG-B	UMG-C
B (ppmw)	0.2	0.3	1.2
P (ppmw)	1.0	0.7	3.0

Five 400-430 kg ingots were grown by directional solidification in silica crucibles in the same conditions with UMG silicon in composition percentages ranging from 10 to 100% (Table 3.2). Together with this UMG material, a certain ratio of recycled silicon (tails, sides and wafers) was added to each ingot. Polysilicon was also added until completing the charge. B concentration is adjusted in each ingot by doping in order to maximize the yield and to get resistivity values between 0.75 and 2.50 Ωcm along the whole ingot to satisfy solar cell efficiency requirements.

Table 3-2: Composition of the five UMG ingots produced

ID Ingot	UMG-Si (kg)	Total Charge (kg)	Added B (ppmw)
10% A	43	428	0.089
10% B	41	429	0.041
10% C	43	431	0.071
25% B	108	430	0.032
100% A	400	402	0.289

Additionally, per each UMG ingot grown, we grew an extra ingot under the same conditions but without UMG Si for reference purposes. In Reference ingots, UMG silicon was replaced by polysilicon. Each ingot was sectioned in twenty five 156mm×156mm bricks, and each brick was cropped (top and bottom) and cut into

200±20 µm wafers. The quality of the ingots was evaluated according to several parameters such as lifetime, resistivity, and presence/absence of inclusions. Resistivity was measured by an Eddy current probe (SEMILAB RT 100) at different heights of the 25 bricks of each ingot. Lifetime was determined in a central and a corner brick by micro photoconductance decay (µPCD) using the equipment TELECOM-STV, MWR-2S-3. Infrarred (IR) images of the four faces of each brick were taken in order to detect micro grains or inclusions (mainly SiC or SiCN). Additionally, B and P concentrations in the melt in each ingot were evaluated from resistivity profiles, modeling these to the Scheil law by the least square method, using 0.8 and 0.35 respectively as B and P segregation coefficients [24]:

$$C_{net} = C_0(B) \times k_B \times (1-f)^{(1-k_B)} - C_0(p) \times k_P \times (1-f)^{(1-k_P)}$$

where

C_{net}: Net dopant concentration

$C_0(B)$ and $C_0(P)$: Boron and phosphorous concentration in molten silicon

K_B and k_P: Boron and phosphorous segregation coefficients

f: Solidified fraction

The ingots were sliced into wafers, and the quality of the wafers was evaluated according to "as-cut" lifetime measured by µPCD (SEMILAB WML-1), resistivity measured by Eddy current, and thickness and total thickness variation (TTV) determined by non-contact capacitive gauging (SEMILAB WMT-3). Wafers were also revised for the presence of microcracks, stains, holes, chips, saw marks, and other mechanical defects.

The yield was measured in two ways: first, as usable length of the bricks, i.e. the length of the bricks from each ingot which fulfils quality specifications: resistivity between 0.75-2.50 Ωcm, p type conductivity, lifetime higher than 2 µs, and absence of inclusions. Secondly, yield is also quantified as "good" wafers produced, i.e. the number of wafers produced per ingot which fulfill quality specifications: the same as for bricks, and thickness between 180 and 220 µm, total thickness variation (TTV) lower than 40µm and absence of mechanical defects (chips, saw marks, etc).

3.1.1. Ingot results

Figure 3.1 and 3.2 show the results of the lifetime and resistivity measured in the central and a corner brick of each UMG ingot, respectively. Central bricks are the ones considered of the highest quality as they are not in contact with the crucible and therefore have less impurities, while a corner brick is considered the lowest quality for being in contact with two walls of the crucible and therefore getting the highest level of impurities from it. Additionally, the lifetime vertical profile of the same brick from the corresponding Reference ingot was included to evaluate the effect of the introduction of UMG-Si in the lifetime.

Lifetime measurements for the central brick are always higher than for the corner brick because of the crucible. Impurities are incorporated from the crucible into the ingot causing a decrease in lifetime. When UMG lifetime profiles are compared with Reference ones, it can be appreciated that the introduction of UMG causes a reduction in lifetime, although the outcome is highly influenced by the UMG supplier and UMG concentration. If 10%UMG ingots (10%A, 10%B and 10%C) are compared, "C" material presents the worst results, with a notorious reduction in lifetime. On the contrary, the "B" material introduction hardly affects the lifetime with results similar to the Reference. When higher UMG concentrations were introduced (25% B and 100%A), the negative effects were further marked. However, worse results were expected for 100% A.

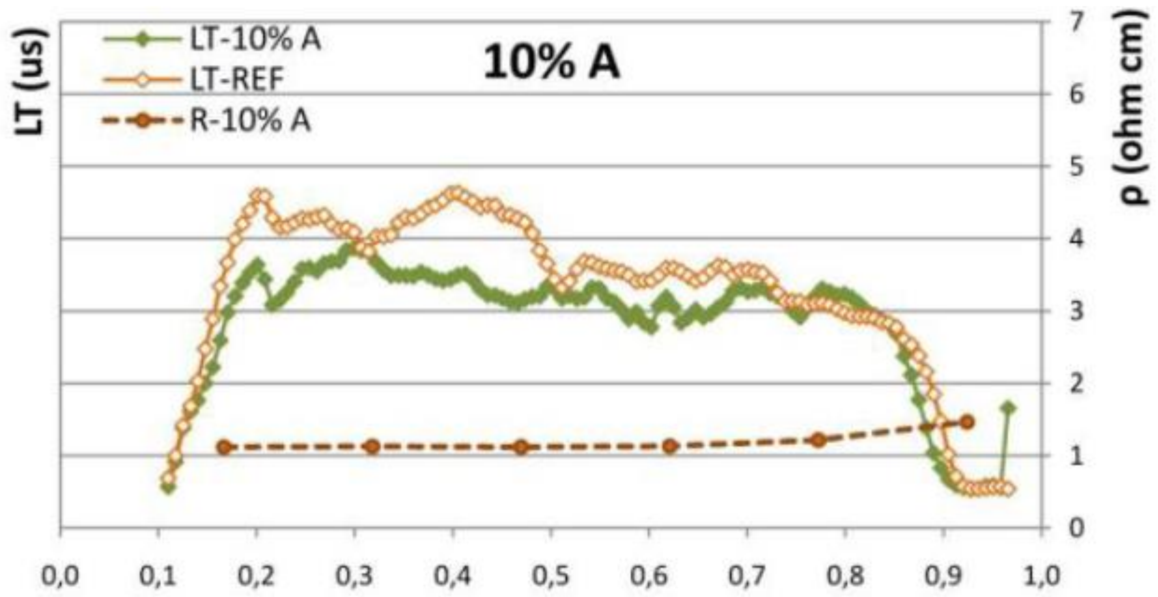
Resistivity profiles in UMG ingots are very important and they are determined by the B and P content in the ingot. Resistivity profiles are different for the central and the corner bricks. The reason is the shape of the interface during the solidification step, being the central part of the ingot the one that solidifies first, and the corners last.

Resistivity profiles for Reference ingots (not shown) are very similar for the five ingots, the resistivity in the bottom is around 1.6 Ωcm at f=0.1 and it decreases upwards until roughly 0.9 Ωcm at f=0.9. Resistivity profiles present a different pattern for UMG ingots due to a higher P concentration. The common behavior in these is an increase of the resistivity towards the top.

In some of the UMG ingots, compensation is even detected (10%C and 100% B) close to the top. In this region, resistivity is very high, because the B and P concentration are similar. Over this region, conductivity changes from p to n-type, and electron concentration is higher than holes; so, resistivity decreases abruptly. This has a negative effect in yield since the usable fraction of the ingot for wafer

fabrication decreases as the purpose is to manufacture p-type wafers. The usable length could be increased slightly by raising the B concentration in the ingots by doping, but at the expense of reducing the base resistivity, and the lower limit for this was fixed at 0.75 Ωcm.

Table 3.3 shows the B and P concentration in the melt of each ingot calculated from Scheil law. It is well known that in compensated ingots, the B and P concentrations estimated from the resistivity are different from those determined from chemical analysis, probably because B and P are not completely ionized in this kind of materials [25]. Even so, these values could be considered as an approximation. From these data, it can be noticed that 10%C and 100%A show higher B and P concentrations than the rest of the UMG ingots.


LT-10% A
LT-REF
R-10% A
10% A
LT (us)
ρ (ohm cm)
0,0
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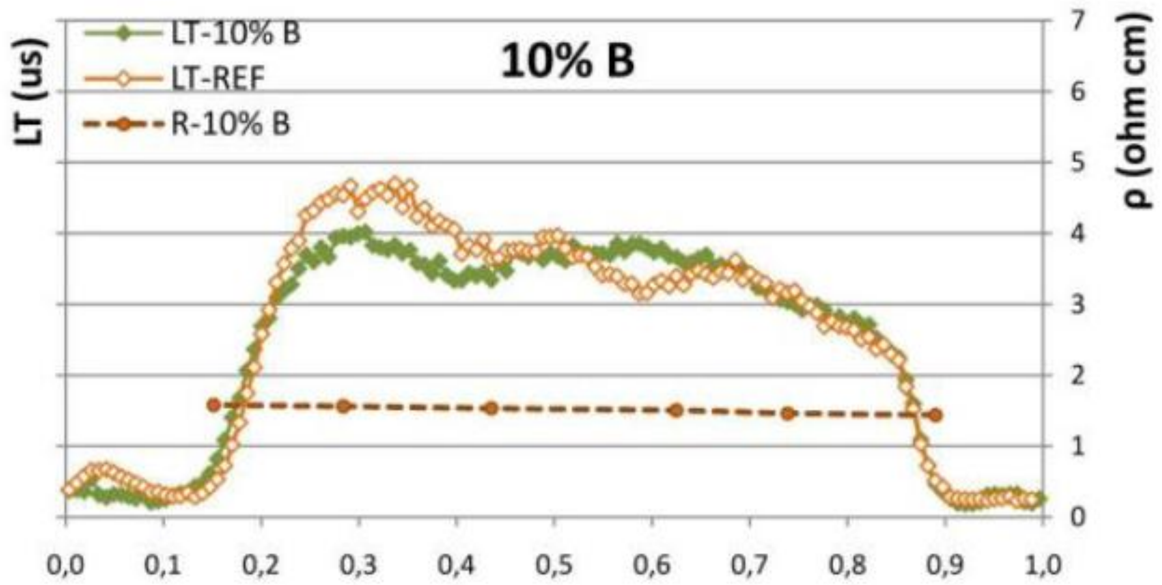
0,7
0,8
0,9
1,0


LT-10% B
LT-REF
R-10% B
10% B
LT (us)
ρ (ohm cm)
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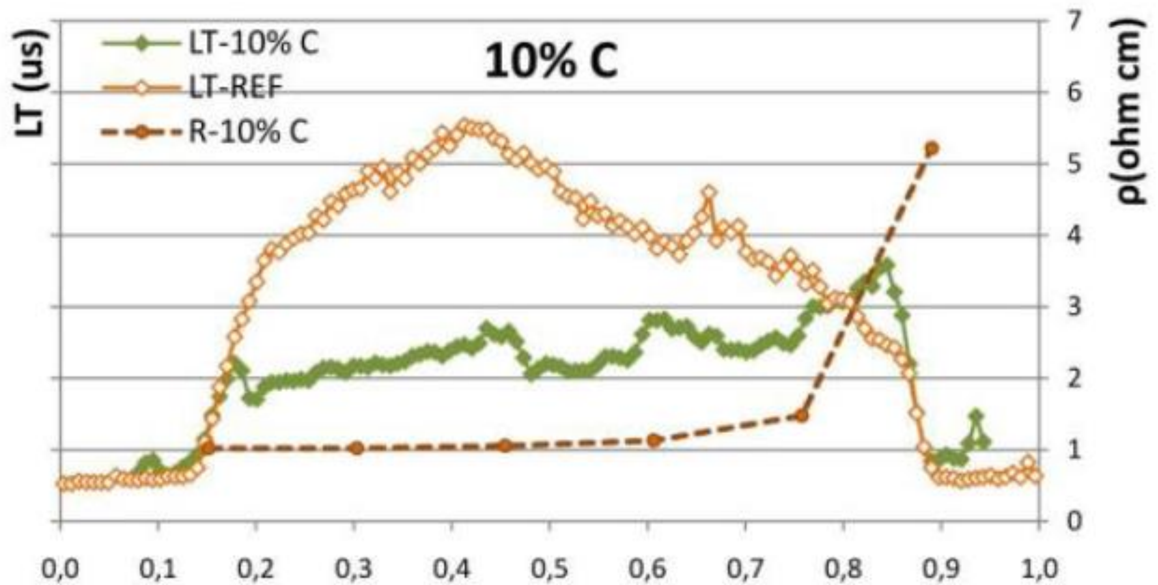
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LT-REF
R-10% C
10% C
LT (us)
ρ(ohm cm)
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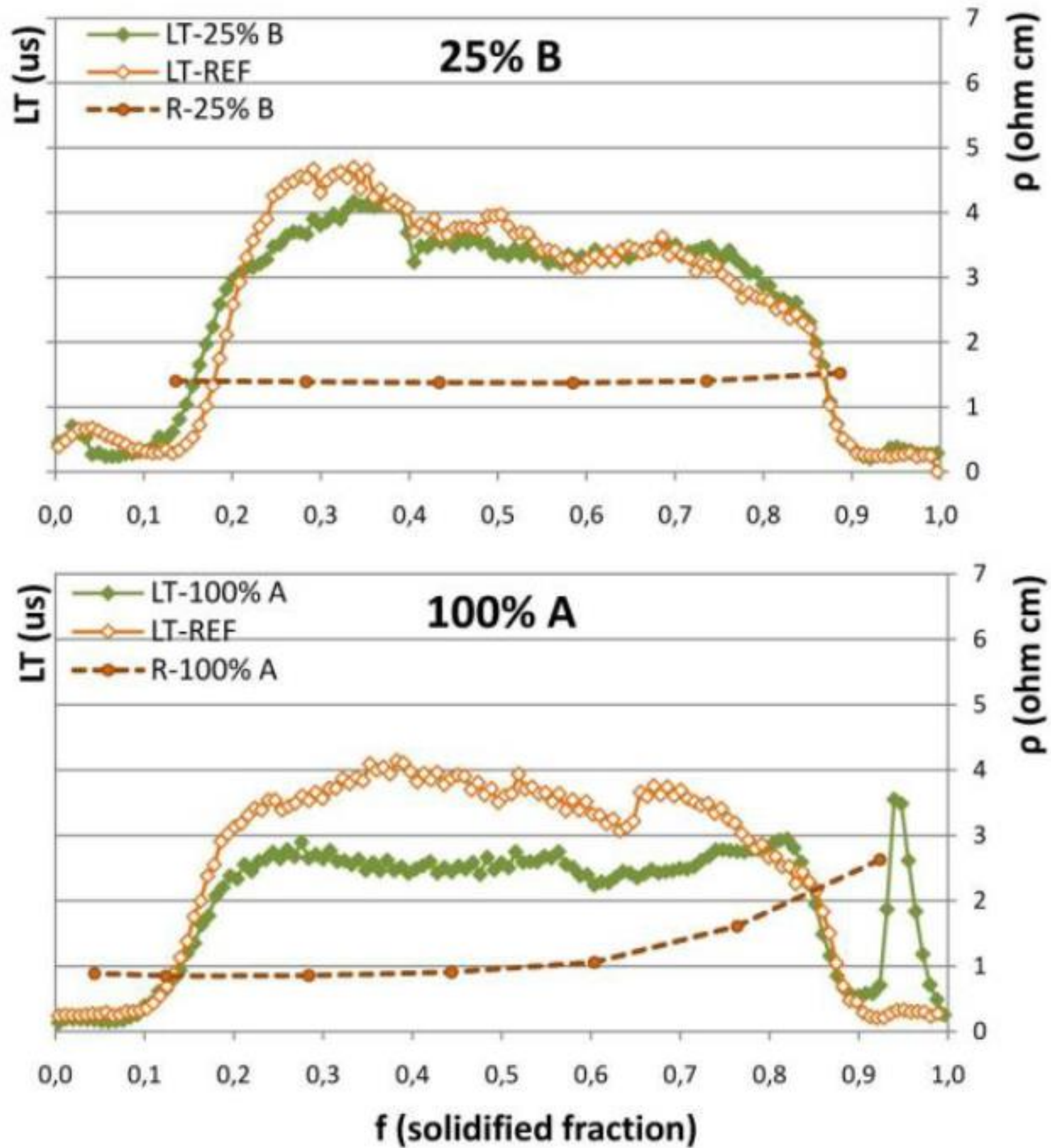
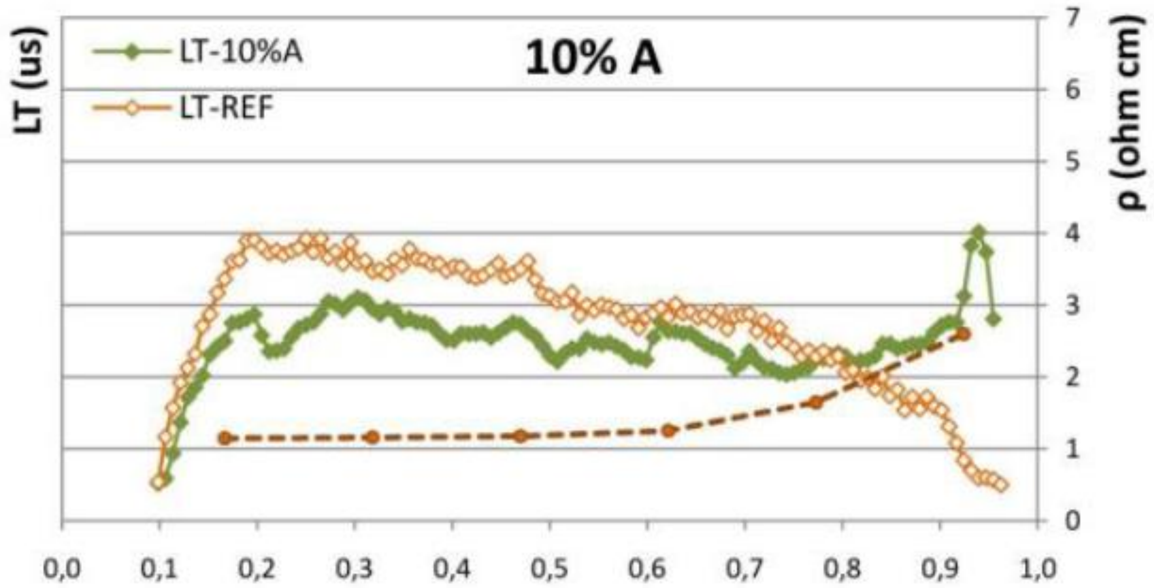


Figure 3-1: Lifetime (left y-axis) and resistivity (right y-axis) vertical profile for the central brick of each UMG ingot; and lifetime vertical profile for the same brick of the corresponding Reference ingot.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LT-10%A
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10% A
ρ (ohm cm)
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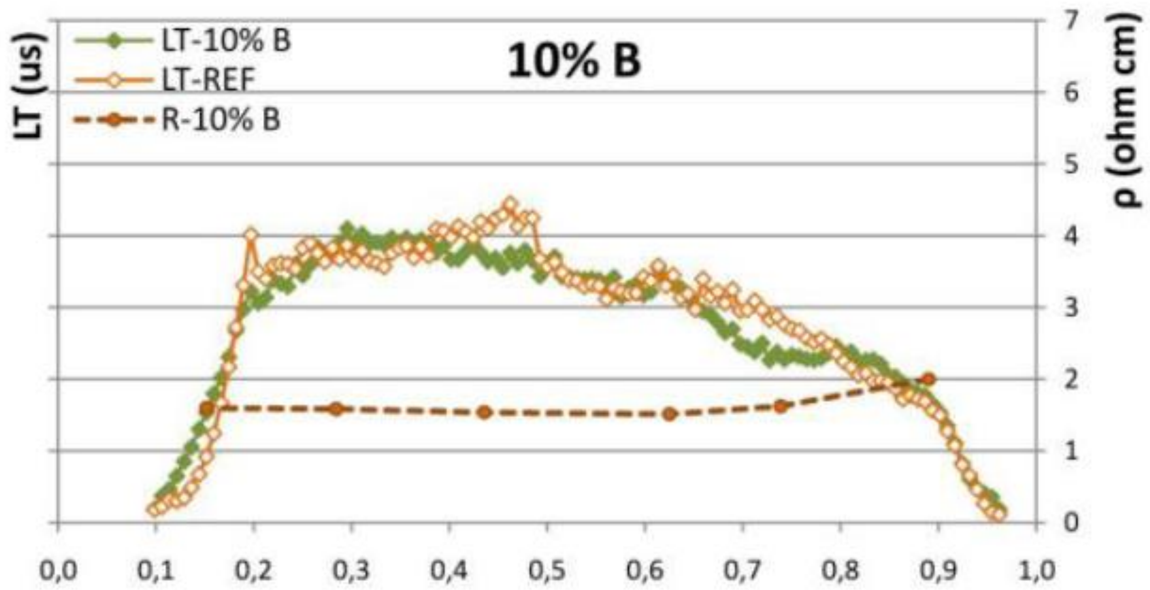
LT (us)
LT-10% B
LT-REF
R-10% B
10% B
ρ (ohm cm)
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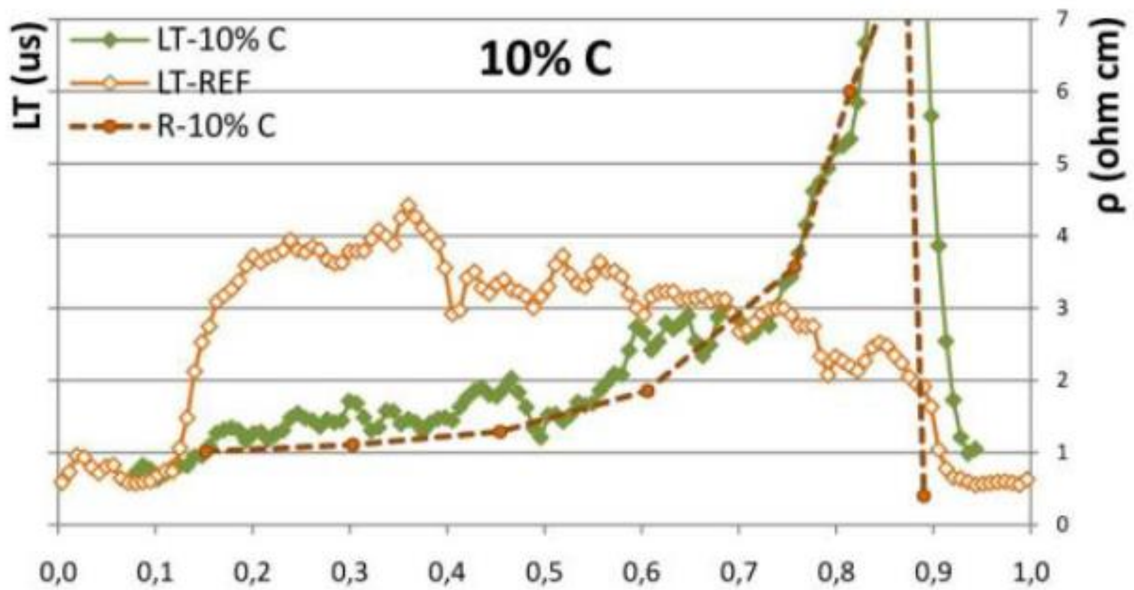
LT (us)
LT-10% C
LT-REF
R-10% C
10% C
ρ (ohm cm)
0,0
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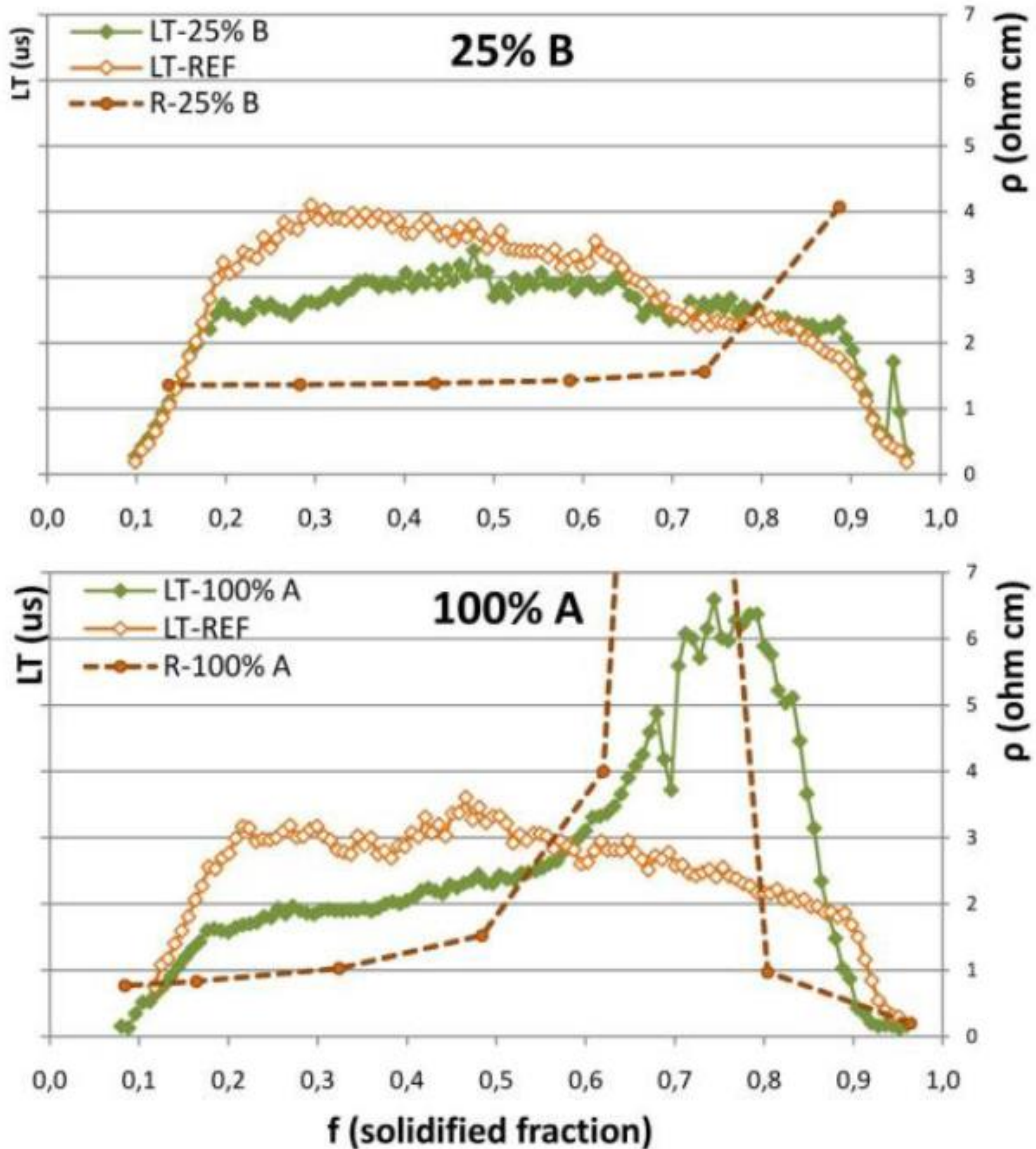


Figure 3-2: Lifetime (left y-axis) and resistivity (right y-axis) vertical profile for a corner brick of each UMG ingot; and lifetime vertical profile for the same brick of the corresponding Reference ingot.

Table 3-3: B and P concentration in the melt of the ingots determined from resistivity profiles and Scheil law.

ID Ingot	[B]melt ppmw	[P]melt ppmw
10% A	0.16	0.26
10% B	0.10	0.10
10% C	0.23	0.57
25% B	0.12	0.18
100% A	0.35	1.08

The compensation region is also associated with an increase of lifetime, even showing higher values than reference in this region. The reason for this is that the contribution of Shockley-Read-Hall (SRH) recombination in this region is lower, therefore the lifetime increases. The yield expressed as useful brick length is showed in table 3.4, where yield is expressed as the percentage of usable length in the test ingots, i.e. brick length used for cutting in wafers fulfilling quality specifications, with respect to the Reference ingot. All the ingots present lower yield than Reference, although the reduction is more intense in 10% C and 100% A ingots. The loss in these two ingots is caused by resistivity values higher than 2.5 Ωcm next to the top and by the more frequent presence of inclusions. Table 2.4 also shows the brick length rejected by the presence of inclusions in each ingot.

Table 3-4: Yield and rejected brick length by inclusions in each ingot.

ID Ingot	Yield %	Rejected brick length by inclusions mm
10% A	97	96
10% B	99	101
10% C	83	122
25% B	96	47
100% A	65	610

The introduction of UMG decreased the yield in the five ingots due to the higher P concentration; lifetime also decreased due to the higher impurity concentration in these materials. However, the effects depend highly on the UMG supplier and the concentration used in the feedstock. Adjusting correctly the resistivity in the UMG

ingot is basic, because by adding B it is possible to increase the yield, although at the expense of reducing the base resistivity.

3.1.2. Wafer results

All the wafers from each ingot were analyzed. According to the results only those wafers which fulfilled all the quality requirements were considered as "good" wafers. Table 3.5 shows the average values of lifetime, resistivity and thickness of the "good" wafers from each ingot. The average of resistivity (R) values was similar for the five ingots except for 10%B which shows a higher value (1.48 Ωcm). However, the resistivity distribution is different, although 100%A has an R average of 1.10 Ωcm, 60% of the wafers showed resistivity lower than 1 Ωcm.

Table 3-5: Yield and average of "as-cut" lifetime, resistivity and thickness of the wafers of each ingot.

ID Ingot	Yield %	LT µs	R Ω cm	Thickness mm
10% A	97	1.6	1.08	193
10% B	95	1.6	1.48	201
10% C	73	2.6	1.09	207
25% B	96	1.7	1.16	195
100% A	74*	2.2	1.10	198

On the other hand, "as-cut" lifetime for 10%A, 10%B and 25%B was similar and also similar to the Reference values, in contrast it was higher for 10%C (2.6 µs) and for 100%A (2.2 us). In figure 3.3, the lifetime of all the wafers from the central brick of 100%A and the corresponding Reference are shown, and it can be seen as 100%A wafers showed higher "as-cut " lifetime than Reference.

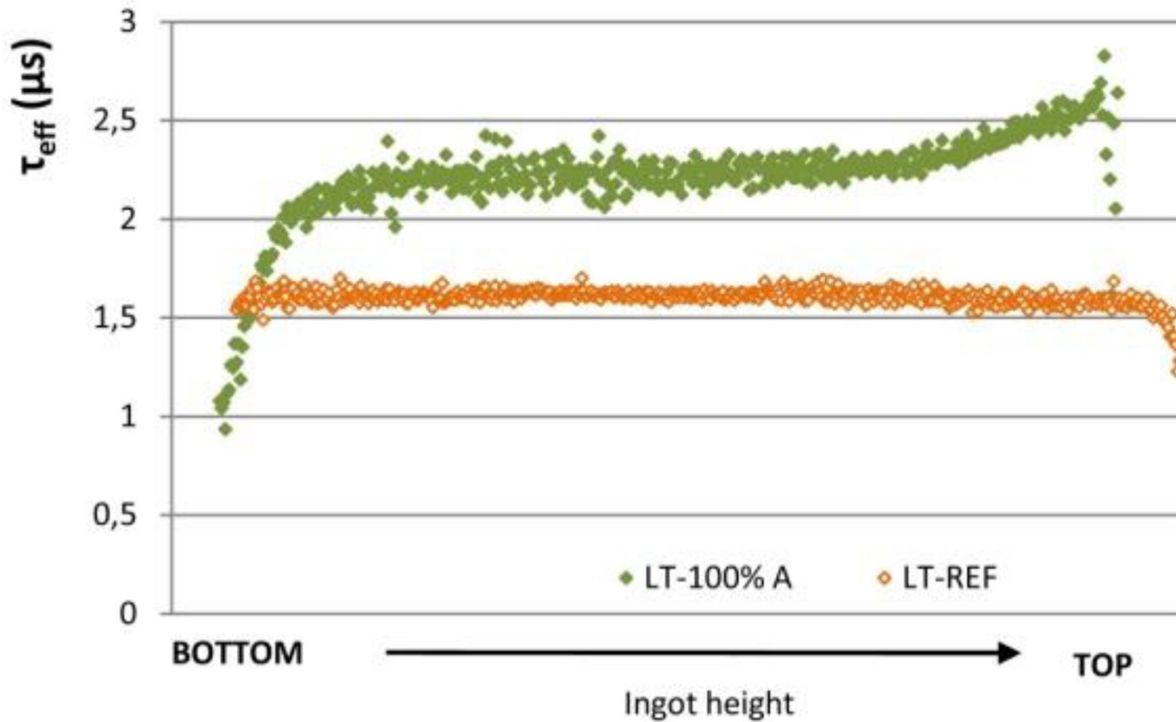


Figure 3-3: "As cut" lifetime of the wafers corresponding to a central brick of the ingots 100%A and Reference.

Due to the thinness of the wafers, it should be acknowledged that "as-cut" lifetime may suffer a significant reduction due to surface recombination [9]. Lifetime is a bulk property of the material, however when lifetime is measured in "as-cut" wafers the measured lifetime (τ_{eff}) depends on, apart from the characteristic lifetime of the material (τ_{bulk}), the thickness, the surface finish, and the diffusivity of the carriers. Therefore, it is well known that "as-cut" lifetime is not a good indicator of wafer quality. Considering that thickness average is similar for all the ingots, if we assume the surface finish similar too, and that 10%C and 100%A showed lower brick lifetime measurements, it seems that surface recombination would have to be lower in more compensated material, maybe caused by a lower mobility of the carriers in these materials [26], and thus, higher τ_{eff} are measured. However, this increase is not associated with an improvement in wafer quality. Finally, yield is also quantified as "good" wafers produced per ingot. This way of measuring the yield is affected by other factors not directly related with the composition, therefore it would not be such a good indicator of the effect of UMG introduction as the usable brick length. Nonetheless, table 2.4 shows the yield expressed as the percentage of "good" wafers obtained from each UMG ingot compared to the corresponding Reference. Again, 10%C and 100%A had the worst

results. Surprisingly, 100% A shows a higher yield than when the usable brick length was considered, although it is necessary to consider that only four bricks of this ingot were cut, and these bricks hardly had inclusions.

3.2. Evaluation of performance of standard and UMG multi crystalline silicon modules in outdoor conditions

The aim of this section is to compare multi crystalline PV modules based on typical solar grade polysilicon and UMG-Si feedstock, manufactured according to the same methods and technology, in a long-time outdoor testing. Very scarce literature can be found addressing this critical topic [81] for the PV industry.

Two modules, one composed of standard polysilicon cells and the other made of UMG-Si cells were placed side by side for long-term outdoor testing in real sun conditions. Detailed module monitoring through I-V and P-V curves was performed, acquiring data every two minutes. This allowed us to get an in-depth knowledge about the module's performance (efficiency, energy yield, etc.) in different operation conditions.

3.2.1. Manufacturing of the photovoltaic modules

The modules were manufactured using the same standard processes and equipment. mc-Si ingots were grown in DC Wafers, Spain, using a directional solidification process for both solar grade polysilicon and UMG-Si (CSSi ©, Silicio Ferrosolar-Ferroatlantica Group). The resulting silicon bricks were sliced into 156x156 cm^2 wafers. Resistivity values were in the range of 1.5-1.7 Ωcm and 0.7-1.0 Ωcm, for polysilicon and UMG-Si materials, respectively. Subsequently, they were transformed into cells using typical acid texturing and screen-printing technologies. To test the natural behavior of the devices, no intentional degradation was performed. The modules were assembled using cells from the same sorting bins. 3x20 cell strings coupled with the corresponding 3-diode junction box were designed to enable the modules comparison using the most common string configuration in the market. Both the cells and modules were manufactured at Instalaciones Pevafersa, S.L. The modules selected for this study were not "best of the class" modules. Both modules have a nominal power around 225W measured at STC conditions (Table 3.6).

Table 3-6: Electrical parameters of modules obtained from flash report at the factory.

Module type	Voc (V)	Isc (A)	Pmp (W)	Rsh (Ω)
Standard	36.81	8.09	225.0	139.8
UMG	37.17	8.08	226.0	48.7

3.2.2. Field test setup

A test bench consisting of a mechanical structure which faces modules towards the south with a 30º inclination is being used (figure 3.4). The testing venue is located at 40º22'N,5º45'W, altitude 1015 m. Both I-V and P-V curves were obtained by means of an electronic load (BK Precision 8510 and KEPCO BOP). The electronic load collects 20 samples for each curve in a sweep time of 20 seconds. The modules and the electronic load were sequentially connected using a relay box, so that individual curves can be obtained every 2 minutes. This system allowed one electronic load to be shared by several modules. Additionally, environment conditions were monitored by a custom-made weather station able to measure both horizontal and in-plane of array irradiances, with Kipp&Zonen CMP11 (secondary standard) and SPLite redundant pyranometers, besides wind variables (speed, direction, etc.) and modules temperature. All these variables were systematically measured every 5 seconds. The modules stayed in open circuit condition between measurements. No differences were found in I-V testing between the two electronic loads.

Figure 3-4: Modules placed in the test bench. The UMG one is the first from the left and the standard the third.

3.2.3. Field test results

After a full year of testing in outdoor conditions, the total irradiation measured in the test venue accounts 1750 kWh/m^2. The available data has been filtered in order to ensure that the conditions are exactly the same for both modules. In this way, the results presented here correspond to the same days of operation for both modules. The difference in irradiation received by the modules is less than 1%. The data used for the calculations accounts for more than 1200k Wh/m^2 of irradiation and represent every climatic conditions existing in the location.

The modules appearance through visual inspection and thermal imager test showed neither aging nor hot spots formation. The results presented here are divided into two categories: performance on a given day and energy production.

3.2.3.1. Daily performance

An example of the common behavior exhibited by the modules on a typical summer day is shown in the figure 3.5. One can observe the irradiance in plane of array, ambient temperature, maximum power and short circuit current evolutions. At first sight, a close behavior between both types of modules is evidenced. At noon, the short circuit current is slightly over its value at standard test conditions, due to the high temperatures, and for the same reason the maximum power decreases to 0.8 times the nominal value despite the irradiance being near 1000 W/m^2. The performance of the modules is dominated by the large variation with temperature of open circuit voltage and fill factor (FF), accounting for most of the power loss. The overall behavior is very similar, with the only difference of the open circuit voltage being a bit higher for the UMG-Si module.

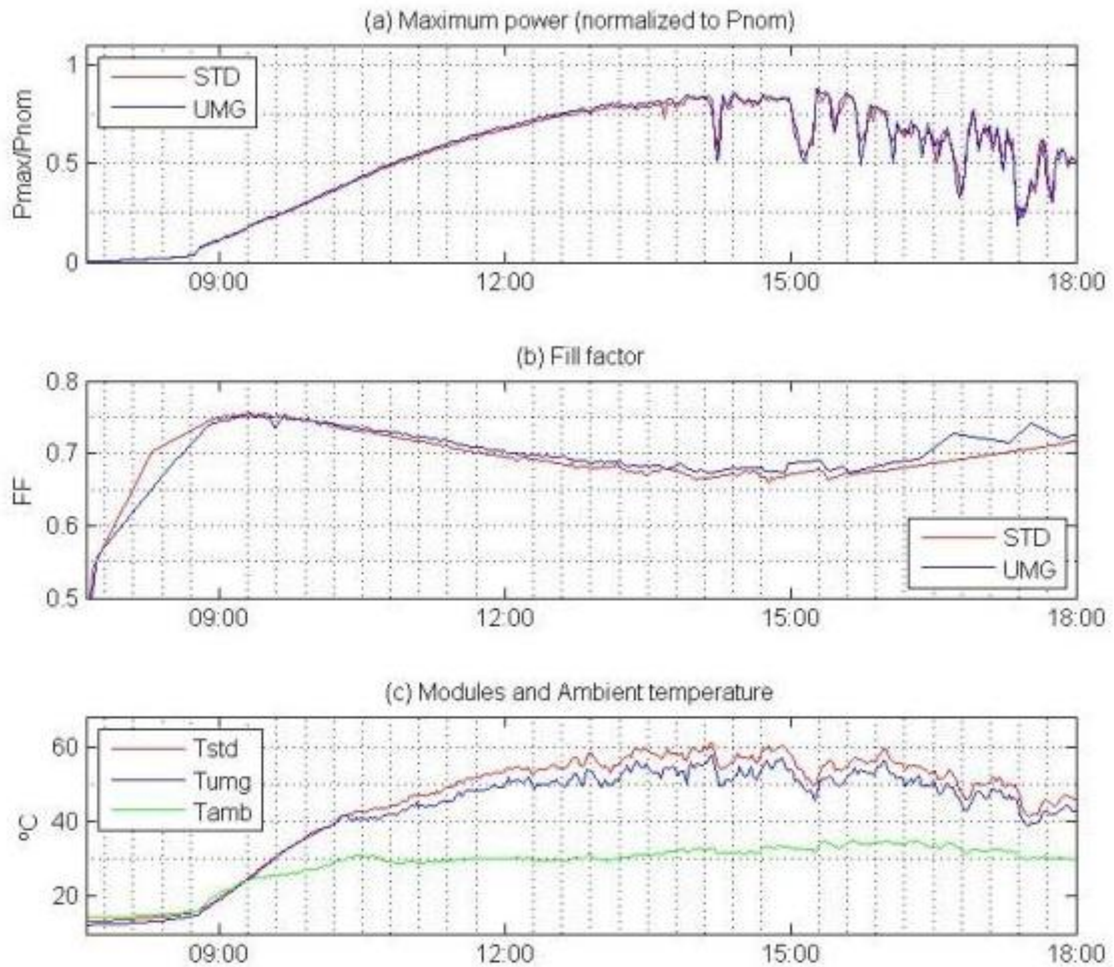


Figure 3-5: Daily evolution of more relevant parameters in a summer day: maximum power (a), fill factor (b), ambient and modules temperatures (c).

Interesting was the comparison of the module's performance at different levels of irradiation, on a clear day (figure 3.6).

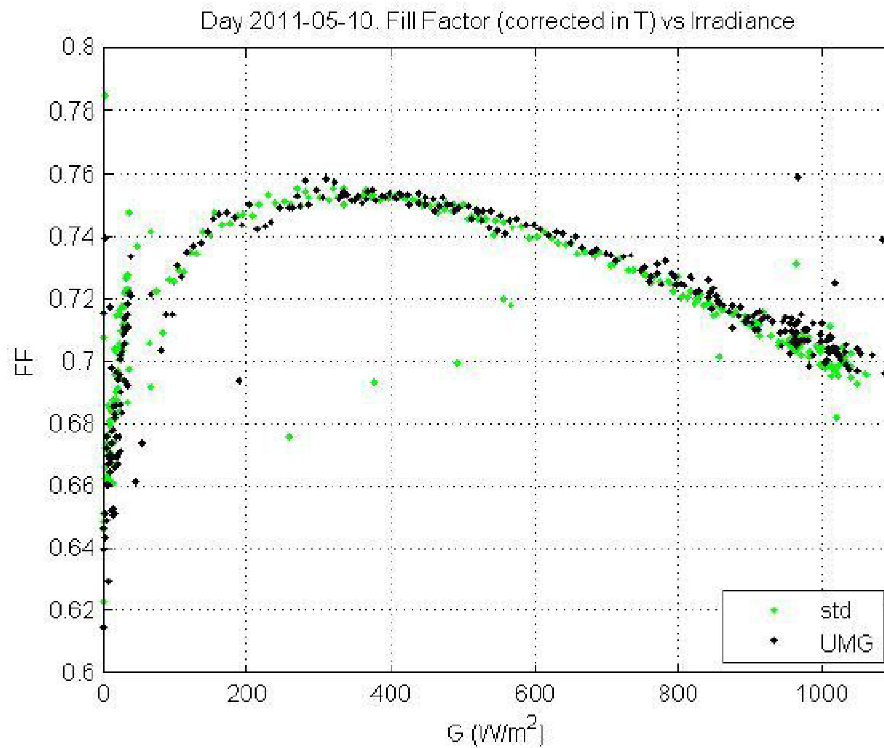


Figure 3-6: Low light performance. Fill Factor vs irradiance.

Usually, this performance is characterized by plotting the relative efficiency *vs* irradiance. This procedure is very simple and very suitable for using it with solar simulators. However, in outdoor testing, the analysis of the relative efficiency is tricky to deal with. Solar light features, such as the influence of the angle of incidence and the direct/diffuse irradiance ratio can lead to detect large differences between clear and overcast days. On the other hand, the modules' performance at low light levels can be better described by the fill factor (FF) [27], as it does not entail as much filtering approaches as in the case of relative efficiency. Furthermore, it is more robust to changes in the spectrum of incident light [28]. Still, the evolution of the FF for both modules showed no important differences, as illustrated in figure 3.6.

3.2.3.2. Energy production

Regarding the energy produced by the modules, in figures 3.7 and 3.8 we show the daily differences in the performance ratio between the two modules during the first year of exposition and in relation to the daily irradiation. This performance ratio (PR) of the modules is calculated as the relation between the actual energy

produced according to the instantaneous P_{mp} exhibited and the final energy generated as a result of the received irradiation, considering its nominal (rated) peak power [29].

$$PR = \frac{\sum Pmeas}{\sum P_{STC} \times \frac{G_{meas}}{G_{STC}}} \times 100$$

where

PR: Performance ratio

P_{meas} and P_{STC}: Power measured and power at standard test conditions (1000 W/m^2, 25^0C, 1.5AM)

G_{meas} and G_{STC}: Irradiation measured and irradiation at standard test conditions

In figure 3.7 the difference in Performance Ratio (PR) of the standard and the UMG-Si module is plotted for each day of testing. The differences in the PR are small but a seasonal variation can be clearly observed. In fact, the trend shows that the standard module is usually performing better between October and March, and the UMG-Si one in summer. So, the UMG-Si module exhibits a better behavior in summertime, whereas the standard one exhibits an improved performance in winter. This can be ascribed to the different temperature coefficients of each module [30] (table 3.7).

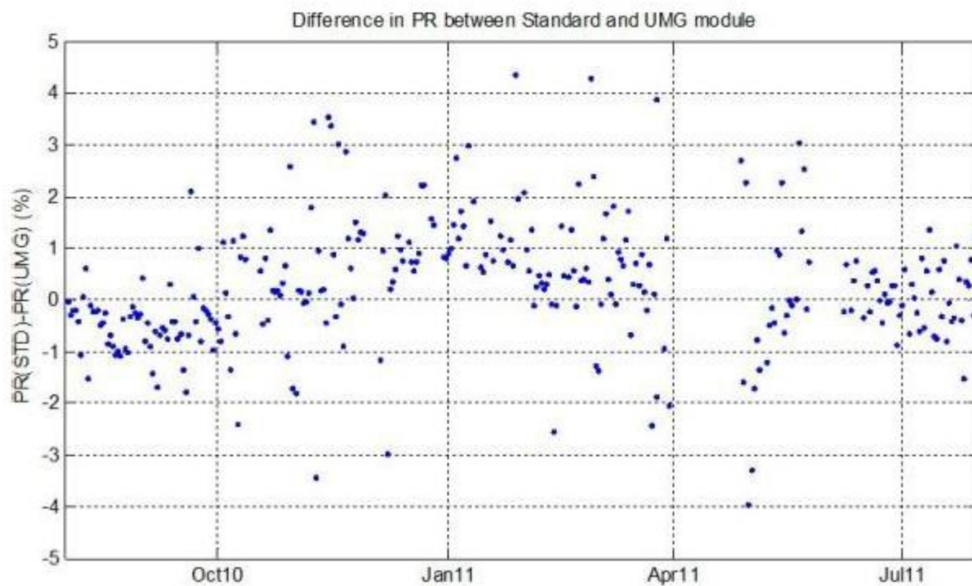


Figure 3-7: Difference in Performance Ratio of modules during the full year.

Table 3-7: Measured coefficients of temperature for both modules.

Module type	Standard	UMG
α (% / K)	$4.96\ 10^{-4}$	$6.87\ 10^{-4}$
β (% / K)	$-3.34\ 10^{-3}$	$-3.12\ 10^{-3}$
ϒ (% / K)	$-4.69\ 10^{-3}$	$-4.1\ 10^{-3}$

In order to clarify this effect, we have plotted in figure 3.8 the difference in PR between the standard and the UMG-Si module vs the daily irradiation. The trend is again clear, showing that the summer days (higher irradiation) the UMG-Si performs better and the winter days (lower irradiation) the standard is a better performer. There are some days apart from this trend, but this can be explained by the natural climatic variability: a cloudy summer day and a sunny winter day can have the same irradiation but the performance is very different.

Figure 3.9 represents the daily yield for eight months of exposition. It can be seen that some days the yield can be even slightly higher than 1. This comes from the combination of low temperatures (in some cases, below 25ºC) and an improved response to irradiances in the 300 W/m² range. After a full year of data collection, the overall energy yield was just under 1% lower for the UMG-Si module (Table 3.8). This small difference can be considered to be inside the experimental error limits, so it can be concluded that both modules have been performing in a totally comparative way.

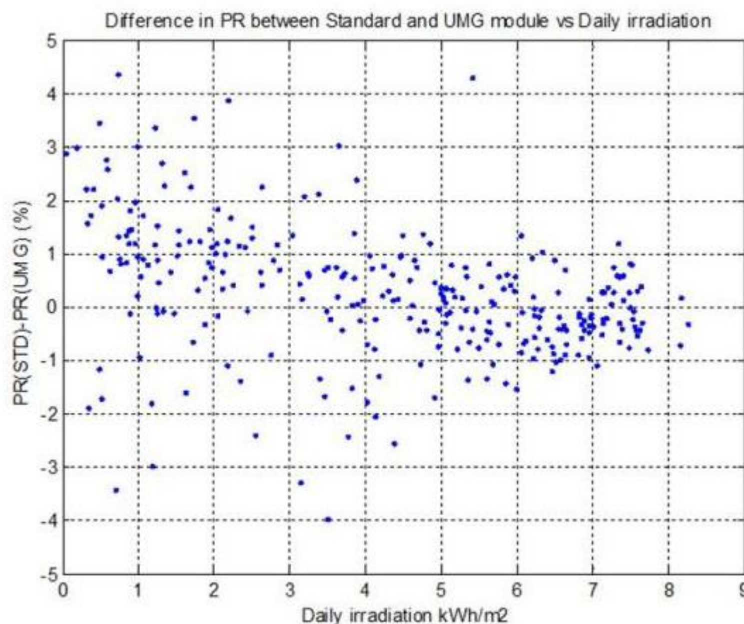


Figure 3-8: Difference in Performance Ratio of modules versus daily irradiation received.

Table 3-8: Summary of the module's energy production.

Module Type	Standard	UMG-Si
Total Irradiation received (kWh/m2)	1235	1216
Ideal Production (kWh)	277.9	273.6
Real Production (kWh)	247.2	242.1
Global Yield	88.97%	88.50%

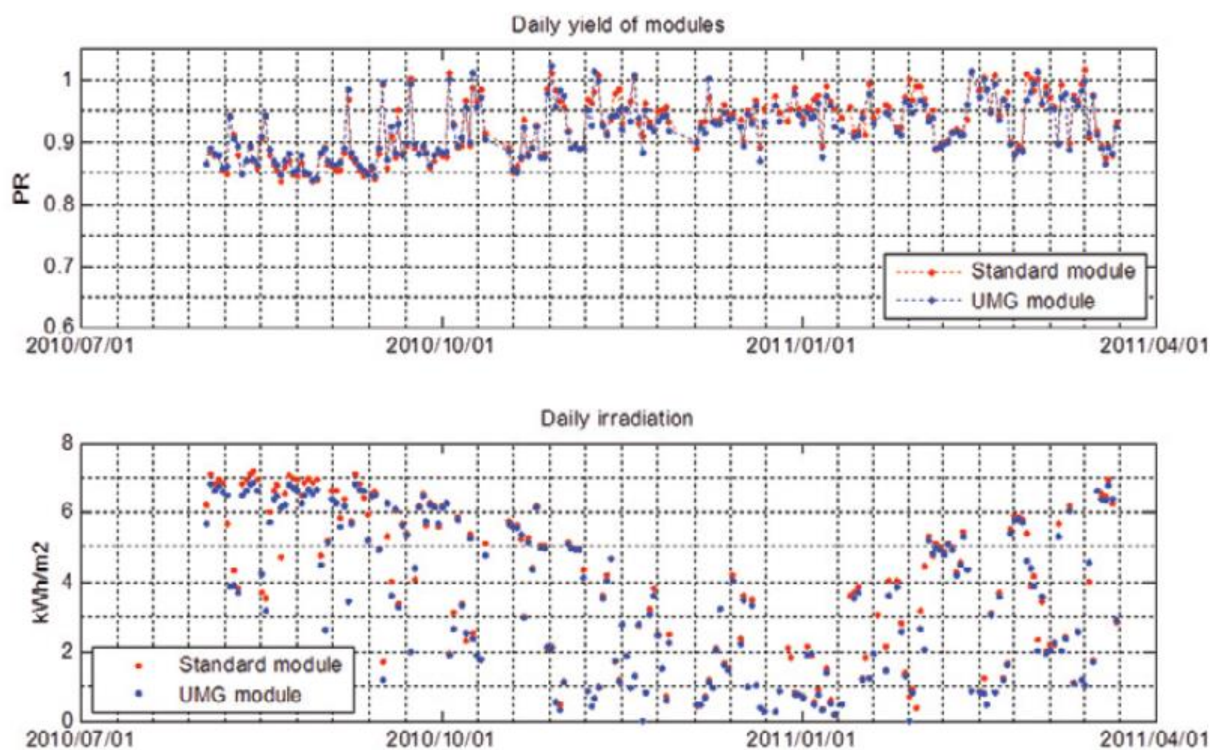


Figure 3-9: Energy production during the period under study. (a) Daily yield. (b) Daily irradiation.

3.2.4. Discussion

According to the results explained above, is it clear that despite the presumed drawbacks of the UMG-Si feedstock, modules manufactured with this material seem to be fully competitive with standard polysilicon-based devices, according to the energy yield exhibited and stability within the first year of equivalent outdoor exposition. In order to summarize the modules performance, Irradiance-Temperature- Efficiency (GTE) matrixes were computed for each module and are

illustrated in figure 3.10. They represent the modules efficiency vs. the irradiance temperature plane, using data collected during the whole period under study. Slight differences due to random partial shading or stains can be also registered.

The main difference found between the modules was again evidenced at both low irradiances and temperatures. In these conditions, the standard module shows an enhanced performance, being its efficiency slightly above 14%.

In contrast, high temperatures and irradiances favor the UMG-Si performance. As it was suggested before, the different temperature coefficients can play here a critical role, which probably arises from the lower resistivity (higher doping level) of the UMG-Si based wafers [32]. As a result, the temperature coefficient of Isc is higher for the UMG-Si material than for the standard, which means that the UMG-Si cells and modules develop a higher increase in current with temperature rising than the standard and this leads to a lower temperature coefficient of power for the UMG-Si module, as is described in [29].

Even though light induced degradation (LID) analysis was not performed in this work, there were no signs of any additional degradation in performance in case of the UMG-Si module with respect to the standard one. This practical result would be in line with previous works [30]. Notice that the results presented in figure 3.6 already corresponded to more than nine months of exposition, with nearly 900kWh/m^2 of cumulated exposition to sunlight for each module.

It could be argued that the fact that modules remain in open circuit conditions between measurements can, to a certain extent, influence the energy yield calculations, as reported by Tsuno *et al.* [31]. However, the effect would be perfectly comparable for both modules, which have very similar efficiencies and were exposed at the same real sun conditions. Particularly, the expected impact on module ageing due to the open condition operation should be related to a lower degradation of the maximum power, as was reported by Skoczek *et al.* [34].

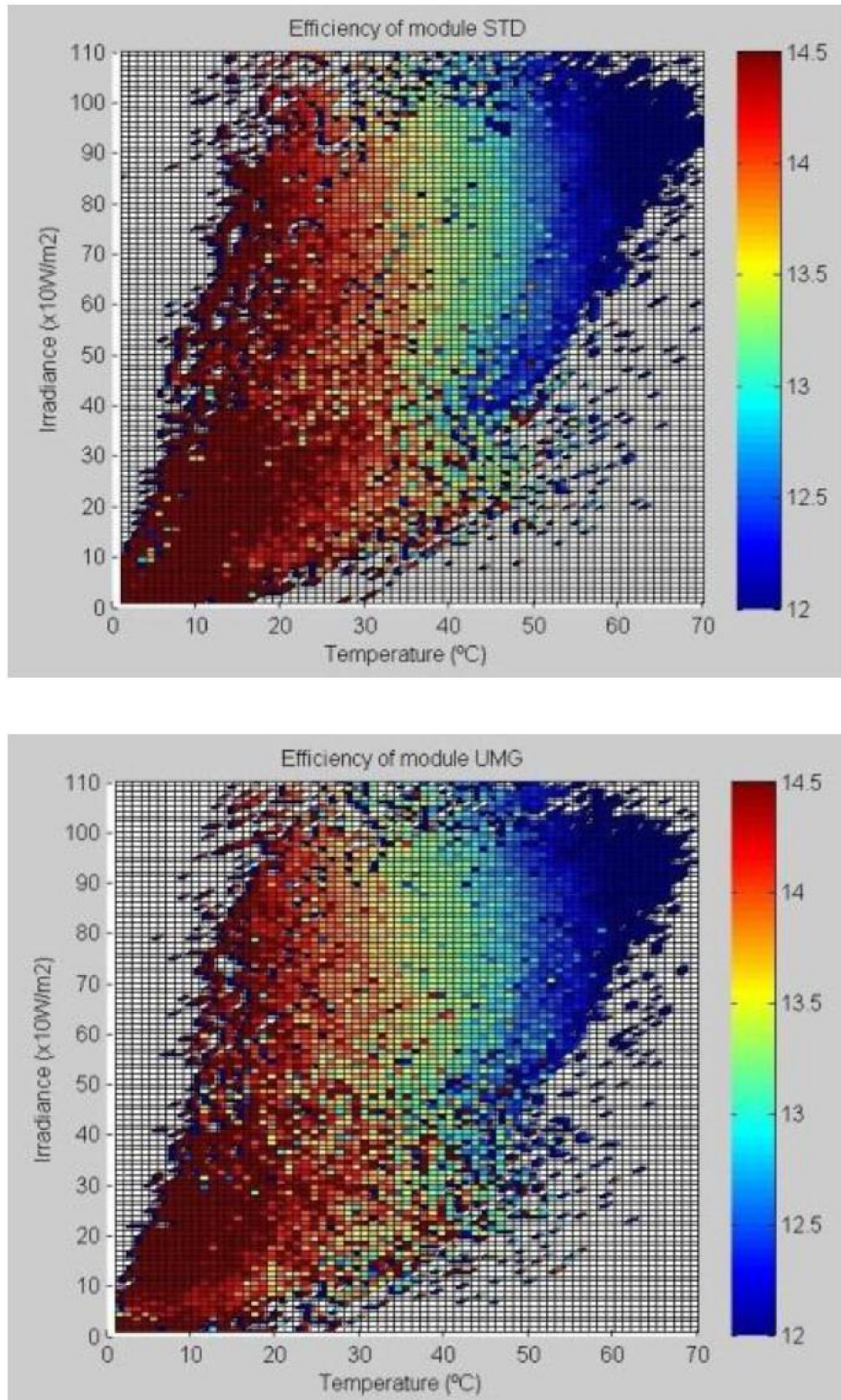


Figure 3-10: Efficiency matrixes for Standard (up) and UMG (down) modules.

3.2.5. Conclusions

The main conclusions of the studies carried out for the use of UMG feedstock for crystal growth are:

- The introduction of UMG Si decreased the yield in all the tests. Lifetime was also affected. However, the degree of reduction depends on the supplier and the quantity of UMG in the composition. "A" material seems to be a good alternative to polysilicon, although these wafers results should be corroborated with results in cells.
- The introduction of UMG Si reduces the usable brick length due to a higher P concentration in these ingots. This length could be maximized adding B but at the expense of reducing the base resistivity.
- The usable length in UMG ingots is not only reduced by resistivity values higher than 2.5 Ωcm, but also by a greater presence of inclusions in these ingots.
- The compensation region which appears in highly compensated ingots is associated with an increase in lifetime caused by a reduction in the SRH recombination.
- "As-cut" wafer lifetime is higher in highly compensated ingots maybe due to lower mobility of carriers.

UMG-Si and standard polycrystalline silicon modules manufactured according to the same elements and technology were tested in outdoor conditions. After a full year of study, the results indicate a comparable behavior. The work entails the collection of a large number of electrical parameters, at real time, using an innovative way of control based on well-known electronic loads connected to the modules. It can be concluded that both the performance and energy production were very similar for the two modules.

The performance differences between UMG-Si and standard polysilicon based mc-Si photovoltaic modules are influenced by several factors:

- Temperature Coefficients: UMG-Si modules tend to perform better at high temperatures and high irradiances due to more favorable temperature coefficients, likely arising from their lower resistivity and higher doping levels.

- Shunt Resistance: Standard modules exhibit higher shunt resistance, which contributes to slightly better performance at low irradiances.
- Open Circuit Voltage: UMG-Si modules have a slightly higher open circuit voltage compared to standard modules.
- Temperature Variations: The performance of both types of modules is significantly affected by temperature variations, with standard modules showing enhanced performance at low temperatures and UMG-Si modules performing better at higher temperatures.
- Light-Induced Degradation: Although not specifically studied in this work, previous studies suggest that UMG-Si modules do not show significant negative effects from light-induced degradation compared to standard modules.
- Irradiance Levels: The modules' performance varies with different levels of irradiance, with standard modules showing slightly higher relative efficiency at low irradiances.

Overall, these factors contribute to the observed performance differences, with UMG-Si modules being competitive with standard mc-Si modules, especially considering their lower cost.

4. Wire breakage and mechanical strength of crystalline silicon wafers

4.1. Wire breakage study on multi wire sawing technology

The objective of efficient sawing is to slice with a high throughput, with a minimum loss of slurry and silicon and with a high quality of the resulting wafers. Since many parameters can be changed, the optimization of sawing becomes a difficult task, which is nowadays mainly carried out by the wafer manufacturers. A catastrophic event during the cutting process is the break of a wire during a cutting cycle, it might result on dismissing the whole lot and send it back to the process after cleaning as scrap material that will be used as feedstock and back to the growing furnace. When a wire breaks it is very challenging to be able to solder the wire and insert it back in the exact same position. Marks on the produced wafers surface are very likely to appear, that if deep, will not be removed during the etching process of the cell manufacturing. Main reasons for a wire cut are the presence of SiC precipitates in the bricks that are harder than the wires and break it, quality defects of the wire, lack of slurry supply, slurry of low quality or recycled and reused too many times, excess tension of the wires, excess of cutting speed, thermal stress, etc.

We will study in this chapter broken and unbroken wire features, in order to better understand why breakages are produced, and therefore set actions to minimize them.

The number of broken wires suffered in a wafer production plant using the MWSS is one of the most critical parameters of the process. It is vital for optimizing the wafer cutting process since it has a significant impact on its economic balance. A line of silicon wafer production will not be optimized until the number of broken wires is minimized. The consequences of wire breakages are: deterioration of the surface quality of wafers (saw marks), or, if irrecoverable, the loss of the whole load, which then has to be recycled.

It is very difficult to assess the real cause of a steel wire break when cutting a brick of silicon, due to the numerous factors involved in the process, especially when some of them remain out of our control. Therefore, even though complete elimination of this failure is considered impossible, minimization is mandatory, in

order to drastically increase process yield.

In an attempt to clarify the possible causes of these breakages, a number of samples of cutting wire (new and used) were taken. Initial diameter was 140 and 130 µm. Subsequently, these samples were observed with a Scanning Electron Microscope (SEM) to study their surface texture and thickness.

4.1.1. Sampling

For the study, the samples were taken from cutting machines model MWSS E500SD-B/5 manufactured by Applied Materials. It was operating with a standard recipe in the usual conditions of production. The same conditions of the slurry were maintained: ratio Kg SiC/L PEG, % SiC and PEG virgin, F-600 SiC and PEG 200 [20].

Wires were taken before cutting (new), and then samples of the same wire were taken after the cut (used). In the used wires, both examples of wires that did not break (taken approximately at half the spool length), and wires that broke (at the vicinity of the breaking spot) were collected. Two different wire suppliers were analyzed.

The same sampling was performed for three different suppliers of SiC. In order to measure the thickness of the samples and qualitatively check the surface of the wires, a scanning electron microscopy (SEM) was used. Summary of the samples is shown in table 4.1.

Table 4-1: Samples (G: 140 µm wire; F: 130 µm wire).

Sample	Status after cut	Wire Supplier	SiC Supplier
1G	Broken	E	A
2G	Unbroken	E	A
3G	Broken	E	A
4G	Broken	E	A
5G	Broken	E	A
6G	Unbroken	D	A
7G	Unbroken	D	A
8G	Broken	D	A
9G	Unbroken	D	A
10G	Broken	D	A
11G	Broken	D	A
12F	Unbroken	D	A
13F	Unbroken	E	A
14F	Unbroken	E	B
15F	Unbroken	E	B
16F	Unbroken	E	C
17F	Unbroken	E	C

4.1.2. Results and discussion

It is quite logical to think that greater wear produces more broken wires, but table 4.2 shows that it is not the determining factor, at least in the 140 µm wire samples examined, sample 2G has the greatest wear and did not break. Moreover, sample 4G, which presented the lowest wear, broke. No sample of 130 µm wire broke although its wear increased up to 11,5 and 10,5 µm.

Before checking the used wires, the new wires were observed with SEM (see figure 4.1).

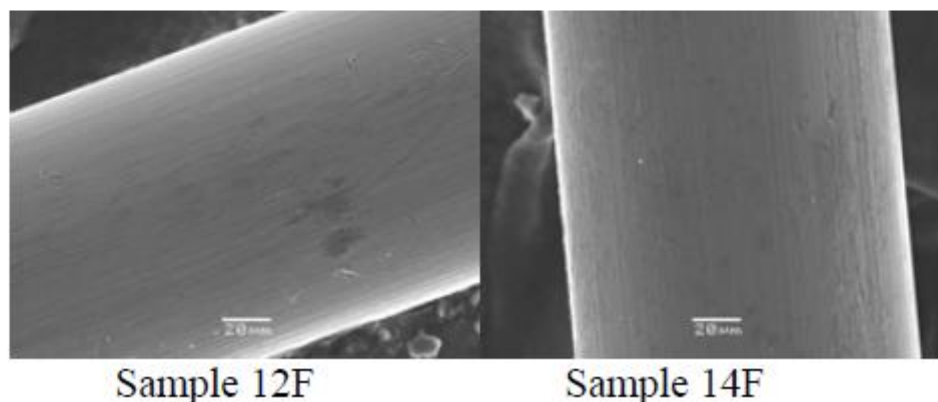


Figure 4-1: Marks in new wires.

Table 4-2: Wear of different samples.

Sample	Status after cut	Wire Supplier	SiC Supplier	Wear (μm)
1G	Broken	E	A	3.3
2G	Unbroken	E	A	7.9
3G	Broken	E	A	5.8
4G	Broken	E	A	2.1
5G	Broken	E	A	3.7
6G	Unbroken	D	A	4.9
7G	Unbroken	D	A	2.6
8G	Broken	D	A	3.6
9G	Unbroken	D	A	3.0
10G	Broken	D	A	6.4
11G	Broken	D	A	4.8
12F	Unbroken	D	A	7.6
13F	Unbroken	E	A	11.5
14F	Unbroken	E	B	5.3
15F	Unbroken	E	B	10.6
16F	Unbroken	E	C	5.9
17F	Unbroken	E	C	6.9

Every sample had marks in the new wire. Likely these marks were produced during the wire manufacturing process [33]. Both samples, broken and unbroken, had the marks before cutting. There are not great differences in surface finish between the broken wires and non-broken wires. However, there is a direct relationship between the presence of longitudinal marks and broken wires. When wires appeared with longitudinal marks at the end of the cut, the wire broke. Longitudinal marks are regular in a two-body cutting regime [34, 35]. Figure 4.2 shows these longitudinal marks.

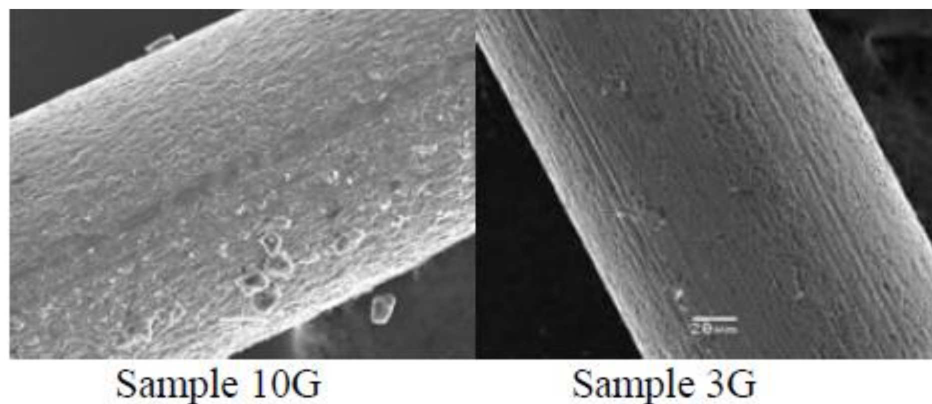


Figure 4-2: Longitudinal marks in used wires.

Some samples presented poor surface finish, but they did not break. Sample 13F (figure 4.3) had a wear of 11,5 µm and deficient surface finish however it did not break. On the contrary, sample 11G with better surface finish and less wear broke.

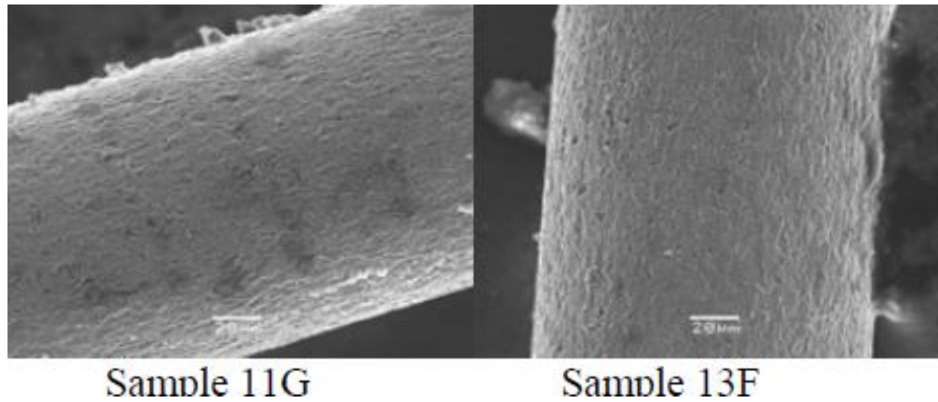


Figure 4-3: Samples with poor quality surface finish.

Figure 4.4 shows used wires with better surface finish, especially sample 17F. SiC Supplier C was less aggressive with the wire than suppliers B and A, at least we assume by the visual appearance of the samples.

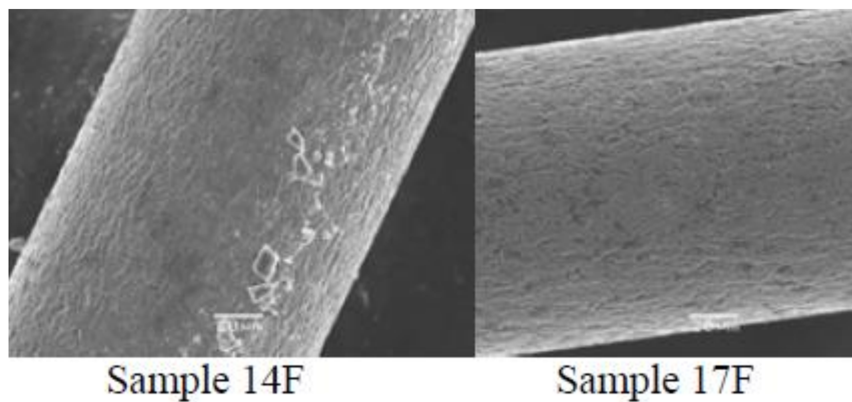


Figure 4-4: Samples with good quality surface finish.

4.2. Mechanical Strength of mono crystalline, multi crystalline and cast-mono wafers

As we have discussed, the cast-mono ingot growth can lead to a different defect structure than the typical Cz-Si process. Thus, the properties of the cast-mono wafers, based on low and high crystal defect densities, have been for the first time studied from a mechanical point of view, comparing their strength with that of both Cz-Si mono crystalline and typical multi crystalline materials.

The study has been carried out employing the four line bending test and simulating them by means of finite element (FE) models. For the analysis, failure stresses were fitted to a three-parameter Weibull distribution. All the theoretical analysis and simulations were done in collaboration with the centre for modelling in mechanical engineering and the department of structural mechanics and industrial construction of the UPM-Madrid.

Cast-mono materials need to be thoroughly studied and characterized, as a series of defects can be observed when comparing diverse zones in an industrial ingot [36–38]. The obtention of very low breakage rates for both wafer, cell and module manufacturers is critical for the PV industry [39,40]. The well-known thermal stresses appearing during the growth process, which result in dislocation formation, can be even harder when a single crystal is growing from the bottom to the top, as the occurrence of microdefects coming from impurities and SiC and Si_3N_4 inclusions is present as in a typical directional solidification system (DSS) based process. It is also known that this internal density of defects influences the mechanical properties of the wafers.

Different ways of characterizing the mechanical issues involved in a solar wafer have been recently reported, as micro-Raman spectroscopy and photoelasticity [44,42]. The interesting results from some of these methods can be correlated with both the stress and the recombination activity of the defects in the crystal. However, they do not imply a direct determination of the mechanical strength of the whole substrate, macroscopically.

In this chapter, a systematic analysis of the mechanical strength of commercial wafers having different crystal features is presented, including two different sets of cast-mono wafers from ingots manufactured in typical DSS furnaces. To this end, four sets of wafers have been prepared: two of them corresponding to the most widely used in the PV industry (mono crystalline Cz and multi crystalline) and the

other two corresponding to the cast-mono ingot growth, characterized by a high and low defect density, respectively, as measured qualitatively by photoluminescence (PL) methods.

The four-line bending test (FLBT) has been chosen for the study because the results consider the type of defects that can appear in the wafers: edge and surface/bulk defects [43–49]. Test results are presented in terms of load–displacement curves, and the failure stress is calculated through numerical models simulating the test. The finite element (FE) method has been employed to model the test taking into account the material properties (the anisotropy in case of mono crystalline silicon wafers) and the nonlinearities present in the test.

Finally, the fracture stresses of each set are fitted to a three-parameter Weibull distribution. Because of the random distribution of defects in the wafers, the size of the stressed material surface affects the strength [47]. This is known as the size effect, and it has been taken into account in this study. The Weibull parameters of each set are compared in order to analyze the mechanical strength of both mono crystalline, multi crystalline and cast-mono wafers in a macroscopic way.

4.2.1. Material considerations

Cast-mono, cast-mono with a high density of extended defects (dislocations and subgrain boundaries) and multi crystalline wafers were obtained from ingots grown using typical industrial DSS furnaces (450-kg charge) by different approaches. Cast-mono samples were specially manufactured by a special mono crystalline seed-assisted growth, on the basis of <100> seed orientation (<010> all along the edges) [36–38].

In order to determine the density of extended defects (both dislocations and subgrain boundaries) in every type of crystalline wafer, a full-surface PL analysis was performed, as illustrated in Figure 4.5.

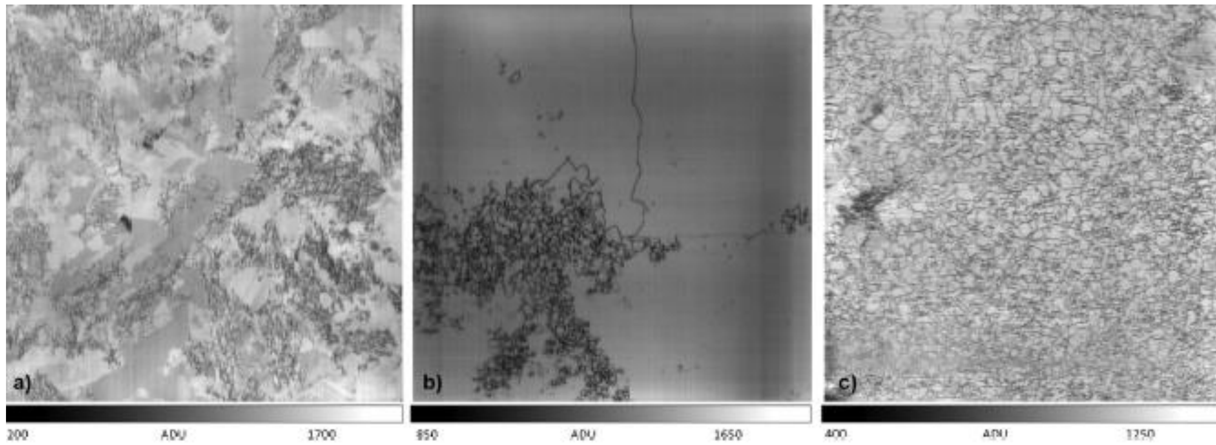


Figure 4-5: PL images (arbitrary scale) of multi crystalline, casting mono and casting mono with high defect density wafers.

Whereas the multi crystalline material presents the typical grain boundaries (GB) and dislocation clusters as extended defects, different cast-mono ingot processes, due to the special thermal-induced stress during the cast growth (no GB that can interact), can result in the formation of a large quantity of sub-GB over the whole wafer surface (Figure 4.5c) [36–38]. Consequently, very low short circuit currents when processing the wafer into a solar cell are reached because of the notorious bulk defect density.

Both the electrical performance and the mechanical properties of a silicon wafer are affected by the bulk crystal defects. Thus, as the defect structure in the cast-mono substrates differs from those from the typical Cz and multi crystalline cast growth approaches, information about the influence in the mechanical strength should be collected and analyzed.

For this purpose, 50 samples (156mm×156mm size) of each type of wafer have been prepared and tested. The as-cut thickness was approximately 200 µm for all the substrates. It is known that the wire cutting process leads to surface damage that determines the mechanical strength of the silicon wafers [46]. This damage has been efficiently removed by reducing the wafer thickness (approximately 25 µm) by means of chemical etching (no texturing). Therefore, the intrinsic contribution of each respective kind of crystal to their mechanical properties has been highlighted and then analyzed. The mean thickness was estimated by mass loss determination after the chemical treatment. Both the mean values and the total variation of each set are shown in table 4.3.

Table 4-3: Mean thickness and total variation of each set.

Set of wafers	Source	Mean thickness and total variation (μm)
Multi crystalline	DC wafers	168 ± 4.2
Square mono crystalline Cz	Commercial	173.1 ± 3.5
Cast-mono	DC wafers	168.1 ± 2.2
Cast-mono (high defect density)	DC wafers	168.5 ± 1.5

For a reliable analysis, it is necessary to consider the special features of the different sets of wafers, that is, one crystal for the mono crystalline Cz and cast-mono cases or many crystals for the multi crystalline set. The mechanical anisotropy of the silicon crystal influences the results [48,49]. The directional dependence of the Young's modulus is shown in Figure 4.6. This behavior can be represented by the following tensor of elastic constants:

$$c_{11} = 165.6\ GP_a$$

$$c_{12} = 63.9\ GP_a$$

$$c_{44} = 79.5\ GP_a$$

The simulation of the test corresponding to wafers of mono crystalline Cz or cast-mono sets requires the consideration of this anisotropy. However, the simulation of multi crystalline samples assumes an isotropic behavior because of the random orientation of each crystal. This isotropic behavior has been characterized by means of a Young's modulus value of E=165.6GPa ([45], [50]) and a Poisson's ratio of 0.23.

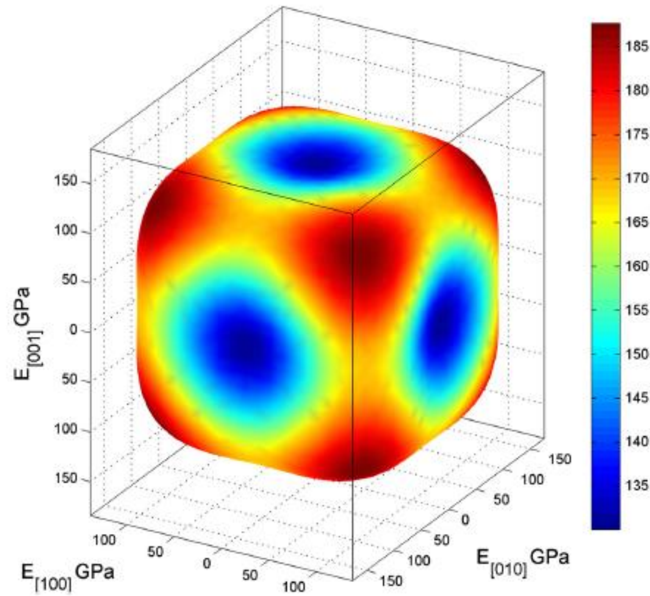


Figure 4-6: Elastic modulus variation of silicon.

4.2.2. Mechanical tests

The FLBT has been employed in this study. In this type of test, the wafer is placed on two supports, and the load is applied through two additional supports on the opposite side of the wafer. Because the loaded area is bounded by the lower supports, both edge and surface damage are taken into account [43–49]. The support and load devices are cylindrical bars with a diameter of 1 cm. The inner and outer span were 40 and 80mm, respectively (Figure 4.7).

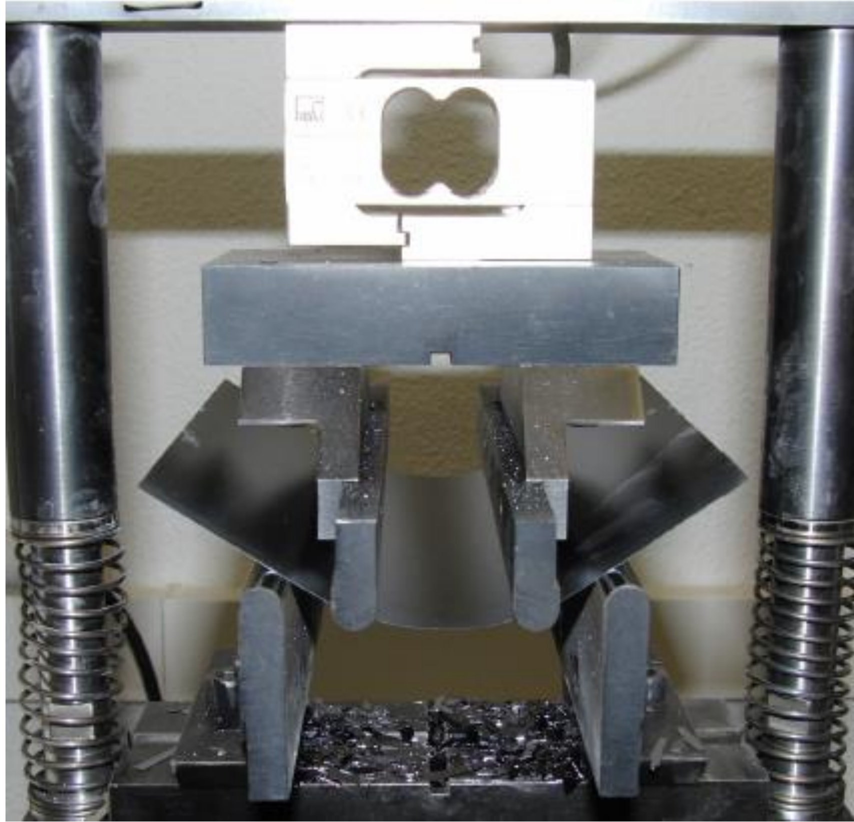


Figure 4-7: Picture showing an example of an FLBT analysis on a silicon wafer.

The measuring range of the force transducer reaches up to 200N. The displacement of the loading devices is imposed, and both the force and the displacement are recorded. In order to ensure a quasi-static condition, a very low velocity has to be used (2.5mm/min). An initial 1N preload is imposed.

For every set of wafers, 50 samples were tested until fracture. The results are shown in terms of load deflection charts (Figure 4.8). It can be observed that the multi crystalline set presents the stiffest behavior of all tests, despite the similar thickness values from table 4.3. This different behavior can be explained by their inherent isotropy, in contrast to the above-mentioned anisotropy of single crystal-based substrates.

Load–displacement curves of mono crystalline based wafers are clearly nonlinear. This behavior stems from large displacements, with an onset at around 8 mm. The previously commented intrinsic stiffness of the multi crystalline substrates results in the lower fracture displacements.

4.2.3. Numerical model

The mechanical characterization of the strength of each set of wafers requires the knowledge of the stress distribution of the wafers in the moment of failure. The FLBT gives information about the relation between the applied displacements and the recorded loads from the initial preload until failure. Figure 4.8 shows nonlinear trends in the load–displacement curves. Therefore, analytical methods, which assume a linear load–displacement relation, are not valid to obtain the stress distribution of the wafers in the moment of failure. This nonlinearity comes from the large displacements occurring in the test, caused by the small thickness of the wafers and the contact between the wafers and the supports. Therefore, the FE method is likely to be chosen for the analysis. This numerical technique obtains approximate solutions to very complex problems, being the most extended for this type of studies [43–49,53,54].

The test was suitably modeled with a 3D FE model, on the basis of eight node shell elements [51]. The material anisotropy was considered for mono crystalline Cz and quasi-mono crystalline cases, implementing the large displacements formulation. The supports have been modeled as a rigid surface with a cylindrical shape, and the contact between them and the wafer was also considered. Contact algorithms require a fine mesh in the contact zone to avoid convergence problems. In order to reduce the number of elements, the mesh size is varied depending on the zone of the wafer, and the double symmetry is considered (Figure 4.9a).

The wafer displacements field corresponding to a displacement of upper supports higher than 11mm is shown in Figure 4.9b. The symmetry expansion has been applied to obtain a better understanding of the whole wafer deflection.

Two FE models have been developed for each set of wafers, for both the thinnest and the thickest wafers. The good agreement between the FE models (both with an isotropic (a) and anisotropic (b) behavior) and the test is presented for the multi crystalline and quasi-mono crystalline sets (Figure 4.10). For the two FE models developed, the whole stress field was recorded for all the load– displacement curves. The stress field in the moment of failure of the other wafers is obtained through a linear interpolation that considers both the elastic energy stored in the wafer before failure and its thickness.

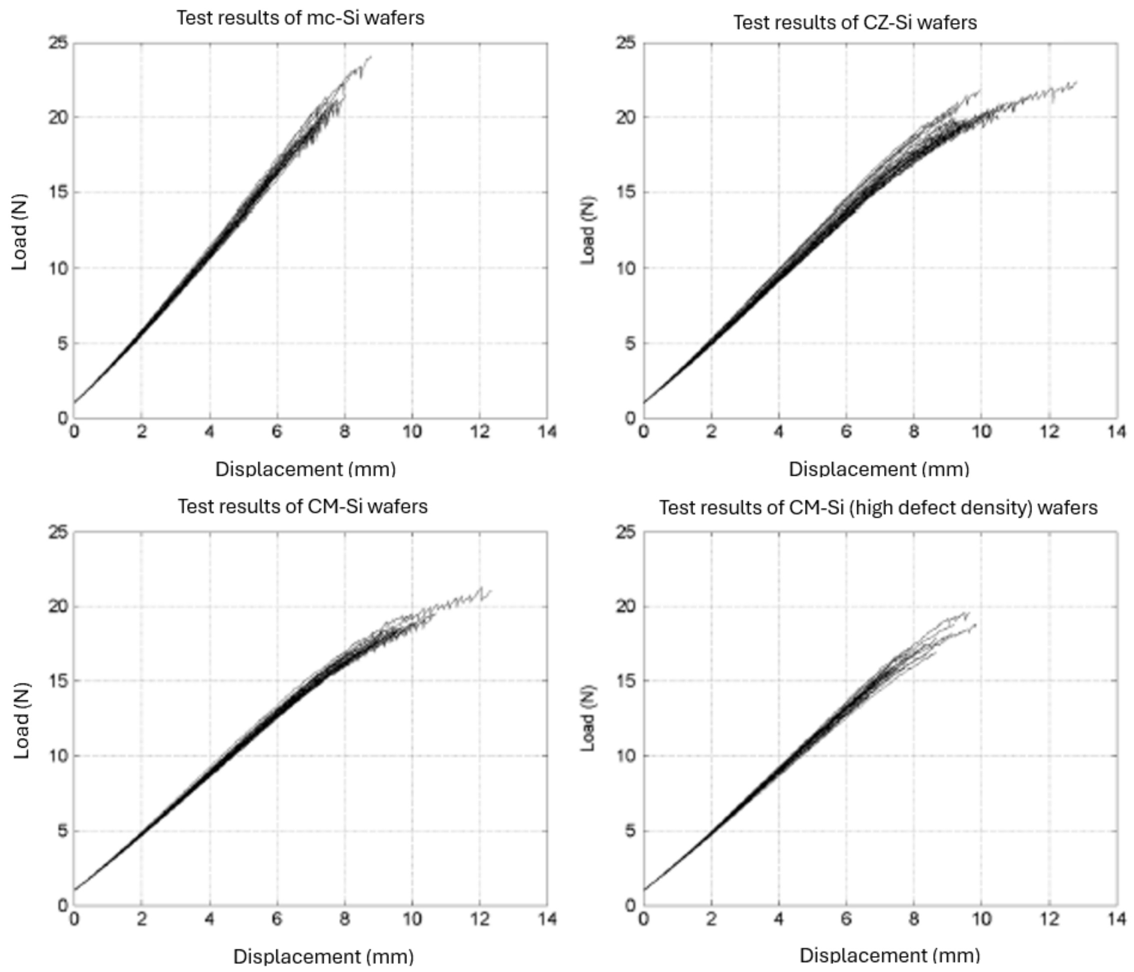


Figure 4-8: FBLT load–displacement plots registered for all the wafer sets (50 samples each.

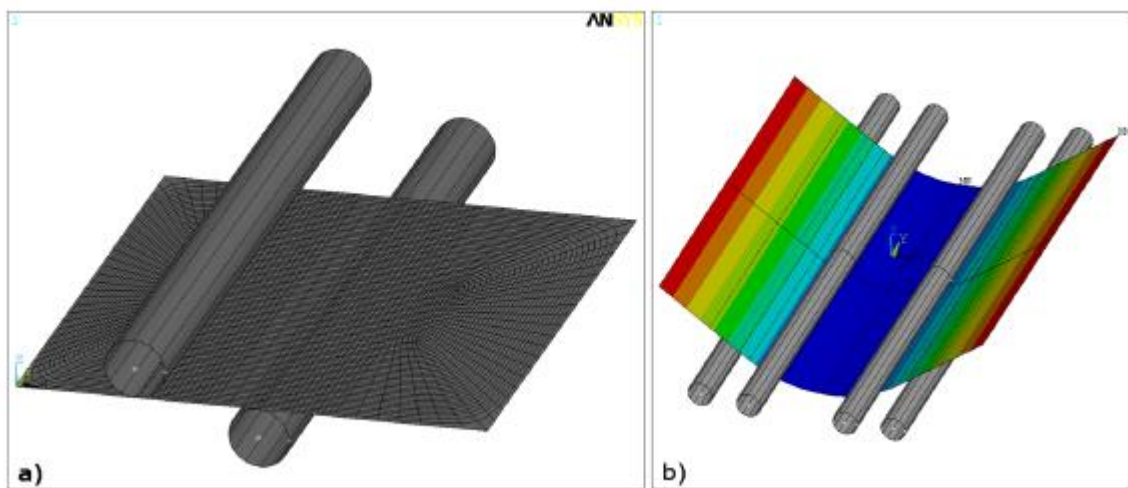
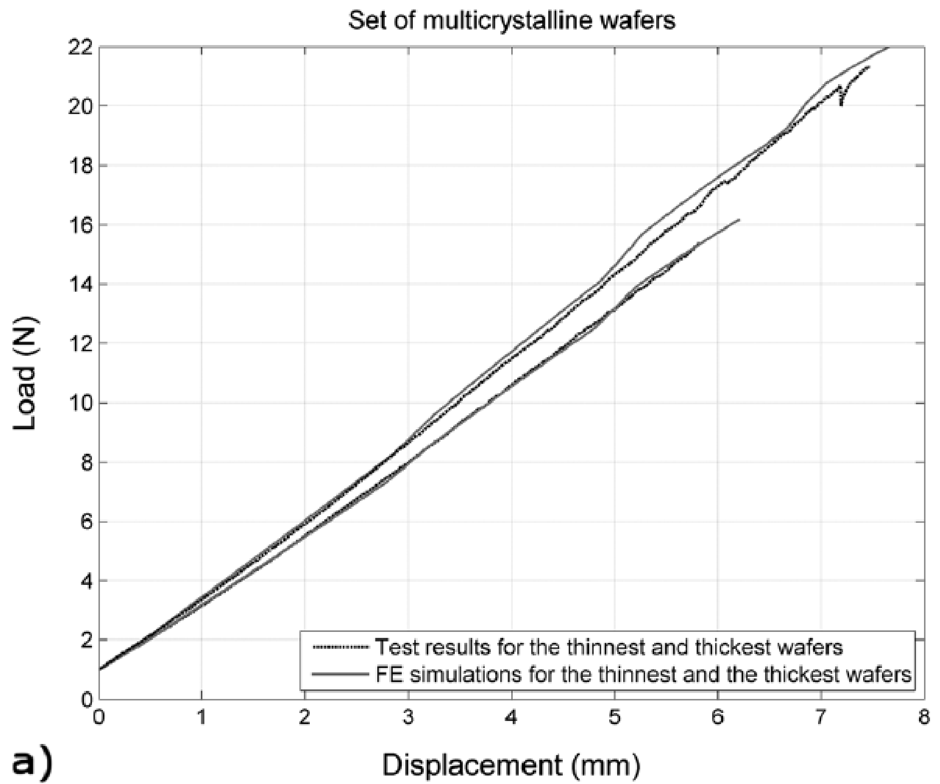


Figure 4-9: Mesh and wafer deflection of the FE model used in this study.



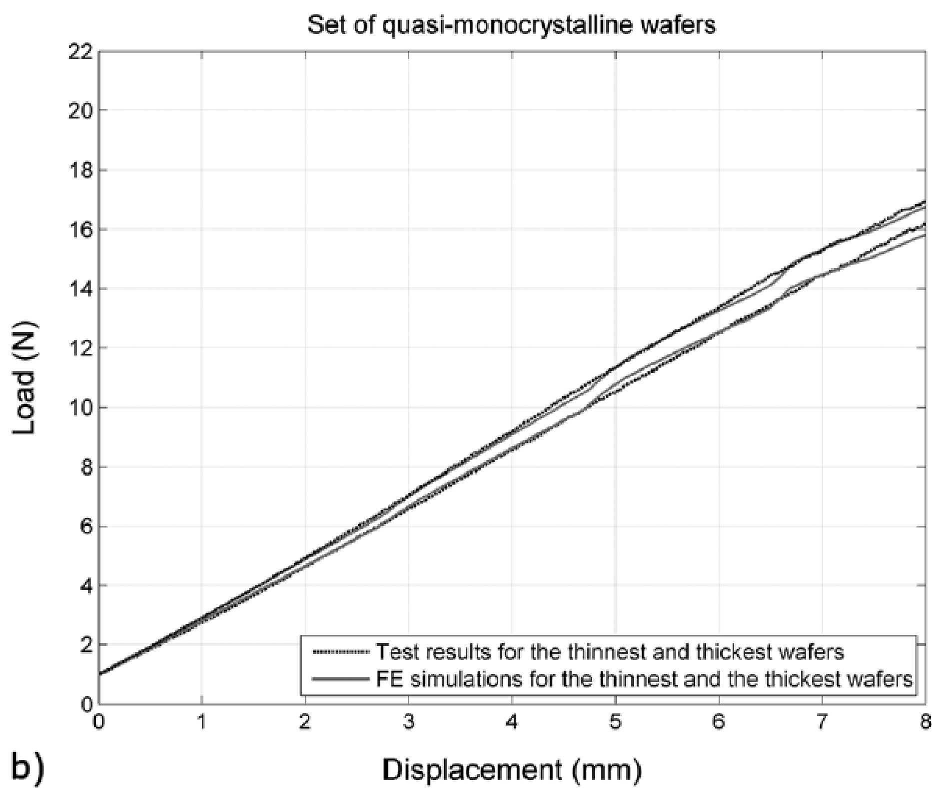


Figure 4-10: Fitting between the tests and the FE models for the multi crystalline (a) and quasi-mono crystalline (b) sets.

4.2.4. Statistical Evaluation

The high scatter that can be observed in the strength characterization of brittle materials needs the use of a cumulative distribution function (cdf) to represent in a reliable way the sample resistance [47]. In order to fit the fracture stresses, a two-parameter Weibull distribution has been widely used [43,45], omitting the existence of a threshold stress. Moreover, the influence of the size effect is often neglected. In this study, the fracture stresses of each set of wafers have been fitted to a three-parameter Weibull distribution [52], permitting a threshold stress value different from zero. Therefore, if the optimum is achieved with a zero value of threshold stress, this set will be fitted to a two-parameter Weibull distribution. The Weibull cdf was originally proposed to characterize the probability of failure of a uni-axially and uniformly tensioned materials (Figure 4.11) [53,57]. It assumes that the random nature of the spatial distribution of defects implies that the strength will decrease with an increase of the stressed area because the probability of having a critical defect will also increase. The failure stresses from the FLBT of each set of wafers cannot be directly fitted to a Weibull cdf because the stress distribution is not uniform and the size effect has to be considered. Przybilla proposed an iterative method [54] that has been developed further in order to take nonlinearities into account.

As the Weibull cdf is valid for a uni-axially tensioned area (ΔA), the failure probability of one sample for a uniaxially tensioned equivalent area Aeq different from ΔA is given by

$$P_{f,Aeq}(\sigma) = 1 - exp\left[-\frac{A_{eq}}{\Delta A}\left(\frac{\sigma - \lambda}{\delta}\right)^{\beta}\right]$$

obtaining the three Weibull parameters, where:

- λ is the location parameter and it represents a threshold stress for which stresses below this value will never lead to the failure of the sample.

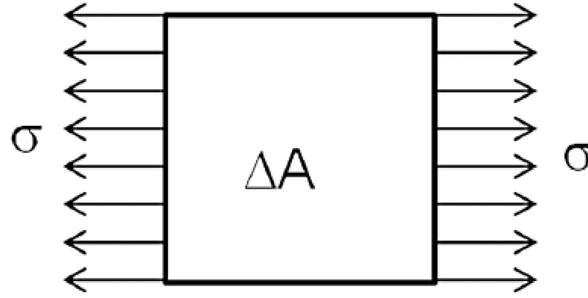


Figure 4-11: Uni-axially tensioned area ΔA.

- δ is the scale parameter. The sum of the scale and the location parameter gives the characteristic fracture stress (sθ), which counts on the 63.2% of the samples that will fail.
- ß is the shape parameter and gives information about the scattering of the results. As ß increases, the dispersion is reduced.

By definition, a specimen having the equivalent area Aeq, subjected in a tensile test to the maximum stress observed in the FLBT, results in the same probability of failure. Therefore, the Aeq,i of the sample i for the three-parameter Weibull distribution can be calculated as follows:

$$A_{eq,i} = \int_{dA(\sigma>\lambda)} \left(\frac{\sigma_i - \lambda}{\sigma_{max} - \lambda}\right)^{\beta} dA$$

where σ_i is the first principal stress of the sample i dependent on the position and σ_{max} is the maximum principal stress of the whole sample. As the FLBT subjects the samples to a practically uni-axial stress state, the failure criterion is the maximum principal stress in the sample.

The method employed to obtain, for each set of wafers, the Weibull cdf for the ΔA chosen as reference has the following steps:

1. The failure stresses of the set analyzed (N samples) are sorted in ascending order. The probability of failure of the *i*th sample is

$$P_{f,i} = \frac{i - 0.3}{N + 0.4}$$

2. The set of σ_i and $P_{f,i}$ is fitted to a three-parameter Weibull distribution by the least square method because each Weibull function can be transformed to a straight line in a double logarithmic graphics being ($\sigma - \lambda$) the abscissa. The two parameters that define the straight line (β and δ) for a given λ are estimated by the least square method. The algorithm does a sweep from $\lambda = 0$ to $\lambda = \sigma_{min}$ (the minimum failure stress of the set), comparing the correlation factor (R^2) of each fitting and taking the one corresponding to the maximum of R^2. Moreover, this method provides the confidence bounds for the scale and shape parameters.

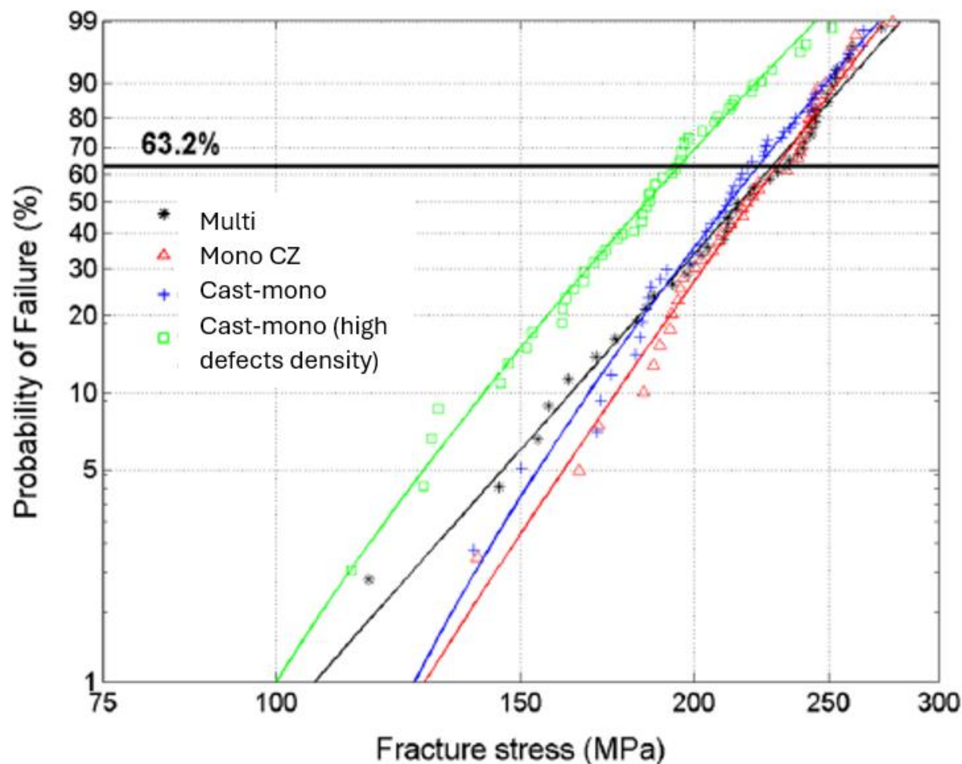


Figure 4-12: Graphical comparison of the Weibull cdf for the four sets analyzed.

3. The A_{eq} of each wafer is calculated. To do this, the location and the shape parameter obtained in the previous step are needed. It is also necessary to have the stress field of each wafer at the moment of failure and the area of each element of the FE simulation. From all these data, the integral is solved, and the A_{eq} of each wafer is obtained.

4. Knowing the equivalent area of each sample ($A_{eq,i}$), the probability of failure of this sample is calculated, corresponding to ΔA, by means of the

following expression:

$$P_{f,i,\Delta A} = 1 - \left(1 - P_{f,i}\right)^{\Delta A / A_{eq,i}}$$

5. The new set of data si, Pf,i,ΔA are fitted to a new three-parameter Weibull distribution, giving three new factors.
6. Coming back to the third step, the iterative process continues till the variation of λ and δ is negligible.

The uni-axially tensioned area chosen has a value of 0.004 mm^2. The results are plotted in a Weibull scale in Figure 4.12 and are summarized in Table 4.4. It can be observed that the multi crystalline wafers fitted to a two-parameter Weibull distribution, whereas the other sets presented a threshold stress.

Table 4-4: Resulting Weibull parameters of each respective set of wafers.

Set	**λ (Mpa)**	**δ (Mpa)**	**β**	**σ_0(Mpa)**
Multi crystalline	0.00	228.21 (191.75 … 271.61)	6.84 (6.62 … 7.06)	228.21
Square mono crystalline Cz	31.93	198.02 (158.64 … 247.18)	7.19 (6.89 … 7.50)	229.95
Cast-mono	69.07	153.78 (128.75 … 183.68)	5.22 (5.03 … 5.40)	222.85
Cast-mono (high defect density)	47.50	148.06 (129.37 … 169.45)	5.02 (4.88 … 5.16)	195.56

Numbers in brackets are the confidence bounds for a confidence level of 95%.

This means that for the multi crystalline set, every action can cause the failure of the sample, whereas for the mono crystalline cases, there exists a threshold stress below that the samples will not fail. As it has been mentioned, all the samples were polish etched before the test, so it seems that the single crystal presents a robust structure that prevents the failure for low stresses while the combination of the crystals (the multi crystalline case) weakens the material, turning it vulnerable even for very low stresses. The analysis of the shape parameter (β) shows that the scattering associated with the cast-mono samples is quite higher than the conventional ones. It is convenient to remark here that the information given by the β parameter is referred to the material that is being characterized, not for the samples tested. Lower values of β imply a major scattering or uncertainty in working with those samples. In Table 4.2, it can be checked that mono crystalline

Cz presents the highest value of ß, and therefore, the uncertainty of working with this set is the lowest while the multi crystalline has a smaller value.

Hence, the characteristic fracture stress of the conventional samples (mono crystalline Cz and multi crystalline) is quite similar because despite that the multi crystalline set has no threshold value, the scattering is bigger, obtaining almost the same value for which the 63.2% of all samples will fail.

On one hand, it seems that the most recommendable is the mono crystalline Cz set because it has a threshold value, the lowest scattering and the biggest characteristic fracture stress. On the other hand, the costless and mature technology of multi crystalline presents also a high value of characteristic fracture stress appearing as a good alternative from a mechanical point of view.

The comparison between the conventional samples and cast-mono wafers shows that as a single crystal, they have a threshold stress. Moreover, the cast-mono set presents a characteristic fracture stress value very close to the conventional ones, showing however a higher data scattering. The characteristic fracture stress of the cast-mono set composed by wafers characterized by high defect densities is 15% lower than the well-known and mature multi crystalline and mono crystalline Cz substrates. From this result, it is confirmed that there is a direct correlation between the high bulk defect density and the intrinsic crystal properties of the wafers, particularly in the case of defected cast-mono substrates. This kind of wafer quality is still likely to be obtained using the common furnace settings and hardware used in the PV industry.

4.3. Conclusions

An analysis of wire breaks has been performed taking samples of broken and unbroken wire with the following conclusions:

- We have observed the presence of longitudinal marks on every broken wire, whereas these marks are absent in unbroken wires. The presence of SiC inclusions in silicon, and the transfer from a three-body to a two-body regime may be an explanation.
- Two-body abrasive wear is caused by rubbing of a softer surface by a hard rough surface while three-body abrasive wear is caused by hard particles entrapped between two sliding surfaces. This factor seems to be more

important than the wire wear, which has a much smaller influence in breakage.

- On the other hand, SiC from different suppliers interact on a different way with the wire ending up on a different surface quality in the wire after the cut.
- No direct correlation between breakage and wire surface finish was observed.
- Longitudinal marks were observed in all broken wires.
- There is no direct correlation between the initial and final thickness of the wires and rupture.

For the first time, the mechanical strength of conventional wafers (properly etched to remove the surface saw damage) mono crystalline Cz and multi crystalline have been compared with the cast-mono substrates with high and low defect density.

The systematic FLBT analysis indicates that the intrinsic crystal properties of the silicon wafers, defect structure included, has a direct influence on the probability of mechanical failure during the PV manufacturing value chain (wafer handling, solar cell metallization, strings lamination, etc.).

Other conclusions can be drawn from this study, as follows:

- Mono crystalline Cz, multi crystalline and cast-mono (low defect) etched wafers showed similar characteristic fracture stress. According to these data, the strength of the three sets are quite similar, but the analysis of the Weibull parameters shows that multi crystalline wafers present defects in their structure that makes possible the failure under low stress field, whereas the mono crystalline Cz and cast-mono (low defect), after the polish etching removing the surface damage, present a minimum threshold below that they will never fail. Moreover, the shape parameter shows that the uncertainty in the strength follows the order cast-mono>multi crystalline>mono crystalline, this result being associated to the crystal structure of each set.
- The cast-mono wafers with high density of defects exhibited the lowest value of characteristic fracture stress (15% lower), confirming the detrimental effect of these bulk defects not only in the electrical properties but also in the probability of mechanical failure during the PV manufacturing processes.

- The uncertainty of the two cast-mono sets is higher than the other two sets. This can be improved by controlling the defect density of this type of wafers.
- High mechanical strength was found in all the cases. However, the cast-mono wafers characterized by large density of bulk defects, due to the noticeable density of extended defects, showed lower fracture tensions.

5. Cast-mono wafers manufacturing process and modules outdoor performance

5.1. Cast-mono wafers manufacturing: crystal defect generation and low wafers performance study

In order to understand this technology better in this chapter we performed a series of casting crystal growth experiments and characterization studies from ingots, wafers and cells manufactured in an industrial approach, showing the main sources of crystal defect formation, impurity enrichment and potential consequences at solar cell level. The previously mentioned technological drawbacks are directly addressed, proposing industrial actions to pave the way of this wafer technology to high efficiency solar cells. Analysis of photoluminescence and laser beam induced current maps were performed in collaboration with the departamento de física de la materia condensada of the University of Valladolid.

Significant problems can be detected when analyzing an ingot manufactured according to the worldwide extended industrial casting standards, as high generation of bulk extended defects, unusual contamination phenomena by residual impurities and the appearance of considerable extended multi crystalline grains regions in the ingot. In addition, mass scale production costs increase, as the mono crystalline seeds reutilization is neither evident nor straightforward. Low solar cell efficiency ingot regions directly associated with low carrier lifetime regions of the cast-mono ingot are present; consequently, the expected high wafer performance and yield can be seriously suppressed.

The literature dealing with defect formation in seed-cast growth is scarce, especially at lab scale background [55].

Numerical simulations addressing some of the previously mentioned issues have also been published, by Gao et al. [56,57].

We review, in this chapter, a detailed and critical analysis of the most deleterious sources of low wafer performance and crystal defect generation during the seed-

cast growth approach based on a series of experiments performed in a full industrial environment (ingot, wafer and solar cell manufacturing).

Both silicon materials and devices have been characterized using several optoelectronic techniques, such as photoluminescence (PL) imaging, microwave photoconductance decay (m-PCD) and high resolution laser beam induced current (LBIC). Finally, practical ideas to manage the technical limitations imposed by this attractive crystal growth process are also proposed.

5.1.1. Experimental setup

Seed-cast growths were performed at DC Wafers Investments, S.L. Spain, using both Directional Solidification (DSS) and Heat Exchange Method (HEM) furnace stations (from GT Solar, USA). Cz-Si ingots for seed manufacturing were produced at CENTESIL Institute, in Madrid (Spain), using a PVA-Tepla Cz puller. The crystal growth processes were labeled according to the number of repeated uses of the original Cz seed (ingot growth runs G0, Gn, Gn + 1, etc.), suitably cropped from the silicon bricks after each growth process. Different mono crystalline seed configurations were tested, from 1-(1x1) to 25-(5x5) silicon slabs.

Bulk carrier lifetime of silicon bricks was measured by a STV Telecom m-PCD instrument (Russia). For the wafer characterization, PL images over the whole wafer surface were collected by a PLI-101 Inline Photoluminescence Imaging System. Minority carrier lifetime analysis was also performed on as-cut wafers, by both the Quasi Steady-State Photoconductance (QSSPC WCT-120, Sinton Instruments, Boulder, CO, USA) and m-PCD mappings (Semilab WT 2000). The wafers were chemically etched to remove the saw damage, then coated by SiNx:H at both sides. Interstitial iron concentration ([Fei]) was also measured, using the Fe–B dissociation technique. An additional phosphorus gettering process (standard POCl3-based process) was implemented to analyze the evolution of [Fei] in the samples.

An LBIC system operating with three excitation wavelengths, from two dual laser diodes (Omicron) with 639–830 nm and 853 nm laser lines, besides a second laser diode (785 nm), was used. A beam splitter directs the laser beam into a trinocular microscope, which is used to focus the excitation laser beam onto the sample surface. Three signals are acquired, stored simultaneously, and correlated to the

sample (x, y) coordinates to building up the LBIC maps: (i) the output power of the excitation laser, (ii) the light power reflected by the wafer; and (iii) the electric current induced by the laser beam (LBIC). Microscope objectives with different magnifications and numerical apertures were used, allowing the acquisition of high spatial resolution LBIC images. The sample is mounted on a motorized translation stage with three stepping motors (XYZ motion) manufactured by Prior Scientific, Cambridge, UK. The software of control acquisition and data treatment was developed under Labview v 8.5. [58].

Solar cells (156mm×156mm) from cast-mono wafers were produced by using two different methods: (i) typical acid texturing processes, $POCl_3$ diffusion and an H-patterned screen-printing metallization (average mc-Si cell efficiency 16.4%); and (ii) alkaline texturing followed by ion implantation emitter formation, without implementing any selective emitter technology.

Gen 5 RTU quartz crucibles (Vesuvius, France) were used to manufacture the ingots, which were based on solar grade polysilicon.

P-type and non-doped Cz-Si <100> oriented mono crystalline seeds (14.0 cm ×14.0 cm) were used for the seed-cast growth experiments. Silicon seed thickness varied from 10 to 30 mm.

5.1.2. Results and discussion

5.1.2.1. Industrial manufacturing of cast-mono ingots. Experimental facts to consider.

A seed-cast growth technique has been successfully implemented to manufacture industrial ingots having clear mono crystalline features. Figure 5.1 shows a transverse section of a 450 kg DSS ingot, showing a large mono crystalline fashioned volume all along the bulk. Some mc-Si regions are also observed at the edges of the ingot, as indicated by arrows in the figure. The wafers sliced from such an ingot are ranged in different cast-mono classes, according to the size of their respective mono crystalline sections (from 100% mono crystalline to less than 75%, in the present case). In particular, a high percentage of full square mono crystalline wafers (15.6 cm x 15.6 cm) can be obtained in a straightforward way, even when using a commercial casting furnace technology.

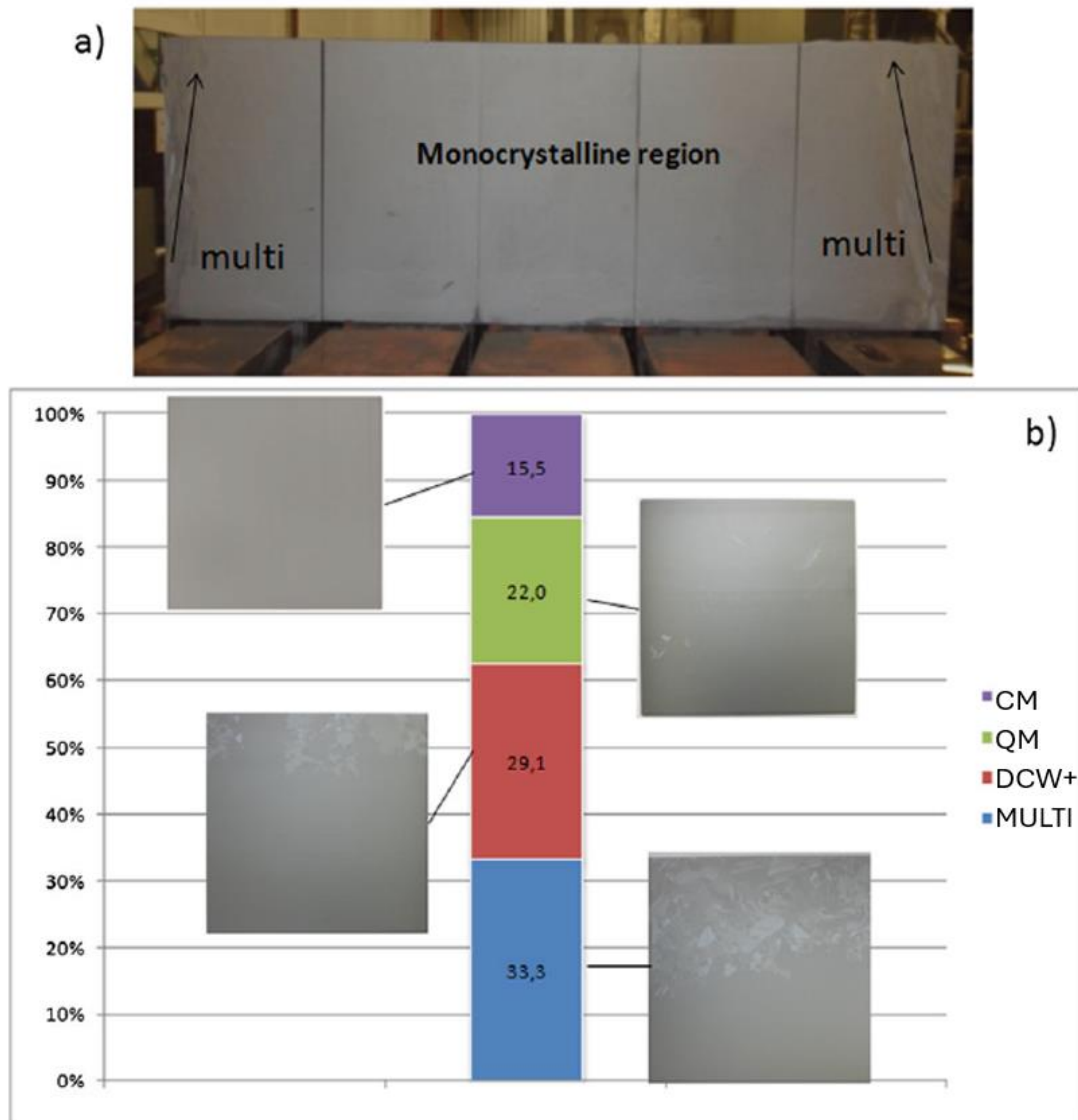


Figure 5-1: (a) Picture of a typical G0 cast-mono ingot manufactured at DC Wafers by implementing the seed-cast growth method (DSS method); (b) Wafer-type distribution according to their percentage of macroscopic mono crystalline feature. CM, cast-mono (100%); QM, quasimono (>90%); DCW+, DC Wafers PLUS (>75%); MULTI, mono/multi and mc-Si (<75%).

However, in a G0 crystal growth process, on the basis of virgin mono crystalline seeds from a Cz ingot, both the proportion of cast-mono wafers and their intrinsic defect density, from the center to the sides and from tail to top, strongly depend on a number of experimental variables, which need to be designed and optimized to

avoid solar cell performance loses. The seed-cast growth method is based on the use of perfectly oriented mono crystalline square silicon slabs, usually <100>, which are properly placed at the bottom of the quartz crucible [15]. The crystal melt/growth process is consequently based on the application of a passive cooling from the bottom of the crucible to geometrically control the melting of the seed up to a defined height, using a calibrated quartz rod, then applying a corresponding cooling before the seed disappears into the melt. As a result, the crystal orientation of the seed is transferred to the top of the ingot. This potentially tricky task can be achieved either by designing and implementing optimized furnace setting parameters (software approach) and/or by adapting the graphite hot zone in the proper way (hardware approach).

The mere fact of placing the seeds into the crucible, besides the quality of their respective edges resulting from the sawing process, can promote the generation of crystal defects in an industrial cast-mono ingot (G0, G1, etc.). This is illustrated in Figure 5.2, in which two different types of seed configurations were tested on the basis of both multi and mono crystalline materials, to check how the junctions between adjacent seeds can act as sources of extended crystal defects.

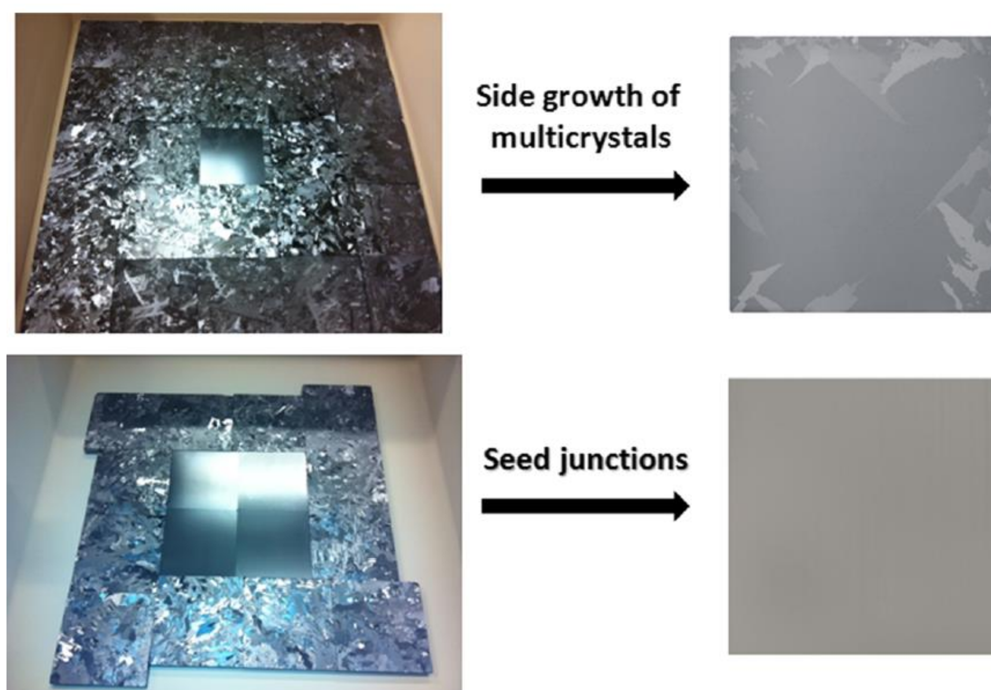
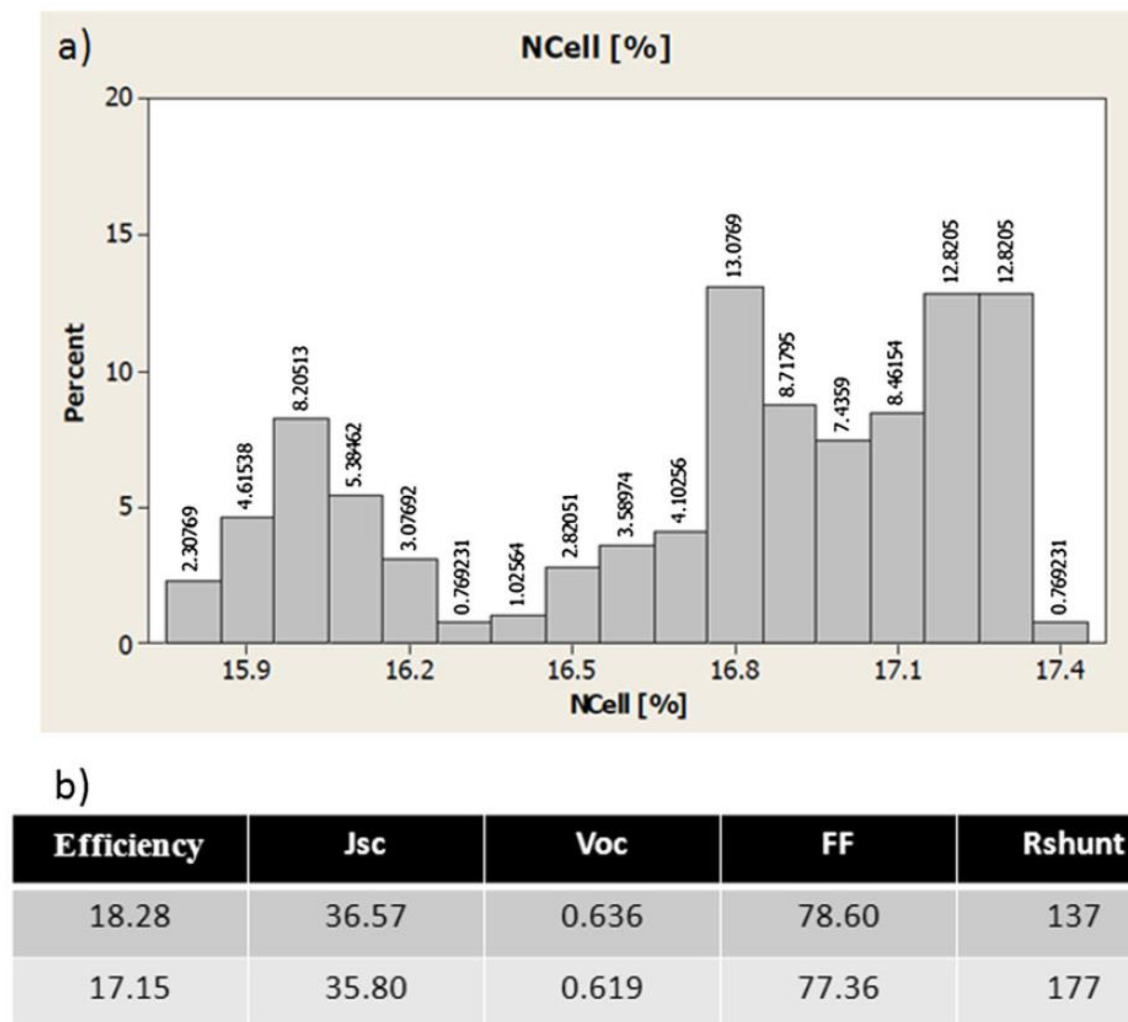


Figure 5-2: Different seed placing schemes to detect potential sources of defects from the very beginning of the seed-cast growth (1x1 centered and 2x2 seed configurations, respectively).

Despite the full mono crystalline aspect of the wafers obtained from the silicon brick obtained using a 2x2 central seed configuration, an analysis of the current–voltage (I–V) solar cell parameters showed large deviations in the absolute efficiency values, exhibiting undesirable low-performance efficiency tails, particularly for wafers arising from the top section of the brick. Such a broadly dispersed electrical performance was also observed in the mono/multi-based brick, resulting however in lower absolute efficiencies by 0.5%, due to the mc-Si side growth. In wafers from a full mono crystalline seed configuration (5x5 seed design), the I–V performance was found to exhibit double peak distribution for both short circuit current (I_{sc}) and open circuit voltage (V_{oc}), which resulted in a double peaked efficiency distribution (Figure 5.3(a)). Interestingly, such a detrimental outcome was markedly observed in wafers having large cast-mono regions, as CM (100% surface) and QM (>90% surface) series. This two-peaked electrical performance distribution was also observed in solar cells made from wafers from an CM series brick (table included in Figure 5.3(b)), but processed using alkaline texturing processes (plus ion implantation P-doping). This confirms the large performance distributions that can be obtained from these industrially cast mono crystalline ingots, even considering the same brick, based on complete mono crystalline wafers.

Crystal growth issues were suggested as the main origin of such a remarkable double peak distribution of the electrical parameters. Thus, an optoelectronic study was conducted, for which both PL and m-PCD minority carrier lifetime analysis over the whole surface of a series of wafers representing the bottom (above the seed region interface) and top sections of the brick were performed.



Efficiency	Jsc	Voc	FF	Rshunt
18.28	36.57	0.636	78.60	137
17.15	35.80	0.619	77.36	177

Figure 5-3: (a) Typical efficiency distribution from a seed-cast ingot for CM and QM wafer series processing. The typical efficiency average value for common mc-Si wafers, using the same solar cell methods is 16.4%; (b) I–V values obtained using alkaline texturing and ion implantation phosphorus doping (without any selective emitter implementation), in the case of CM wafers from the same brick. The values represent the average parameters resulting from the two-peaked solar cell distribution that was observed.

The PL analysis of Figure 5.4 allowed to conclude that an undesirable propagation of extended defects from bottom to top clearly occurred (similar to what is typically observed in mc-Si cast growth), which seems to be favored by the seeds junctions at the very beginning of the growth run. The m-PCD lifetime analysis revealed exceptionally high Fe interstitial concentration [Fei] at the bottom region of the bricks (ca. 5.3×10^{12} cm^{-3}), decreasing by more than one order of magnitude (ca.

1.4 x 10^{11} cm^{-3}) when going from bottom to top (Figure 5.4), regardless of the low segregation coefficient of this element in silicon (2 x 10^{-5}). Therefore, this would indicate that the efficiency decrease of solar cells made of wafers sliced from the top sections of the ingot is mostly dominated by the defect generation during the crystal growth. Indeed, it is well-known that the distribution of the Fe contamination, mostly entering the melt by solid-state diffusion from the crucible and silicon nitride coating, tends to move from interstitial to precipitated [63,64], from bottom to top of the ingot.

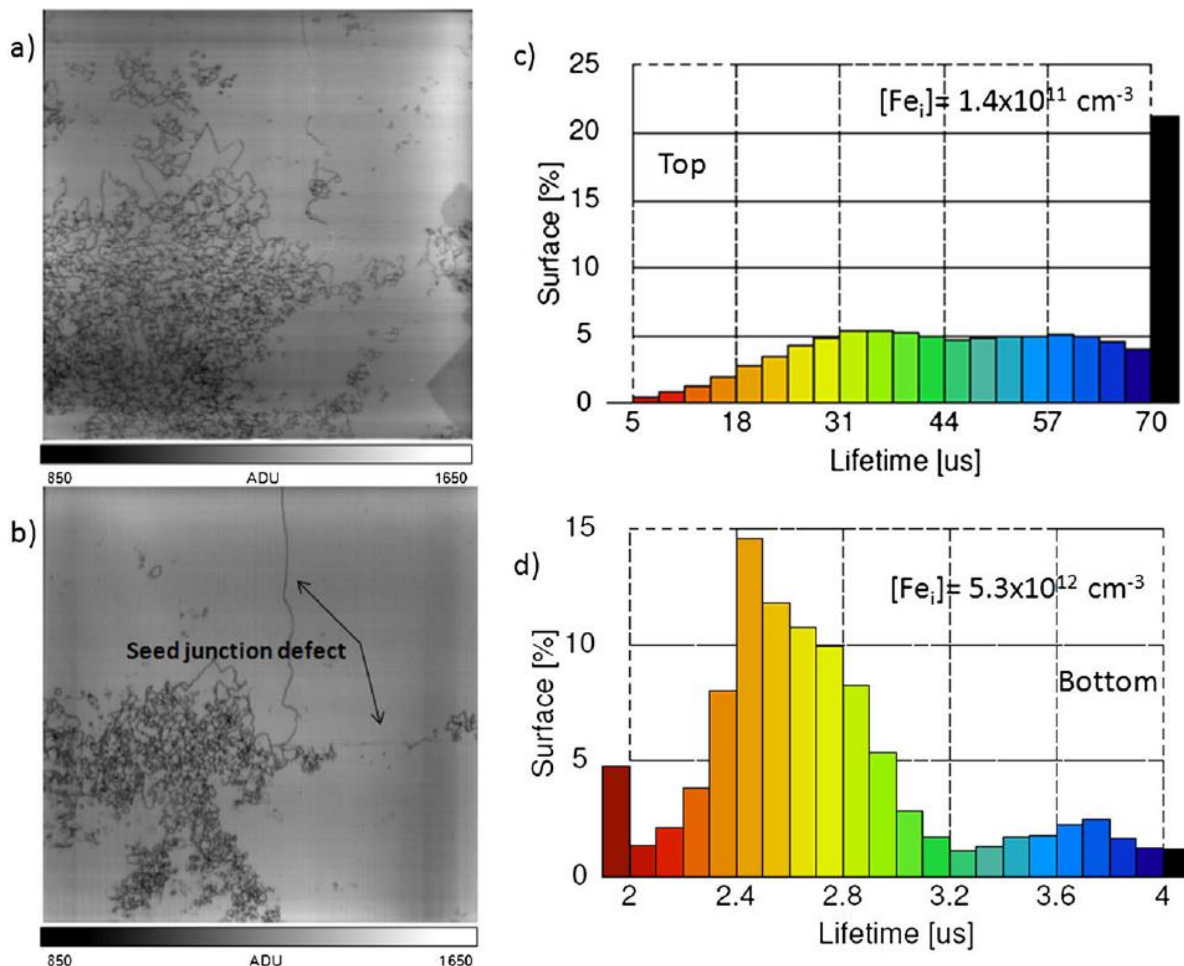


Figure 5-4: (a) Photoluminescence image of an as-cut wafer from the top of the brick; (b) same analysis corresponding to a wafer from a lower region; (c) carrier lifetime histogram and [Fei] values of a wafer from the top of the brick; and (d) same analysis, wafer from the brick's bottom.

Thus, in order to investigate this effect on cast-mono wafers, Figure 5.5 illustrates the evolution of [Fei] before and after a typical phosphorus gettering (PDG) process. It can be observed how the initial [Fei] concentrations are differently reduced after implementing the same PDG process. The gettering effect is markedly observed in the case of bottom wafers ([Fei] decrease in more than two orders of magnitude), which demonstrates that most of the Fe present in the crystal is presented under a dissolved state. In contrast, the effect of the defect generation towards the top results in lower [Fei] reduction, which suggests that Fe can move to precipitation sites, probably the defective regions observed by PL mappings.

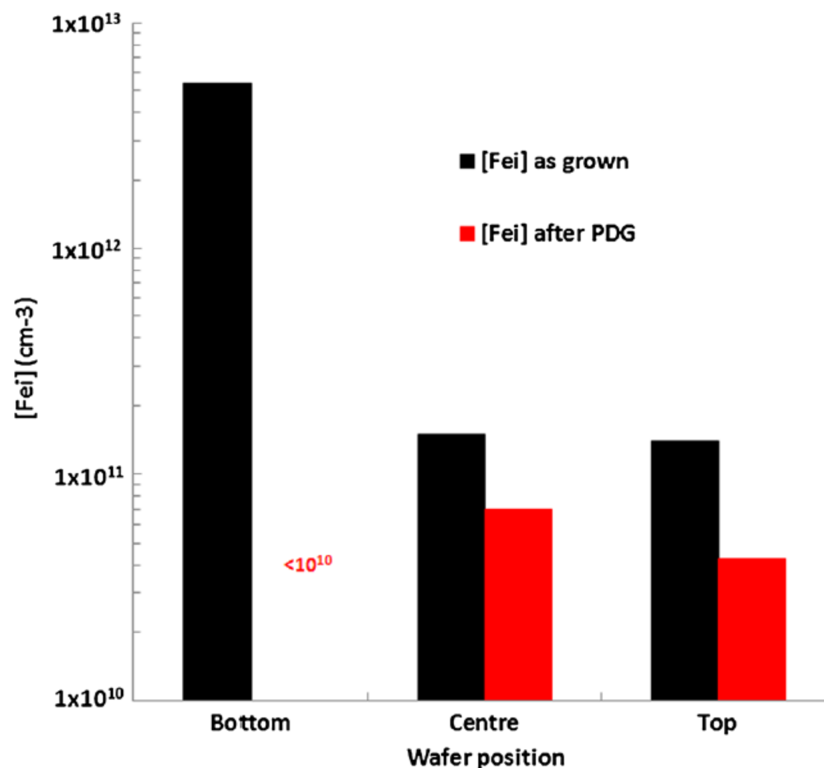


Figure 5-5: Evolution of the [Fei] before and after phosphorus gettering for wafers from bottom to top of a cast-mono brick (1.1 Ω-cm average resistivity).

This consistency between low lifetime and high Fe concentration at the bottom zone of the brick is directly attributed to the competition between the rate of Fe segregation just after the crystal nucleation and the back-diffusion of Fe coming from the crucible walls and coating just before the melting phase end [56]. This

effect results in both seed degradation and pronounced low lifetime tails above the seed, even more marked than in a typical mc-Si cast growth figure 5.6 (a)), which can have an important influence on the yield and mass production of this particular type of ingots. In addition, a higher lateral curvature is evident when implementing the seed-cast growth approach in a typical DSS casting furnace (figure 5.6 (b)), in comparison with a common mc-Si process (figure 5.6 (c)). This is a consequence of the higher thermal gradients occurring during the growth, because the thermal history of the silicon mass differs from each other's type of ingot growth approach (table 5.1), due to the aforementioned passive heat extraction from the bottom of the crucible. Figure 5.7 represents two detrimental phenomena occurring in a brick squared from the ingot corner, from bottom to top, measured by PL: (a) increase of the mc-Si patterns towards the center of the brick; and (b) propagation of extended defects in the mono crystalline region of the wafer.

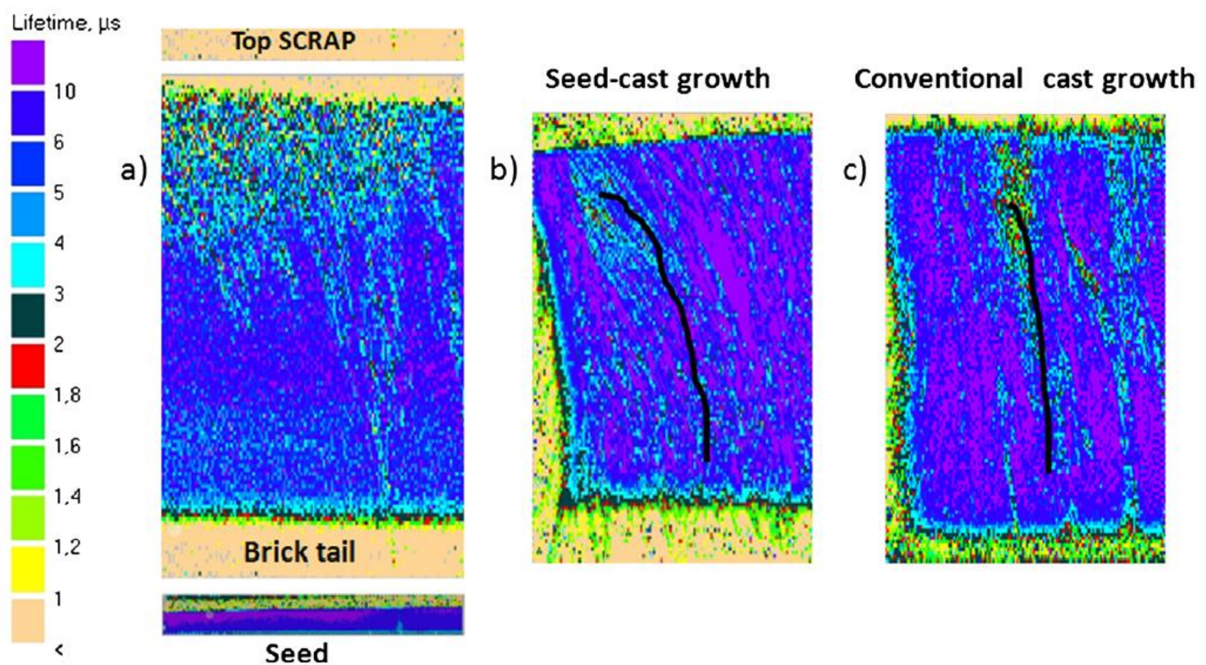


Figure 5-6: (a) Microwave photoconductance decay lifetime mapping of a brick (central) from a seed-cast growth process; (b) cropped brick (lateral) from the same ingot; and (c) cropped brick (lateral) from a common mc-Si cast ingot.

Table 5-1: Comparison between thermal gradients for a seed-cast and a normal cast processes at three different stages of the crystal growth, at both the center and the lateral sides of the ingots, calculated from experimental data.

Thermal gradient K/cm

Interface position	Seed-cast		Normal cast	
	Center	Lateral	Center	Lateral
2 cm	15.1	10.4	12.9	9.8
12 cm	12.6	10.3	11.5	9.1
24 cm	8.8	7.1	8.9	6.8

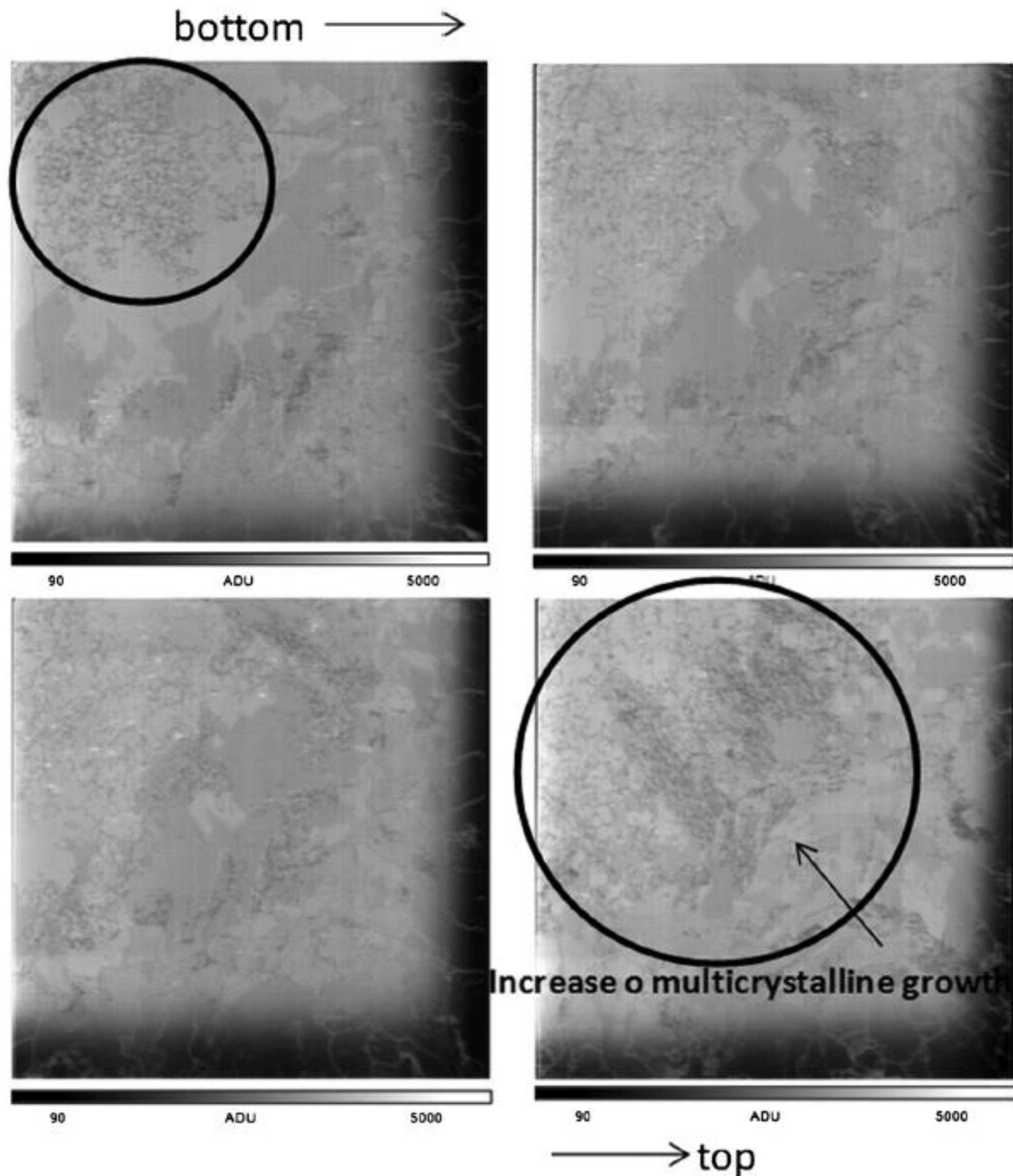


Figure 5-7: Photoluminescence (PL) images of as-cut wafers of a corner brick, squared from a seed-cast ingot. The arrow indicates the mc-Si grown region increase, whereas the circles count on the density of extended defects growing from bottom to top, at the mono crystalline region of the wafer. The low activity dark regions at the right-down sides of the PL images are due to contact between silicon and the crucible walls, typically more contaminated from solid-state diffusion of impurities.

5.1.2.2. Towards the seed recycling

The use of high-quality Cz-Si mono crystalline seeds is definitely critical for the obtention of high performance cast-mono wafers. From an industrial standpoint, the implementation of this growth approach at mass scale requires a detailed cost analysis and optimization to obtain profitability. A critical issue of the process refers to the manufacture and treatment of Cz-Si ingots to make mono crystalline seeds, which can play a major role on both the cost per wafer and the cost per Watt. Therefore, the recycling of the virgin seeds (from a G0 process) seems mandatory.

From the results presented before, the bottom section of the ingots, including the seed part, appears to be significantly affected after the first ingot growth run. Both crystal and impurity effects were noticed. Therefore, the question at this point is to know how much the quality of the seed is degraded in that region and what can be the consequences in the performance of wafers from Gn ingot growth runs.

For that purpose, a series of industrial size ingots were manufactured, monitoring the transverse m-PCD lifetime degradation of the seeds after consecutive seed-cast crystalline growths. Figure 5.8 illustrates an example, in which the analysis of half an ingot section—after a G0 process (degradation of the individual seeds after one cast-mono process), then of G1 seeds to be used for the next growth run—collecting data from every respective seed profile. The figure includes also the lifetime map of one of the virgin seeds used to make the cast-mono ingot.

The degradation after the ingot growth process increases significantly, according to the following degradation features:

1. Lifetime degradation towards the crucible base. Both solid-state diffusion of metal impurities and high oxygen concentration from the crucible are likely to be the causes of such a quality degradation.
2. Curved melting front of the seed. Both the heat exchange paths offered by the graphite's hot zone and the used furnace settings during the seed-cast growth result in a non-linear melting behavior of the seeds near the crucible walls. This is critical for recycling the seed, as the consecutive Gn slabs will contain larger mc-Si patterns, which will be transferred from the very beginning of the process. Also, these mc-Si grains propagate to the center of the ingot from bottom to top, as stated before (Figure 5.7).

3. Low lifetime region at the top of the seed. The larger the fraction of the melted seed, the deeper the low lifetime region after crystallization. Also, the back-diffusion of Fe, which can promote the generation of crystal defects, is increased with seed recycling.
4. Low lifetime seed junctions. The respective edges of the seeds act as defect nucleation regions. In addition, the silicon melted mass over the slabs, presumably contaminated by Fe, just prior to the crystal growth beginning, can percolate through those geometric imperfections, degrading those transition zones after solidification. This phenomenon would be also related to the degradation of the seed region in contact with the crucible base. Therefore, the more the number of seed recycling processes, the larger the lifetime degradation occurs in the slabs.

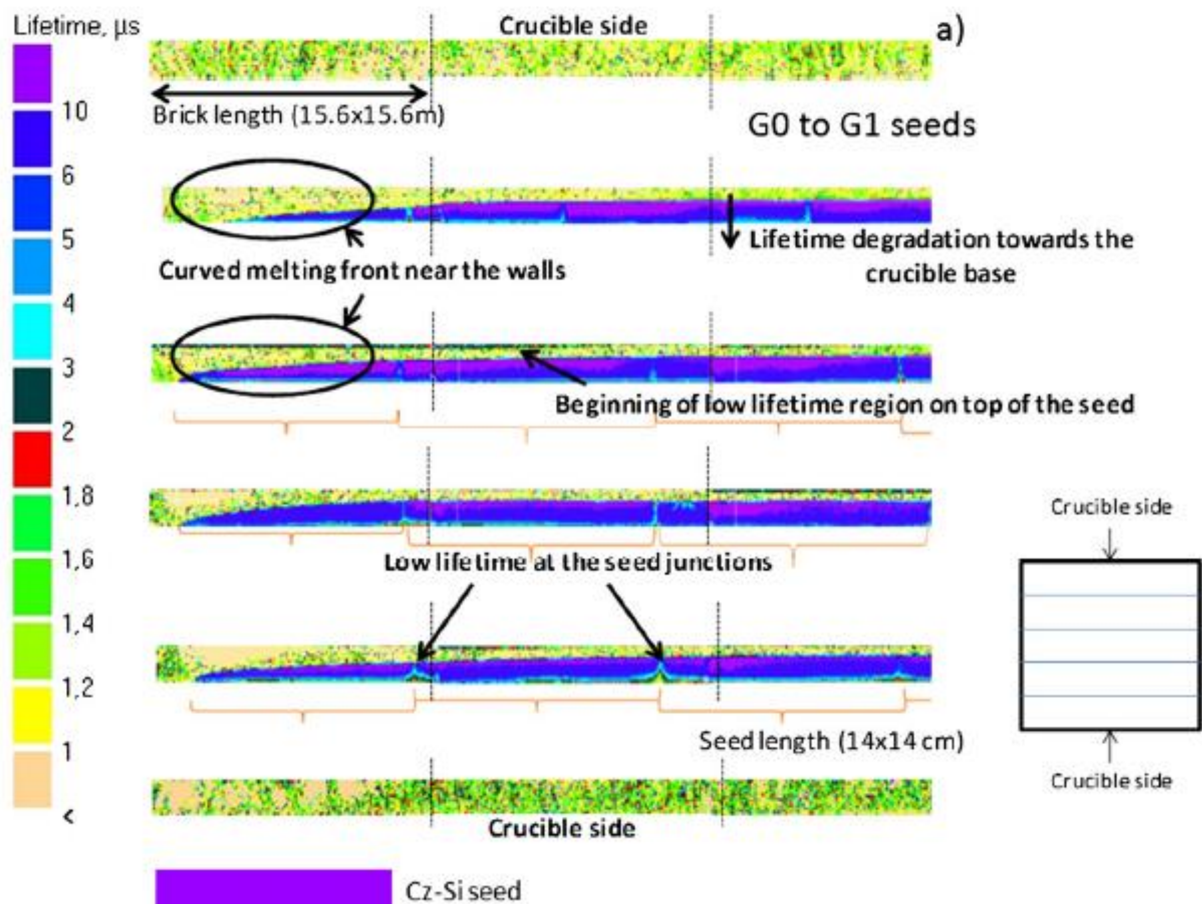


Figure 5-8: (a) Transversal microwave photoconductance decay lifetime mappings for a series of cropped seeds (14 cm x 14 cm x 2 cm size) after having been used in the same G0 ingot growth (after just one seed-cast process). The scheme represents the section of half a directional solidification ingot (25 bricks 15.6 cm x 15.6 cm size). A sketched chart of the top of an ingot is included as an inset, in order to clarify the cross sections of the seeds illustrated on the left side of the figure; (b) lifetime mappings of the same seeds after a second ingot growth (G1 process), in this case showing the entire 5 x 5 seeded ingot.

Consecutive recycling of the seeds can result in important loss of wafer electronic quality by >0.7% in absolute efficiency. This is mainly caused by the remarkable decrease in the I_{sc} values, as the density of extended bulk defects dramatically increases. For a solar cell manufacture, the use of wafer alkaline texturing processes could mitigate to a certain extent such an adverse outcome, in terms of cost production balance issues (fair cost/W ratio). Figure 5.9 (a) illustrates a PL analysis on wafers sliced from a G2 ingot.

The image shows a cast-mono wafer crisscrossed by dark line defects over the full surface, which directly results in poor I–V solar cell performances. A simple surface cleaning by KOH/HCl etch agents reveals the presence of crystal defects, such as subgrain boundaries [61] (Figure 5.9 (b)).

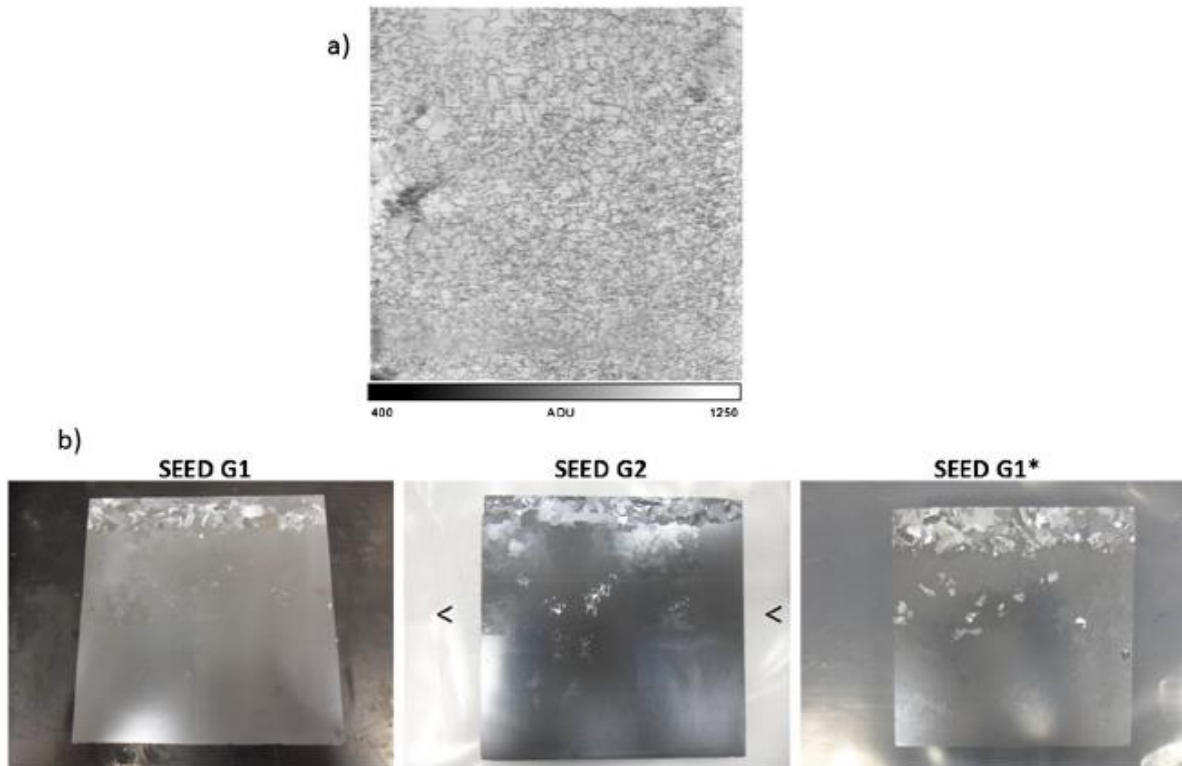


Figure 5-9: (a) Photoluminiscence image of a full cast-mono wafer (15.6 cm x 15.6 cm) coming from a Gn ingot, characterized by a large density of defects; (b) pictures of different seeds coming from the same lateral brick. G1* corresponds to a silicon slab used as cast-mono seed, extracted from the immediate section above the G1 seed. Its crystal quality is rather poorer than that of a G2 seed.

Moreover, a reduction of the percentage of the cast-mono wafer yield per ingot can also be noted. Therefore, a mass production implementation of the seed-cast growth approach needs a dedicated and cost balanced technical revision.

The typical thermal stresses appearing during the silicon growth process, which result in plastic deformation leading to networks of dislocations, are suggested to be more pronounced from bottom to top. The occurrence of microdefects due to impurities precipitation, and SiC and Si_3N4 inclusions is also present in a seed-cast growth process, as it happens in a typical mc-Si casting process. As we

described in chapter 4, the presence of bulk defects influences the mechanical properties of the wafers. Therefore, an increase in the macroscopic breakage yield during the industrial handling can be expected. In chapter 4 we also showed that there are direct effects of such a high density of defects (Figure 5.9 (a)) in the fracture tension limits of the wafers, as determined by a systematic four-line bending test (FLBT) analysis where we described that a batch of 50 highly dislocated cast-mono wafers exhibited up to ca. 15% lower fracture tension average values than an equivalent number of samples of dislocation-free Cz-Si square mono crystalline wafers, showing in any case a reasonable tension fracture behavior. These wafers were chemically etched to remove the surface damage generated during the sawing process, in order to highlight the intrinsic mechanical properties of the wafers.

The strain field of dislocations influences its recombination activity [62]. Consequently, additional studies on the electrical performance of these defects were performed using high spatial resolution LBIC analysis (better than 1 mm) on solar cells manufactured from different Gn-based wafers.

LBIC maps (Figure 5.10) illustrate different charge capture activities from extended defects of neighboring regions, in the mono crystalline region of the wafer. Indeed, the electrical activity of such defects was found to be dependent on the Gn ingot growth, which would imply both an increase of the density of decorating defects and higher precipitated impurities, in agreement with the loss of solar cell efficiency when increasing the number of seed recycling processes. All the previously mentioned seed degradation sources still indicate that the recycling and/or regeneration of the original Cz-based silicon slab, even if highly recommended at industrial level, is not a straightforward task. However, both the quality devaluation effects produced on the seeds after consecutive cast-mono ingot growth runs, and the extended defects generation during crystal growth can be alleviated to some extent. This can be achieved by designing and conducting a series of process optimizations and hardware modifications. The improving strategies can be listed as follows:

1. Progressive melting of the seed during consecutive growth cycles, starting from an optimized silicon slab thickness. Perfect control of the melting front just before the initiation of the crystal growth is also recommended.

2. Promotion of a preferential heat flux along the seed versus the crucible sides, in order to avoid high thermal stresses that can generate high dislocation densities and decrease the mc-Si lateral pattern formation. This should be achieved by modifying the graphite susceptor design and properties and/or the graphite block constituting the crucible base. Also, the crucible thickness can play a role, as it is formed by low thermal conductive fused silica.
3. In case of using a series of small size Cz-Si seeds to promote the mono crystalline growth, and not only one large crystalline silicon slab located at the bottom of the crucible, a high-quality sawing process of the original seeds and the subsequent recycled fragments shall be performed. The control of the silicon orientation at the seeds cross sections should be taken into account, in order to get more stable crystalline boundaries between seeds.
4. Use low Fe contaminated crucible/inner coatings.
5. Use different seed orientations to support the cast-mono outcome all over the ingot, mainly at regions near the crucible sides and corners.
6. At solar cell level, a defined optimization of the texture processes for the non-perfect mono crystalline quality of the cast-mono wafers would help to increase the cost/performance ratio, balancing the production costs over all the PV silicon chain.

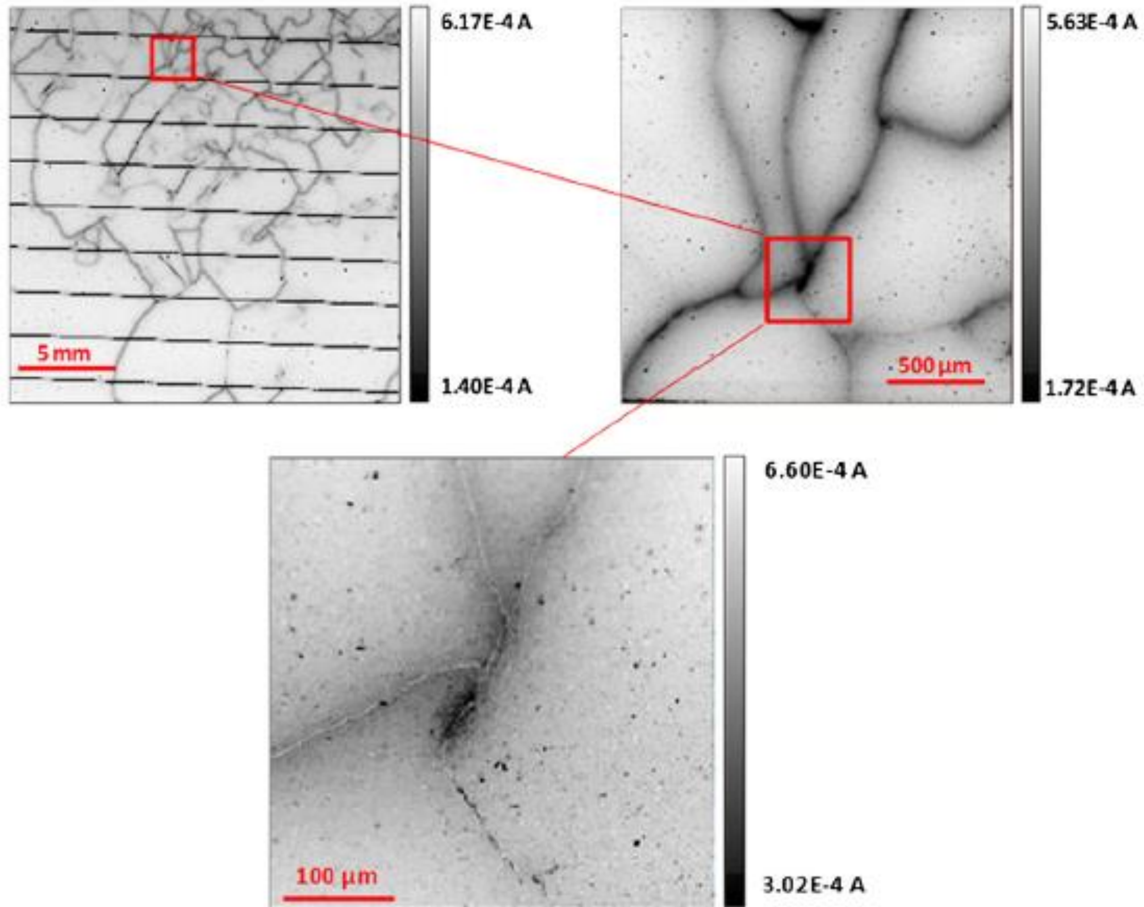


Figure 5-10: Laser beam induced current maps (830nm light excitation) of a solar cell made from a G1 ingot wafer. The three images represent different spatial resolutions. Note how the electrical activity of the intragrain defects appears non-homogeneous as the resolution is enhanced, which is the consequence of the impurity atmosphere surrounding the dislocations. In the largest resolution image, one clearly observes a bright contrast line drawing the defect and the dark atmosphere (charge capture) surrounding it.

5.2. Yield Performance of standard multi crystalline, mono crystalline and cast-mono modules in outdoor conditions

In this study we report for the first time the field performance of a CM-Si based PV system and compared it with similar technologies. To do so, we put in the field three small installations consisting of 12 modules each and next to each other, all of them using the same manufacturing technology for cells (PERC- passivated emitter and rear cell technology) and modules, same manufacturing equipment and raw materials, being the only difference between the systems the wafers technology employed. Two of the systems are manufactured through the same casting technology (Direct solidification system-DSS [63][64][65]) and the same equipment but in one of them we grew mc-Si and on the other one CM-Si. The third system uses standard Cz silicon wafers. The facilities have been closely monitored for three years for the casting technologies and for 17 months for the Cz system, and the performance data is shared and analyzed in this study.

5.2.1. Materials and methods

5.2.1.1. Description of the installation

The three generators used for this experiment consisted on 12 glass-backsheet PV modules model CS3U manufactured by Canadian Solar, each mounted on typical two rows portrait fixed racking system. One of the systems used CS3U-P (P3) mc-Si modules for a total of 4.06 kWp (Array mc) other used CS3U-P (P5) CM-Si modules for a total of 4.50 kWp (Array CM) and the last one used CS3U-MS Cz-Si modules for a total of 4.54 kWp (Array CZ). All systems were located next to each other in a Canadian Solar testing facility in Suzhou China coordinates N 31.3 E 120.8, south oriented, 25^0 tilt and without shadowing, as shown in Fig. 5.11. Each generator was connected to the grid through a Huawei Sun 2000-10 KLT inverter of 10 kW.

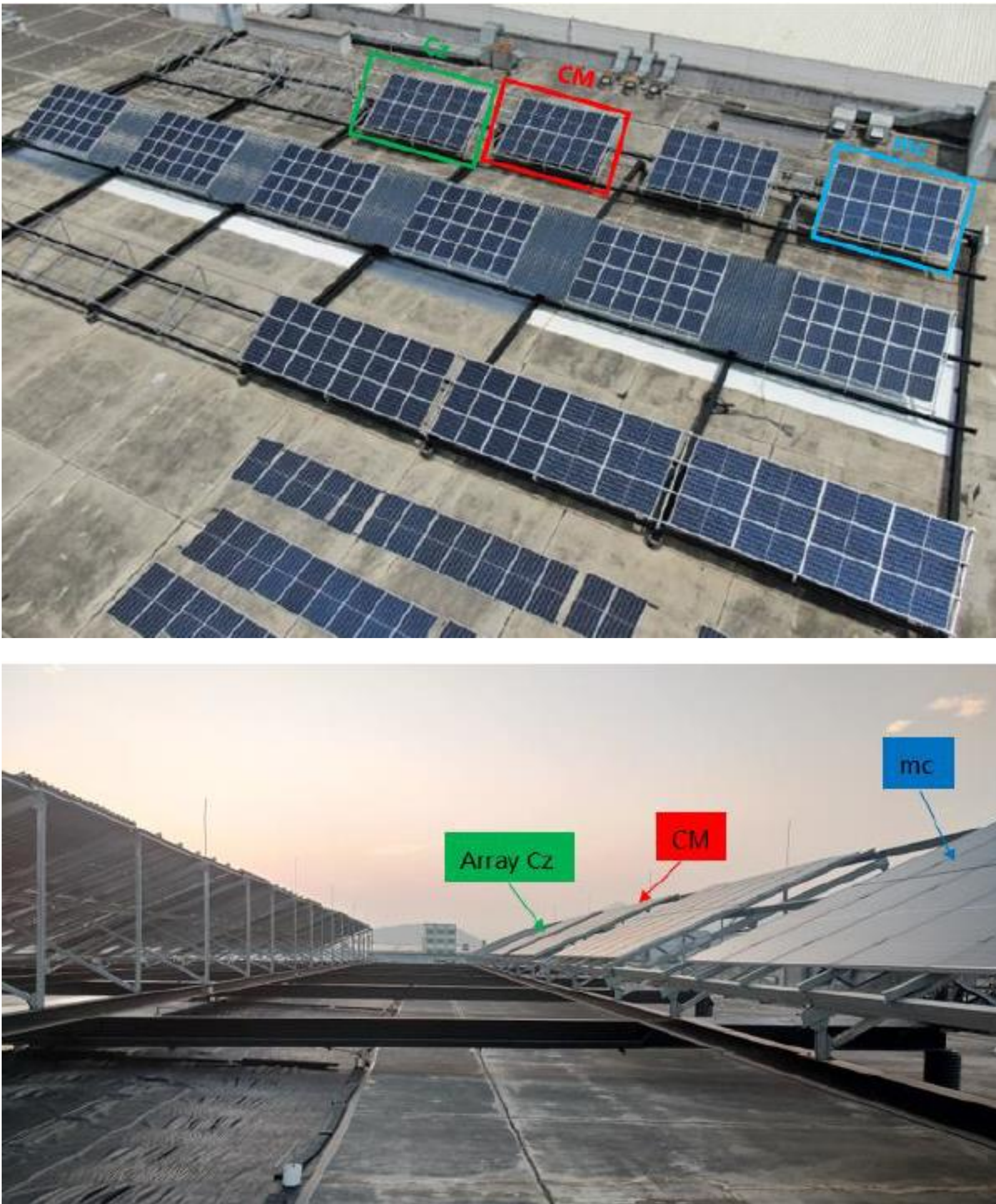


Figure 5-11: Two different views of the field trial test setup.

5.2.1.2. Data collection

Detailed measured module electrical parameters under Standard Test Conditions (STC) after 120 kWh/m2 outdoor exposure are shown in Table 5.2.

Table 5-2: Modules electrical information summary.

Array mc	SN	Initial Power (W)	Pm [W]	Vm [V]	Im [A]	Voc [V]	Isc [A]
1	Y1019206450004	337.21	337.0	38.3	8.79	46.1	9.26
2	Y1019206450005	337.53	338.4	38.4	8.81	46.2	9.27
3	Y1019206450006	339.01	337.2	38.4	8.79	46.1	9.25
4	Y1019206450007	338.02	337.2	38.4	8.79	46.1	9.25
5	Y1019206450008	338.61	339.0	38.4	8.83	46.2	9.3
6	Y1019206450009	338.36	338.0	38.4	8.81	46.1	9.28
7	Y1019206450010	337.00	339.6	38.4	8.85	46.1	9.31
8	Y1019206450012	339.63	337.5	38.4	8.79	46.1	9.27
9	Y1019206450013	338.51	338.5	38.4	8.81	46.1	9.28
10	Y1019206450015	338.65	339.0	38.4	8.82	46.2	9.3
11	Y1019206450016	339.02	338.7	38.4	8.81	46.2	9.27
12	Y1019206450017	337.21	338.6	38.4	8.82	46.2	9.27
Sum			**4058.7**				

Array CM	SN	Initial Power (W)	Pm (W)	Vm (V)	Im (A)	Voc (V)	Isc (A)
1	Y1019206450052	374.25	375.1	39.4	9.52	48.1	10.02
2	Y1019206450053	375.27	374.3	39.4	9.5	48	10
3	Y1019206450054	373.67	375.3	39.4	9.52	48.1	10.02
4	Y1019206450055	374.47	375.5	39.4	9.53	48.1	10.02
5	Y1019206450056	375.13	375.7	39.4	9.53	48.1	10.04
6	Y1019206450057	375.01	375.0	39.4	9.52	48.1	10.01
7	Y1019206450058	372.71	374.5	39.4	9.51	48	10.01
8	Y1019206450059	374.85	374.9	39.3	9.53	48	10.04
9	Y1019206450060	374.58	373.7	39.4	9.5	48	9.99
10	Y1019206450061	375.74	374.6	39.4	9.51	48.1	10.03
11	Y1019206450066	373.89	372.7	39.3	9.48	48.1	9.96
12	Y1019206450069	375.52	373.9	39.5	9.47	48.2	9.94
Sum			**4495.2**				

Array CZ	SN	Initial Power (W)	Pm (W)	Vm (V)	Im (A)	Voc (V)	Isc (A)
1	Y1019246361116	377.71	377.7	39.78	9.49	48.14	10.02
2	Y1019246361114	377.99	378.0	39.89	9.48	48.15	10.04
3	Y1019246361108	377.37	377.4	39.98	9.44	48.07	10.04
4	Y1019246361121	377.26	377.3	39.77	9.49	48.13	10
5	Y1019246361112	378.24	378.2	39.79	9.5	44.16	10.04
6	Y1019246361111	378.92	378.9	39.89	9.5	48.16	10

7	Y1019246361115	376.66	376.7	39.87	9.45	48.11	10.03
8	Y1019246361113	378.79	378.8	39.77	9.52	48.12	10.04
9	Y1019246361118	377.89	377.9	39.66	9.53	48.03	10.04
10	Y1019246361117	378.06	378.1	39.76	9.51	48.12	10.01
11	Y1019246361109	378.03	378.0	39.73	9.52	48.06	10.03
12	Y1019246361110	379.58	379.6	39.77	9.54	48.18	10.05
Sum			**4536.5**				

Table 5.3 shows the temperature coefficient of power (γ), voltage (β) and current (α) for the three mc-Si, CM-Si and CZ-Si based modules provided by the manufacturer and 83 measured in accordance to standard procedures.

Arrays CM and mc were measured from 26th of July 2019 until 19th of July 2022 while array CZ was measured from 20th of August 2019 until 31st of December of 2020. System performance (DC and AC Voltage and Current and AC Power) and ambient data (Ambient and module temperature measured at 4 different points for each array, wind speed and direction, inclined plane irradiance and horizontal irradiance and rain) were measured every minute using the equipment described in Table 5.4. There was no difference in the equipment employed or the location of the sensors on the arrays.

Table 5-3: Modules electrical information summary.

Temperature Coefficient	**γ (Pmax) (%/°C)**	**β (Voc) (%/oC)**	**α (Isc) (%/0C)**
CS3U-335P(P3)(mc-Si)	-0.38	-0.31	0.05
CS3U-370P(P5) (CM-Si)	-0.37	-0.29	0.05
CS3U-370 MS (Cz-Si)	-0.37	-0.31	0.05

Table 5-4: Measurement equipment list.

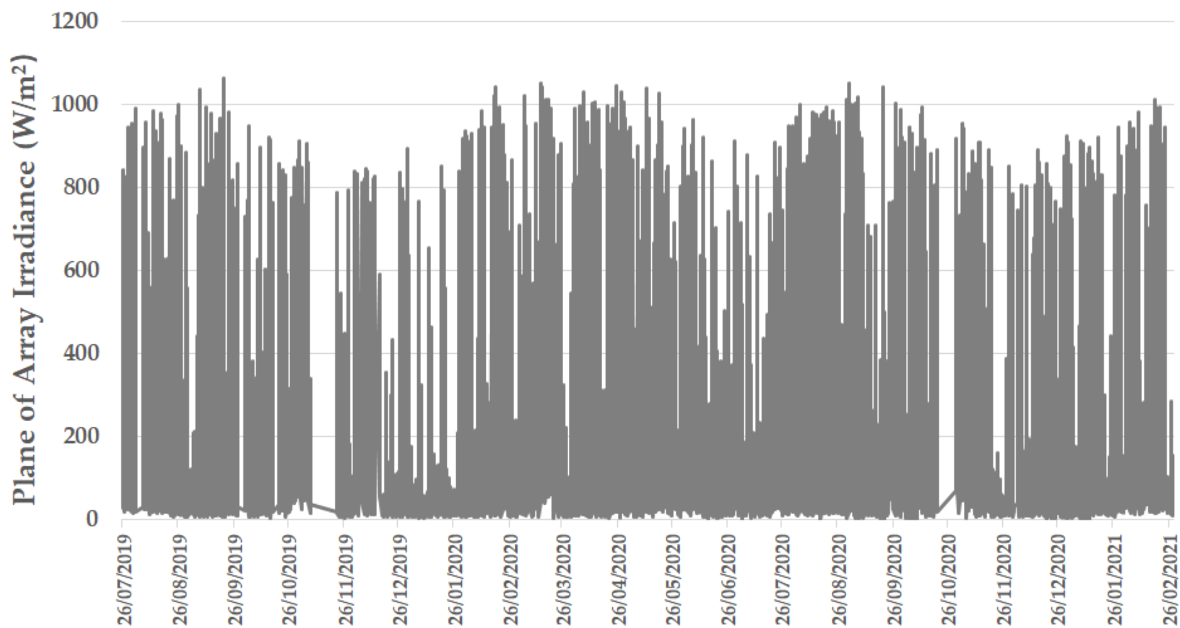
Equipment	**Vendor**	**Model**	**Tolerance**
DC Meter	GMC-I	V604s-20A	Voltage : ±0.2% Current : ±0.2%
Wind speed sensor	Met one	034b	V<10.1m/s : ±0.1m/s V>10.1m/s : ±1.1%*display value
Wind direction	Met one	034b	±4°
Rain sensor	Intell-sun	PHYL	±4%
Ambient temperature sensor	Rotronic	HC2S3	±0.1℃@20℃ ; ±0.3℃@-40℃
Humidity sensor	Rotronic	HC2S3	±0.8%*display value
Pyranometer	Kipp & Zonen	CMP10	Yearly instability <0.5%
Module temperature sensor	SUYI	PT100	±0.2℃@25℃

5.2.2. Results

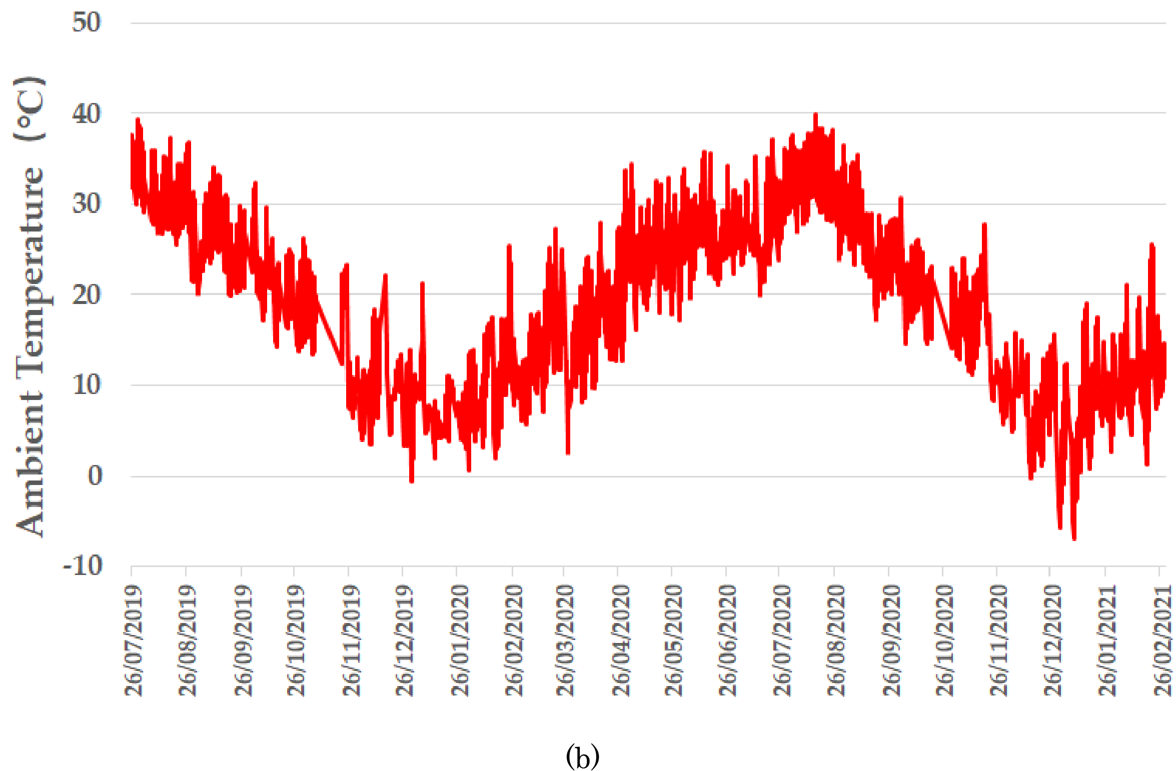
After the respective years of testing in outdoor conditions, the total irradiation measured in the system accounts for 3600 kWh/m2 for the period of measurement of Arrays mc and CM, and 1715 kWh/m2 for the period of measurement of Array CZ. During the testing period the facility did not provide data for a total of 13 weeks out of the 156 weeks of the testing period of three years (which also affected the Array CZ) for several reasons (system downtime or failed measurement from any sensor or measurement equipment in either of the arrays). Thanks to the long testing period we can assume that the data represent any climatic condition in the location.

The modules appearance through visual inspection showed no significant aging or degradation or hot spots or any other performance phenomena.

The performance of the systems in a given day is compared in these results as well as the energy production (yield) during the testing period. Figure 5.12 plots the site weather information over the testing period, Ambient temperature and Irradiance at the array plane.



(a)

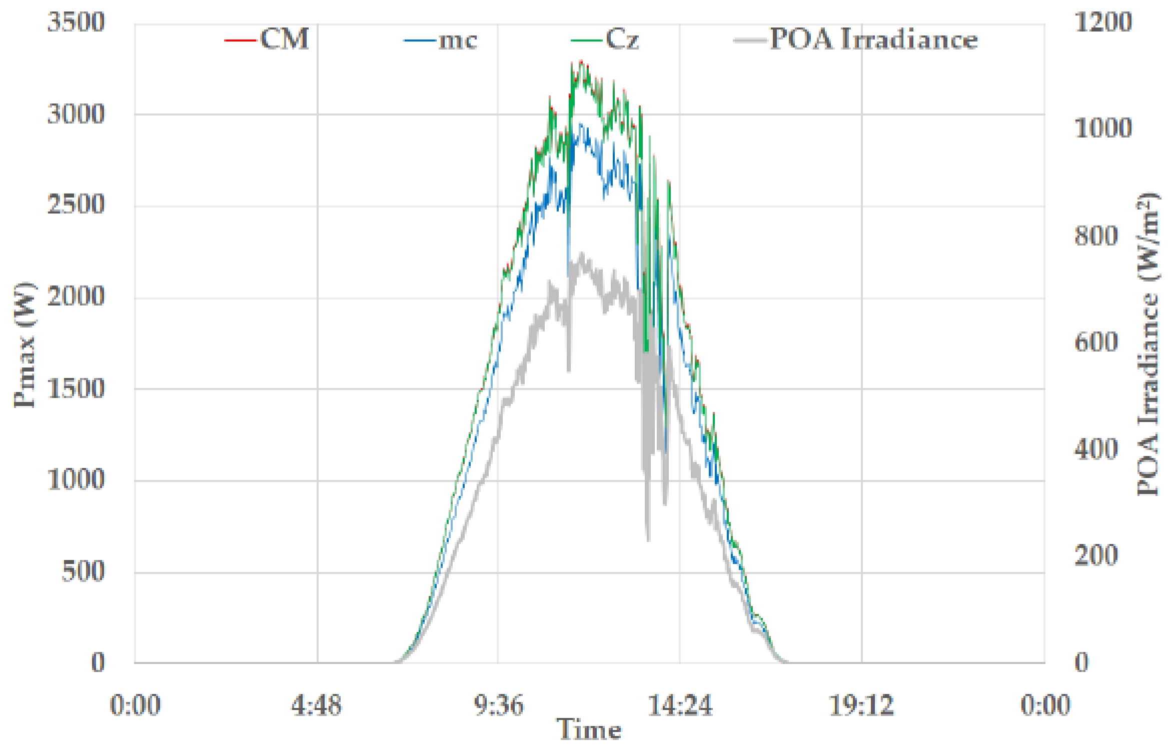


(b)

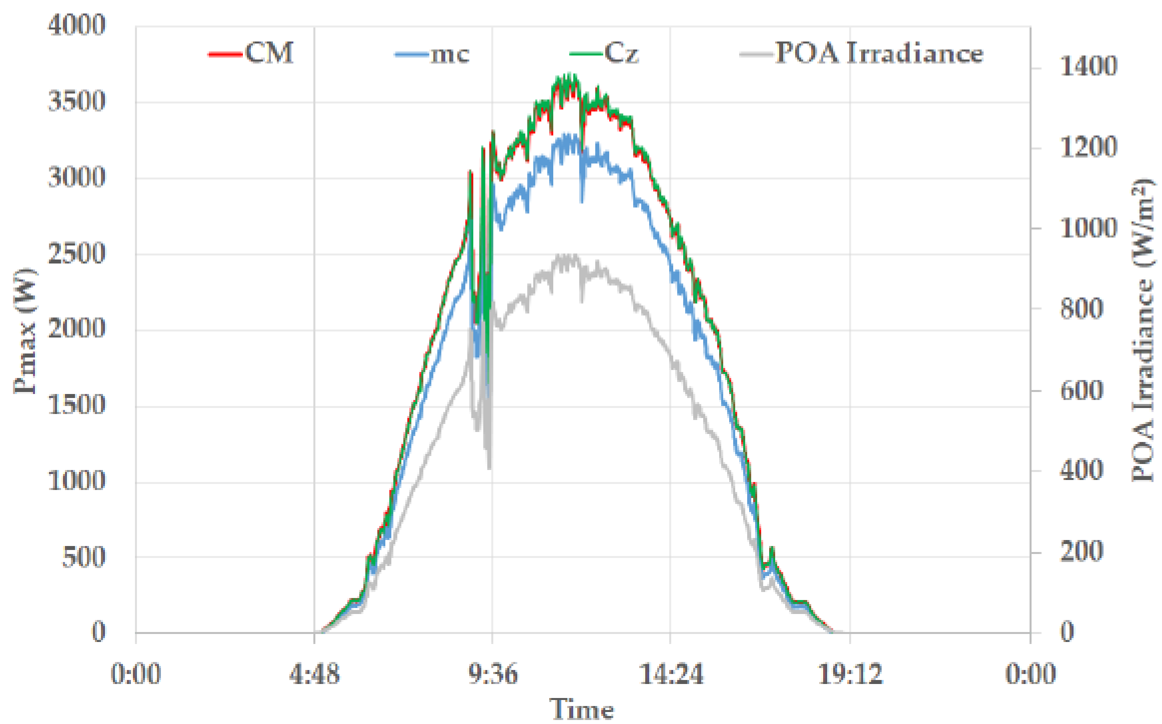
Figure 5-12: (a) Plane of array irradiance (W/m^2) over time; (b) Ambient T (^0C) over time.

5.2.2.1. Daily performance

Figure 5.13 shows the behavior of the systems in a standard winter day and summer day. The maximum power vs the time of the day is represented and compared to the pyrometer of array (POA) measurement. Arrays CM and CZ show almost identical results with higher Pmax than mc since the systems have more Wp installed.



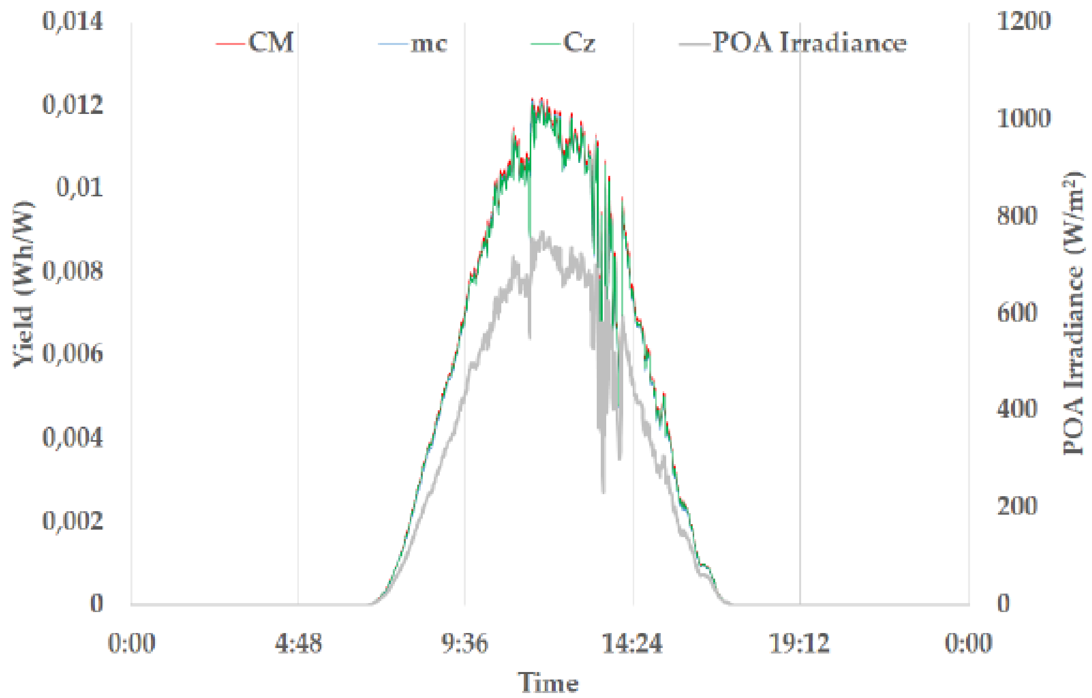
(a)



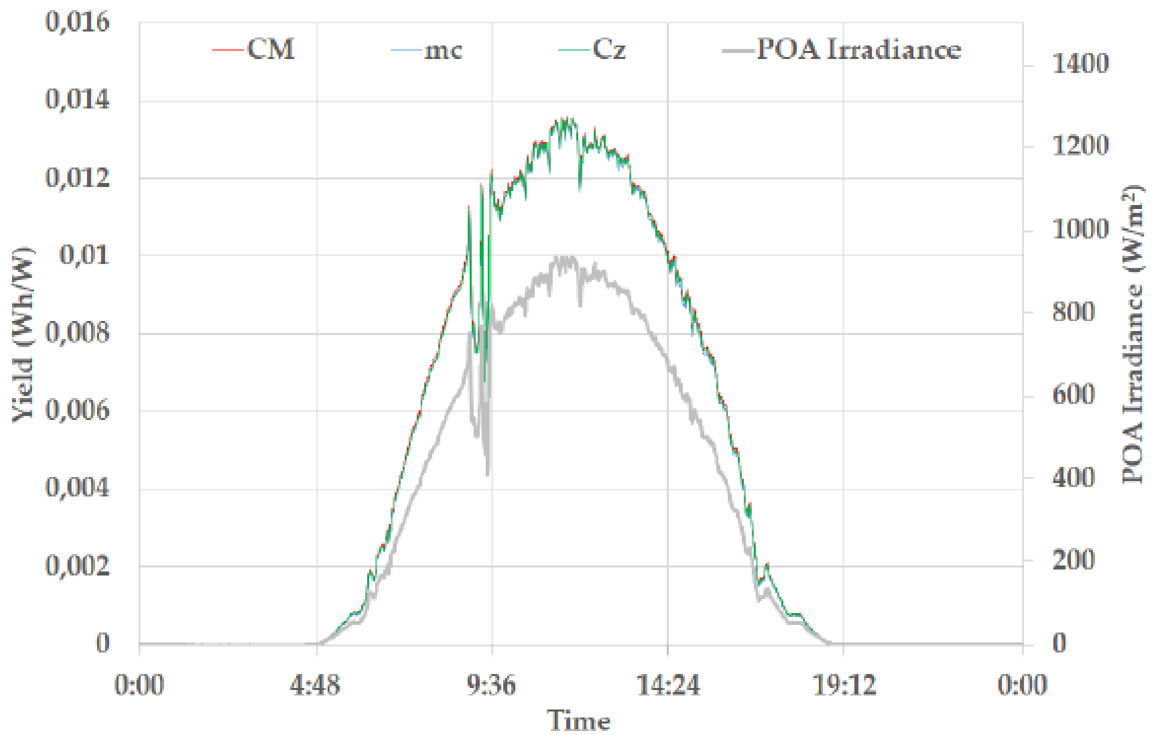
(b)

Figure 5-13: (a) Power vs POA on 28/12/2020 (Cloudy day); (b) Power vs POA on 2/06/2020 at the bottom (Sunny day).

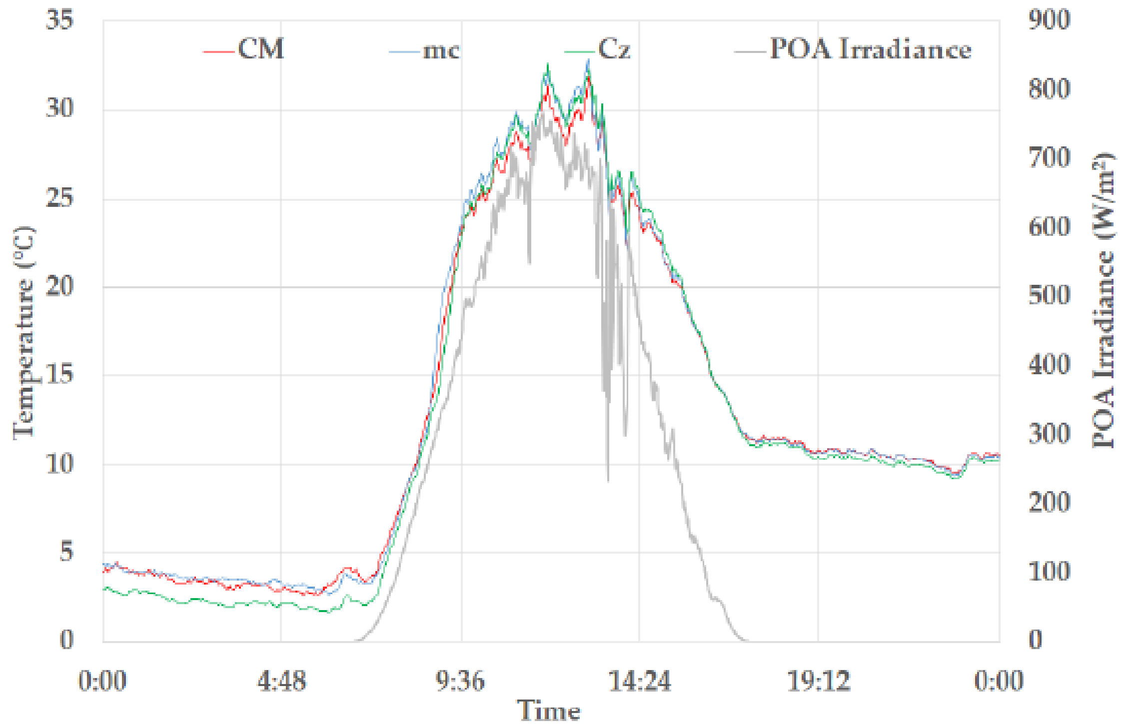
The daily yield curves are also very similar but with array CM consistently higher along the day as shown in Figure 5.14 for a typical winter and summer day. The temperatures of the modules are also shown in the same figure.



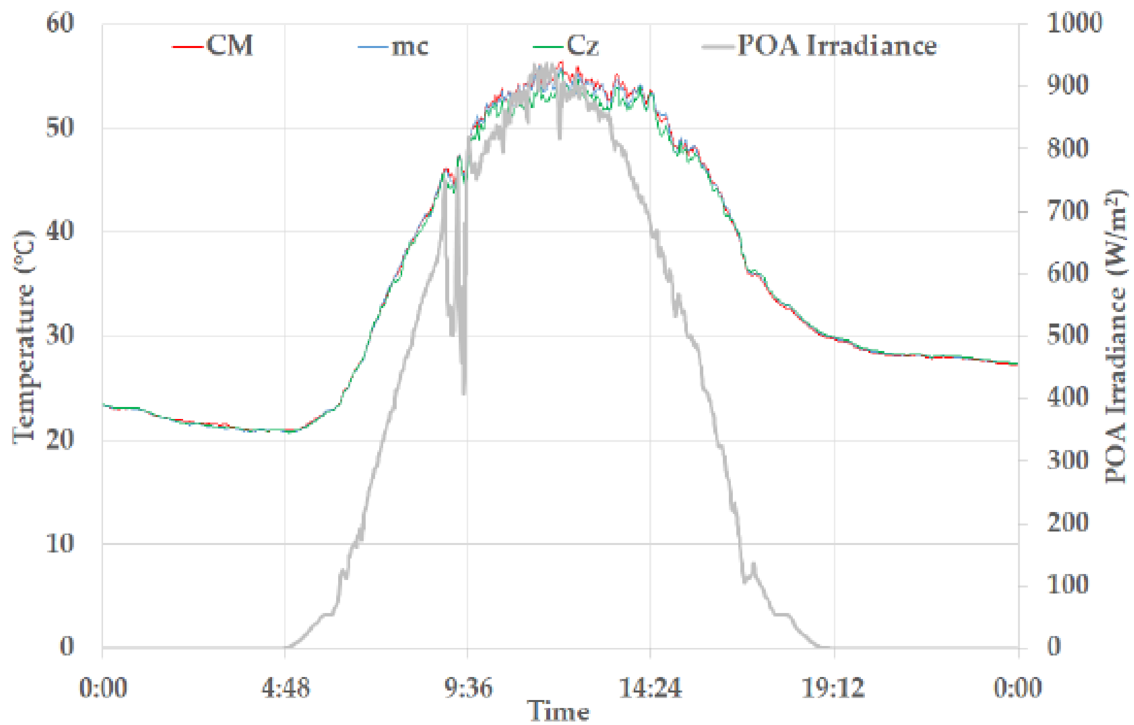
(a)



(b)



(c)



(d)

Figure 5-14: (a) Yield on 28/12/2020 (Cloudy day); (b) Yield on 2/06/2020 (Sunny Day); (c) Temperature on 28/12/2020; (d) Temperature on 2/06/2020.

Using the cloudy day figure 5.13 graph the kick-in and kick-out times are examined in figure 5.15 and they are almost simultaneous events in all systems. In fact in a sample of 30 consecutive days CM activated 17 times later and 13 times earlier or equal to mc, concluding that both systems have a very similar or identical activation energy. The result is very similar when compared to the Array CZ.

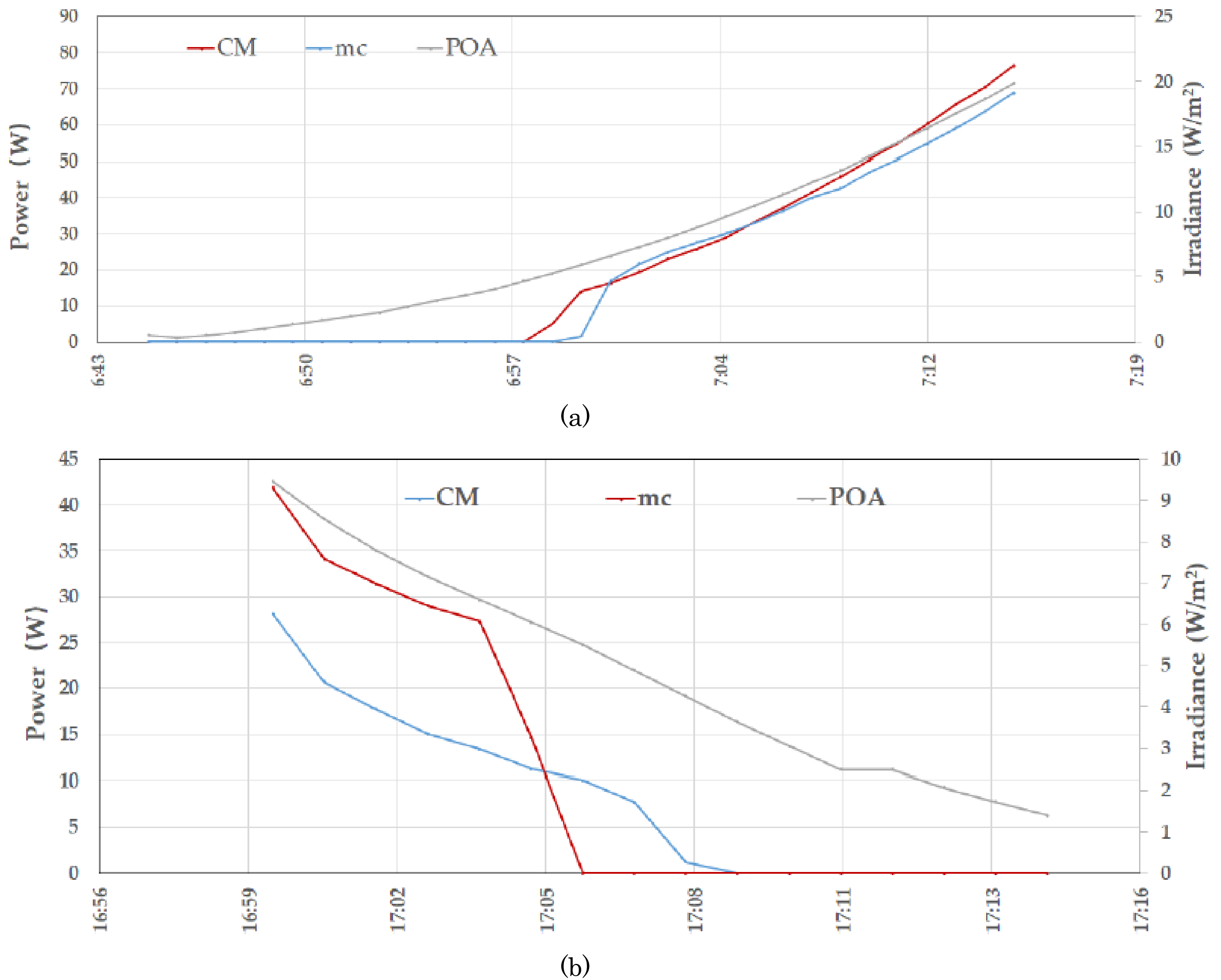


Figure 5-15: Inverter starting production on 28/12/2020; (b) Inverter stopping production on 28/12/2020.

5.2.2.2. Energy yield

Related to the energy production of the systems we collected a total of 143 weeks of production of the mc and CM systems and 61 weeks for the CZ system under the same conditions, a total of 156 (mc and CM) and 74 (CZ) weeks were measured but as already mentioned 13 of those presented measurement problems on different equipment or events of default such as loose cables, inverters defaults, etc. that invalidated the data.

Figure 5.16 shows the monthly energy yield of the systems in kWh/kWp and the difference on the energy yield of the systems.

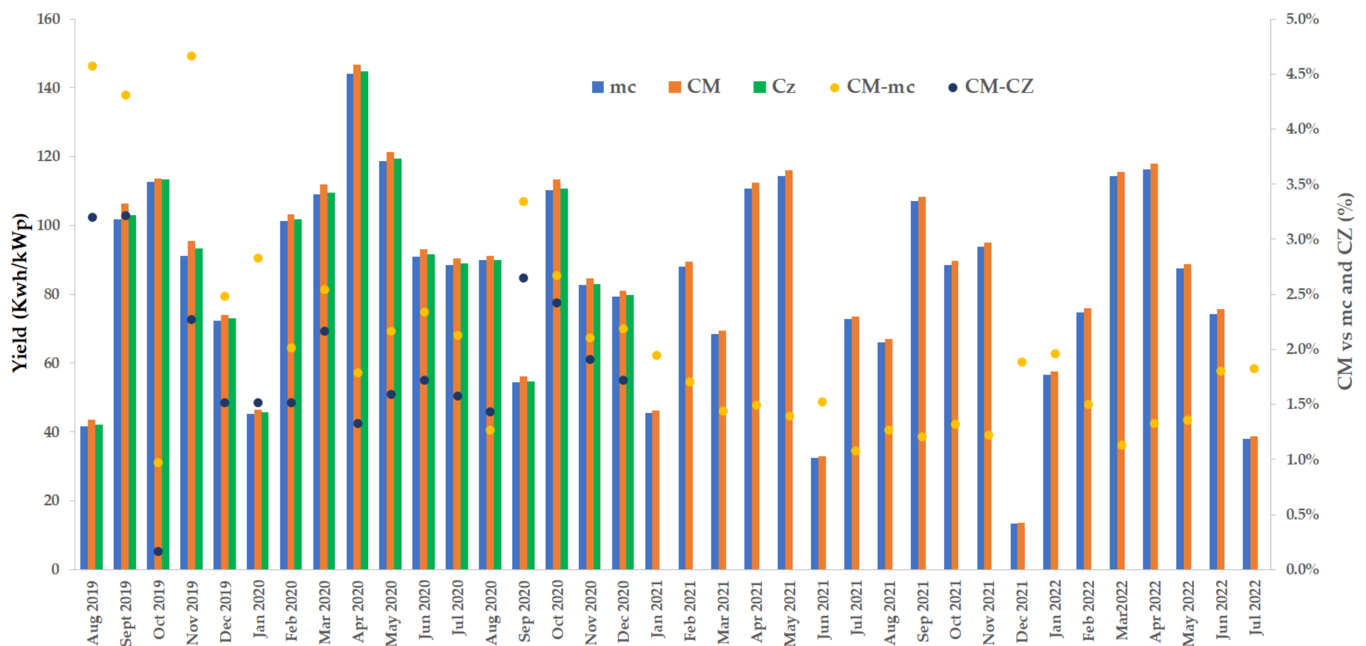


Figure 5-16: Bars to the left y-axis represent the monthly Energy Yield (kWh/kWp) and the dots to the right y-axis represent the yield delta between systems in %.

We can see that in every single month the performance of the CM system is better than the mc one with an average of 1.5% higher energy yield. Unexpectedly the energy yield obtained from CM is also 1% higher than the CZ one while it is well documented that it should be the other way around. This would require further study, nevertheless the systems perform all of them in a very similar way and this is consistent overtime which signals no abnormal degradation on the MC system.

The energy yield of the three arrays were modelled with commercial simulation software PVSyst , and the results were compared to the measured data.

A summary of PVSyst simulation inputs parameters is shown in table 5.5. The low light performance data were determined by taking the average values of actual laboratory test measurements of the modules used and the thermal factor that was provided by the manufacturer.

Table 5-5: PVSyst inputs parameters.

Low light (W/m^2)	**CS3U-335P(P3) (mc-Si)**	**CS3U-370P(P5) (CM-Si)**	**CS3U-390MS (Cz-Si)**
200	-4.20	-1.30	-3
400	-1.70	0.20	-0.8
700	-0.40	0.40	0
800	-0.40	0.20	0.20
Thermal Loss Factor Uc (W/m^2K)	30.1	31.7	31

Figure 5.17 shows the monthly energy yield of the three systems in kWh/kWp both measured and simulated. We notice that in every single month the performance of the CM-Si based system is better with an average of 1.54% higher energy yield than the mc-Si based one and of 1.00% of the Cz one. For the simulations this difference is slightly higher: 1.73% and 1.02% respectively.

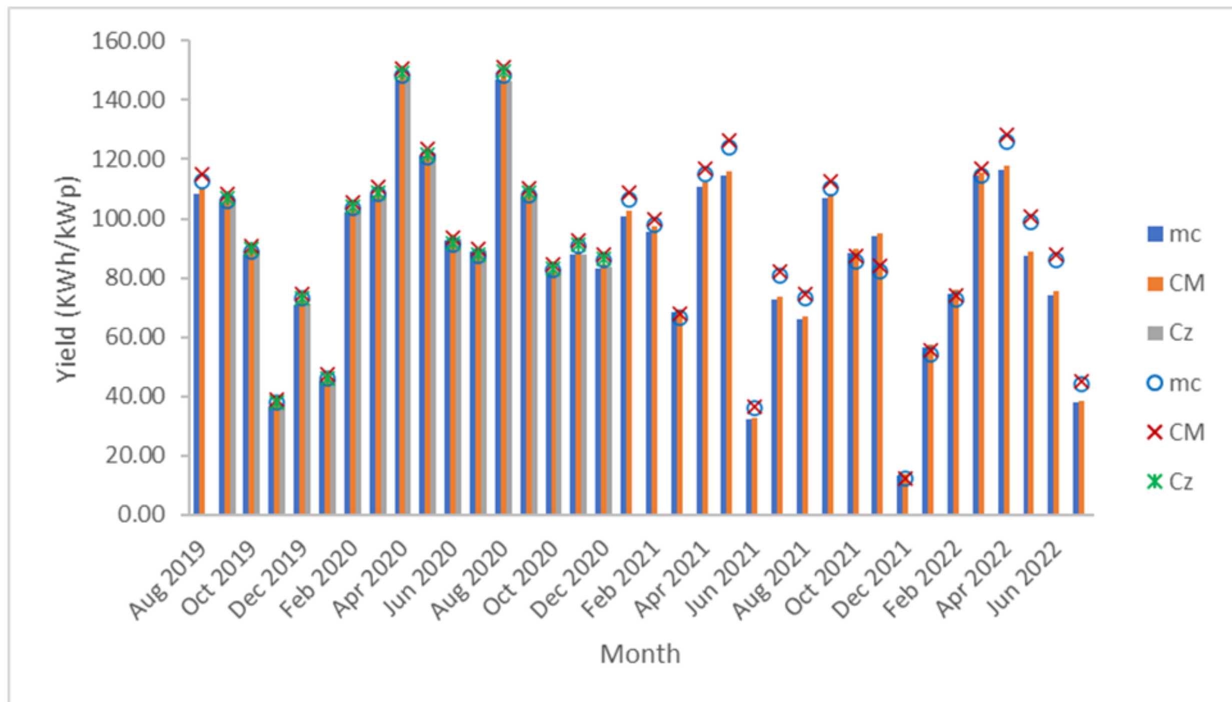


Figure 5-17: Measured (bars) and simulated (crosses) yield of the three arrays.

Figure 5.18 shows the correlation between measured and simulated data for the three systems and as it can be noticed the CM system does not show a significant different performance than mc and Cz modules. PVSyst simulations are pretty accurate for the three modules systems:, the difference between simulated results and measured results was verified by the index of MBE/AV (Mean Bias Error over Absolute Value) and it was between 1% and 3% for the three systems, while the RMSE (Root Mean Squared Error) was between 1% to 5% that are considered reasonable errors for a simulation as reported by Freeman et al. [60].

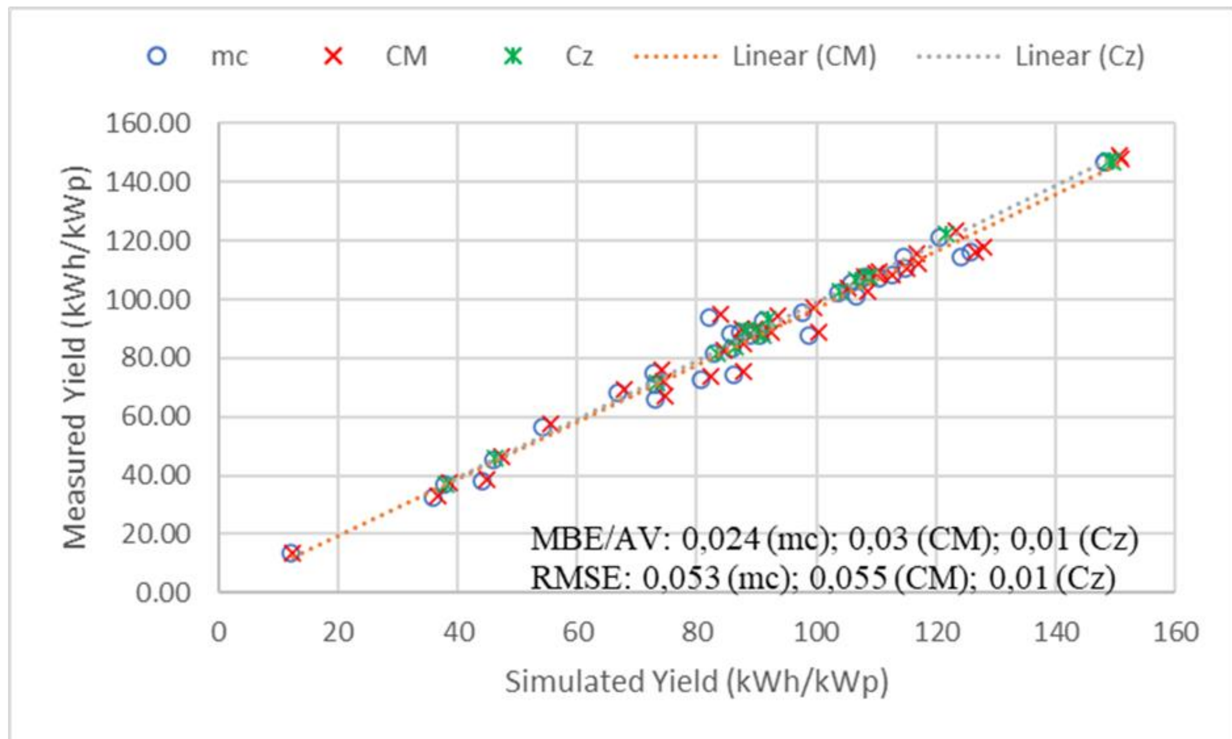


Figure 5-18: Measured and simulated results correlation.

There is extensive literature about the validity of simulation tools for yield performance analysis [22] and of PVSyst in particular as a valid software tool that is extensively used in science and commercial simulations. There are several parameters to pay attention to in order to obtain a simulation that represents the system properly as we managed to do in this work. Beyond the obvious accurate representation of the system on parameters such as shading, dust, etc. one of the most important variables to consider is the meteorological data base to be used. In our simulation we used a local weather station with which we could maximize the accuracy of the simulation.

5.2.2.3. Performance ratio and degradation

The Performance Ratio (PRSTC) is calculated as the relation between the actual energy produced according to the power at the maximum power point Pmp exhibited and the final energy generated as a result of the received irradiation, considering its nominal (rated) peak power. We corrected it by the average temperature of the system as indicated below where γ is the module temperature power coefficient and T is the average temperature of the module in the period considered.

$$PR = PR_{STC} * \left(\frac{1}{1 - \frac{\gamma}{100} * (T - 25)} \right)$$

Figure 5.19 shows that CM array has systematically a higher PR than the other two ones, which seems strange for the CZ system that should behave better as commented before. Again, the behavior of the PR of the CM system is consistent over time not showing signals of significant degradation. Considering that the first years are the most relevant ones when it comes to degradation [68] the data analyzed for 156 weeks should cover the most critical period. The results do not show any evidence that could result in a concern about the reliability of the silicon when the CM route is the one used, quite the opposite.

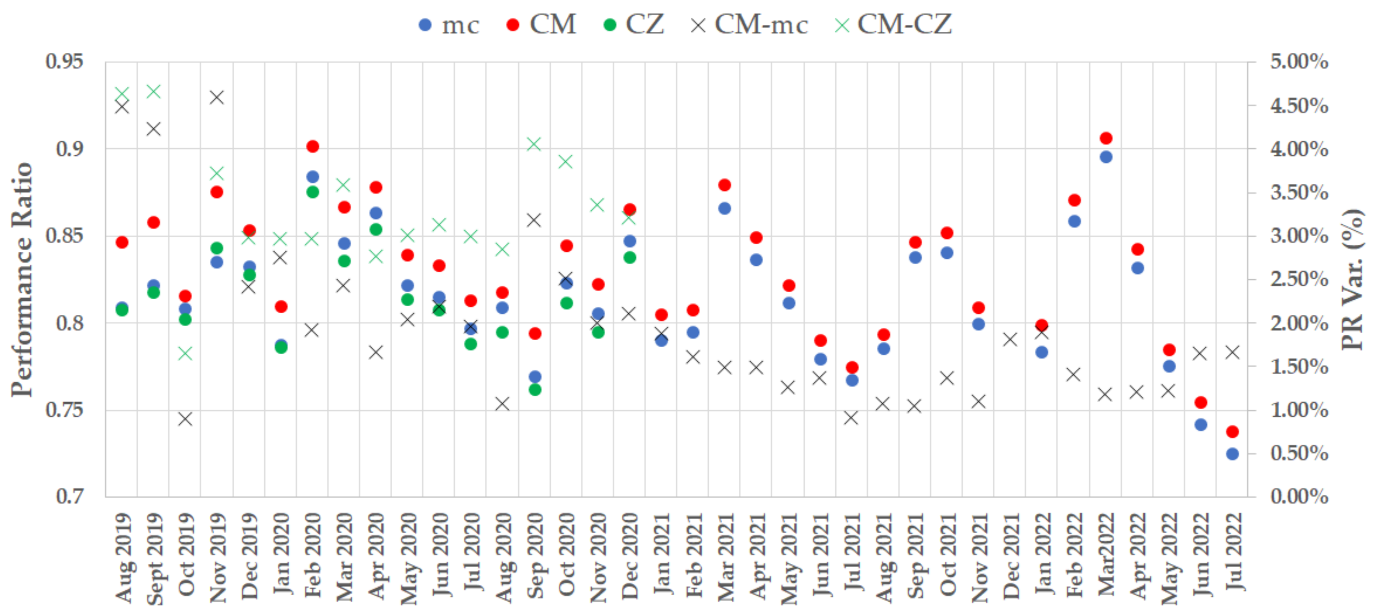


Figure 5-19: Dots to the left Y axis represent Performance Ratio over time and cross to the right y axis represent the PR delta between systems in %.

5.2.3. Discussion

5.2.3.1. Comparison of CM-Si vs mc-Si

According to the results above, CM-Si based modules provide systems that with a very similar cost generate more energy than mc-Si based ones, in particular on this experiment 2% higher average yield was measured over a period of 3 years. Both systems started and stopped delivering energy at the same time of the day but the CM-Si had a better behavior as shown by the higher yield and higher PR.

Figure 5.20 plots the yield difference between both systems under different radiation conditions. We can see that the yield difference is on the higher side at lower radiation meaning that the CM-Si based system could behave better than the mc-Si based one at low light, although is not very conclusive based on the results obtained.

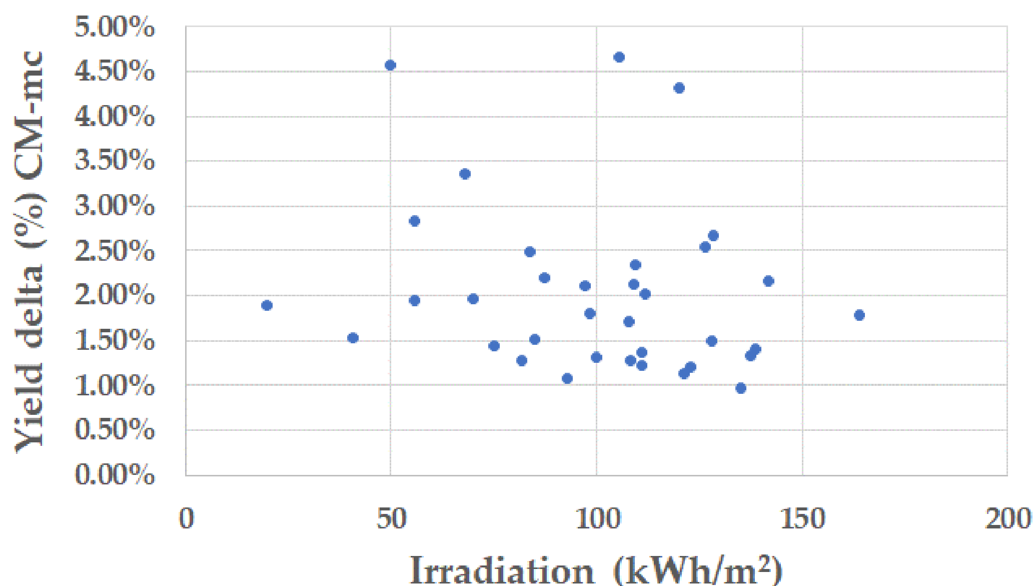


Figure 5-20: Monthly Yield Difference of the CM and mc systems.

While the system behaves better also with the Temperature as shown by the measured coefficient temperature in Table 5.2 we believe low light has a higher effect since the main difference between the CM-Si and the mc-Si based modules is the defect (dislocation and grain boundary) density. The mc-Si module with a larger defect density is slower to react to the light energy of the low energy state, and even though we cannot see this with an earlier kick, we can see it with a

weaker performance under low light conditions of the mc-Si based system. Recent research has demonstrated that temperature coefficients are illumination-dependent [69] with variations moving from 30% to double, depending on the cell technology and conditions, which could also explain the further improvement under low irradiance.

Table 5.6 shows the main parameters measured at the crystal level of samples of both modules and Figure 5.21 shows electroluminescence (EL) and metalloscopy samples pictures of both types of modules where the higher defect density can be noticed on the mc-Si based one.

Table 5-6: Crystal main parameters.

Parameter	CM-Si	mc-Si
Oxygen content (ppma)	5-8	5-8
Dislocation density (pcs /cm2)	500-1000	104-106
Grain boundary density (pcs/cm2)	~0	1-20
Resistivity (Ω.cm)	1-1.2	1-1.2

Even though light-induced degradation analysis was not performed in this work, there is no sign of significant performance difference over time between the two systems as shown in figure 5.19.

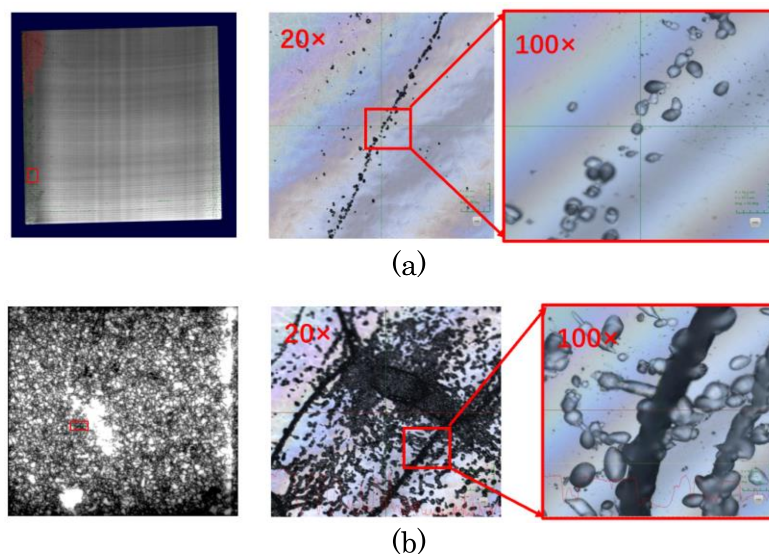


Figure 5-21: Electroluminescence (EL) and metalloscopy samples pictures of CM (a) and mc (b) modules.

5.2.3.2. Comparison of CM-Si vs Cz-Si

When in Figure 5.22 we plot again the yield difference between both systems under different radiation conditions, we can see now that the yield difference is almost constant with no difference in performance for low or high light, which makes us think that the main difference in the yield is due to the better performance under temperature of the CM system.

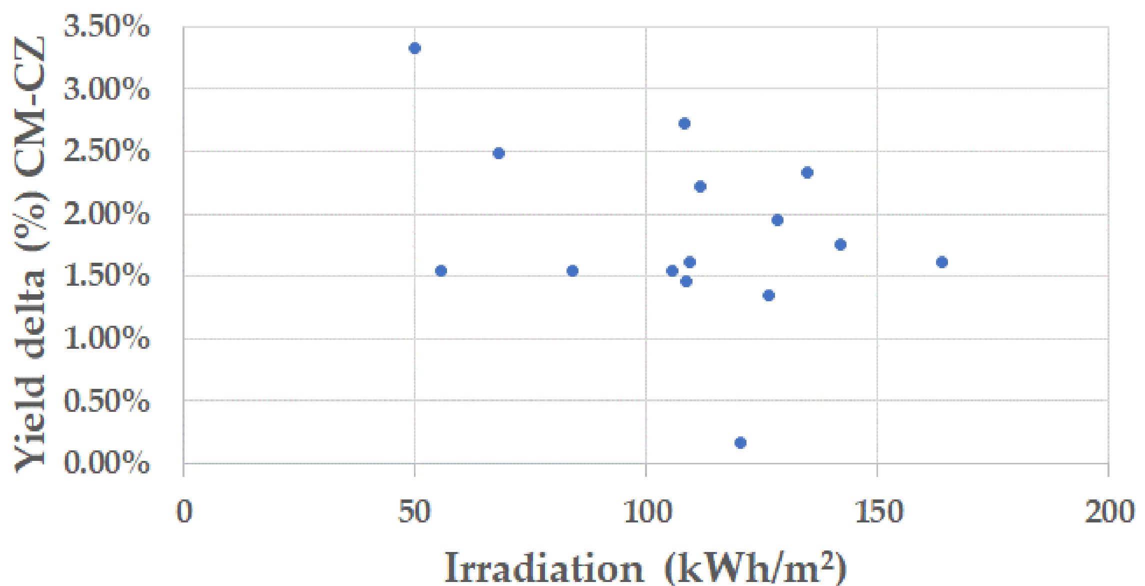


Figure 5-22: Monthly Yield Difference of the CM and CZ systems.

5.2.4. Conclusions

- High device efficiency at optimized production costs by the cast-mono technique seems possible, using common multi crystalline cast furnaces.
- An undesirable propagation of defects from bottom to top has been detected with efficiencies variation between top and bottom wafers on the 0,5% absolute range.
- Due to the passive heat extraction from the bottom of the crucible, a higher lateral curvature occurs when implementing the seed-cast growth approach in a typical DSS casting furnace in comparison with a common mc-Si process.

- 15% of the ingot produced mono crystalline wafers and 22% wafers not fully mono crystalline but showing the same performance. 29% of the ingot produced mc-Si wafers with a significant part of the surface being mono crystalline resulting in higher efficiency. These percentages rapidly drop when the seed is recycled.
- Recycling the seeds resulted in more than 0,7% loss in absolute efficiency as the density of extended bulk defects dramatically increases. The main reasons are crucible contamination, curved melting front of the seed with more mc-Si at the crucible walls, lower lifetime region at the top of the seed that is melted, and low lifetime at the seed junctions.
- In order to recycle the seed without a dramatic drop in performance, a preferential heat flux along the seed versus the crucible sides should be achieved to minimize the formation of mc-Si in seed sides close to the crucible
- Recent studies reported good results of cast-mono wafers for the last cell technologies, including the n-type HJT [70] by applying a well-established phosphorus gettering process the goal of minimizing metal impurities in the wafers is achieved, obtaining absolute increases in efficiency of up to 1,1% thereby aligning with the preparation of low-cost HJT cells for this type of wafers.
- When we manufacture CM-Si modules and deploy them in the field the results obtained demonstrate that CM-Si a very valid technology that does not show signs of relevant degradation after several years of operation and whose performance can be better than mc-Si modules and similar to CZ-Si modules.
- Both the energy yield and the PR over time have been quantified and compared among the three technologies, not finding significant differences on their performance.
- The energy yield over time has been simulated and compared among the three technologies, showing that the cast-mono modules simulations correlate as well as the other technologies.
- The outdoor behavior of these technologies in simulations and in the field is very similar among the three technologies.

- There is equipment that was manufacturing GWs a year of casting silicon wafers that is being scrapped and that instead could be manufacturing CM-Si since it is a very valid technology, as this study shows, that could be employed in utility scale PV plants. This equipment sitting aisle adds to the CO_2 footprint the electricity required to manufacture unnecessary new equipment.

6. Conclusions and future work

PV experienced remarkable growth thanks to all the technological evolutions that it managed to achieve and the size of the market that allowed the economies of scale required to achieve the cost reduction that made all this possible.

Crystalline silicon is the clear winner as the technology of the substrate, the wafer, on which the cells and modules are built on. In the way to get where we are today with the Cz-Si as the dominant player, many technologies were explored, some of them discarded and some of them just not giving the importance they deserve.

Attending to the material composition, the chemistry of the material, one of those technologies was the UMG-Si. Attending to the crystal of the wafer, the physical part of the material, one of those technologies was CM-Si.

We focus this thesis on trying to understand better both UMG-Si and CM-Si and we obtained very interesting results that open new questions that deserved to be further explore.

6.1. UMG-Si

For what it relates to UMG-Si we found out that the material is not very homogeneous, and it varies heavily from one supplier to another. In any case, independently of the supplier, in one grade or another, we found that the introduction of UMG-Si as raw material in the process always decreased the yield and lifetime. We also concluded that the more UMG-Si introduced the lower the yield and the lifetime.

The usable brick length is also reduced due to the high values of P in this material. This can be compensated with B but at the expense of reducing the base resistivity and it will always mean less usable length than without UMG-Si. When this compensation is very heavy, we could notice an increase in lifetime caused by a reduction in the SRH recombination maybe due to lower mobility of carriers.

When we add UMG-Si to the feedstock inclusions appear after the growth process and the usable length is reduced even more, this effect can be even bigger than the

resistivity when defining the usable length and it depends heavily on the supplier employed.

We have seen in the literature Cz-Si ingots grown with UMG-Si and very recently we have seen CM-Si growth using this material. Only 0,5% absolute efficiency drop was reported using the TOPCon cell technology [71] versus Cz-Si reaching efficiencies of 22,65%.

These results are very promising although right now we do not believe that using 100% UMG-Si is going to be viable due to the losses of usable length and the heavy impact of efficiency in the overall cost of a PV plant.

On the other hand, we are certain that using UMG-Si as a percentage of the feedstock will reduce the materials cost without a heavy quality impact. To prove that we made modules of 100% UMG-Si material and compared its outdoor performance with modules without any UMG-Si on their feedstock and after a full year of study the result were very similar in both modules. Therefore, we should not expect lower performance in modules made with smaller percentage of UMG-Si, the focus should be on finding the optimum point on the manufacturing yield.

We did experiments with up to 25% of UMG-Si and of 100% and the usable length was still acceptable for 25% and for certain suppliers. More work should be conducted trying to find the optimal percentage of UMG-Si that could be acceptable from the manufacturing yield perspective, doing the analysis from 25% to 100% and different suppliers.

Consistency from the different manufacturers it is also important if we are to make a robust manufacturing process, more work needs to be done trying to identify how the different elements of each manufacturer come into play and how to make a more standard material.

The mechanical consistency of wafers containing UMG-Si should be analyzed in the same way as we do in this work for CM-Si.

Finally, I would like to suggest the manufacturing of CM-Si modules based on 100% UMG-Si and study its outdoor performance. Also, we should try to monitor the performance of the current work for longer than a year and monitor if the degradation is similar to no UMG-Si modules.

6.2. CM-Si

We analyzed the process of manufacturing CM-Si in detail, the mechanical strength of the wafers produced, and the modules performance of modules based on CM-Si wafers in outdoor conditions for 3 years.

Starting with the manufacturing process, one of the critical parts beyond the growth that we also studied in detail, is the slicing process of the wafers, and particularly the wire breakages. Wire breakages have a devastating effect when they happen and are the main factor to have a good manufacturing yield together with the growth yield and the usable length of the bricks. In order to understand the reason behind the wire breaks better we analyzed the wire itself before and after a cut for wires that broke and wires that did not break and we observed the presence of longitudinal marks on every broken wire, whereas these marks are absent in unbroken wires. The presence of SiC inclusions in silicon, and the transfer from a three-body to a two-body regime may be an explanation. This factor seems to be more important than the wire wear, which has a much smaller influence in breakage

Future work intends to relate the longitudinal marks with SiC inclusions on the silicon blocks. Analyze the effect of different materials to be cut seems interesting too, thus, the same analysis made here could be done with CM-Si and UMG-Si and compare the results. We should suspect that UMG-Si bricks might suffer higher breakage rates due to higher contents of SiC. The work we made here always considers the same wire diameter, for future work it would be interesting to find out if with different wire diameters we observe similar results.

As the interaction of SiC with the wire seems to be the key factor in the process a future work could focus on the change of the SiC shape after different rounds of slurry recycling, trying to understand how the SiC is affected by the recycling process and when the number of breakages starts to be uneconomical vs the number of recycling cycles.

Nowadays commercial operations are made with diamond wires, a similar analysis to the one performed here would be interesting for this new wire technology.

For the first time, the mechanical strength of conventional wafers (properly etched to remove the surface saw damage) Cz-Si and mc-Si have been compared with CM-Si substrates with high and low defect density. The systematic FLBT analysis

indicates that the intrinsic crystal properties of the silicon wafers, defect structure included, has a direct influence on the probability of mechanical failure during the PV manufacturing value chain (wafer handling, solar cell metallization, strings lamination, etc.).

Cz-Si and CM-Si with low defects showed similar characteristic fracture stress. The strength of the three technologies is quite similar but the analysis of the Weibull parameters shows that multi crystalline wafers present defects in their structure that makes possible the failure under low stress field, while this does not happen in Cz-Si and CM-Si with low defects. However, when the CM-Si has high density of dislocations, it is the worst performing wafer with the lowest value of characteristic fracture stress (15% lower), confirming the detrimental effect of these bulk defects not only in the electrical properties but also in the probability of mechanical failure during the PV manufacturing processes.

We analyzed also in very detail the growth process of CM-Si and although we obtained very promising results with mono wafers behaving on a very similar way to Cz-Si ones, even when modules are produced and they are deployed on the field, it is clear that the process is difficult to control and presents several challenges. In order to maximize the percentage of CM wafers created the thermal gradient needs to be very carefully and accurately controlled especially at the beginning of the growth. The seed employed and the configuration used also has a big influence on the quality of the crystal growth. Unlike in the Cz process, in the cast-mono the dislocations do not propagate out of the ingot but all along it and are carried out and multiplied very easily from the bottom to the top of the ingot.

To be more economic, recycling the seed is relevant, thus, we made a study to understand the quality of the crystals when we recycle the seed finding significant grow in the number of dislocations when the seed is recycled just one time. When a virgin Cz seed is the one used, the orientation of the crystal needs to be <100> and the quality of the surface very good, although the edges between seeds is a bigger source of dislocations when several seeds are employed. The configuration of the seeds at the bottom of the crucible is very important and any imperfection in the surface will result in dislocations propagation. In principle the growth should be slower than when growing mc-Si and a perfect control of the melting front specially just before the initiation of the crystal growth is recommended.

Interstitial iron concentration is another problem that shows up mainly coming from the crucible that precipitates at the top of the ingot due to the segregation coefficients effect, reducing lifetime dramatically. In order to minimize this effect, the content of iron in the coating should be minimized

At solar cell level, a defined optimization of the texture processes for the non-perfect mono crystalline quality of the cast-mono wafers would help to increase the cost/performance ratio, balancing the production costs over all the PV silicon chain.

There are several GWs of cast-mono modules in the field and to our knowledge, this is the first time that field performance of cast-mono modules throughout a long period of time has been reported. The results obtained from this study demonstrate that is a very valid technology that does not show signs of relevant degradation after several years of operation and whose performance is better than mc-Si modules and similar to CZ-Si modules. Both the energy yield and the PR over time have been quantified, simulated and compared among the three technologies, showing that the cast-mono modules simulations correlate as well as the other technologies. The behavior of these technologies in simulations and in the field is very similar among the three technologies.

The results show a performance of the CM system better than the mc one with an average of 1.5% higher energy yield. Unexpectedly the energy yield obtained from CM is also 1% higher than the CZ one while it is well documented that it should be the other way around. This would require further study, nevertheless the systems perform all of them in a very similar way and this is consistent overtime which signals no abnormal degradation on the MC system.

There are GWs of casting equipment not being utilized today because the mc-Si technology has been abandoned that could be used to produce CM-Si that we have proved provides very encouraging results both during the manufacturing process and on the field. There is a lot of capital that could be saved and a significant environmental impact prevented by using this equipment instead of producing new one.

We conclude that UMG-Si is a technology that is worthy to remain exploring not as a 100% feedstock but to be blended with polysilicon reducing materials cost and that CM-Si is a technology showing good results with the latest cell technologies and we proved performs well in the field and without significant degradation.

Nowadays the cost of manufacturing PV modules is so low that represents less than 15% of the cost of a solar plant, and if storage using Li-ion batteries is included below 8%. Therefore, the cost of the module is not that relevant anymore while its efficiency is since affect to the cost of the overall system. Any technology with a significant gap in efficiency will struggle significantly to succeed. Very promising results have been published with the gap between CM-Si and Cz-Si being reduced significantly and different techniques to minimize the dislocations propagation such as induced grain boundary [72] and micro twins introduction [73] that open the way to further reduce the efficiency gap. Also as the cell technology evolves towards HJT, it is possible that the quality required of the bottom substrate is reduced without affecting the overall efficiency significantly [74] being therefore a path that deserves to continue being explored if not for the cost reduction that seems to be less important as we reach such dramatic modules pricing, but from the environmental point of view since these substrate require significantly less energy on its manufacturing process and would result in a lower module carbon footprint.

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