

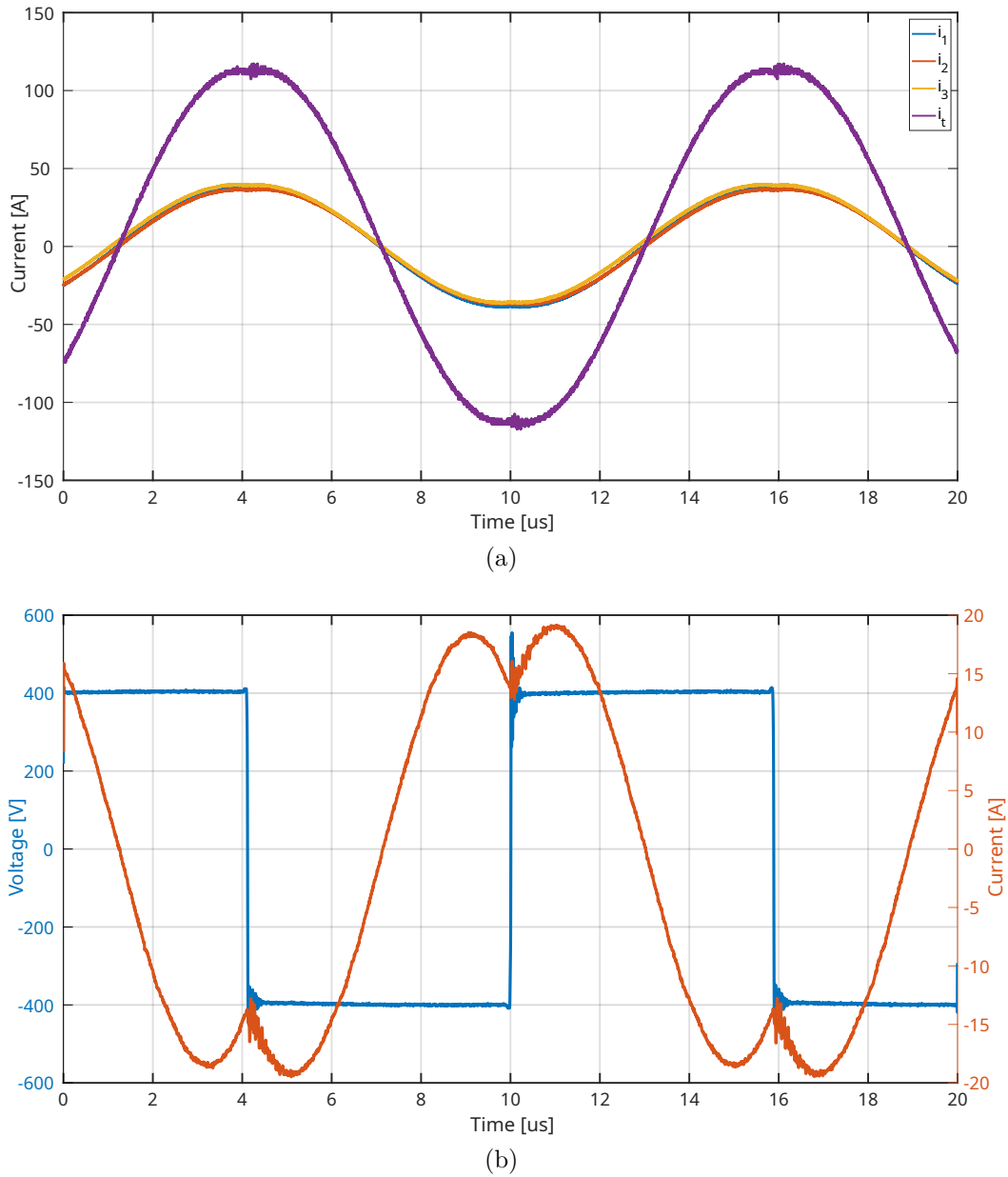


Figure 3.13: a) Measured currents in the three conductors of the tertiary winding and the total current b) Voltage and current of the primary inverter

3.4.1 CC/CP charging

A series of tests is conducted in order to test the claims given in this work. The system was tested in three significant positions, where the simulated value of the relative coupling coefficient ξ is equal to 0.6, 1 and 1.3. In Table 3.3 measured parameters of the system in all of the three considered cases are given. In each of the cases, system was first tested both using the CP and CC charging methods. Table 3.4 shows the summarized data of the CP and CC conducted tests. The power for CP charging is chosen in a way that it is

ξ	Constant Power Charging		
	Battery Current	System Efficiency Range	Charging Power
1.27	36.14 A - 49.12 A	95.75% - 96.54%	30 kW
0.99	36.14 A - 49.12 A	95.82% - 96.35%	30 kW
0.62	25.30 A - 34.43 A	93.63% - 94.82%	21 kW
	Constant Current Charging		
	Battery Current	System Efficiency Range	Charging Power
1.27	34 A	95.91% - 96.52%	20.7 kW - 28.2 kW
	45 A	95.86% - 96.72%	27.5 kW - 37.4 kW
0.99	34 A	95.72% - 95.93%	20.7 kW - 28.2 kW
	45 A	95.85% - 96.35%	27.5 kW - 37.4 kW
0.62	34 A	94.04% - 94.82%	20.7 kW - 28.2 kW

Table 3.4: Overview of the CP and CC conducted tests and results

possible to be reached for all of the battery voltages from the considered range. The current at the secondary coil will be highest when the battery voltage is lowest, and it is this case that determines the maximum power for CP charging. On the other hand, with the CC charging method, charging power increases with the increase in battery voltage. In both cases, the limiting factor is the rated current of the primary and secondary coils, as they are limited by the conditions given in the end of Section 3.3. The charging times using the CP and CC charging methods as the later one has higher average power delivered to the EV battery.

First, the test with the highest relative coupling coefficient is conducted. In CP charging mode it is tested for the power transfer of 30 kW. For the variation of the battery voltage in the entire range between 610 V - 830 V, the system efficiency was between 95.75% and 96.54% and the battery current was between 36.14 A and 49.12 A. Current and voltage waveforms of the primary and secondary inverters in this case are given in Figs. 3.14a - 3.14c, for battery voltage levels of 610 V, 710 V and 830 V, respectively. CC charging was done with two different values of the charging current, 34 A and 45 A. In the first case of CC charging, system efficiency was between 95.91% and 96.52% while the charging power was between 20.7 kW and 28.2 kW. Currents and voltages of the primary and secondary inverters, for this case, are given in Figs. 3.14d - 3.14f. In the second case, system efficiency was between 95.86% and 96.72% and the charging power was between 27.5 kW and 37.4 kW. Currents and voltages of the primary and secondary inverters, for this case, are given in Figs. 3.14g - 3.14i. As it can be seen from the given data, CC charging is more appropriate for this charger type as it allows for higher power transfer with higher battery voltage levels, thus confirming the statement given in the previous Section.

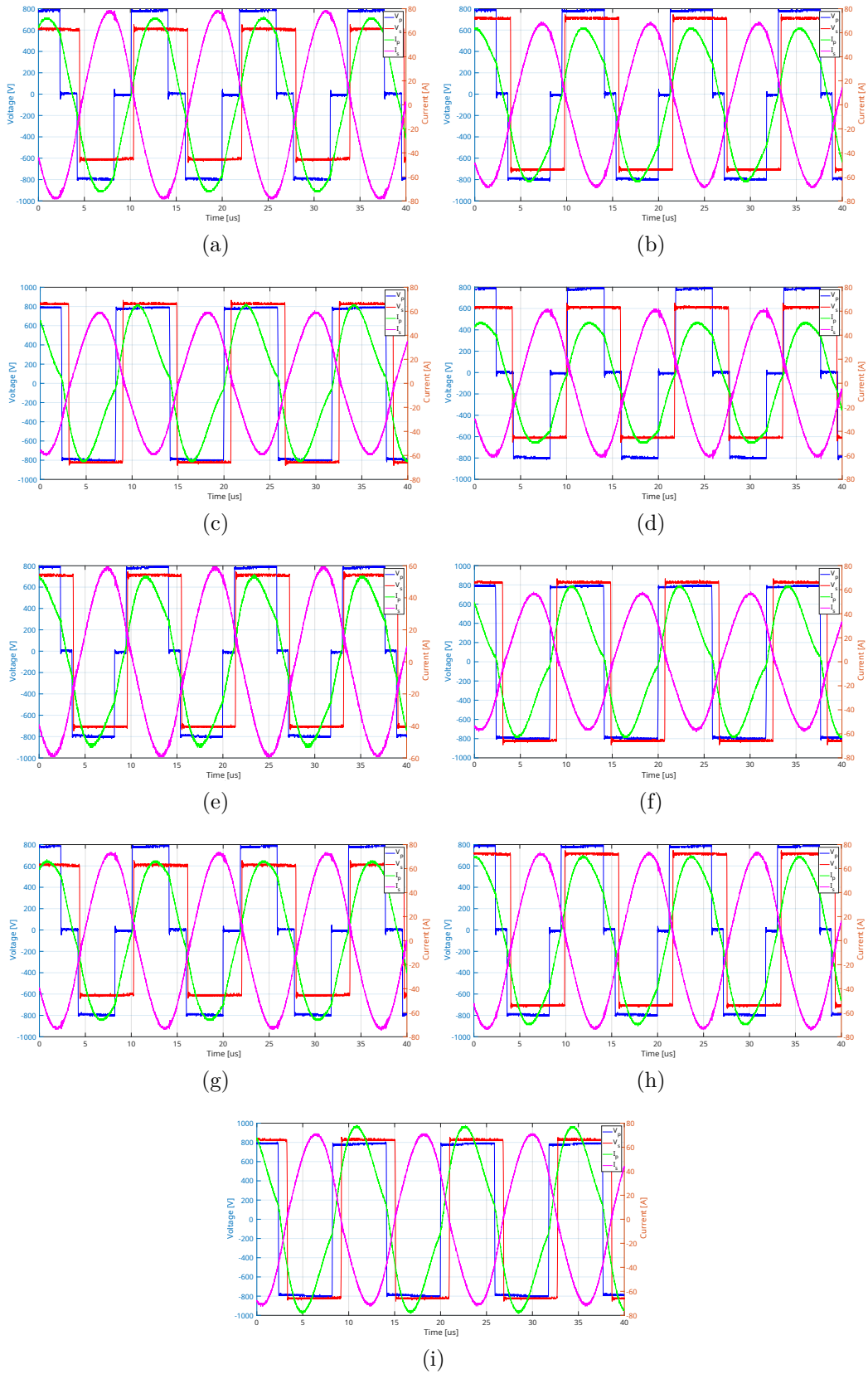


Figure 3.14: Currents and voltages of the primary and secondary inverters for $\xi = 1.27$,
a) $V_{batt} = 610$ V, $P = 30$ kW b) $V_{batt} = 710$ V, $P = 30$ kW c) $V_{batt} = 830$ V, $P = 30$ kW d)
 $V_{batt} = 610$ V, $I = 34$ A e) $V_{batt} = 710$ V, $I = 34$ A f) $V_{batt} = 830$ V, $I = 34$ A g) $V_{batt} = 610$ V,
 $I = 45$ A h) $V_{batt} = 710$ V, $I = 45$ A i) $V_{batt} = 830$ V, $I = 45$ A

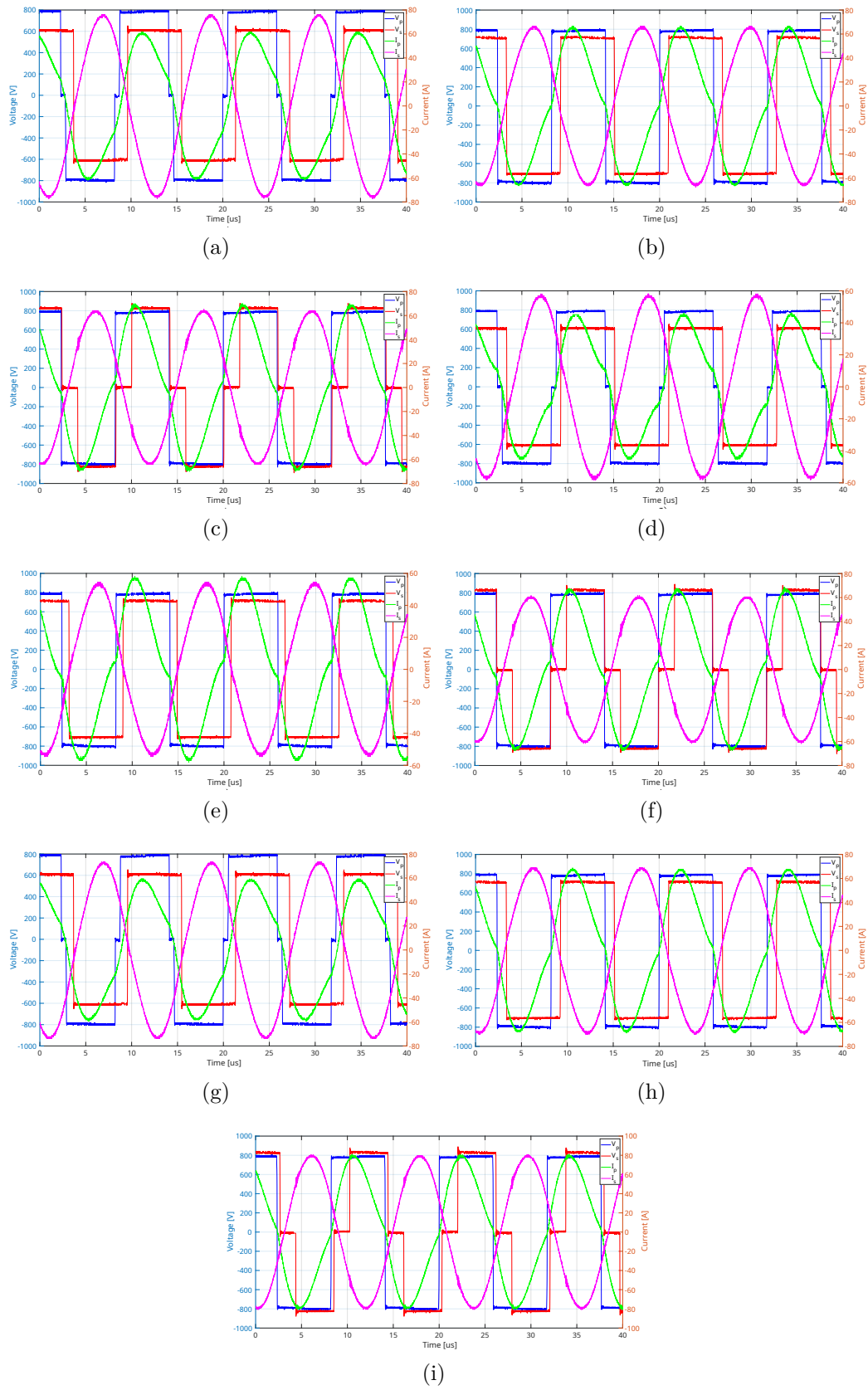


Figure 3.15: Currents and voltages of the primary and secondary inverters for $\xi = 0.99$,
 a) $V_{batt} = 610\text{ V}$, $P = 30\text{ kW}$ b) $V_{batt} = 710\text{ V}$, $P = 30\text{ kW}$ c) $V_{batt} = 830\text{ V}$, $P = 30\text{ kW}$ d)
 $V_{batt} = 610\text{ V}$, $I = 34\text{ A}$ e) $V_{batt} = 710\text{ V}$, $I = 34\text{ A}$ f) $V_{batt} = 830\text{ V}$, $I = 34\text{ A}$ g) $V_{batt} = 610\text{ V}$,
 $I = 45\text{ A}$ h) $V_{batt} = 710\text{ V}$, $I = 45\text{ A}$ i) $V_{batt} = 830\text{ V}$, $I = 45\text{ A}$

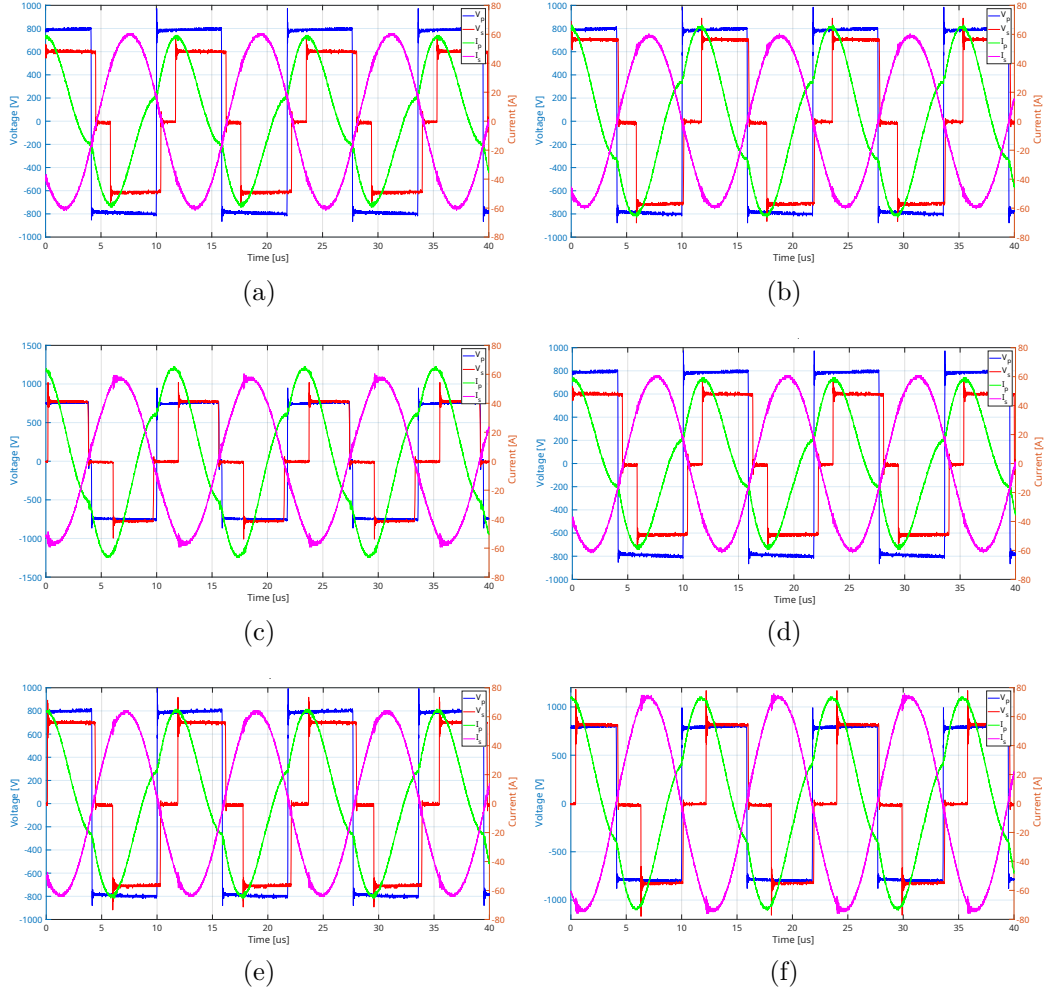


Figure 3.16: Currents and voltages of the primary and secondary inverters for $\xi = 0.62$,
a) $V_{batt} = 610$ V, $P = 21$ kW b) $V_{batt} = 710$ V, $P = 21$ kW c) $V_{batt} = 830$ V, $P = 21$ kW d)
 $V_{batt} = 610$ V, $I = 34$ A e) $V_{batt} = 710$ V, $I = 34$ A f) $V_{batt} = 830$ V, $I = 34$ A

In the second position in which the system was tested, for $\xi = 0.99$, same tests as with $\xi = 1.27$ are conducted. In CP charging mode the system is tested for 30 kW power level. Measured efficiency of the system was between 95.82% and 96.35%, while the charging current varied between 36.14 A and 49.12 A. Figs 3.15a - 3.15c depict the voltage and current waveforms for the battery voltage levels of 610 V, 710 V and 830 V. Figs 3.15d - 3.15f show the voltages and currents in the case of the CC charging mode, with the battery current equal to 34 A, for the same three battery voltage levels as in previous cases. Measured efficiency of the system in this case was between 95.72% and 95.93%, while the charging power was between 20.7 kW and 28.2 kW. Case where the battery is charged with the constant current of 45 A is shown in Figs. 3.15g - 3.15i. Achieved system efficiency was between 95.85% and 96.35% while the charging power was between 27.5 kW and 37.4 kW.

In the case where the relative coupling coefficient ξ is equal to 0.62, i.e.,

when both the clearance and misalignment are maximal, it is not possible to transfer the nominal power in the entire considered voltage range of the battery. For that reason, the system is tested in the CP charging mode with the power level of 21 kW that is achievable for all of the battery voltage between 610 V and 830 V. Figs. 3.16a - 3.16c show the currents and voltages of the primary and secondary inverters during these tests, in the three characteristic points of the battery voltage interval. System efficiency was in range between 93.63% and 94.82%, while the battery current was in between 25.30 A and 34.43 A. Figs. 3.16d - 3.16f depict the relevant waveforms under CC charging test, where the battery voltage was equal to 610 V, 710 V and 830 V, respectively, and the battery current was equal to 34 A. The efficiency of the system in these tests was in range between 94.04% - 94.82%, while the charging power varied between 20.7 kW and 28.2 kW. Fig. 3.17 gives the measured system efficiency curves for different battery voltage levels and in different cases of CC and CP charging that were tested.

Fig 3.18. shows the losses breakdown in the nominal case that is shown in Fig. 3.15b. Input voltage is 800 V, battery voltage is equal to 710 V, the relative coupling coefficient ξ is equal to 1, while the power being transferred to the EV battery is equal 30 kW. As it can be seen, dominant are the conduction losses in the tertiary winding. Due to its position and size, the tertiary winding makes a convenient place to concentrate the system losses as it is purely passive element with relatively big dissipation area. Yet, if these losses were mitigated to the inverter bridges, it would require them to have better cooling and would cause lower system efficiency as the resistance of one of the semiconductors is higher than the entire resistance of the tertiary circuit, thus justifying for the proposed solution of having high tertiary current and concentrating the losses there. Also, the key to maintaining the high system

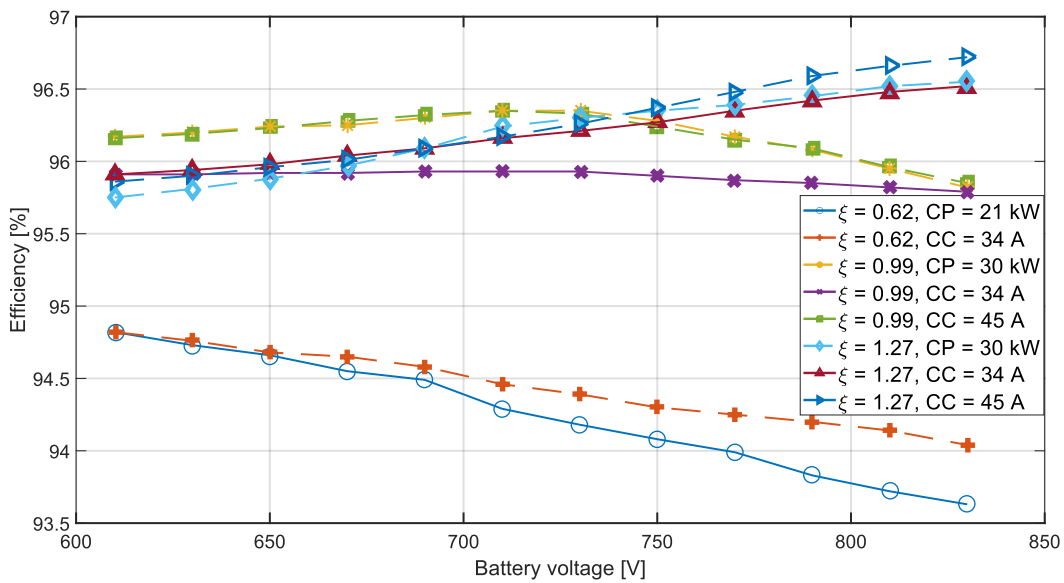


Figure 3.17: System efficiency in CC and CP charging tests

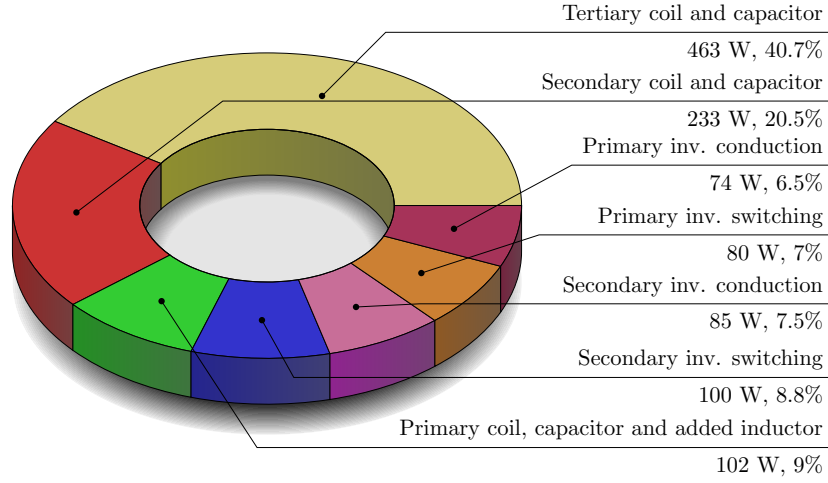


Figure 3.18: Losses breakdown in the nominal condition

efficiency during the following CV charging is to reduce the tertiary current by reducing the primary and secondary duty cycles as it will be shown. Cooling of the tertiary winding in the prototype was air-forced. In the case of having primary and tertiary coils encapsulated, it would be necessary to devise a ventilation system to guide the air inside the structure and to allow for the required cooling conditions.

3.4.2 CV charging

After CC and CP charging test, efficiency of the system was examined under CV charging conditions, being that it is present both in CC/CV and CP/CV charging methods, in the second half of the battery charging process. Table 3.5 summarizes the CV charging results. System was tested with the same relative coupling coefficients as in the previous tests. Battery voltage was kept constant at 830 V while the battery current was changing between the maximum for each of the given cases, and the 10% value of the maximum current of 45 A, below which when the current drops, we consider that the battery is fully charged.

Figs. 3.19a and 3.19b show relevant waveforms of the system for the case with the relative coupling coefficient equal to 1.27 during the CV charging

Constant Voltage Charging				
ξ	Battery Voltage	Battery Current	System Efficiency Range	Charging Power
1.27	830 V	4.5 A - 45 A	92.22% - 96.72%	3.7 kW - 37.5 kW
0.99	830 V	4.5 A - 45 A	91.95% - 95.85%	3.7 kW - 37.5 kW
0.62	830 V	4.5 A - 34 A	91.29% - 94.04%	3.7 kW - 28.2 kW

Table 3.5: Overview of the CV charging results

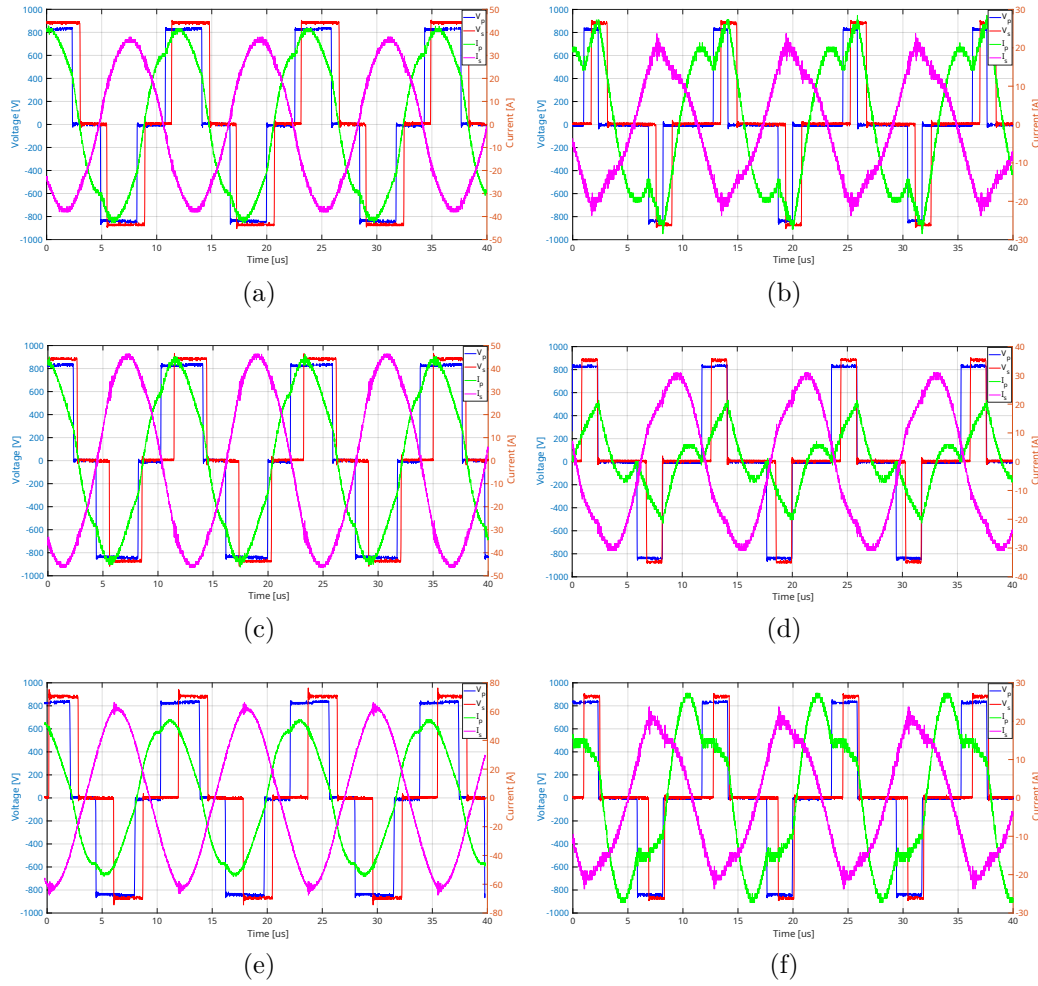


Figure 3.19: Currents and voltages of the primary and of secondary inverters in CV charging mode for battery voltage equal to 830 V a) $\xi = 1.27$ $I = 20$ A b) $\xi = 1.27$ $I = 4.5$ A c) $\xi = 0.99$ $I = 20$ A d) $\xi = 0.99$ $I = 4.5$ A e) $\xi = 0.62$ $I = 20$ A f) $\xi = 0.62$ $I = 4.5$ A

part of the process, in two instants when the battery current is equal to 20 A and 4.5 A, respectively. Case with the battery current equal to 45 A is already given in Fig. 3.14i. System efficiency decreased together with the decrease in battery voltage, ranging from 96.72% to 92.22%, while the charging power changed from 37.5 kW to 3.7 kW.

In Figs. 3.19c and 3.19d, analogously to the previous case, currents and voltages are given for the case of $\xi = 0.99$. Efficiency of the system decreased from 95.85% to 91.95%, while the change in the charging power is the same as in the previous case. Figs. 3.19e and 3.19f show the waveforms for the case with minimal relative coupling coefficient. Case with the maximal charging current of 34 A in this case is given in Fig. 3.16f. As the charging current decreased from 34 A to 4.5 A in this case, the system efficiency decreased from 94.04% to 91.29%, while the charging power decreased from 28.2 kW to 3.7 kW. Fig. 3.20 shows the variation of system efficiency with the change

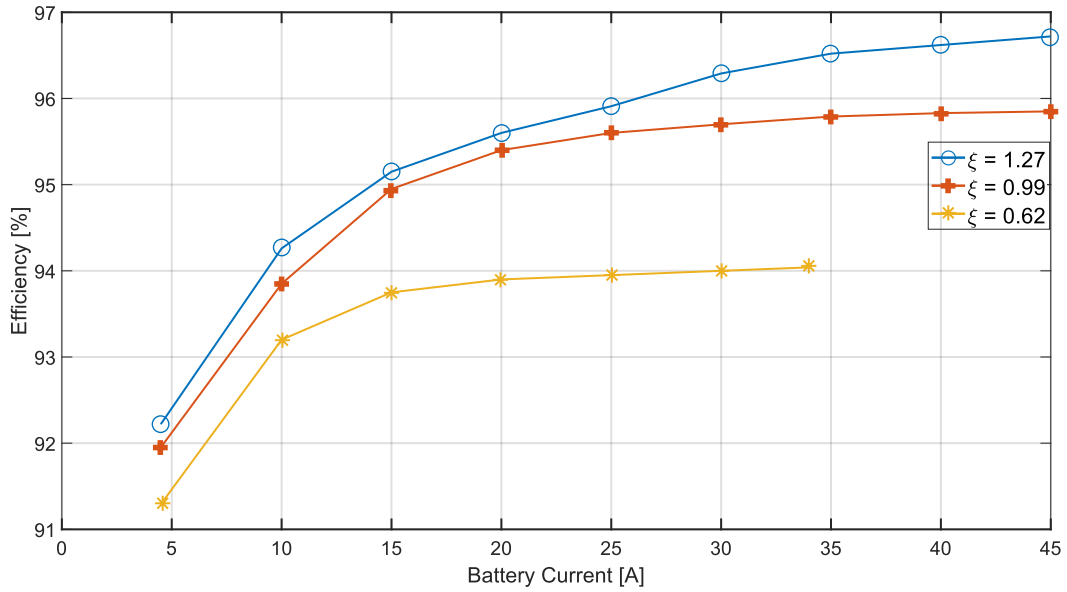


Figure 3.20: System efficiency in CV charging tests

in battery current during the CV charging period, for the three previously discussed cases. All of the efficiencies measured in this work were obtained by utilizing the internal measurements of the Regatron programmable DC sources that were used for energizing the system.

Although the primary and secondary currents get distorted in the CV charging process due to higher presence of harmonics in the primary and secondary voltages, tertiary current will remain sinusoidal as its first harmonic is dominant due to the impedance characteristic of the circuit given in Fig. 3.8a.

3.4.3 Thermal considerations

Overall system losses in the nominal condition are given in Fig. 3.18. As it can be seen, the losses in the tertiary winding are dominant. While testing the presented prototype, air-forced cooling with 700 LFM was used for refrigerating the coils of the ground assembly, mainly the tertiary coil. The temperature of the hottest point of the tertiary winding reaches 94 °C in steady-state. Although high, this is still far away from the 180 °C limit of the isolation of the used Litz wire. This is, thermally, the most critical part of the system. As for the inverters, same air-forced cooling as for the ground assembly was used. The transistors were placed on top of the heatsink as shown in Fig. 3.12d. The thermal resistance between the case of the transistor and the ambient is, approximately, 0.15 °C/W. In the steady-state, while operating in the nominal point, under the given cooling conditions, the measured temperature of the case reaches 52 °C which is, having in mind the thermal resistance between junction and case from the datasheet of the used transistors, far under the limit for SiC technology.

3.4.4 Comparison to other works and V2G test

Table 3.6 gives the comparison between this work and the other relevant ones that were mentioned in the analysis of the state-of-the-art in the Introduction. As it can be seen, in terms of power level it is significantly higher than other cited articles. As for the system efficiency, it is in the top of the class, as are [50] and [37]. Out of all of the cited works, it is the only one that provides bidirectionality feature of the system. Misalignment is considered, as it is the crucial thing for EV charging applications.

To conclude the testing of the system, V2G mode of operation is checked. This mode of operation was checked for $\xi = 0.99$ and for battery voltage equal to 830 V while the power of 30 kW was being transferred to the primary side. Waveforms obtained during this test are given in Fig. 3.21. Measured efficiency of the system was 95.76%.

From the presented, it is clear that the proposed tuning method and design of the S-S-S compensated three-coil IPT charger satisfies the most important requirements of the current SAE standard proposal in terms of the coil sizes and system efficiency, potentially presenting a solution for high-power, high efficiency bidirectional EV charger. The swing in the relative coupling coefficient in this work, that comes as the consequence of considered clearance and misalignment area, is lower then the one predicted by the SAE standard. In this work we have presented the algorithm how to design the IPT system based on the proposed principles that has, as one of its input parameters, the clearance and misalignment area for which the system is designed. From the analysis presented in this article, it is possible to deduce that with the increase of swing in the relative coupling coefficient, the swing in the system efficiency will increase as well, due to loss of soft-switching conditions. However, the presented system has more than enough margin, in terms of system efficiency and power transfer capability that are defined in the SAE standard, to present a potential candidate for a real-life applications.

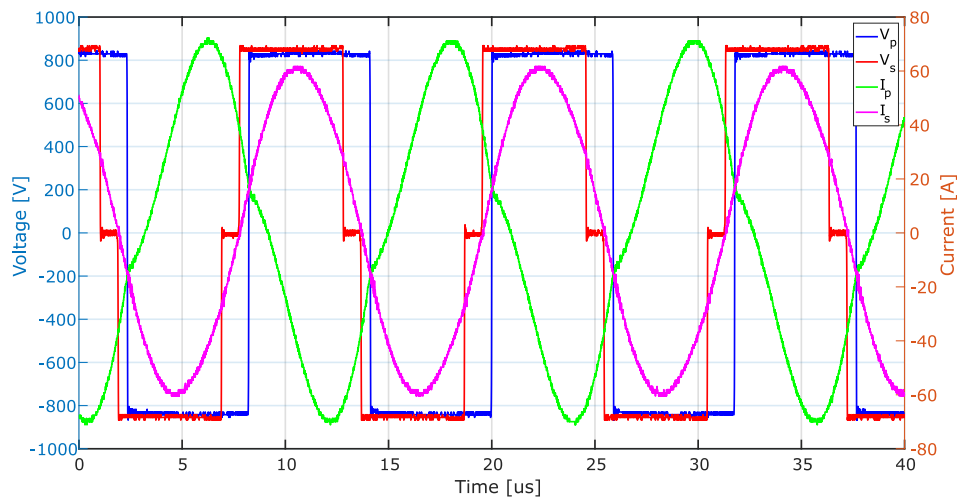


Figure 3.21: System operating in V2G mode of operation

Work	Number of coils	Compensation strategy	Application	Bidirectional	Coupling coefficient	Power level	Efficiency
This work	3	Modified S-S-S	EV Charging	Yes	$k_{ps} \in [0.126, 0.258]$ $k_{st} \in [0.140, 0.286]$	3.7 kW - 37.4 kW	91.29% - 96.72%
[42]	3	S-S-LCLCC	Battery Charging	No	$k_{ps} = 0.02$ $k_{st} \in [0.051, 0.092]$	30 W - 840 W	60% - 91.2%
[43]	3	S-S-S	EV Charging	No	$k_{ps} \approx 0$ $k_{st} \in [0.071, 0.082]$	60 W - 325 W	62.5% - 83.5%
[45]	3	Modified S-S-S	General IPT	No	$k_{ps} = 0.191$ k_{st} Unk.	1.1 kW - 6.6 kW	94.27% - 95.57%
[46]	3	S-S-S and Hybrid Topology	Battery Charging	No	$k_{ps} = 0.023$ $k_{st} = 0.092$	40 W - 384 W	50% - 90.8%
[49]	3	Hybrid Topology	Battery Charging	No	$k_{ps} \in [0.157, 0.29]$ $k_{st} \in [0.095, 0.24]$	120 W - 450 W	80% - 92.5%
[50]	3	S-S-P	Battery Charging	No	$k_{ps} = 0.204$ $k_{st} = 0.183$	41 W - 258 W	92% - 96%
[125]	3	LCC-LCC-S	EV Charging	No	$k_{ps} \in [0, 0.06]$ $k_{st} \in [0.024, 0.078]$	100 W - 3.5 kW	32% - 90%
[36]	2	LCC-LCC	EV Charging	No	$k_{ps} \in [0.075, 0.175]$	330 W	88.13% - 88.3%
[37]	2	LCC-LCC	EV Charging	No	$k_{ps} = 0.3$	0.8 kW - 6.6 kW	90.5% - 95.1%

Table 3.6: Comparison with other relevant IPT systems from state-of-the-art

3.5 Conclusions

Key points of this Chapter are:

1. A comprehensive equivalent circuit of the three-coil IPT system is derived.
2. Tuning method for the S-S-S compensated three-coil IPT system, suitable for the high-power and high-efficiency bidirectional EV charger, is proposed. By compensating the low magnetizing inductance, system efficiency is increased. The proposed tuning method leads to the functionality of the system, where the entire system is taken down to an equivalent inductor seen between two voltage sources, leading to seamless control of the system and allowing for implementation of both CC/CV and CP/CV charging methodologies, as well as easy transition between G2V and V2G modes of operation.
3. Design procedure of the IPT system based on the considered three-coil compensation strategy is outlined.

A 30 kW prototype was developed based on the proposed design procedure. Extensive tests with power level ranging between 3.7 kW to 37.4 kW are conducted in order to verify the proposed tuning method, achieving high efficiency, between 91.29% and 96.72%, over the entire range of considered clearances and misalignments, battery voltages and battery charging currents/power levels, proving the effectiveness and applicability of the proposed tuning method.

Single-Stage IPT Charger Based on a Three-Phase to Single-Phase Matrix Converter

Research is what I'm doing when I don't
know what I'm doing.

Wernher von Braun

IN the previous Chapter, compensation strategy of the IPT system based on the auxiliary coil and the three capacitor resonant circuit is proposed. In this Chapter, a single-stage IPT EV charger based on the Three-phase to Single-phase Matrix Converter (TSMC) is presented, employing the previously shown compensation strategy. **Contributions** of this Thesis that are presented in this Chapter are:

1. The novel modulation technique for the TSMC that ensures a steady flow of power to the EV's battery. This is achieved by preserving the phase and RMS value of the output voltage's first harmonic. This technique includes a flipping pattern that allows the converter to effectively handle both active and reactive power, while maintaining high power factor and low THD of the grid currents which is a characteristic that none of the existing modulation strategies have.
2. The power flow control method between the primary and secondary sides that is free of any wireless communication between the MCUs that control the converters, and that is employed in order to achieve stable energy transfer to/from the battery of the EV.

3. The start-up procedure enabling for soft start of the system, avoiding a potential failure due to the overcurrent conditions.

In Section 4.1, the operating principle of the proposed EV charger is explained. Section 4.2 contains a derivation and a description of the basic idea of the employed modulation strategy. Section 4.3 contains the final version of the modulation that is implemented. Section 4.4 disseminates the power flow control, outlines the problem of synchronization between the primary and secondary MCUs, and presents the applied solution. The experimental verification of the ideas presented in this work is given in Section 4.5.

4.1 Proposed circuit topology and functionality

The proposed topology is given in Fig 4.1. It employs a matrix converter topology as a cycloconverter. This means that high-frequency voltage used for excitation of the IPT link is generated directly from the grid, without any intermediate DC link. In this way power density is increased as massive DC link capacitors are eliminated and two power conversion stages are integrated into a single one. The trade-off for achieving the mentioned benefits is the relatively complex modulation and control of the considered converter. Also, due to the existence of four-quadrant switches that do not provide a free-wheeling path the current during the commutation process, it is necessary to employ an additional diode snubber circuit, as it is shown in the considered Figure. All of these remarks will be explained later in this Chapter. It can be seen from the given Figure, that the employed compensation of the IPT link is the S-S-S compensation strategy with the auxiliary winding. The operating principle, design methodology and parameter tuning of the IPT system that is compensated in this manner is presented in the previous Chapter. In the case of the TSMC topology considered in this Chapter, parameters of the resonant capacitors are determined using the equations (3.13)-(3.15), allowing for the entire IPT link to be represented as an equivalent inductor, as it was explained previously. Having in mind the resonant nature of the IPT link, it is valid to assume that only the first, i.e., the fundamental harmonic, contributes to the exchange in active power between the two sides. Equation (3.16) is the one determining the active power that is being taken to/from the EV battery.

The topology from the Fig 4.1 has to provide all the functionalities that the classical multistage topology from Fig. 2.7 does. This means it has two main tasks:

1. Ensure a constant power flow to/from the EV battery. In this way, advantages of the system being connected to the three-phase electrical grid are fully utilized, removing unnecessary, low-frequency, power pulsations on the EV side. When talking about the constant power flow,

we are considering it from the point of view of the electrical grid, not from the point of view of the high-frequency resonant link, where power will be pulsating nonetheless as the resonant link has only single phase. From the point of view of the high-frequency resonant link, we desire a constant average power over one high-frequency period. The completion of this task is a necessary, but not sufficient condition for the completion of the second task.

2. Ensure compliance with the grid code. From this aspect, it is important to have low THD of the grid currents and high power factor.

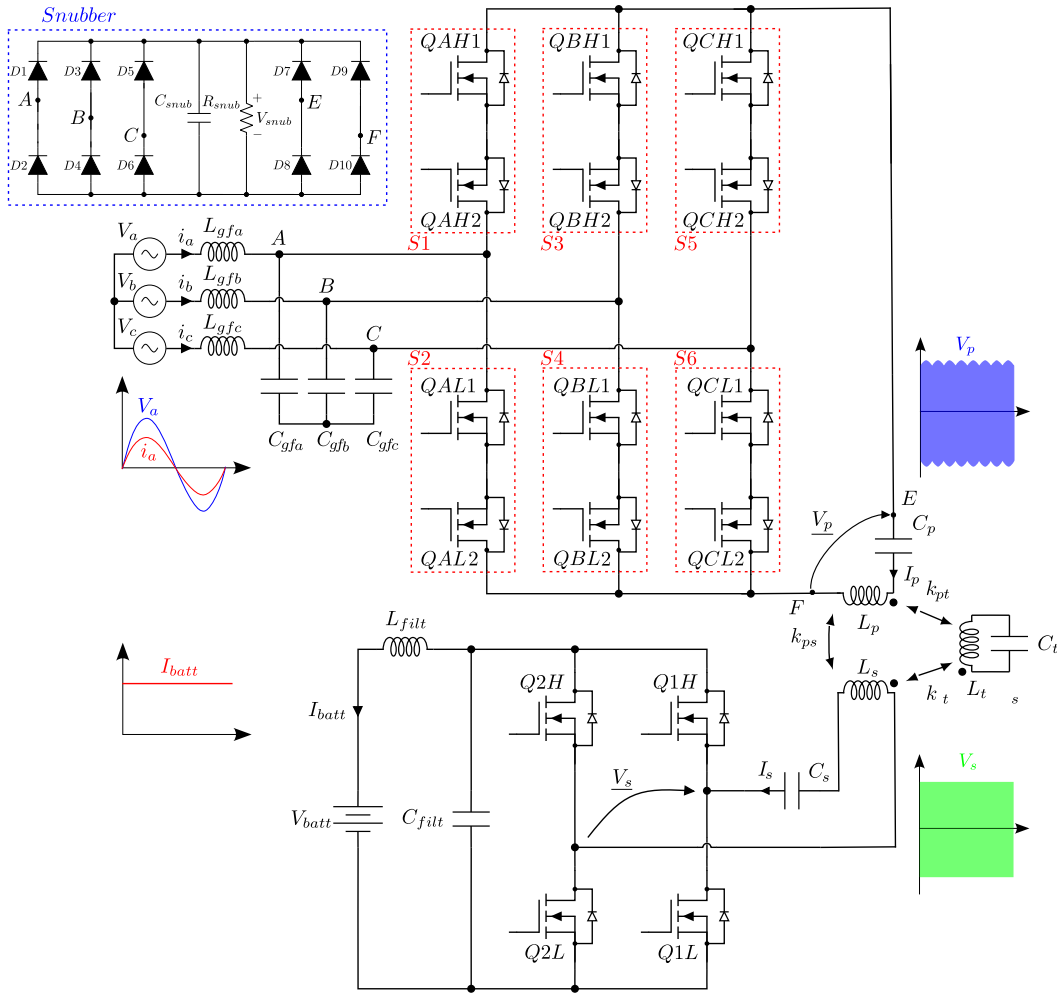


Figure 4.1: Proposed topology of the considered single-stage IPT EV charger

From the equation (3.16) it is clear that to have a constant power flow, it is necessary to have 3 things constant:

1. RMS value of the 1st harmonic of the TSMC's output voltage, U_p
2. RMS value of the 1st harmonic of the secondary inverter's output voltage U_s .
3. Phase shift between TSMC's output voltage and secondary inverter's output voltage

Because the EV's battery is placed directly at the output of the secondary inverter, it is justified to consider that the output voltage of the secondary inverter is rigid (over one grid period, for the high-frequency dynamics that is being analyzed). Thus, by keeping a constant duty cycle of the secondary inverter, 2nd point from the previous list is ensured. This leaves the modulation strategy of the TSMC with the 1st task, while the synchronization algorithm has to fulfill the 3rd one from the previous list. However, the part of the 3rd task can be assigned to the TSMC in order to ease the burden from the synchronization algorithm.

Let us suppose that the signals for controlling the TSMC and the secondary inverter are both generated on the same MCU. Fig. 4.2 depicts three signals: output voltage of the TSMC, voltage of the secondary inverter, and a fixed square-wave reference with 50% duty cycle that is generated inside the MCU and has the same frequency of 100 kHz as the previous two. The

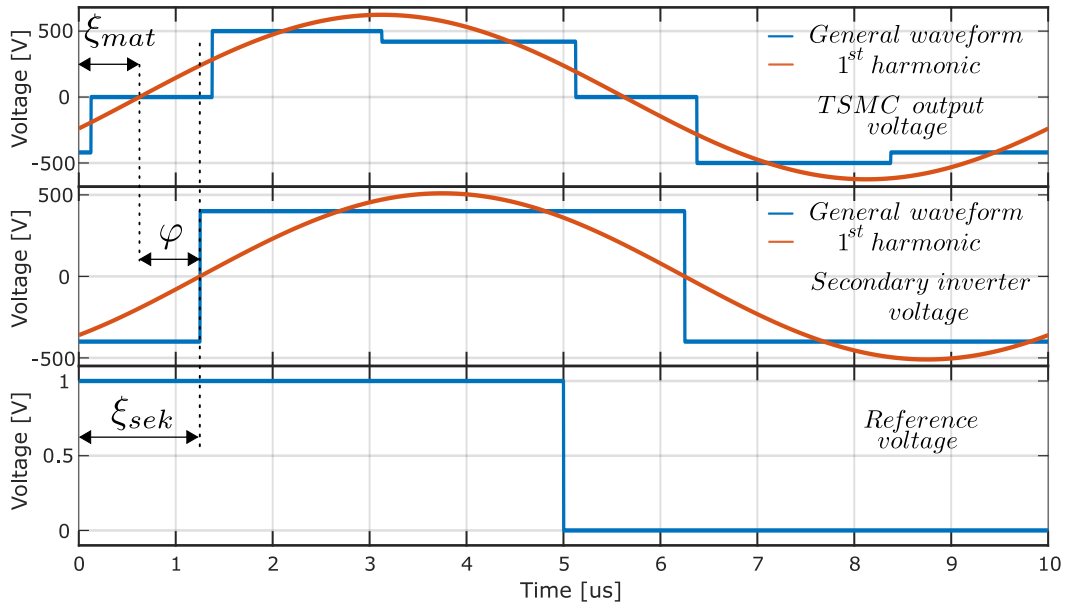
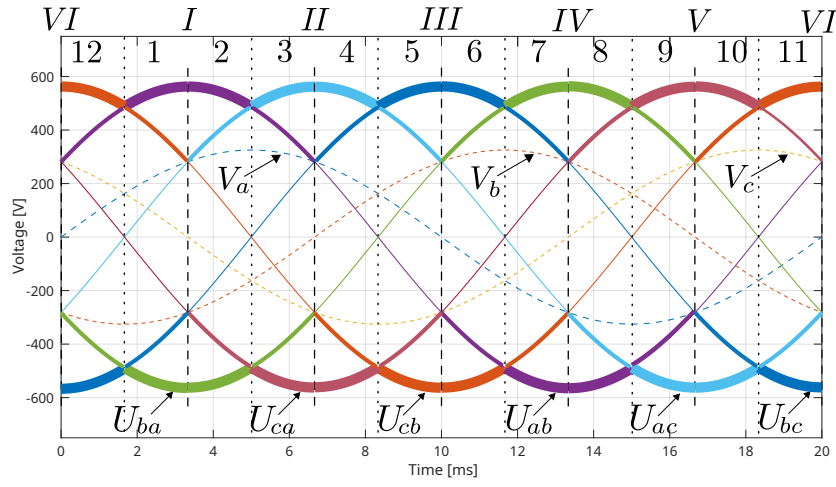


Figure 4.2: Phases of TSMC's output voltage and secondary inverter voltage respective to an invariable reference voltage

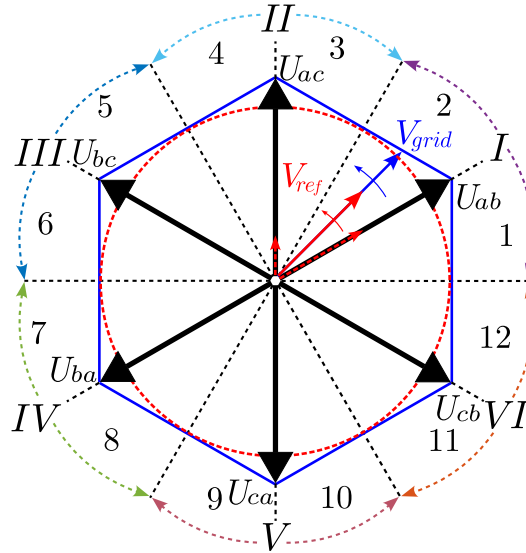
phase shift from the equation (3.16) that determines the power flow can now be expressed in the following manner:

$$\varphi = \xi_{mat} - \xi_{sek} \quad (4.1)$$

If self-phases of the 1st harmonics of both converter voltages ξ_{mat} and ξ_{sek} , which are given respective to the invariable reference voltage, are kept constant over time, it is clear that the task of the synchronization algorithm would be only to adapt the phase shift φ by acting on the self-phase of the secondary ξ_{sek} when there is a change in the desired power transfer. Unfortunately, that is not the case. Because the secondary inverter is controlled by a different



(a)



(b)

Figure 4.3: Line-to-line voltages used for obtaining output high frequency AC voltage a) time-domain b) vectorial

MCU, self-phase of the secondary inverter ξ_{sek} will change over time as explained in Section 3.4. However, this is a low frequency change, that is easily cancelled by the power control loop. If ξ_{mat} would also be time-varying, that would pose an additional, unnecessary task for the synchronization loop, that we want to avoid.

Deficiency of the standard SVM and of the modified SVM that is presented in [75] is that they fail to maintain the self-phase ξ_{mat} of the TSMC's output voltage constant, as well as the RMS value of its first harmonic U_p ; rather they maintain constant the overall RMS of the TSMC's output voltage. To explain this, it is necessary to introduce the voltage waveforms of the grid that are used for generating the output voltage of the TSMC. Fig. 4.3a depicts 6 line-to-line voltages of a three phase system and their usage in obtaining the output voltage. The entire period of the grid voltage is divided into 6 sectors and 12 sections. In each of the sections the highest and the second highest voltage, as well as their negative counterparts, are used for generating TSMC's output voltage. Vectorial representation of this is given in the Fig. 4.3b. Now, let us consider the output voltage of the TSMC that would be generated if the previously mentioned SVMs were applied. Fig. 4.4 shows the generated voltage in two different instants of the grid period with the given reference voltage equal to its maximum value (red inner circle in Fig. 4.3b). Neither RMS value of the 1st harmonic of the voltage is preserved, neither is the phase. The difference in the RMS values of the TSMC's output voltage in the two given cases is 12.7% while the difference in self-phases ξ_{mat} equals to 12.1°. When plugged into the equation (3.16), these oscillations in U_p and ξ_{mat} would cause an oscillation in the power flow between the primary and secondary sides. The frequency of these oscillations would be 300 Hz, i.e., 6 times higher than the grid frequency, similarly to the ripple frequency of the six-pulse rectifier. That is two orders of magnitude higher than the frequency

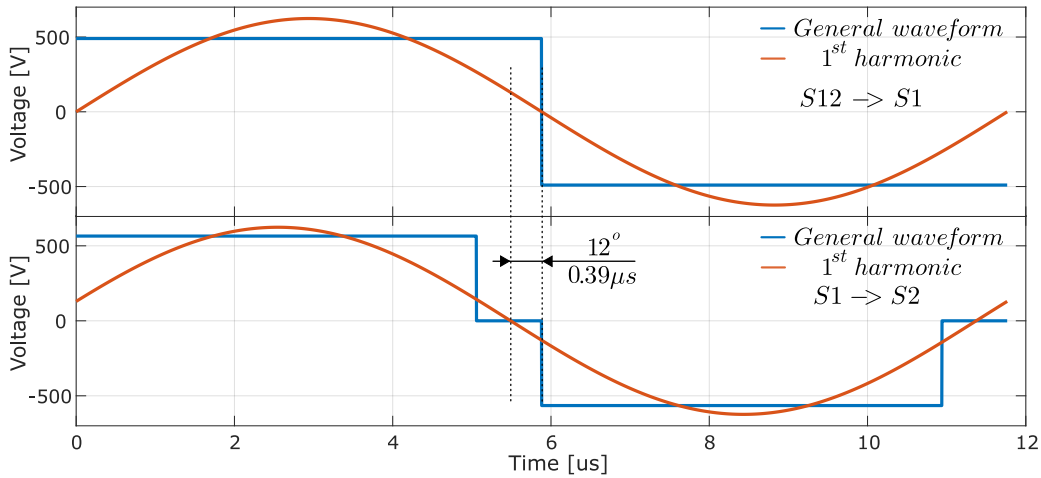


Figure 4.4: Output voltage of the TSMC and its first harmonic obtained using SVM, in two different instants of the grid period - transitions from S12 to S1 and from S1 to S2

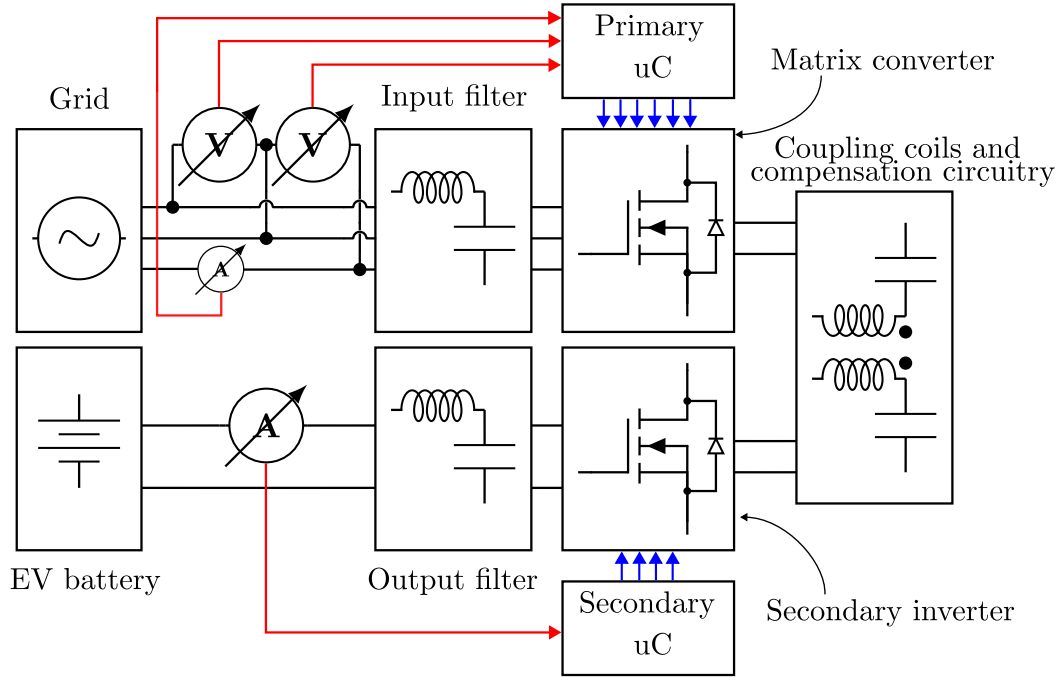


Figure 4.5: Block diagram of the system with the necessary measurements

of change in the self-phase of the secondary inverter ξ_{sek} , which is caused by the different MCUs that control the primary and the secondary side. If these oscillations in power level are not suppressed correctly by the synchronization loop, consequences would be:

1. Increased THD of the grid currents and the impossibility of achieving PFC
2. A large output filter before the EV battery required to filter out the 300 Hz component of the output DC current

In the following chapters a novel modulation method of the TSMC will be presented. It preserves both RMS value of the 1st harmonic and self-phase of the TSMC's output voltage. In this way, stable power flow is maintained, while keeping the design requirements of the synchronization loop at the minimum level.

The proposed topology does not ensure that only active power is taken from the TSMC like in [75]; rather, certain amount of reactive power will also be required. That is where another novelty of the presented modulation strategy of TSMC in this work comes from. It comprises a special flipping pattern used for generating the output voltage of the mentioned converter that gives it capability of handling reactive power at its high-frequency output while keeping the high power factor of the currents that are being taken from the grid.

The advantages of the matrix topology are the elimination of the DC link

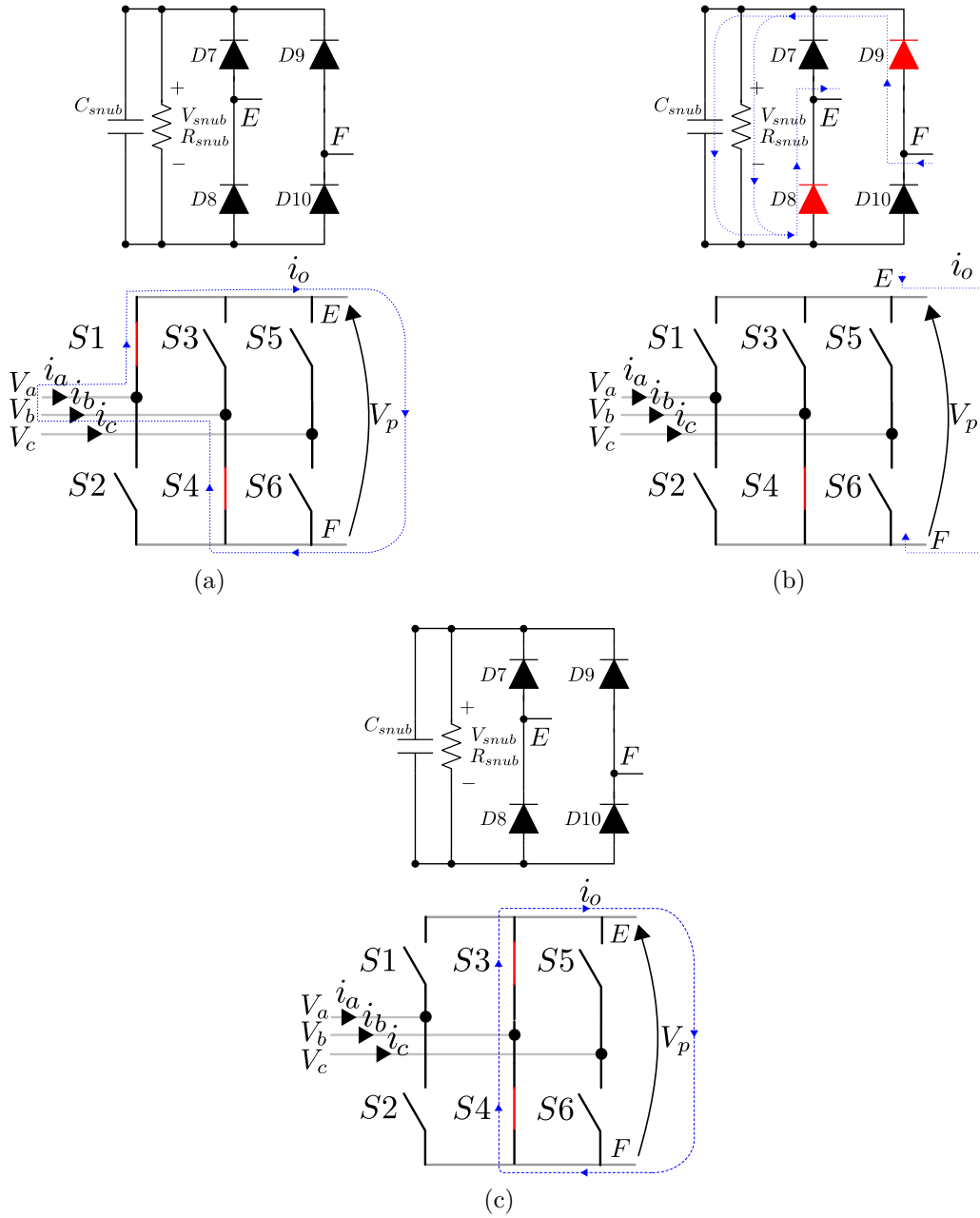


Figure 4.6: Switching transition between S1 and S3 and the role of the snubber a) S1 conducting b) Snubber conducting c) S3 conducting

and the need to use a bulky capacitor on the primary side, and reduction of the input filter interfacing the grid, thus reducing the size of the converter. Because switches employed in the matrix topology are four-quadrant, there are no free-wheeling paths for the secondary current to close itself during commutation transitions. For this reason, a snubber circuit is employed as shown in Fig. 4.1 [126]. The given snubber has only protective role - to provide the free-wheeling path for the output current during commutation process,

thus preventing potential dangerous over-voltages across the switches of the TSMC. This is depicted in Fig 4.6, where the commutation process between switches S1 and S3 is depicted. Without loss of generality, output current of the TSMC is assumed to be positive over the entire encompassed time-span. This leads causes that during the snubber conduction period, diodes D8 and D9 are conducting, clamping the output voltage to $-U_{snub}$. When the output i_o current is negative, the other two diodes D7 and D10 conduct, clamping the output voltage to U_{snub} . The input part of the snubber that is connected to the electrical grid with diodes D1 to D6, that is given in the Fig 4.1, serves only to generate the rigid value of the snubbers DC voltage U_{snub} . Resistor in the DC part of the snubber circuit serves to dissipate the energy from the snubber capacitor that is being absorbed during the switching transition. From the point of view of the circuit layout and design, it is important to maintain all of the parasitic inductances from the part of the circuit shown in Fig 4.6b as low as possible, meaning that the diodes D7 to D10 need to be placed closely to the transistors, as well as the snubber capacitor being that it is this capacitor that dominantly takes on the output current of the TSMC during the switching transition. Being that the energy given to the snubber circuit during the commutation process is dissipated as heat on the R_{snub} , it is desirable to reduce the duration of this process to minimum, in order to reduce the lost energy. For this reason dead-time values in this application are often set to zero, relying on the sufficiency of the turn-on and turn-off delays of the switches and difference between them.

The proposed system requires 3 measurements for achieving synchronized operation between the primary and secondary side converters and having a stable power transfer between the two, as well as an additional control measurement of a grid current in order to achieve complete independence on any wireless communication between primary and secondary MCUs. The matrix converter requires two voltage measurements for synchronized operation with the grid and a measurement of one of the grid currents for obtaining information power transfer status. The secondary inverter requires measurement of its output current because that is the value it will control, in order to achieve the desired charging/discharging of the electric battery. The block diagram of the system with the employed measurements is given in Fig. 4.5. The matrix converter functions in an open loop, i.e., it does not have closed-loop control of any of his input or output values. The secondary MCU controls the inverter by adjusting its phase so that the battery current is equal to the reference. More details on this topic are given in Section 3.4.

4.2 Basic variant of the proposed modulation strategy

The basic variant of the TSMC's modulation that is proposed in this Thesis has three main tasks to fulfill:

1. To provide the constant RMS value of the 1st harmonic of the output voltage U_p
2. To provide the constant self-phase ξ_{mat} of the primary side voltage
3. To ensure that the active power at the output of the TSMC is distributed over the phases of the grid in such a way that low THD and high PF of the grid currents are achieved.

The calculus that is presented in this Section is based on the **assumption** that the current at the output of the TSMC is purely sinusoidal and is in phase with the first harmonic of TSMC's output voltage. Enhanced modulation strategy where a flipping pattern is added to the modulation to provide reactive-power-handling capability to the TSMC is given in the following Section.

For generating the output voltage of the TSMC, the proposed modulation uses the highest and the second highest grid voltage in every instant of the grid period, as well as their negative counterparts. This is the same as with the SVMs that are mentioned before, and it is done in order to give the converter a possibility to operate with the highest possible range of the output voltage that is possible to achieve. Fig. 4.7 shows the output voltage of the TSMC u_p during one switching period as well as its first harmonic U_p and the output current i_o that, according to the assumption, is in phase with U_p . The

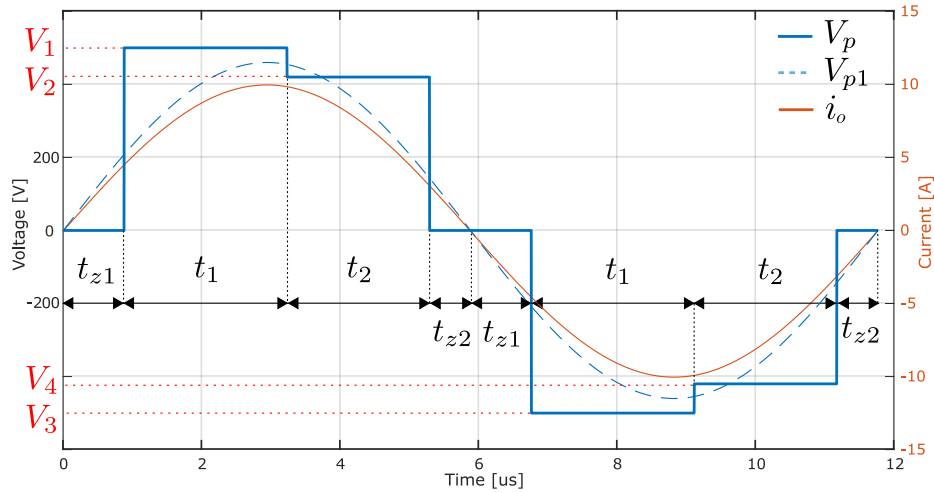


Figure 4.7: TSMC's output voltage, its first harmonic and assumed output current

final goal of this modulation calculus is to obtain the values of times t_{z1} , t_1 , t_2 , and t_{z2} that are marked in the given figure so that all of the tasks from the beginning of this chapter are accomplished.

As the consequence of all of the symmetries that exist between the voltages that are used to generate the output voltage of the TSMC, it is sufficient to calculate the mentioned times for only one Section of one Sector and then apply them correctly in all other Sections and Sectors. Without loss of generality, let us perform the calculus for Section 1 of Sector I. For the considered Section, the values of the voltages V_1 , V_2 , V_3 and V_4 that are marked in Fig. 4.7 are given by the following equations:

$$V_1 = U_{ab} = U_{L-L} \sin(\pi/3 + \theta) \quad \theta \in [0, \pi/6] \quad (4.2)$$

$$V_2 = U_{cb} = U_{L-L} \sin(2\pi/3 + \theta) \quad \theta \in [0, \pi/6] \quad (4.3)$$

$$V_3 = -V_1 \quad (4.4)$$

$$V_4 = -V_2 \quad (4.5)$$

where U_{L-L} is equal to the amplitude of the grid line-to-line voltage and θ is the angle that describes the used voltages in each instant of the considered Section. These voltages are considered constant in one period of the output voltage u_p because the switching frequency is three orders of magnitude higher than the grid frequency. The considered Section, that is, the considered interval of θ , can be discretized into n small segments $[\theta_0, \theta_1, \dots, \theta_i, \dots, \theta_n]$, $\theta_i = i\pi/6n$, where the grid voltages can be considered constant. Now, the system can be examined on one of the segments of the previous interval, θ_i , in order to obtain the four unknown values of time.

Fig. 4.8 shows the switching states during one period of the TSMC's output voltage. Equations relating the grid currents to the output current of the TSMC and the TSMC's output voltage to the grid voltages in one half-period of the switching cycle are given below.

$$\left. \begin{array}{l} i_a = i_b = i_c = 0 \\ V_o = 0 \end{array} \right\} t \in [0, t_{z1}] \cup [T/2 - t_{z2}, T/2] \quad (4.6)$$

$$\left. \begin{array}{l} i_c = 0 \\ i_a = -i_b = i_o \\ V_o = V_{ab} \end{array} \right\} t \in [t_{z1}, t_{z1} + t_1] \quad (4.7)$$

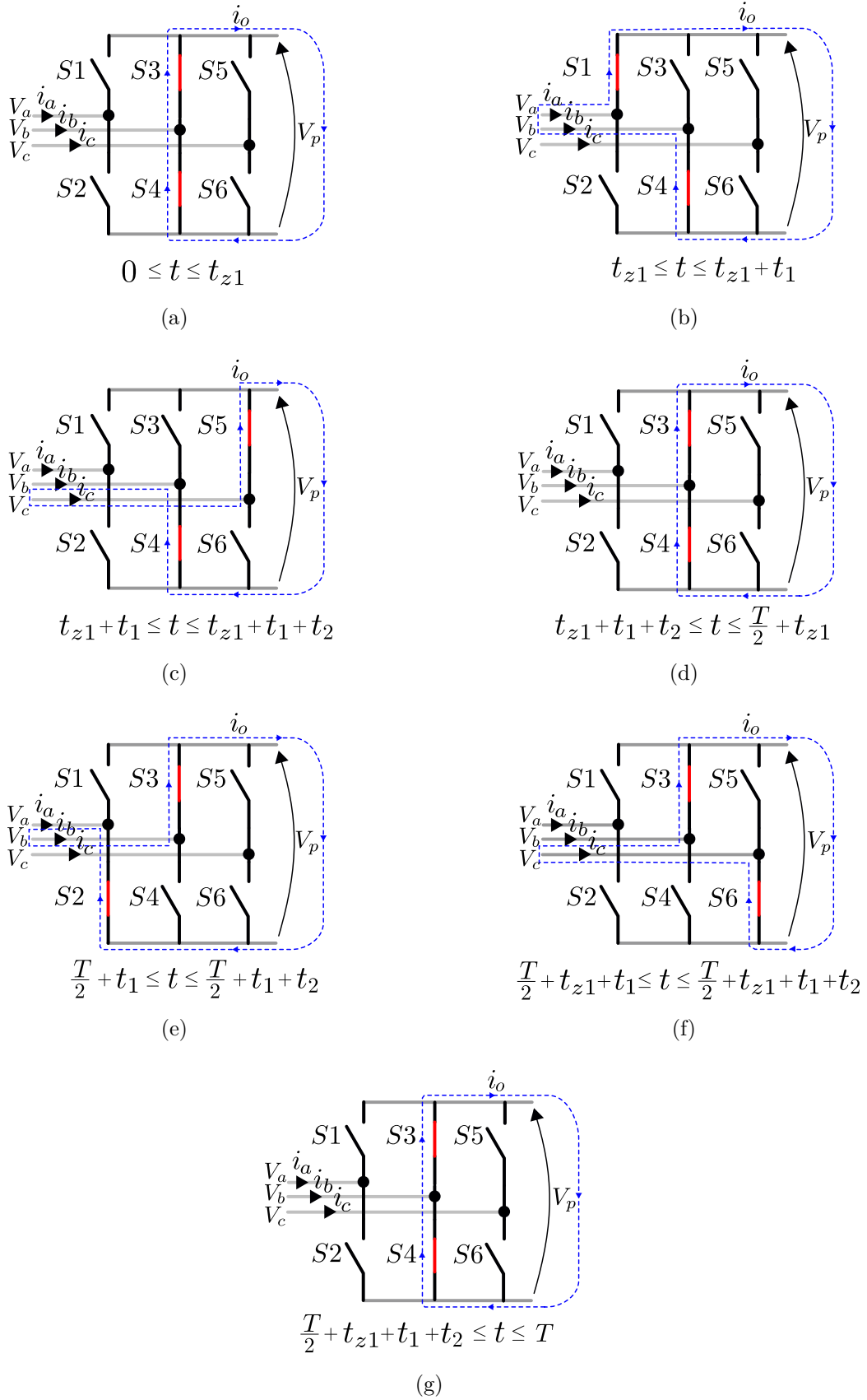


Figure 4.8: Switching states during one period of the TSMC's output voltage for Sector I, Section 1

$$\left. \begin{array}{l} i_a = 0 \\ i_c = -i_b = i_o \\ V_o = V_{cb} \end{array} \right\} t \in [t_{z1} + t_1, T/2 - t_{z2}] \quad (4.8)$$

From equations (4.6)-(4.8) it is possible to calculate the average values of the grid currents during one period of the high frequency voltage.

$$i_a = (2/T) \int_{t_{z1}}^{t_{z1}+t_1} i_o(t) dt \quad (4.9)$$

$$i_b = -(2/T) \left[\int_{t_{z1}}^{t_{z1}+t_1} i_o(t) dt + \int_{t_{z1}+t_1}^{T/2-t_{z2}} i_o(t) dt \right] \quad (4.10)$$

$$i_c = (2/T) \int_{t_{z1}+t_1}^{T/2-t_{z2}} i_o(t) dt \quad (4.11)$$

According to the initial assumption, the output current is in phase with the first harmonic of the output voltage of the TSMC as shown in Fig. 4.7.

$$i_o = I \sin(\omega t) \quad (4.12)$$

To achieve low THD of the grid currents it is required that each of them is proportional to its corresponding grid voltage. From this fact following equations are obtained:

$$V_a(\theta_i)/V_b(\theta_i) = i_a/i_b \quad (4.13)$$

$$V_a(\theta_i)/V_c(\theta_i) = i_a/i_c \quad (4.14)$$

It is possible to show that the last two equations are equivalent for the considered system because the following conditions that are always satisfied:

$$V_a + V_b + V_c = 0 \quad (4.15)$$

$$i_a + i_b + i_c = 0 \quad (4.16)$$

Two equations are defined with the given tasks of the modulation that are related to the RMS of the 1st harmonic of TSMC's output voltage and its self-phase. These conditions can be expressed in the best way using the sine and cosine arguments of the Fourier transform of the TSMC's output voltage that is shown in Fig. 4.7.

$$V_{RMS} = (\sqrt{2}/T) \int_0^{T/2} V_p(t) \sin(\omega t) dt \quad (4.17)$$

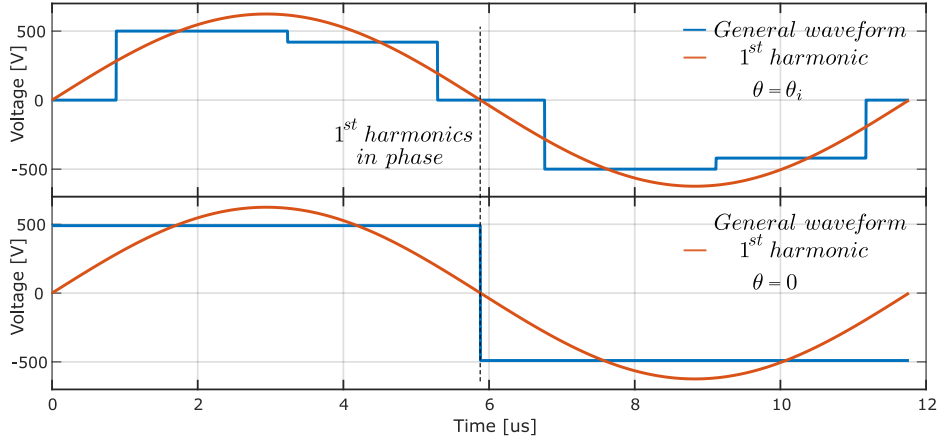


Figure 4.9: TSMC's output voltage for $\theta = 0$ and $\theta = \theta_i$

$$0 = (\sqrt{2}/T) \int_0^{T/2} V_p(t) \cos(\omega t) dt \quad (4.18)$$

V_{RMS} is the desired RMS value of the output voltage of the TSMC. The equation (4.18) basically means that the self-phase ξ_{mat} of the TSMC's output voltage is always kept constant and equal to its value that is obtained in the instants $\theta = 0$. In these instants, with the given reference of the voltage u_p equal to its maximum possible value (red circle in Fig. 4.3b), the voltage u_p is a square-wave. Fig. 4.9 shows the voltage V_p in instants $\theta = 0$ and $\theta = \theta_i$.

The last equation that is used to close the system correlates the sum of all of the four variable time values with the time period of the TSMC's output voltage, i.e., with the switching frequency.

$$t_{z1} + t_1 + t_2 + t_{z2} = T/2 = 1/2f_{sw} \quad (4.19)$$

Equations (4.13), (4.17), (4.18) and (4.19) form a full system of equations that is used to find the unknown time values t_{z1} , t_1 , t_2 and t_{z2} . Due to its complex form, an analytical solution of the given system of equations is almost impossible to find. Using MATLABs numerical solver it is possible to obtain the wanted solution of the system. The equations are solved for all of the

Sector	I		II		III		IV		V		VI	
Section	1	2	3	4	5	6	7	8	9	10	11	12
V_1	S_1S_4	S_1S_4	S_1S_6	S_1S_6	S_3S_6	S_3S_6	S_3S_2	S_3S_2	S_5S_2	S_2S_2	S_5S_4	S_5S_4
V_2	S_5S_4	S_1S_6	S_1S_4	S_3S_6	S_1S_6	S_3S_2	S_3S_6	S_5S_2	S_3S_2	S_5S_4	S_5S_2	S_1S_4
V_3	S_3S_2	S_3S_2	S_5S_2	S_5S_2	S_5S_4	S_5S_4	S_1S_4	S_1S_4	S_1S_6	S_1S_6	S_3S_6	S_3S_6
V_4	S_3S_6	S_5S_2	S_3S_2	S_5S_4	S_5S_2	S_1S_4	S_5S_4	S_1S_6	S_1S_4	S_3S_6	S_1S_6	S_3S_2
V_z	S_3S_4	S_1S_2	S_1S_2	S_5S_6	S_5S_6	S_3S_4	S_3S_4	S_1S_2	S_1S_2	S_5S_6	S_5S_6	S_3S_4

Table 4.1: Switches used for generating output voltage of the TSMC across all Sectors and Sections

discrete values of θ and a look-up table is formed from this data, that is later used in the control algorithm. Table 4.1 shows the combination of switches that are used for generating the output voltage of the TSMC throughout all Sectors and Sections.

The previously described modulation ensures the output voltage of the TSMC has constant RMS of the 1st harmonic U_p and the constant self-phase ξ_{mat} , thus it provides a stable power flow between the primary and secondary side. Derivation in this chapter relies on the assumption that the output current of the TSMC is sinusoidal and in phase with the first harmonic of the TSMC's output voltage. The sinusoidality of the mentioned current is a justified assumption because of the resonant nature of the used compensation circuit. However, as the consequence of the compensation topology described in the previous Chapter, the phase of the TSMC's output current is not guaranteed to be in the phase with its output voltage. Repercussions of this are given in the following Section, and an enhancement is added to the proposed modulation strategy.

4.3 Enhanced modulation strategy

The non-zero phase shift between the output voltage and current of the TSMC means that the converter is handling not only active but a reactive power as well at its output. Considering that this converter consists only out of transistors, it does not have passive reservoirs of reactive power. This means that its input and output reactive powers are equal. The goal of this chapter is to investigate the influence of the reactive part of the output power on the objectives of the TSMCs modulation that have been set in the previous chapter, and to present a novel solution that enables TSMC to process reactive power at its output while keeping low THD of the grid currents.

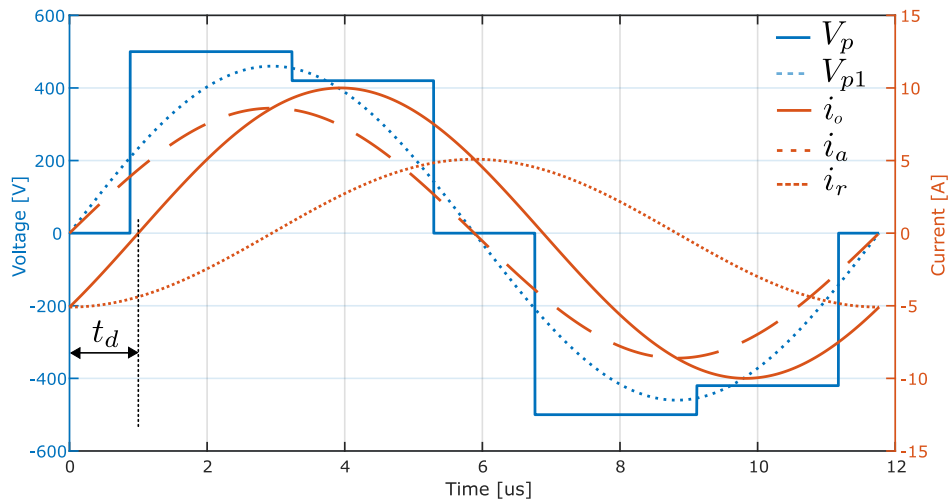


Figure 4.10: TSMC's output voltage and current

The deviation of the output current from the waveform that was assumed in the previous chapter will contribute to the increased THD of the grid currents, i.e., it will not influence the stable power flow between the primary and secondary side. However, in order to make this solution comply with the grid standards, it is necessary to keep the THD of the grid currents below 5%. Fig. 4.10 shows the output voltage of the TSMC and its output current. The output current can be dissolved as sum of its active and reactive parts respective to the output voltage:

$$\begin{aligned} i_o &= I \sin(\omega(t - t_d)) \\ i_o &= i_{act} + i_{rct} \end{aligned} \quad (4.20)$$

$$\begin{aligned} i_{act} &= I \cos(\omega t_d) \sin(\omega t) \\ i_{act} &= I_a \sin(\omega t) \end{aligned} \quad (4.21)$$

$$\begin{aligned} i_{rct} &= -I \sin(\omega t_d) \cos(\omega t) \\ i_{rct} &= I_r \cos(\omega t) \end{aligned} \quad (4.22)$$

The modulation strategy described in the previous chapter can be applied separately to both active and reactive components of the output current in

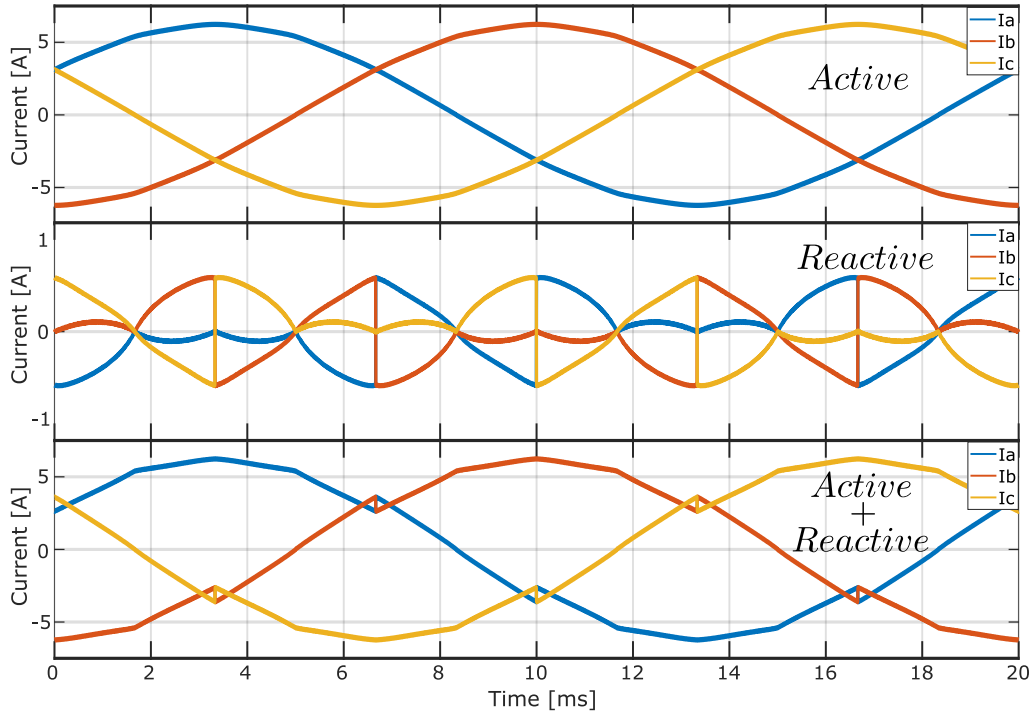


Figure 4.11: Simulated results of the grid currents obtained by processing active part of the output current i_{act} , reactive part of the output current i_{rct} and the resulting grid current that is the sum of the previous two. Output current i_o has the amplitude $I = 10$ A and phase $\omega t_d = 10^\circ$

order to obtain the grid currents. Fig. 4.11 shows the simulated waveforms of the grid currents obtained by applying the modulation strategy to the active and reactive parts of the output current, as well as the resulting grid currents that are equal to the sum of the two. In the given case, the phase shift between the output current and the first harmonic of the output voltage is 10° . As can be seen, when the described modulation is applied, the reactive component of the output current of the matrix converter transforms itself into higher-order harmonics of the grid current, significantly influencing the THD of the resulting grid current. The dependance of the THD of the grid currents on the phase of the output current respective to the first harmonic of the output voltage is given in Fig. 4.12. The maximum value permitted by the standard is achieved in the narrow range of phases of the output current $[-9^\circ, 8^\circ]$.

An enhanced modulation of the TSMC is proposed in order to give converter the possibility to process the reactive power at its output while keeping the low THD of the grid currents and high PF. Let us observe the following: if one half-period of the output voltage is taken and flipped around the middle point of the half-period, neither RMS nor the phase of the first harmonic of the output voltage will change. This is shown in Fig. 4.13, and it is the consequence of the derivation of the output voltage waveform given in the previous chapter. Let us assume that in two consecutive switching periods the voltages given in Fig. 4.13 are applied, where in the first switching period the original pattern is applied while in latter, the flipped pattern is applied. A change in the grid voltage levels during this time can be neglected considering ratio between grid and switching frequency, thus, the corresponding voltages in the two cases will be considered equal. The following calculus will be done for Sector I, Section 1. Equations (4.9)-(4.11) determine the grid currents

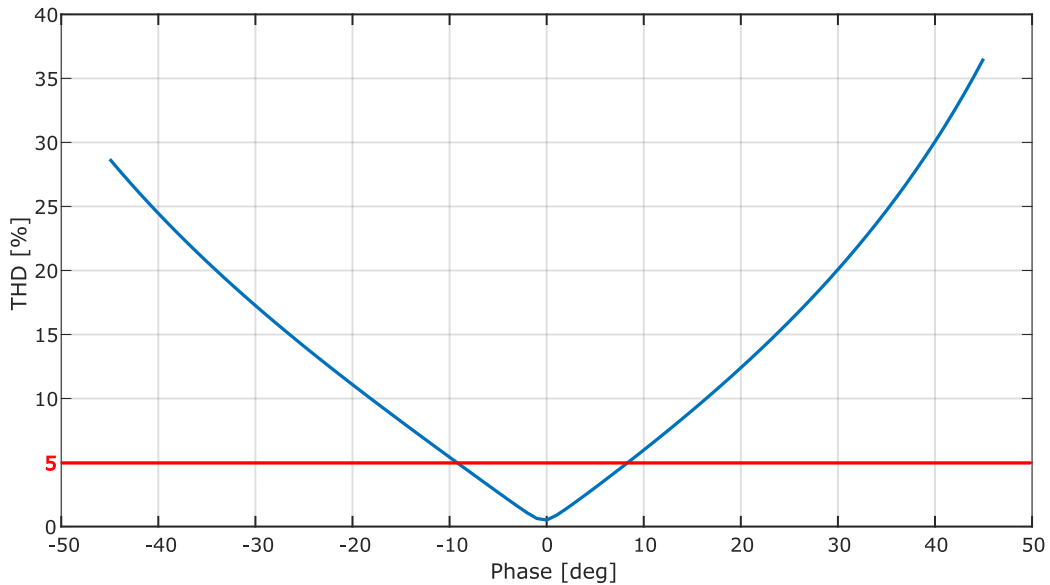


Figure 4.12: THD of the grid currents in dependance on the phase of the output current

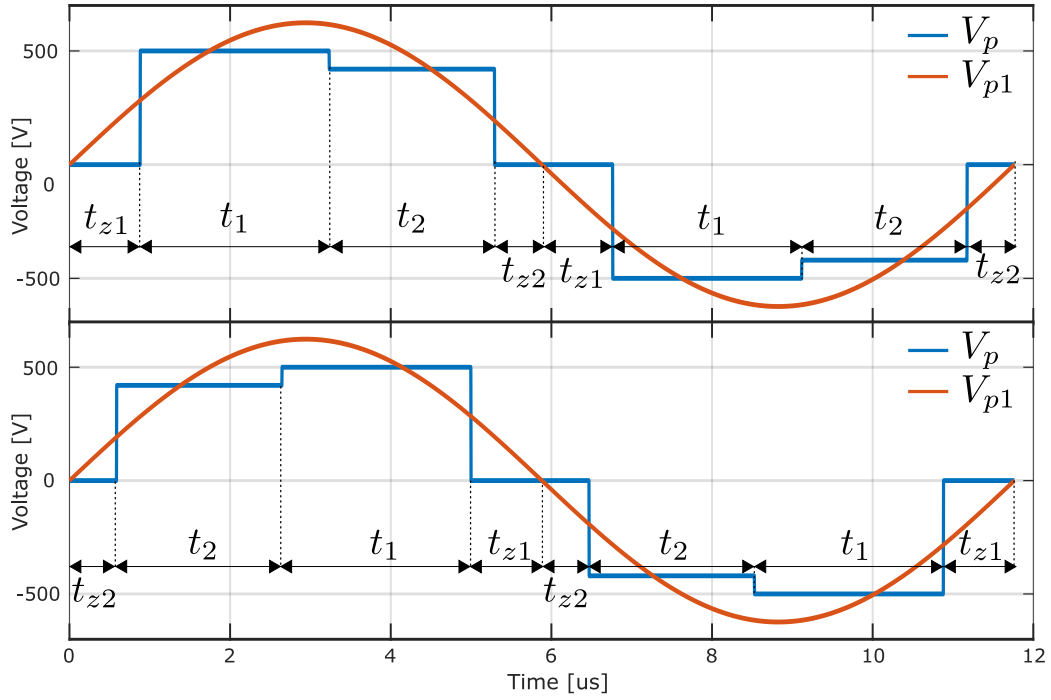


Figure 4.13: Original output voltage waveform and flipped output voltage waveform – RMS and phase of the first harmonic of the output voltage are conserved

during the first switching cycle. During the second switching cycle, with the flipped pattern applied, the grid currents are given by:

$$i_a = (2/T) \int_{t_{z2}+t_2}^{T/2-t_{z1}} i_o(t) dt \quad (4.23)$$

$$i_b = -(2/T) \left[\int_{t_{z2}}^{t_{z2}+t_2} i_o(t) dt + \int_{t_{z2}+t_2}^{T/2-t_{z1}} i_o(t) dt \right] \quad (4.24)$$

$$i_c = (2/T) \int_{t_{z2}}^{t_{z2}+t_2} i_o(t) dt \quad (4.25)$$

Combining equations (4.9)-(4.11) with (4.23)-(4.25) it is possible to obtain the average value of the grid current during two switching cycles carried out in previously described manner:

$$i_a = (1/T) \left[\int_{t_{z1}}^{t_{z1}+t_1} i_o(t) dt + \int_{t_{z2}+t_2}^{T/2-t_{z1}} i_o(t) dt \right] \quad (4.26)$$

$$i_b = -(1/T) \left[\int_{t_{z1}}^{T/2-t_{z2}} i_o(t) dt + \int_{t_{z2}}^{T/2-t_{z1}} i_o(t) dt \right] \quad (4.27)$$

$$i_c = (1/T) \left[\int_{t_{z1}+t_1}^{T/2-t_{z2}} i_o(t) dt + \int_{t_{z2}}^{t_{z2}+t_2} i_o(t) dt \right] \quad (4.28)$$

Due to the properties of sine and cosine functions the following equations are true:

$$\int_{t_x}^{t_y} \sin(\omega t) dt = \int_{T/2-t_y}^{T/2-t_x} \sin(\omega t) dt \quad (4.29)$$

$$\int_{t_x}^{t_y} \cos(\omega t) dt = - \int_{T/2-t_y}^{T/2-t_x} \cos(\omega t) dt \quad (4.30)$$

Replacing the expressions for active and reactive part of the output current that are given in equations (4.20)-(4.22) into the equations that define the average grid current in two consecutive switching cycles (4.26)-(4.28) and having in mind the properties of the sine and cosine functions that are given above, one obtains:

$$i_a = (2/T) \int_{t_{z1}}^{t_{z1}+t_1} I_a \sin(\omega t) dt \quad (4.31)$$

$$i_b = -(2/T) \int_{t_{z1}}^{T/2-t_{z2}} I_a \sin(\omega t) dt \quad (4.32)$$

$$i_c = (2/T) \int_{t_{z1}+t_1}^{T/2-t_{z2}} I_a \sin(\omega t) dt \quad (4.33)$$

This means that the average grid current over the interval of two switching cycles, where the second one is flipped, is equal to one that is produced only

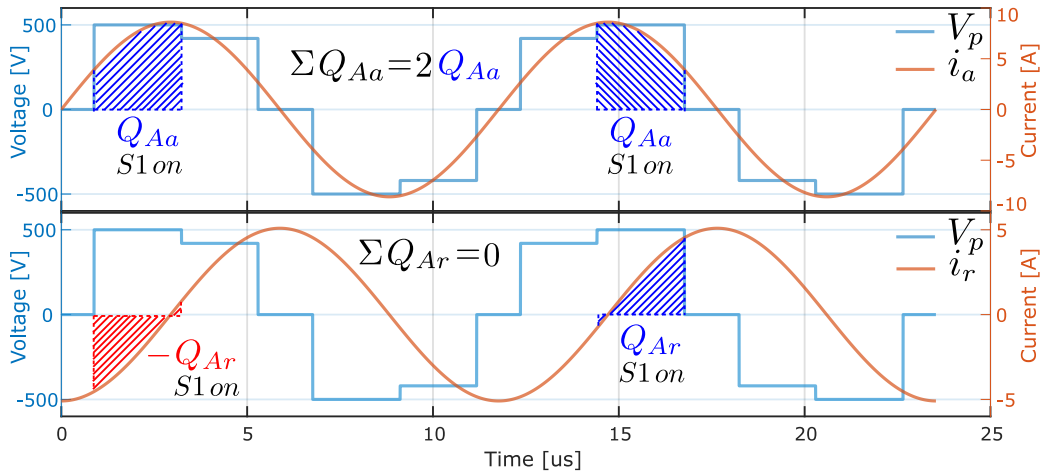


Figure 4.14: Graphical representation of the enhanced modulation strategy acting on active and reactive components of the TSMC's output current

by the active component of the output current, while the average value of the reactive component is equal to zero. Fig. 4.14 is given in order to visualize the previous calculus and its conclusion on the example of phase A of the grid. It shows two consecutive switching cycles, one is normal and the other one is flipped. Only positive half-periods are considered, while in the negative ones everything is analogous. In the upper graph, it is shown how the enhanced modulation strategy acts on the active component of the output current, while the lower graph shows how it acts on the reactive component of the output current. Hatched surfaces represent the values of the integrals that are present in equation (4.26). What was proven analytically now is visible - flipping the waveform in the explained way does not influence the average value of the grid current that exists as a consequence of the active component of the output current, but it does lead to zero average value of the grid current that exists as a consequence of the reactive component of the output current. The influence of the reactive component of the output current will result as a high frequency ripple with frequency equal to half of the switching frequency. Fig. 4.15 shows the simulated grid currents obtained with the previously described modulation strategy. Now, the THD of the grid currents will depend on the

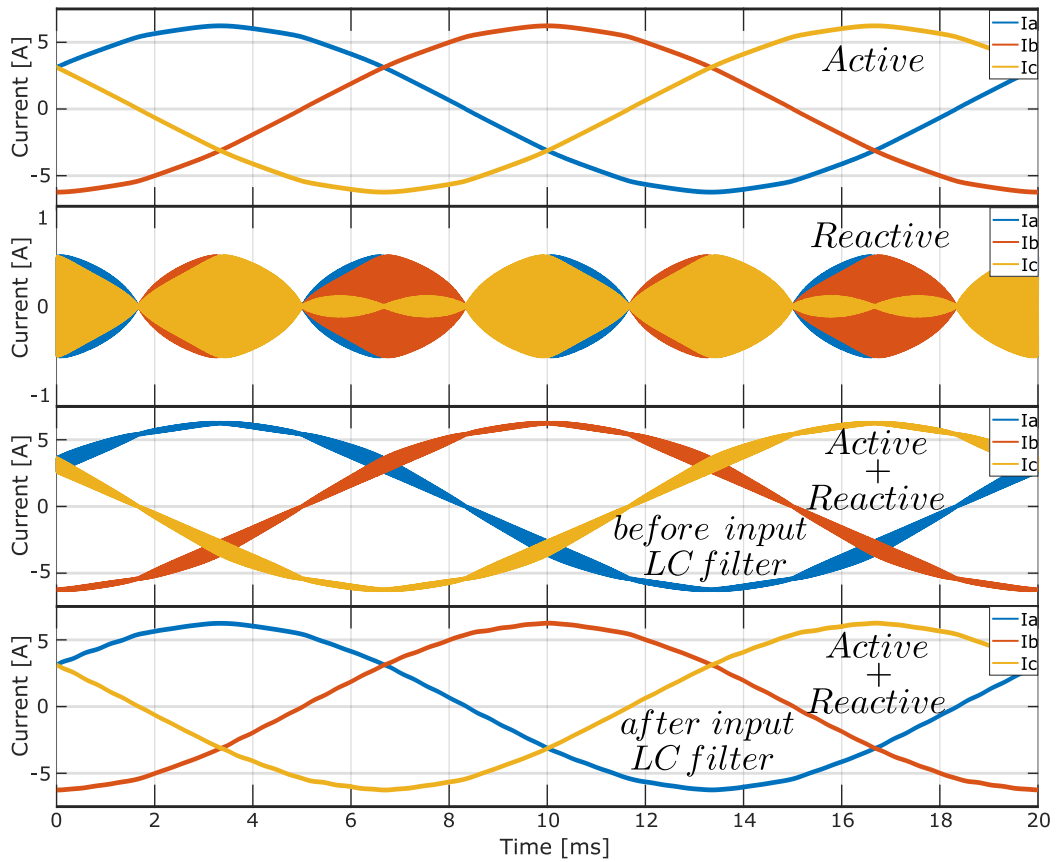


Figure 4.15: Simulated results of applying the enhanced modulation strategy on active and reactive part of TSMC's output current

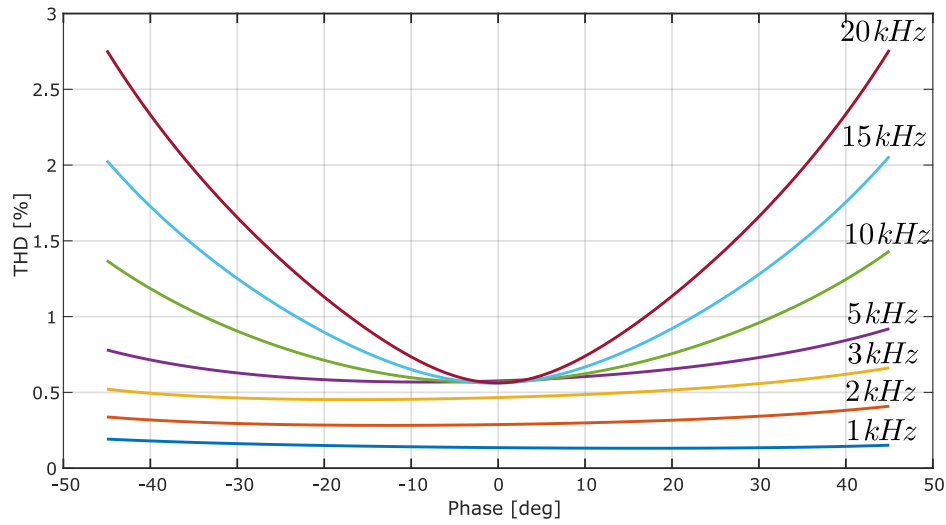


Figure 4.16: Dependency of THD of the grid currents on phase of the TSMC's output current for different cutoff frequencies of the input filter

cutoff frequency of the input filter, and on the phase of the output current. This dependency is given in Fig. 4.16. Clearly, the THD of the grid currents with this kind of modulation satisfies the standard-determined value in the entire range of potential phases of the output current that is of interest. With the presented modulation strategy employed, the matrix converter achieves all defined goals and satisfies all that standard demands. In reality, THD will be slightly higher than the value given in Fig. 4.16 due to measuring tolerances and delays, as well as due to the presence of higher harmonics in the output current of the matrix converter.

4.4 Power flow control

The IPT charger for EVs is made up of two physically separated parts—the part that is placed on the ground and the other one onboard the vehicle. Because of this, two separate MCUs will be required to control the converters, as shown in Fig. 4.5. Due to the difference in frequencies of crystal oscillators, which determine the MCUs operating frequency, there will inevitably exist a difference in the switching frequencies of the primary and secondary converter. This difference, which is usually around a few Hertz [89], causes a constant change in the phase shift between primary and secondary converters, consequently leading to a constant change in the power flow and inoperability of the system.

In papers [88], [89] more in-depth analysis can be found related to this topic, only in those cases there is no matrix converter, rather they are synchronizing two full-bridge inverters of the classical system given in Fig. 1. In both papers, the existence of non-real-time wireless communication between the MCUs is present as well as estimation of the magnetizing inductance. This

is mainly due to the fact that the topology that is present in both of the papers contains the classical SS compensation strategy described in Chapter 1. Another novelty in our work, which is a consequence of the applied compensation strategy, is the synchronization method between primary and secondary converters. Fig. 4.17 depicts a block diagram on which we base the proposed synchronization strategy.

Between the primary and secondary MCUs, wireless communication does not exist, neither does the estimation of the magnetizing inductance. The matrix converter operates independently, synchronized with the grid, generating the high frequency voltage using the previously described modulation strategy. The secondary MCU controlling the inverter is the one in charge of synchronization. Its task is to constantly adjust the phase of the secondary inverter in order to keep the phase shift between primary and secondary constant, thus keeping power flow and battery current constant. The reference of the battery current is provided by the Battery Management System (BMS). A simple PI controller is in charge of keeping the current at the given level, providing the necessary phase of the secondary voltage at its output. To tune the PI controller, the considered system will be represented using a simple model in which the entire structure of the coupling coils and compensation circuitry is reduced to an equivalent inductor as described in the previous Chapter. The current of the EV battery is given by the following equation:

$$I_{bat} = (4/\pi\sqrt{2})U_p'' \sin(\varphi)/\omega L_{eq}'' \quad (4.34)$$

where U_p'' and L_{eq}'' are, respectively, the RMS of the first harmonic of the output voltage of the TSMC reduced to the secondary side and the equivalent serial inductance at the operating frequency reduced to the secondary side. The difference in clock frequencies causing constant phase shift in voltages between the two sides will be modeled as an external disturbance with a ramp-like shape. The influence of the output LC filter on the dynamic response of the battery current is neglected. Considering that the system has the highest amplification in the vicinity of zero phase shift, i.e., $\cos(\varphi_0) = 0$, the constants of the PI controller will be determined for the system at this point. The simplified block diagram of the system used for tuning the PI controller is given in Fig. 4.18. K_{fb} and T_f are gain and time constant that describe gain and delayed that are introduced by the measuring and filtering system of the battery current. As mentioned before in this chapter, frequency of the disturbance is around few Hertz. To maintain the simplicity of the PI controller on the one side, and the precise reference tracking capability on the other, it is necessary that the bandwidth of the closed-loop system is high enough, at least an order of magnitude higher than the frequency of the disturbance. In this way, the steady state error, caused by the incapability of the PI controller to completely suppress the ramp-like disturbance, is kept low. For this reason, 100 Hz is chosen as the bandwidth of the closed-loop system. An overshoot in the response to the step change in current reference is not desirable; thus, phase margin should be chosen conservatively. The

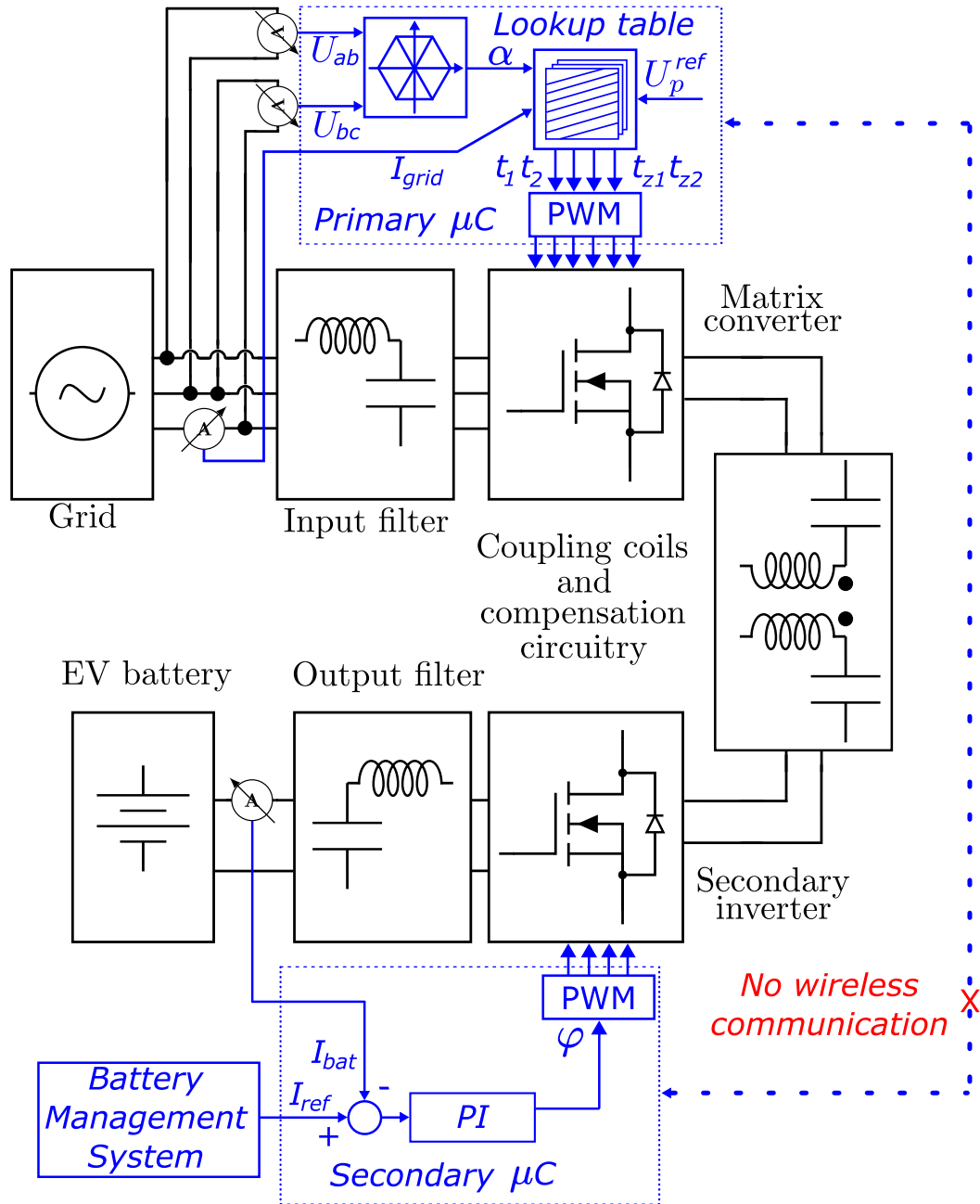


Figure 4.17: Block diagram of the used control and synchronization strategy

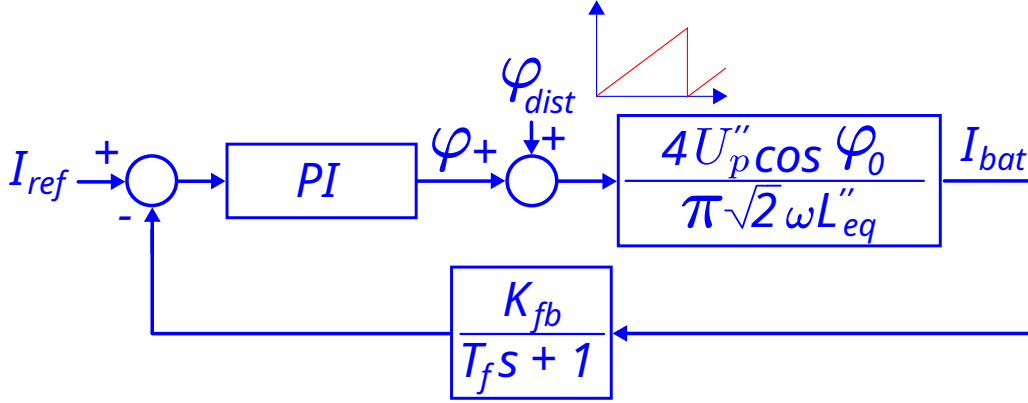


Figure 4.18: Simplified block diagram of the system

value chosen in this work is 60° .

When the primary and secondary sides are working without synchronization, stable power transfer is not possible. However, worse than that is that the primary and secondary currents will be higher than under normal working conditions. On the startup of the system, the initial phase shift between the voltages is unpredictable. To prevent potential failure during the startup, both the primary and secondary sides start with a reduced duty cycle, thus decreasing the RMS values of the voltages and currents during the synchronization process. In Fig. 4.17, U_p^{ref} stands for the internal reference of the RMS value of TSMC's output voltage that determines which lookup table will be used for generating the output voltage of TSMC at the given moment. Different lookup tables contain different values of the times t_1 , t_2 , t_{z1} and t_{z2} as it is explained in Section 3.2, thus determining different values of the RMS of TSMC's output voltage. Once synchronized operation is reached, the output voltages of the primary and secondary converters gradually increase to their nominal values. Primary MCU detects secondary inverter entering synchronous operation by measuring that the grid current is stable. Once the duty cycles reach nominal values, battery charging process can begin. Battery is charged by controlling the output DC current of the secondary inverter. Reference for this current is given by the BMS as it is shown in Fig. 4.17. Let us note here, that the information about State of Charge of the EVs battery is not sent to the primary, because primary does not require it for its operation. Secondary is the one constantly adjusting its phase-shift relative to primary, thus adjusting the power transfer and the DC current that it controls, and charges the battery in the way it is required. Once the battery is fully charged, instead of stopping operation, secondary inverter continues to work keeping the phase shift at zero degrees for certain predefined amount of time. During this time, sensor of the primary current detects that no power is being taken from the grid. After the predefined time expires, both converters gradually reduce their duty cycle and stop operating.

4.5 Experimental results

The prototype of the matrix converter that is used in the experiments is given in Fig. 4.19, while Fig. 4.20 shows the look of the entire system. The parameters of all elements of the system are given in Table 4.2. First, the synchronization test between the primary and secondary sides is conducted. The results are given in Fig. 4.21. The Fig. 4.21a shows the period of unsynchronized work, as well as the moment when control of the battery current on the secondary was enabled, i.e., the moment of synchronization. Figs. 4.21b, 4.21c, and 4.21d show voltages and currents of the matrix converter and secondary inverter in different moments during the synchronization process. Directions of the currents correspond to ones marked in Fig. 4.1. Waveform of the TSMC's output current is determined by the active and reactive power levels that are being exchanged between the two sides, as well as by the excitation of the compensation circuit by higher-order harmonics in TSMC's output voltage. As it can be seen, once synchronized, current is composed only out of higher-order harmonics, and part that is purely reactive. This is the consequence of the control algorithm described in the previous Chapter and the fact that the reference for the battery current is zero until the charging begins. After the primary and secondary voltages are synchronized, duty cycles gradually increase until nominal output voltages are achieved, after which the charging of the EV battery starts.

Two different modes of operation have been tested, G2V and V2G. In the first one, G2V, input power is equal to 3.68 kW as can be seen in Table 4.3, while the output voltage and current are 403.8 V and 8.6 A, respectively,

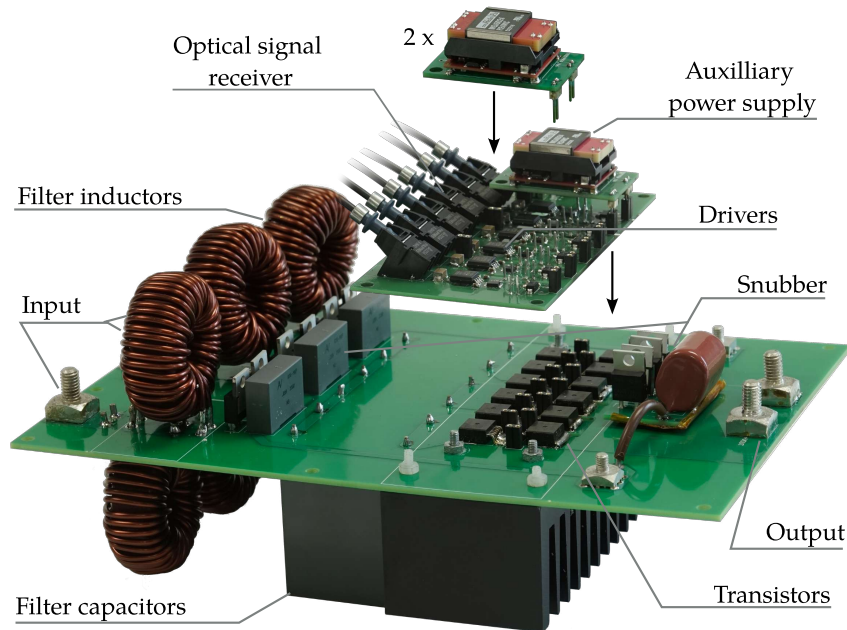


Figure 4.19: Prototype of the three-phase to single-phase matrix converter

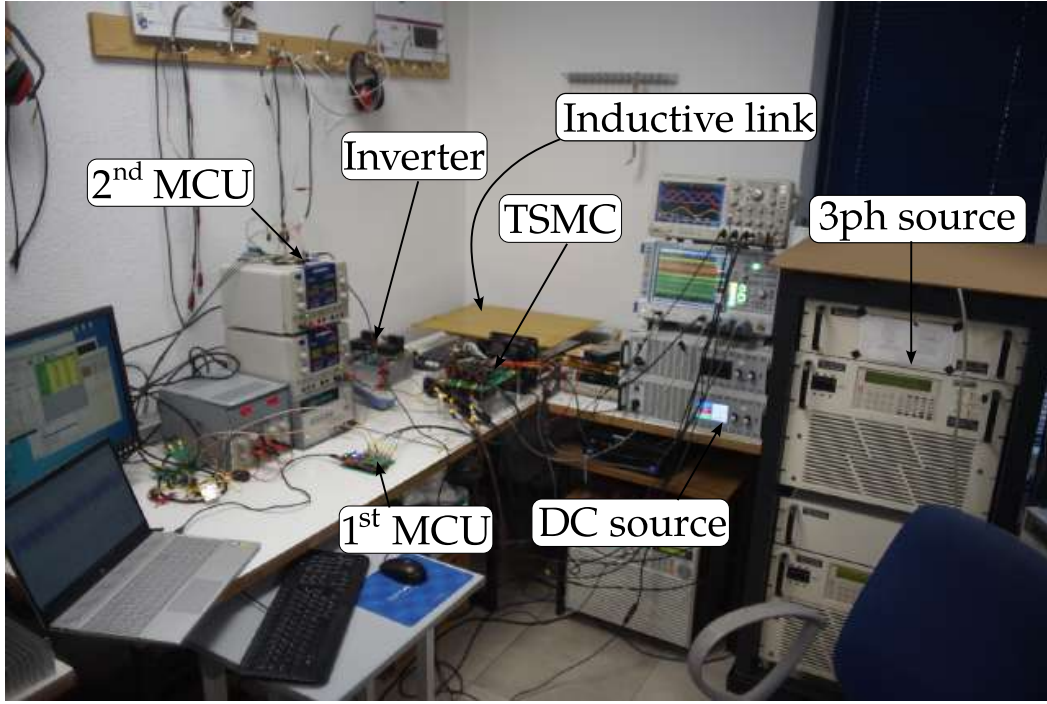


Figure 4.20: Experimental setup

meaning transferred power is 3.47 kW, implying efficiency of the system of 94.3%. In Fig. 4.22 currents and voltages of the TSMC and secondary inverter are given, while Fig. 4.24 shows the voltage and current of phase A of the grid as well as the currents in all three phases of the grid. The THD of the grid currents is 3.2%, which is below the standard defined value of 5%. All of the relevant grid parameters in this case are given in Table 4.3. The power factor of the system is 0.997 which complies with the grid requirements. Calculated breakdown of all of the losses in the system in this particular case is given in Fig. 4.26. Due to the applied compensation, full ZVS on the secondary is achieved, thus the switching losses in the secondary inverter are negligible.

In the second mode of operation, V2G, the grid power represents the transferred power and equals 3.62 kW. The voltage and current of the inverter are equal to 403.8 V and 9.43 A, giving 3.8 kW of input power, which means that the overall efficiency of the system is 95.15%. In order to achieve this efficiency with a classical 4-stage system it would require all 4 stages to have 98.7% efficiency which is hard to achieve, thus this solution presents itself not only being smaller but also more efficient than the classical one. The THD of the grid currents is the same as in G2V mode and equals 3.2%. The power factor is 0.975 which is also compliant with the grid requirements. In this case, Fig. 4.23 depicts the currents and voltages of the TSMC and secondary inverter, while Fig. 4.25 shows the voltage and current of phase A of the grid as well as the currents in all three phases of the grid. All of the relevant grid parameters for the considered test are given in Table 4.4.

Symbol	Quantity	Value
V_{grid}	Grid voltage	3×400 V
f_{grid}	Grid frequency	50 Hz
L_{filt}	Input filter inductor	78 μ H
R_{filt}	Filter inductor resistance	10 m Ω
C_{filt}	Input filter capacitor	11 μ F
C_p	Primary capacitance	429 nF
C_s	Secondary capacitance	97.5 nF
C_t	Tertiary capacitance	78 nF
L_p	Self-inductance of the primary winding	42.44 μ H
L_s	Self-inductance of the secondary winding	69.96 μ H
L_t	Self-inductance of the tertiary winding	24.51 μ H
L_{ps}	Mutual inductance between the primary and secondary winding	22.28 μ H
L_{pt}	Mutual inductance between the primary and tertiary winding	25.64 μ H
L_{st}	Mutual inductance between the secondary and tertiary winding	19.02 μ H
L_{pa}	Added inductance in primary	32.55 μ H
L_{ta}	Added inductance in tertiary	21.57 μ H
R_p	Primary AC resistance at 85 kHz	120.15 m Ω
R_s	Secondary AC resistance at 85 kHz	80.37 m Ω
R_t	Tertiary AC resistance at 85 kHz	85.56 m Ω
$S_1...S_6$	TSMC transistor	NTBG020N090SC1
$Q_{1H}...Q_{2L}$	Secondary inverter transistor	G3R20MT12N
f_{sw}	Switching frequency	85 kHz
V_{batt}	Battery voltage	400 V
L_{inv}	Inverter filter inductor	None
C_{inv}	Inverter filter capacitor	560 μ F
C_{snub}	Total snubber capacitance	4.8 μ F
R_{snub}	Snubber resistance	32 k Ω

Table 4.2: Parameters of the system

Delays introduced by RC filters of the measured grid voltages and utilization of digital controls leads to imperfect execution of the modulation strategy proposed in Section 4.3, thus producing a certain consumption of the 50 Hz reactive power. The nature of this reactive power depends on the power flow in the system. Input filter capacitors inject 548 var into the grid while con-

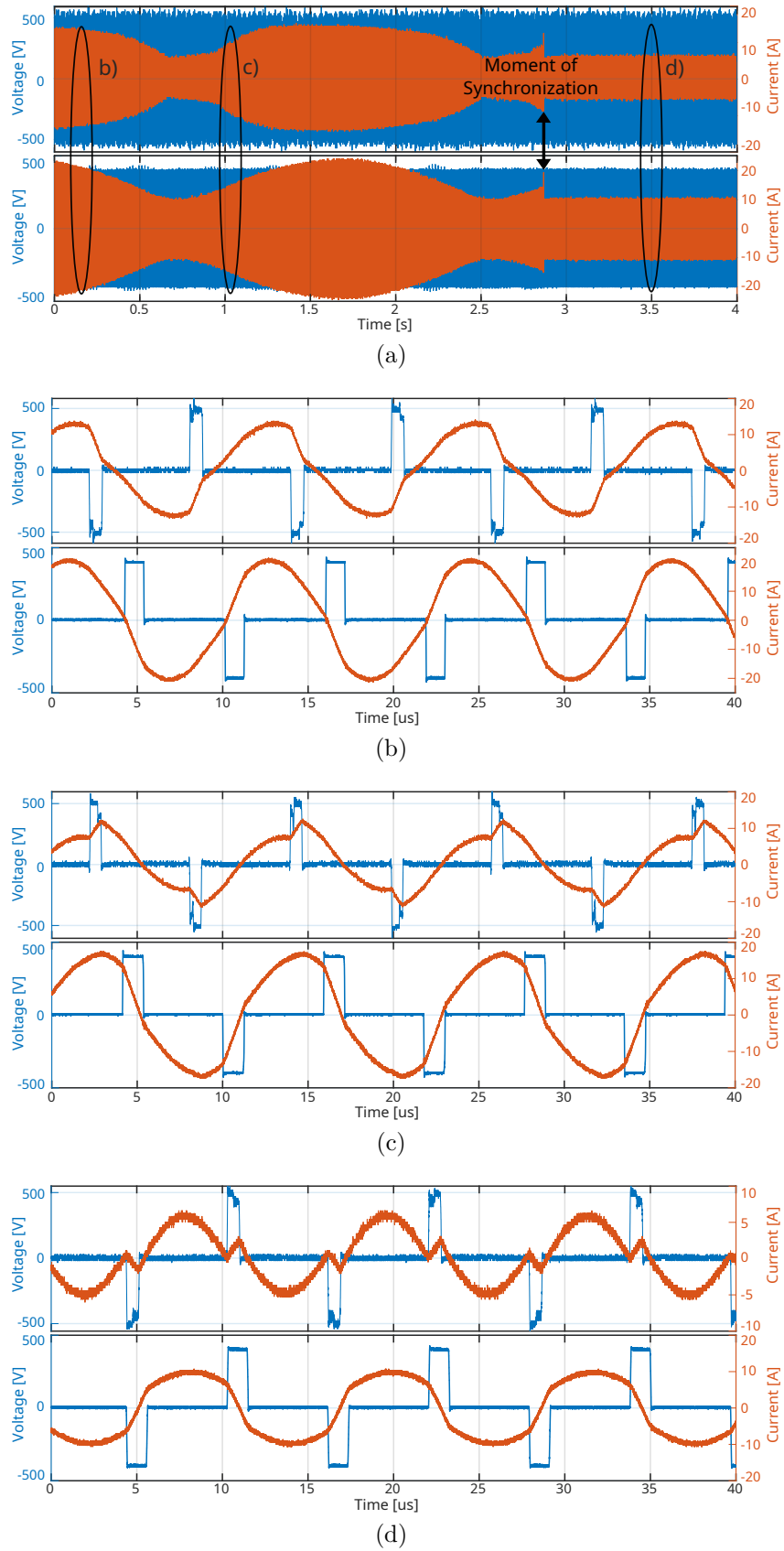
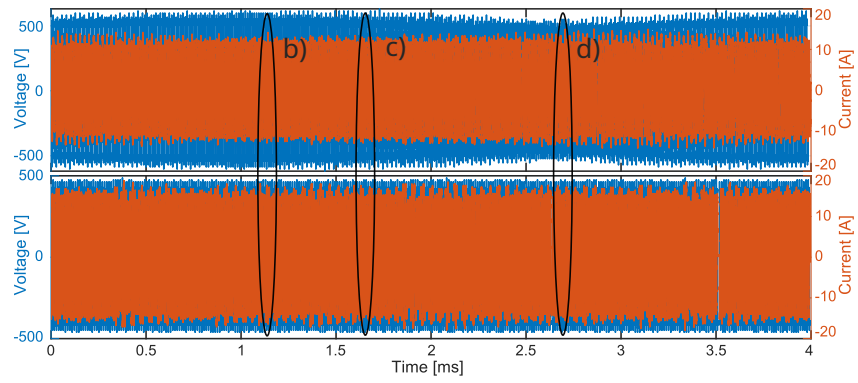
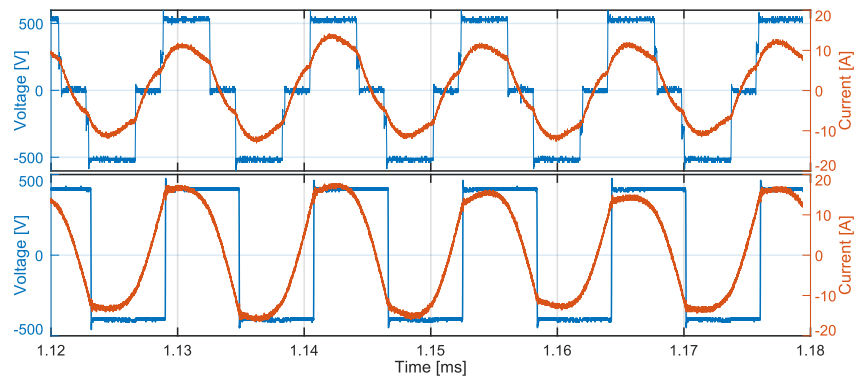


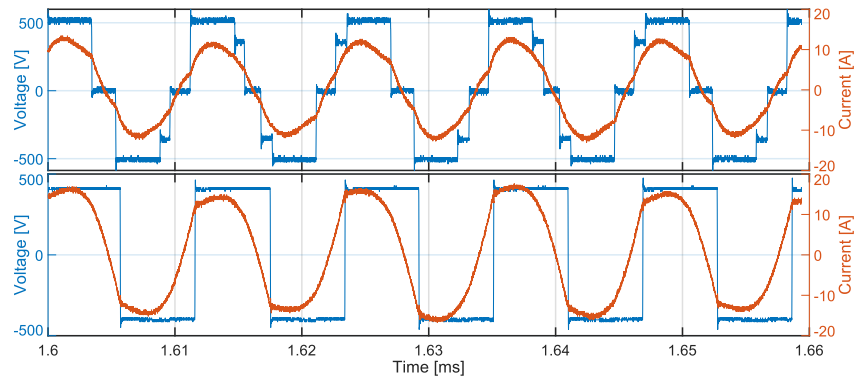
Figure 4.21: Voltage and current of TSMC (top) and inverter (bottom) during the synchronization process



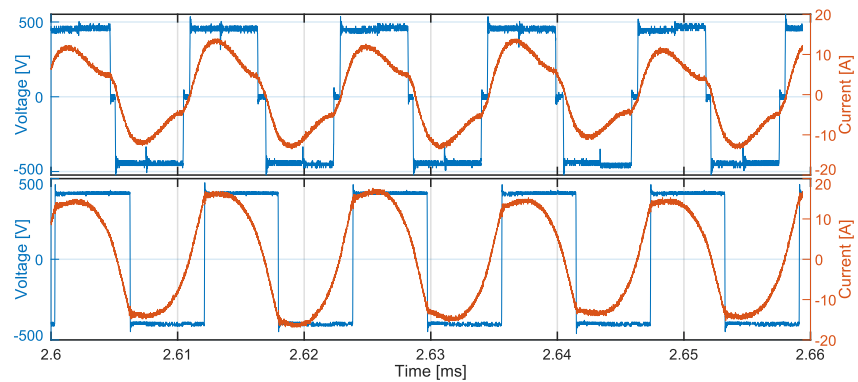
(a)



(b)

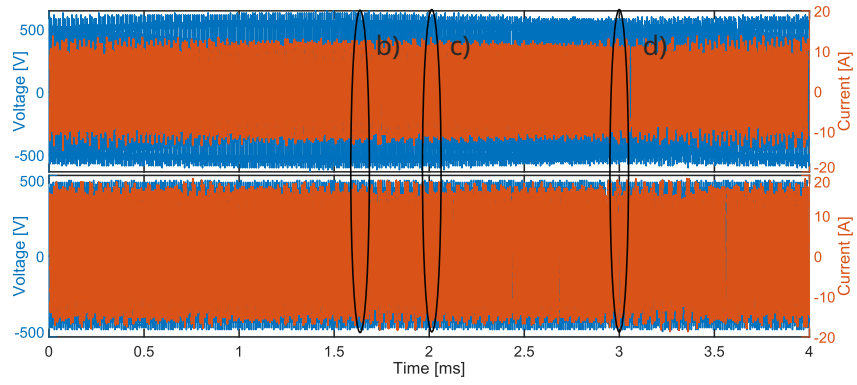


(c)

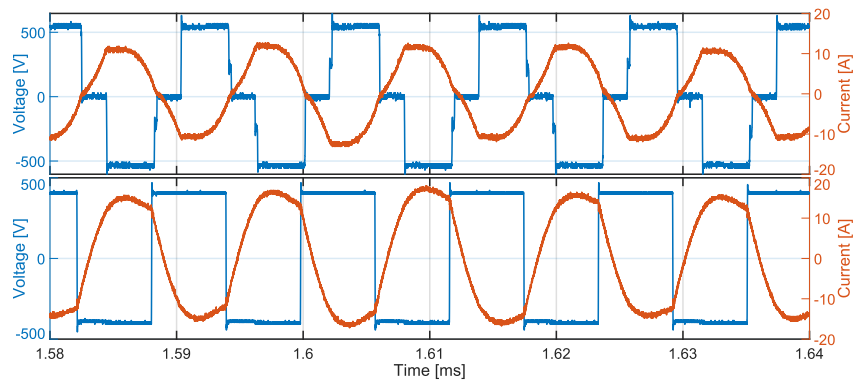


(d)

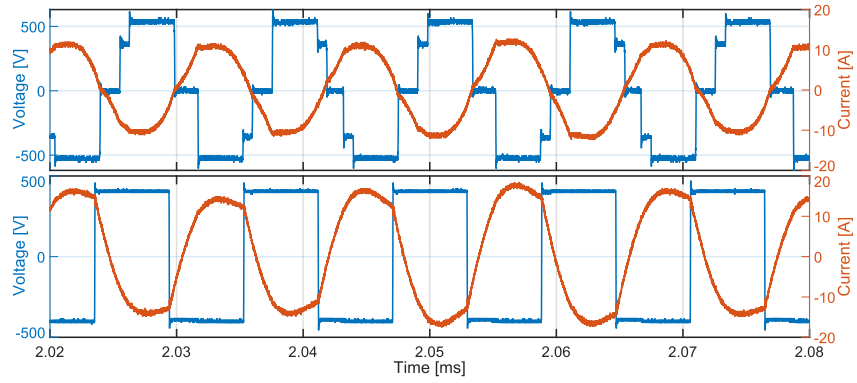
Figure 4.22: Voltage and current of the TSMC (top) and inverter (bottom) for 3.68 kW G2V mode of operation



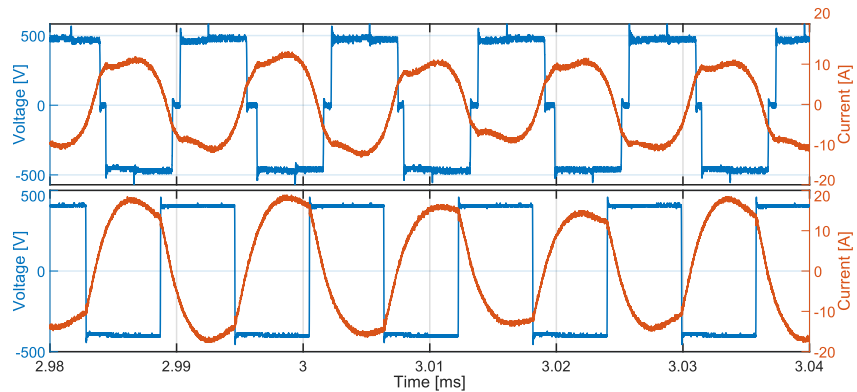
(a)



(b)



(c)



(d)

Figure 4.23: Voltage and current of the TSMC (top) and inverter (bottom) for 3.8 kW V2G mode of operation

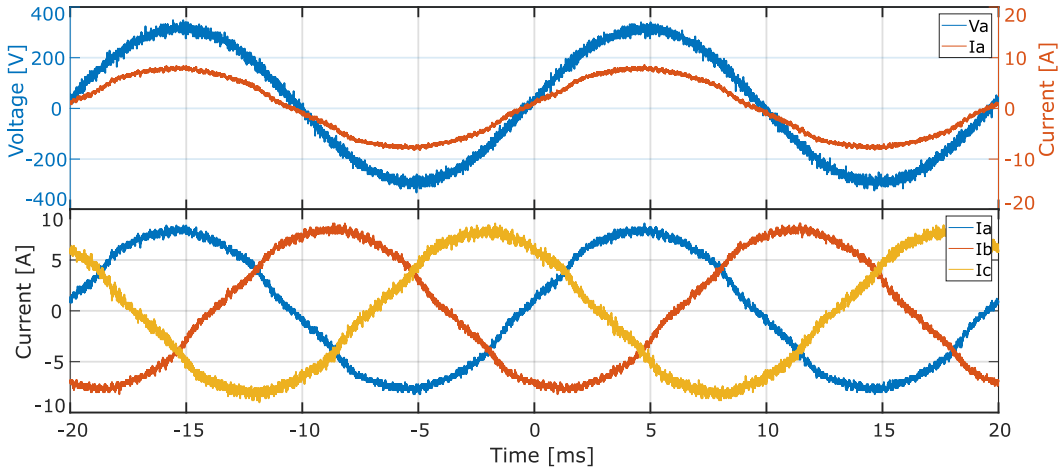


Figure 4.24: Voltage and current of the phase A of the grid (top) and grid currents (bottom) for 3.68 kW G2V mode of operation

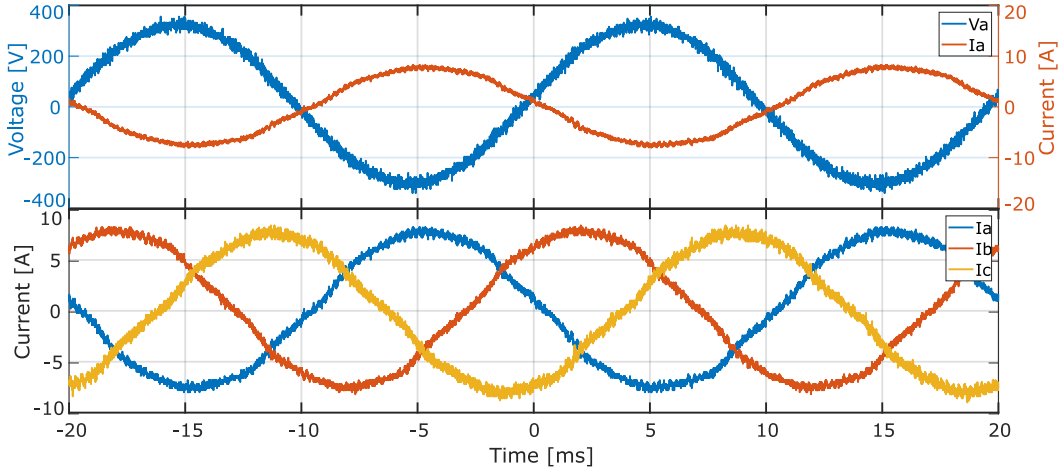


Figure 4.25: Voltage and current of the phase A of the grid (top) and grid currents (bottom) for 3.8 kW V2G mode of operation

sumption of input filter inductors can be neglected. In G2V mode, the reactive power of the matrix converter is inductive in nature, thus it decreases the total reactive power injected into the grid. In V2G the reactive power of the matrix converter is also capacitive, which contributes to more reactive power being injected into the grid. This is used to explain the existing difference in power factor between G2V and V2G modes of operation, and it is verified in the simulation by introducing $200 \mu\text{s}$ of delay into the system.

Table 4.5 compares the proposed work with the existing two-stage three-phase IPT chargers that are present in the literature and that are mentioned in the Introduction chapter of this work. Parameters that are compared are: topology, number of primary semiconductors, compensation strategy of the inductive link, consideration of synchronization between MCUs, bidirectionality, output power, efficiency, THD and PF. As can be seen from the table, number of semiconductor devices in the employed topology is around average

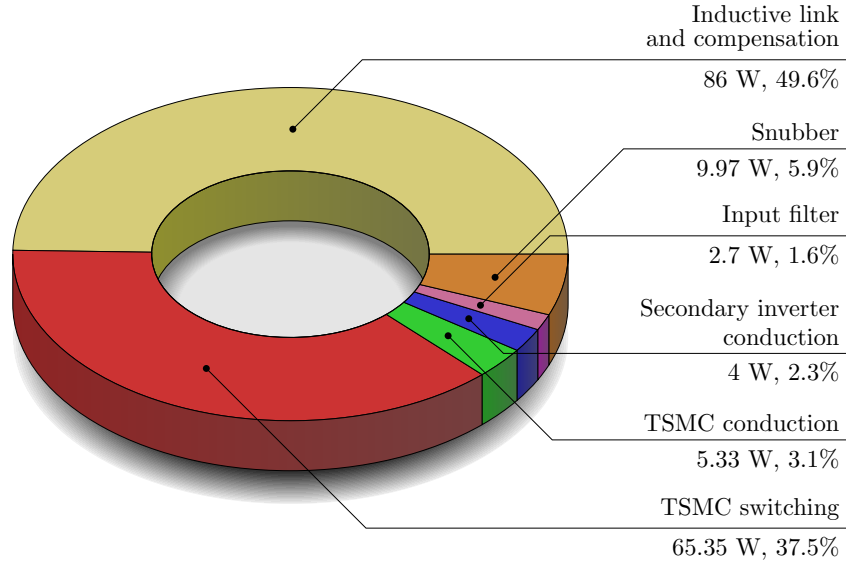


Figure 4.26: Losses breakdown of the system

Parameter	Phase A	Phase B	Phase C
V_{rms} [V]	218.04	218.23	218.31
I_{rms} [A]	5.639	5.620	5.664
P [kW]	1.226	1.223	1.232
Q [var]	-0.091	-0.096	-0.100
I_{thd} [%]	3.266	3.261	3.233
PF	0.997	0.997	0.997

Table 4.3: Relevant parameters of the grid in the G2V mod of operation with 3.68 kW of input power

Parameter	Phase A	Phase B	Phase C
V_{rms} [V]	224.21	224.52	224.69
I_{rms} [A]	5.524	5.494	5.530
P [kW]	-1.207	-1.203	-1.213
Q [var]	-0.277	-0.273	-0.268
I_{thd} [%]	3.272	3.239	3.222
PF	-0.975	-0.975	-0.975

Table 4.4: Relevant parameters of the grid in the V2G mod of operation with 3.8 kW of input power

in the class. TSMC in [74] is realized with 4 four-quadrant switches, i.e. 8 MOSFET devices in total, but the maximum voltage that can be achieved at its output is lower than in the cases of [75], [76], [78] and this work. Solutions [94] and [95] come with low number of semiconductors, however in the case of the first one this is reflected in the higher THD of the grid currents, while the latter one has a rather complex inductive link. From the aspect of

Topology	No. of primary semiconductors	Compensation strategy of the inductive link	MCU synch.	Bidirectional	Output Power	Efficiency	THD	PF
TSMC (Proposed work)	12 MOSFETs	Auxiliary winding and resonant capacitors	Yes	Yes	3.6 kW	95.15%	3.2%	0.975
SWISS-Rectifier based [83]	20 MOSFETs	Double-sided LCC	No	Yes	1.2 kW	95.2%	2.5%	0.993
Oak Ridge Converter [94]	6 MOSFETs	Double-sided LCC	No	No	20 kW	93%	9-10%	0.98-0.99
Integrated 3ph AC-DC [95]	6 MOSFETs	Double-sided LCC	No	No	1.6 kW	91.5%	3.2%	1.0
TSMC [75]	12 MOSFETs	Double-sided LCC	No	Yes	60 W	75.1%	Unk.	Unk.
TSMC [74]	8 MOSFETs	Series-Series	No	No	300 W	85%	Unk.	Unk.
TSMC [78]	7 IGBTs 6 Diodes	Series-Parallel	No	No	267 W	88.2%	14.3%	0.67
TSMC [76]	12 MOSFETs	Series-Series	No	No	2 kW	92.1%	3%	Unk.

Table 4.5: Comparison with other single-stage Three-phase IPT chargers

power, only the solution based on Oak Ridge Converter has reached higher output power. Considering the power level that is reached by the TSMC in this work, this solution can be applied in 3.3 kW charging applications predicted by the standard [24]. As for the efficiency, proposed solution is in the top of the class, with similar efficiency to solution based on SWISS-Rectifier [83]. Another importance of this work is that it is the only one in the class to investigate and discuss the influence of two different MCUs controlling the system, and offer a solution for the problem caused by different clock frequencies of the two MCUs. Also, bidirectionality feature is not commonly encountered in this area, considering that only 3 out of 9 mentioned solutions have it. Inductive link compensation that was employed in this work is not typical for the class, however it provides the desired functionality of the inductive link as explained in Chapter 3. The TSMC topology and the presented modulation could also be used with other compensation strategies, such as widely-adopted double-sided LCC, or simpler ones such as Series-Series. However, if that was the case, synchronization algorithm would be more complex, more similar to ones presented in [88], [89]. From the aspect of THD of the grid currents and power factor, it complies with the grid code, as does the majority of other solutions for which the data of THD and PF are given. Comparing the high-frequency output current of the TSMCs that are present in the table with the output current of the TSMC in this work, the one in this work has slightly higher presence of higher-order harmonics, as the consequence of the employed compensation strategy. When it comes to the data related with the input, i.e. grid currents of the TSMC and their THD and PF, benefits of the novel modulation strategy are clearly visible as the presented TSMC is able to achieve low THD and high PF while being the only one to consider aggravating conditions of having two MCUs controlling different parts of the system.

4.6 Conclusions

Key points of this Chapter are:

1. In order to minimize the number of power conversion stages and increase power density and level of integration, in the bidirectional inductive power transfer system, we have proposed a utilization of the three-phase to single-phase matrix converter. A novel modulation strategy is presented, providing stable power transfer from the grid to the battery, high power factor, and low THD of the currents that are being taken/injected into the grid. Additionally, the modulation of the TSMC contains the flipping pattern that enables processing of both active and reactive power by the matrix converter, whereby the active power is taken from the mains while reactive power is taken from the filtering capacitors.

2. The compensation of the magnetizing inductance based on the third winding and accompanying resonant circuit is implemented as the one suitable for this application. In this way, seamless power flow control is achieved, as well as the increase in overall efficiency of the system. Power flow control and its key problem, the synchronization between the microcontrollers, is considered, and solution is offered in order to demonstrate that the system is possible to realize in a real-life application. Also, a start-up procedure that enables soft start of the system is proposed, avoiding potential failure due to overcurrent conditions.

A prototype of the system has been built in order to demonstrate the functionality of the proposed ideas. A power transfer of 3.6 kW with 95.15% efficiency has been achieved with 3.2% THD of the grid currents and 0.975 PF, thus confirming the applicability, enhanced dynamic performance, and efficiency of the proposed solution.

A Three-Phase Single-Stage IPT System Based on DD²Q Coil Topology

But; there is always a but.

Daniel Rios Linares

UNTIL this point in the Thesis, compensation strategy based on the intermediate coil and a single-stage charger based on TSMC have been presented. In this Chapter, a high-power, three-phase, single-stage IPT EV charger based on DD²Q coil topology, and powered by TSMC is presented. The topology of the TSMC in this Chapter is different than the one in the previous Chapter, thus it will be necessary to propose a suitable modulation strategy. Since the Three-phase to Single-phase Matrix Converter in this Chapter has lower number of semiconductor devices comparing to the one from the previous Chapter, it will be referred to as Reduced Three-phase to Single-phase Matrix Converter (RTSMC). **Contributions** of this Thesis that are presented in this Chapter are:

1. The employed topology of the charger, combining the known benefits of the single-stage topology relying on the RTSMC, with the three-phase DD²Q coil structure. Using the proposed topology, it is possible to have a small front-end converter and a compact IPT structure, allowing for high power density of the system.
2. The modulation strategy for the RTSMC, that allows for low THD of the grid currents and high power factor.

3. The proposed control strategy of the system in case of misalignment, that utilizes both phase-shift and duty cycle control of the primary converter, in order to obtain equal power distribution across the phases, both of the primary and of the secondary sides.

Fig. 5.1 depicts the topology of the considered charger. Each phase of the IPT link is energized using a RTSMC converter. System operates synchronized to the grid, where each RTSMC converter generates a voltage with constant RMS and phase of the 1st harmonic at its output, and distributes its output current across the phases of the grid in the appropriate way to achieve low THD and high PF of the grid currents. IPT link is compensated using a double-sided LCC compensation technique due to its reported high efficiency from the state-of-the-art, although any other compensation strategy can be employed, depending on the desired system behavior, as it was explained in the previous Chapters of the Thesis. On the secondary side there is a half-wave rectifier connected at the output of each of the phases of the inductive link. In this way, phase decoupling is achieved with the least amount of semiconductor devices. Due to the employed compensation technique, system exhibits gyrator behavior, charging the EV battery with a constant current. Inductive link is made using a DD²Q structure, allowing for a compact three-phase IPT system. When transmitter and receiver structures are aligned, there is coupling only between corresponding phases, as it is shown in Fig. 5.1. In this case system behaves as a parallel connection of three independent IPT chargers. Since this charger is intended for EV applications, misalignment between transmitter and receiver structures is expected. This will lead to complex system behavior that will be explained in detail in this Chapter.

In Section 5.1, characteristics of the DD²Q structure are presented. A design methodology for a system that utilizes the considered coupling structure is given in Section 5.2. Section 5.3 disseminates into the proposed converter topology. The modulation of the employed RTSMC is outlined in Section 5.4. The proposed control strategy for power balancing is described in Chapter Section 5.5. Section 5.6 shows the experimental validation of the ideas proposed in this article. Finally, conclusions are given in Section 5.7.

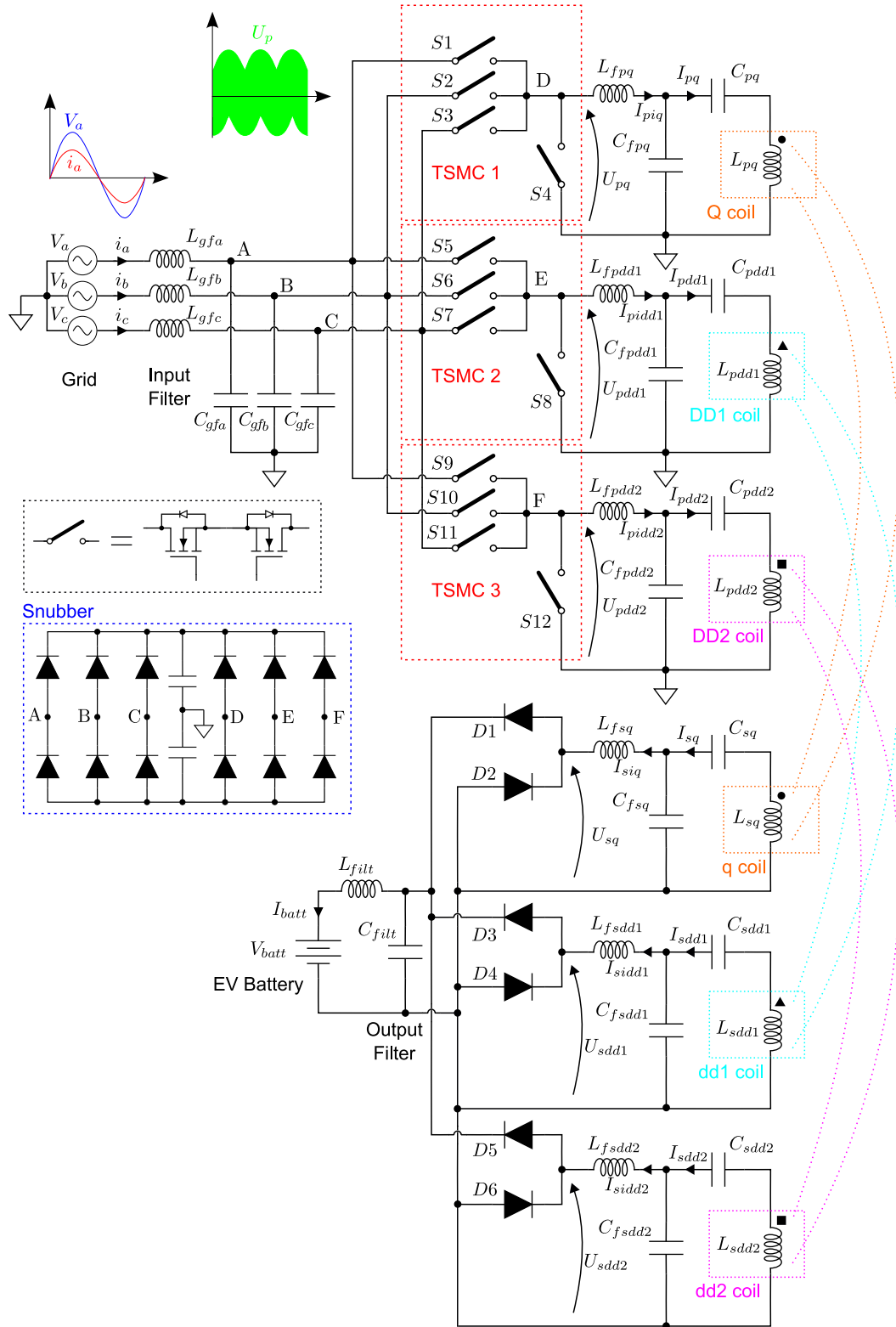


Figure 5.1: Topology of the proposed charger

5.1 DD²Q coil structure

The DD²Q coil structure was already mentioned in Chapter 1. For the reasons of readability, Figures depicting structure and magnetic fields are repeated here. Fig. 5.2a depicts the used DD²Q coil structure. In the proposed system, both transmitter and receiver are constructed in this manner. The given structure has an important property, that the three coils making it, are mutually decoupled. This comes as the consequence of the mutually orthogonal magnetic fields that are produced by each of the coils. Fig. 5.2b gives the overview of the magnetic fields of the DD²Q structure. It is important to note, that all of the compact three-phase IPT structures, that are mentioned in the state-of-the-art, have mutually decoupled coils of the transmitter and receiver structures. This is important as it diminishes any circulating active or reactive power between the coils that are on the same assembly, and allows for higher efficiency of the system. The DD²Q coil structure has several advantages over the other compact structures from the Chapter 1:

1. It is made out of simple and common double D and Q coils, that are comprised by the current SAE standard proposal [24].
2. It can be used both for three-phase charging and single-phase charging.
3. It has the benefit of high coupling coefficient of the Q coil and low stray field of the DD coil [108].
4. Each of the coils utilizes the entire surface of the charging pad, thus maximizing the per-turn inductance of the windings.

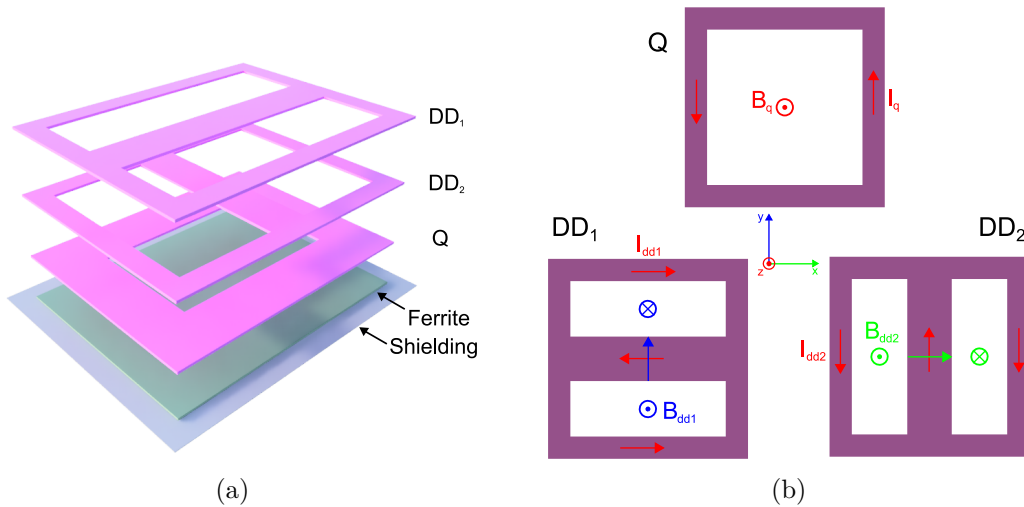


Figure 5.2: a) DD²Q coil structure b) Magnetic fields of the DD²Q coil structure

If the transmitter, i.e., the ground assembly (GA), and the receiver, i.e., the vehicle assembly (VA), are aligned, it is clear that the coupling exist only between the corresponding phases - Q coil of the transmitter will be coupled only to the Q coil of the receiver etc. However, in the EV charging applications a lateral misalignment between the GA and VA is expected. Under these conditions, coupling between the non-corresponding phases will appear, and it is necessary to balance the system. This will be discussed in detail in Section 5.5.

5.2 Design Procedure

In the Fig. 5.3, the flowchart of the proposed design procedure is given. First, the input parameters have to be determined:

1. Dimension constraints for the coils. In the case of this work, the dimensions of the coils are determined based on the current standard proposal SAE J2954, yielding the transmitter size of 650 mmx 500 mm and the receiver size of 400 mm x 400 mm.
2. Clearance between the ground assembly and the vehicle assembly. Targeted class of clearance distances is Z3, meaning that the clearance ranges between 170 mm and 250 mm.
3. Current rating of the Litz wire used for making the coils. The Litz wire used in this work is made out of 3000 strands of 70 μm diameter, yielding 52 A rated current, assuming the current density of 4.5 A/mm².
4. Rated power of the charger which, in the considered case, equals to 12 kW.
5. Nominal DC voltage levels of the primary and of the secondary side. In our case they are both equal to 400 V.
6. Topology of the converter is given in Fig. 5.1. Each phase of the coils is compensated using a double-sided LCC compensation strategy. On the primary side there are three RTSMC converters powering the resonant circuits of each of the phases, while on the secondary sides there are three half-wave diode rectifiers.

According to the annotation from Fig. 5.1, tuning of the compensation network is done in the way to satisfy the following equations:

$$1 = \frac{1}{\omega^2 C_{fpk} L_{fpk}}, \quad k \in \{q, dd1, dd2\} \quad (5.1)$$

$$1 = \frac{1}{\omega^2 C_{fsk} L_{fsk}}, \quad k \in \{q, dd1, dd2\} \quad (5.2)$$

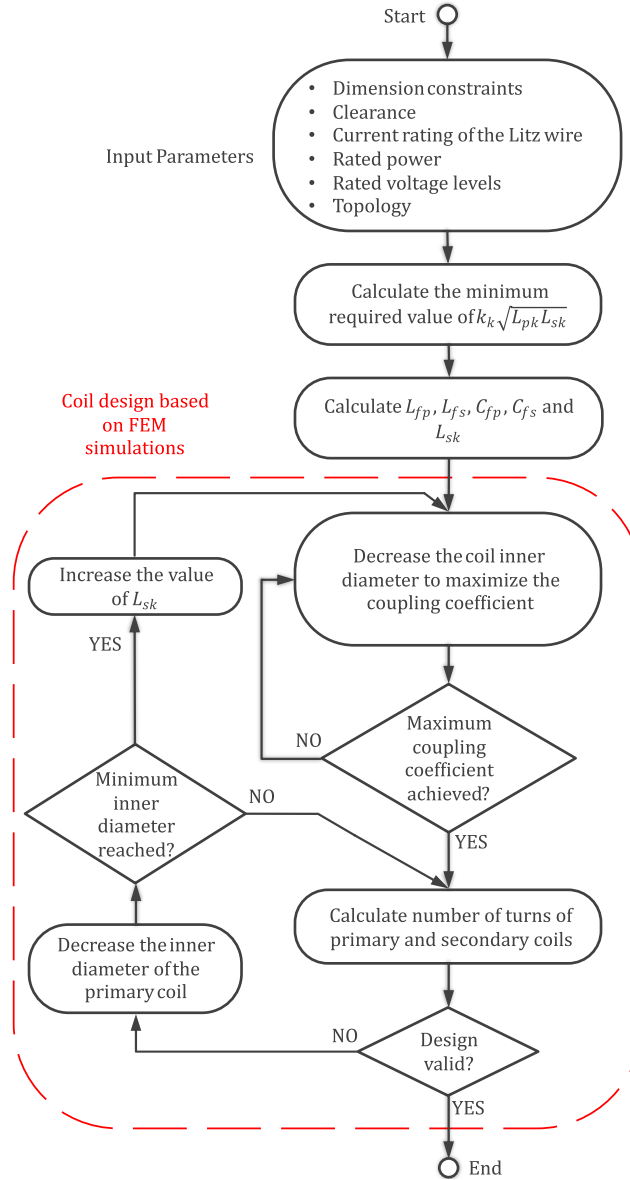


Figure 5.3: Design procedure flowchart

$$1 = \frac{1}{\omega^2 C_{pk} (L_{pk} - L_{fpk})}, \quad k \in \{q, dd1, dd2\} \quad (5.3)$$

$$1 = \frac{1}{\omega^2 C_{sk} (L_{sk} - L_{f sk})}, \quad k \in \{q, dd1, dd2\} \quad (5.4)$$

System compensated using a double-sided LCC compensation strategy exhibits behavior of a current source at the output for a voltage-fed input as it was explained in the Chapter 2. Values of the currents that are marked in Fig 5.1 are determined via the following relations:

$$\underline{I}_{pk} = j \underline{U}_{pk} \omega C_{fp}, \quad k \in \{q, dd1, dd2\} \quad (5.5)$$

$$\underline{I}_{sk} = -j \underline{U}_{sk} \omega C_{fs}, \quad k \in \{q, dd1, dd2\} \quad (5.6)$$

$$\underline{I}_{pik} = j\underline{U}_{sk}\omega^3 C_{fs}C_{fp}M_{psk}, k \in \{q, dd1, dd2\} \quad (5.7)$$

$$\underline{I}_{sik} = -j\underline{U}_{pk}\omega^3 C_{fs}C_{fp}M_{psk}, k \in \{q, dd1, dd2\} \quad (5.8)$$

Active power that is being transferred via each phase is given with the following equation:

$$P_k = \text{Re}\{j\underline{I}_{pk}\underline{I}_{sk}\omega M_{psk}\} = I_{pk}I_{sk}\omega M_{psk}, k \in \{q, dd1, dd2\} \quad (5.9)$$

Once the input parameters are determined, power per phase is determined as one third of the rated power. From the equation (5.9) it follows that the power level is proportional to the mutual inductance. The mutual inductance M_{psk} is given with:

$$M_{psk} = k_k \sqrt{L_{pk}L_{sk}}, k \in \{q, dd1, dd2\} \quad (5.10)$$

In order to fully utilize the copper cross-section of the Litz wire, the RMS values of the 1st harmonic currents are chosen to correspond to the rated current of the Litz wire $I_{pk}^{max} = I_{sk}^{max} = 52 \text{ A}$, $k \in \{q, dd1, dd2\}$. Each phase is intended to deliver one third of the rated power. From this, it is possible to calculate the necessary value of the product:

$$k_k \sqrt{L_{pk}L_{sk}} = P_{rat}/(3I_{pk}I_{sk}\omega), k \in \{q, dd1, dd2\} \quad (5.11)$$

Because all of the coils are made out of the same wire, values L_{fp} and L_{fs} are chosen the same for all of the phases. They can be calculated from the following equations:

$$L_{fp} = V_p^{max}/\omega I_{pk}^{max}, k \in \{q, dd1, dd2\} \quad (5.12)$$

$$L_{fs} = V_s^{max}/\omega I_{sk}^{max}, k \in \{q, dd1, dd2\} \quad (5.13)$$

C_{fp} and C_{fs} are calculated from the equations (5.1) and (5.2). To determine the values of C_{pk} and C_{sk} it is necessary to design the IPT link first. Being that the different coils have different coupling coefficients, it is necessary to design each phase separately. Now comes the iterative process of designing each of the coils [123], [127]. During this process finite element analysis software has to be used. In this work we have used ANSYS MAXWELL. The receiver is designed with the lowest possible self-inductance values being that in this way we add the least amount of weight to the vehicle. With the chosen compensation topology this is determined by the following inequality:

$$L_s > L_{fs} \quad (5.14)$$

The goal is to maximize the coupling factor by tuning the inner diameters of the windings. Once the maximum coupling factor is obtained and the coil

inner diameters are fixed it is possible to determine the number of turns of the secondary coils. Necessary self-inductance of the primary coil for each of the phases is calculated from equation (5.11), thus the number of turns of the each of the phases of the primary is obtained.

Design is considered valid if it is possible to construct all of the primary and secondary coils with the number of turns that have been determined, and in that case the designing process is finished. Otherwise, it is necessary to decrease the coupling factor by decreasing the inner diameter of the winding, thus achieving more space to make the required turns. If the inner diameter has been reduced to 0 and it is still not possible to make the primary winding, than the value of the secondary self-inductance is increased and the iterative process is done once again. Having in mind that each phase handles one third of the rated power, the values of self-inductances of primary and secondary coils are three times lower compared to the single-phase solution and easier to be achieved, thus significantly facilitating the given iteration process. For the system that is considered in this work, parameters of the system in the end of the designing stage are given in Table 5.1.

Parameter	Value	Parameter	Value
L_{pq}	29.8 μH	L_{sq}	13.9 μH
L_{pdd1}	47 μH	L_{sdd1}	22 μH
L_{pdd2}	45 μH	L_{sdd2}	21.2 μH
C_{pq}	157 nF	C_{sq}	1.53 μF
C_{pdd1}	88.7 nF	C_{sdd1}	337.4 nF
C_{pdd2}	93.5 nF	C_{sdd2}	365.6 nF
C_{fp}	468 nF	C_{fs}	302 nF
L_{fp}	7.49 μH	L_{fs}	11.61 μH

Table 5.1: Simulated parameters of the considered IPT system

5.3 Proposed converter topology

The main goal of this Chapter is to propose both converter and structure topology for a single-stage, three-phase IPT charger for EV applications. Once the coil topology is selected, it is necessary to select the converter topology that will energize the coils. As it will be explained in the Chapter 5.6, the selected converter topology has to be able to provide independent control of each phase of the three-phase charger. In this Thesis, we have decided to choose a direct matrix converter based topology being that is one of the most common AC/AC topologies that can be encountered, and for its known benefits of lack of the bulky DC link capacitors, small input filter interfacing the grid [90], [128] and relatively low number of utilized semiconductors comparing to some other proposed solutions, for this type of application [35].

Fig. 5.4 shows the commonly encountered direct matrix converter topolo-

gies from the state-of-the-art. It is assumed that each phase of the IPT link is energized with a separate converter of a certain type. The matrix converter shown in Fig. 5.4a utilizes 6 four quadrant switches. As it has the highest number of semiconductors it can achieve the highest constant RMS value of its output voltage. If this topology is used, it is possible to maintain the RMS value of the matrix converters output voltage, and to have constant power transfer across each phase of the IPT link. Power of each of the phases of the IPT link is equally distributed over the three phases of the grid.

Topology depicted in Fig. 5.4b has 4 four quadrant switches. It can achieve constant RMS of its output voltage, with the highest value being 2.2 times smaller than the highest value of the output voltage of the previous configuration. Also, as it will be shown in the following Chapter, for the desired functionality of this topology, one of the switches will commute with the two times higher frequency from the one of the output voltage. Power that is being transferred across one phase of the IPT link is constant, it is uniformly distributed across the phases of the grid, as well as the total power of all three phases is.

Previous two topologies can both be characterized as TSMC. The topologies shown in Fig. 5.4c and 5.4d can be regarded as Single-phase to Single-phase Matrix Converter (SSMC). The given SSMC topologies differ in the number of switches and by that in the RMS value of the output voltage. However, neither of them cannot have a time-invariable value of the output voltage, rather the value of the output voltage they can achieve is determined by the voltage of the phase of the grid that the given converter is connected to. From this fact follows that the power that is being transferred per phase of the IPT link is not constant, rather it is pulsating with the frequency equal to twice the grid frequency, and, above that, in order to achieve PFC, the instantaneous power needs to be proportional to the absolute value of phase voltage of the grid. All of the previous data is summarized in the Table 5.2.

Being that the chosen topology will be used for energizing all three phases of the IPT link it is desirable to reduce the number of employed semiconductors. Also, the entire system is intended to function under misalignment co-

Topology	Switches per phase	Total number of switches	RMS of the output voltage	Constant power flow
TSMC I (TSMC)	6	18	Constant - Max. 490 V	Yes
TSMC II (RTSMC)	4	12	Constant - Max. 220 V	Yes
SSMC I	4	12	Variable 0 V - 292 V	No
SSMC II	2	6	Variable 0 V - 146 V	No

Table 5.2: Comparison of the topologies from Fig. 3

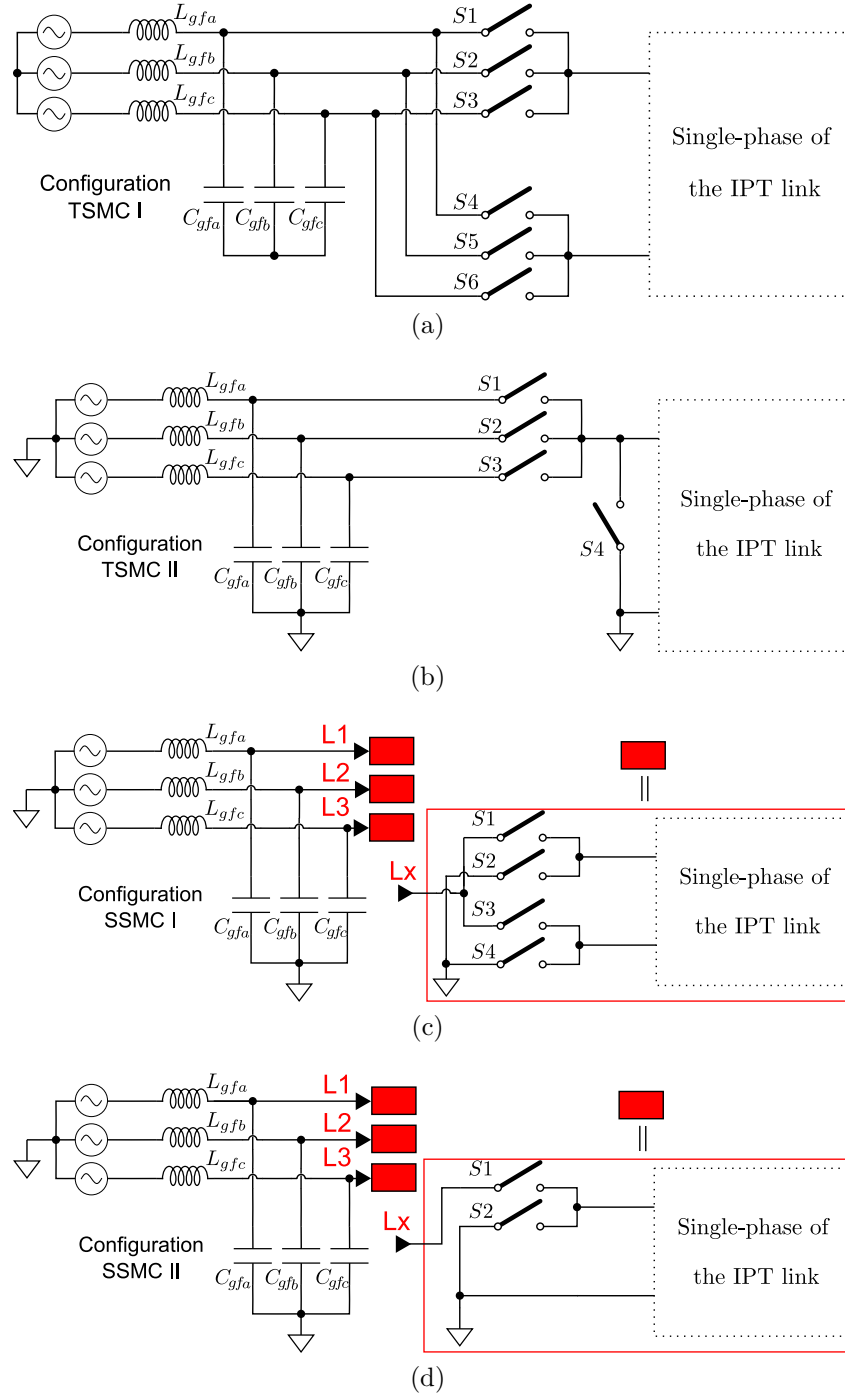


Figure 5.4: Direct Matrix Converter Topologies a) TSMC - 6 switches b) RTSMC - 4 switches c) SSMC I - 4 switches d) SSMC II - 2 switches

nditions. Not being able to arbitrarily choose the power level in a certain phase of the IPT link, would introduce difficulties to the control algorithm. For these reason, the topology shown in Fig. 5.4b is chosen for interfacing the grid.

On the secondary side, at the output of the resonant link, each phase has a half-wave diode rectifier. Reason for choosing this topology on the secondary is because it offers rectification of a sinusoidal current with the minimal number of semiconductor devices, while maintaining complete independence between the different phases of the system. Namely, if a typical three-phase diode rectifier topology were used, there voltages marked on Fig. 5.1 U_{sq} , U_{sdd1} and U_{sdd2} would be dependent not only on the current of the corresponding phase but also on the current of another one, making the system control more challenging.

System operates in a way that the RTSMC that interfaces the grid, generates a high-frequency voltage waveform utilizing certain combination of the grid voltages, with constant RMS and phase of the 1st harmonic over time. Combination of the utilized grid voltages depends on their instantaneous value in the moment of generating the output voltage. This voltage will cause a current on the secondary side that is proportional to the excitation primary voltage and that is rectified by the secondary diode bridge. In the same way that primary voltage causes secondary current, secondary voltage will cause primary current, that will be dominantly sinusoidal due to the resonant nature of the circuit. This sinusoidal current is distributed across the phases of the grid in accordance to the instantaneous values of the grid voltages, so that the high PF and low THD of the grid currents is achieved.

For the selected topology it is recommended to utilize a protective diode snubber as it is shown in Fig. 5.1 [126], [129]. This is done to provide a free-wheeling path for the converters output current during the commutation process and protect switches from the potential over-voltage. For the selected topology it is necessary to use a different snubber topology than the ones presented in [126], [129]. The input three-phase diode rectifier that is connected to the grid as shown in Fig 1, determines the DC snubber voltages that will be used for clamping. Fig. 5.5 depicts the role of the used diode snubber during the commutation process. The commutation between phase A and phase B is shown. It is assumed that the output current is positive. During the dead-time, while both S1 and S2 are open, the output current closes through the diode D8 as it is shown in Fig. 5.5b, clamping the output voltage to the voltage of the snubber capacitor. The incremented charge of the snubber capacitor during this period, will dissipate once the switch S2 turns on, as it is shown in Fig. 5.5c. If the output current was negative, process would be the same, only diode D7 and the upper snubber capacitor would take part in the clamping process instead of D8 and lower capacitor.

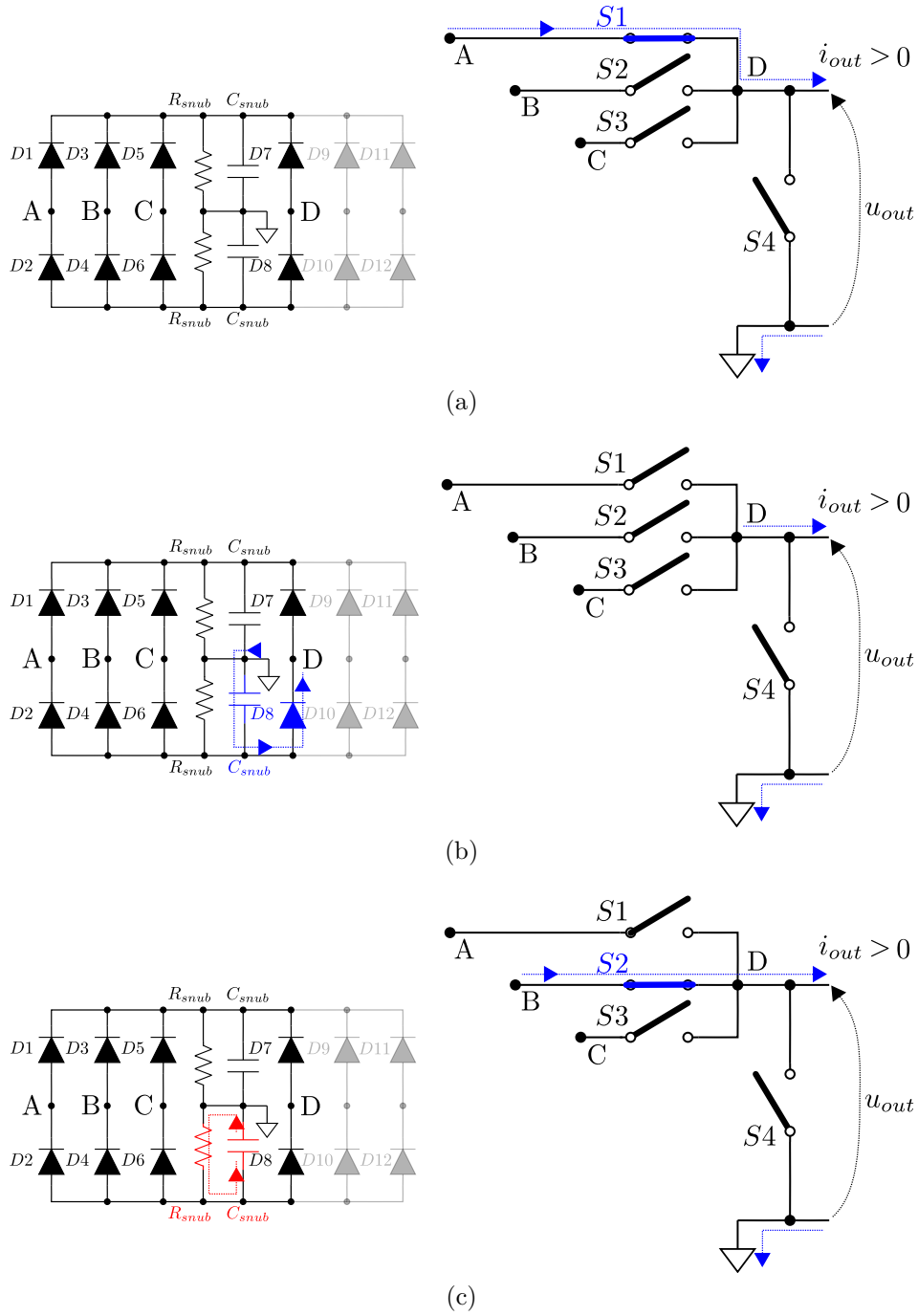


Figure 5.5: Functionality of the snubber circuit during the commutation process between switches $S1$ and $S2$

5.4 Modulation strategy of the RTSMC

When determining the modulation of the considered RTSMC, first it is necessary to define the tasks that the modulation needs to complete. In the case of this Thesis, there is a total of 2 tasks that the RTSMC needs to accomplish:

1. Ensure constant power flow from the grid to the EV battery.
2. Ensure compliance of the converter with the grid code, i.e., ensure low THD of the grid currents and high power factor.

Active power that is being transferred across one phase of the IPT link is given with equation (5.9). Currents I_{pk} and I_{sk} for $k \in \{q, dd1, dd2\}$ are directly proportional to the primary and secondary voltages U_{pk} and U_{sk} as it is given in equations (5.5) and (5.6). If we assume that the battery voltage is constant in the interval of time that is the same order of magnitude as the switching period, it is clear that to have a constant power flow it is necessary to have a constant RMS of the first harmonic of the RTSMC's output voltage. As it will be shown later in this Chapter, phase of the each of the secondary voltages, in general case, is influenced by all of the voltages of the primary. In order to have constant power flow and to avoid any potential power fluctuations, task of maintaining the constant phase of the first harmonic of the RTSMC's output voltage is added. These are the same tasks as were for the modulation of the TSMC in the previous Chapter. What is different is the converter topology and the voltages that are at ones disposal, making the entire modulation different to the one that is already presented.

The employed converter contains 4 bidirectional switches. Three of those

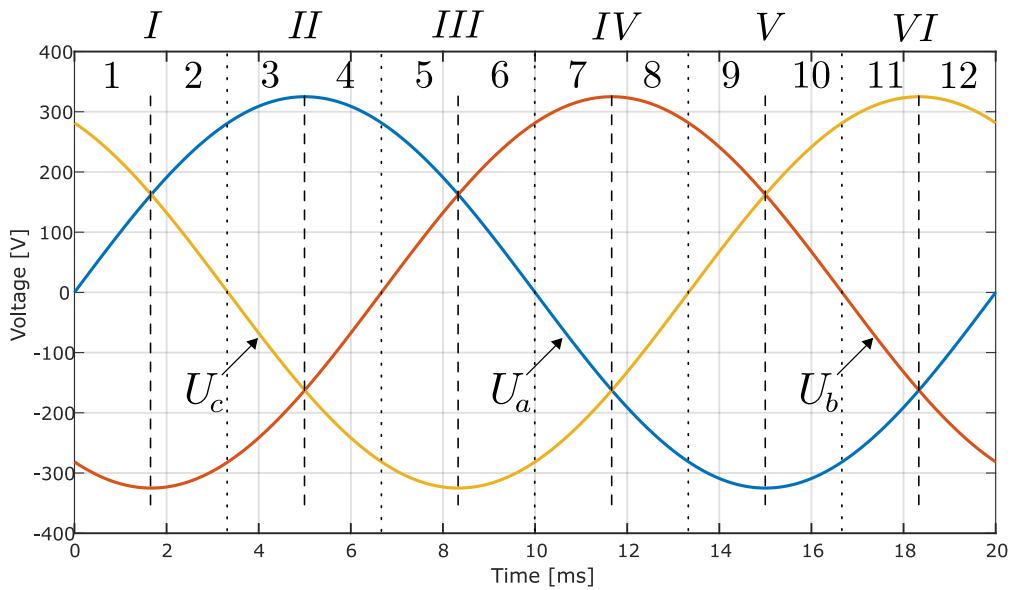


Figure 5.6: Grid voltages over a single period with division to 6 Sectors and 12 Sections

switches connect one pole of the RTSMC's output to each of the three phases of the grid. The other pole of the RTSMC's output is connected to the neutral point of the grid. The fourth bidirectional switch is used for short-circuiting the RTSMC's output. This means that it is possible to achieve four different voltage levels at the output of each RTSMC. Grid voltage over a single grid period are given in Fig. 5.6. Period is divided into 6 Sectors and 12 Sections. During each switching period all of the grid voltages are utilized. Depending on the parity of the actual Sector of the grid, there are two possible patterns for generating the output voltage of the RTSMC that are given in Fig. 5.7. In the case of actual Sector being odd, pattern for generating RTSMC's output

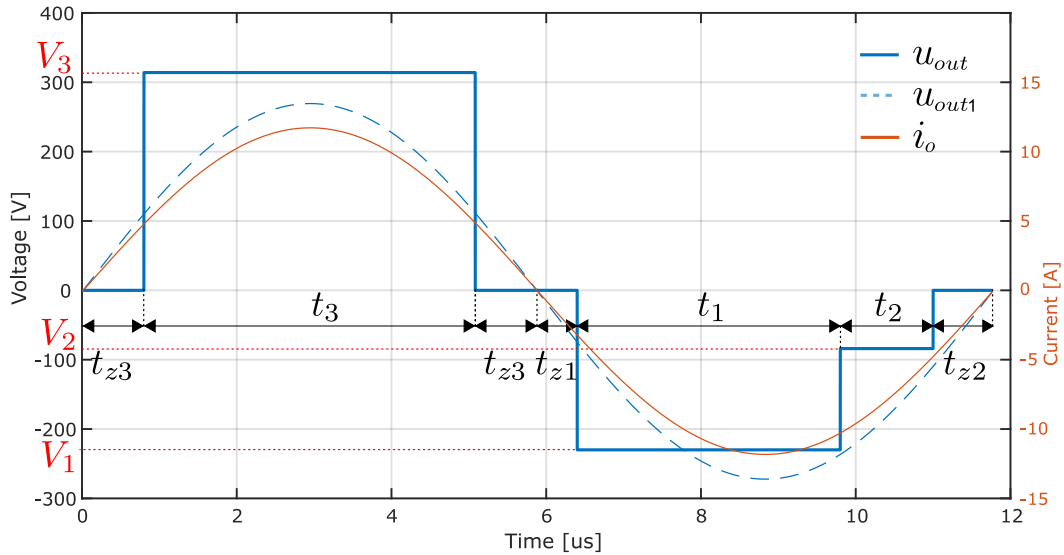
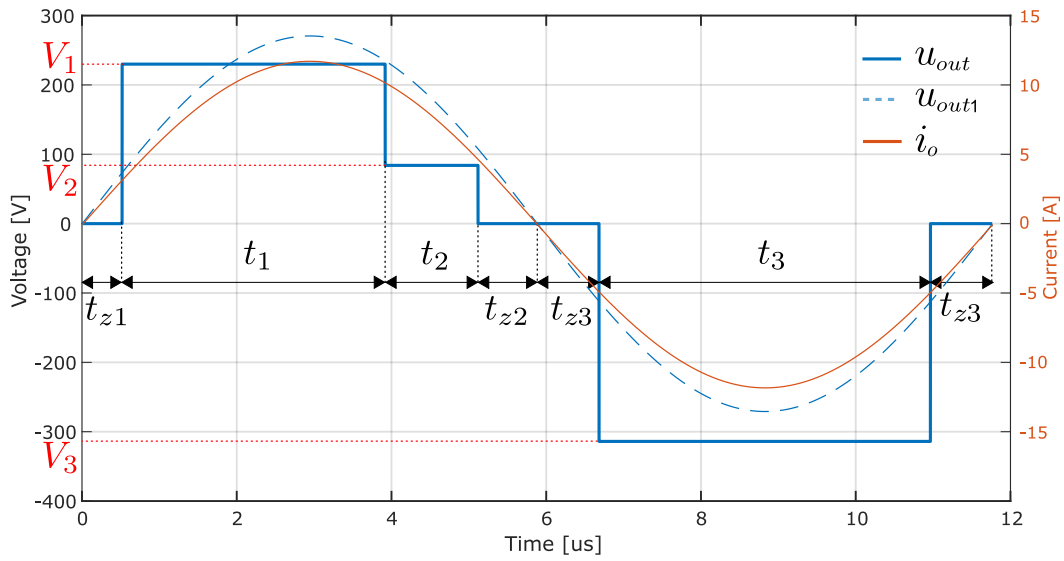


Figure 5.7: Output voltage waveform of a single RTSMC and its first harmonic a) Odd Sectors b) Even Sectors

voltage is given in Fig. 5.7a, while in the case of Sector being even, pattern from Fig. 5.7b is used. As it was noted before, maintaining a constant phase of the first harmonic of the secondary voltage is necessary to avoid potential fluctuations of active power. For the reason of simplicity, it is defined that the desired phase of the first harmonic of the RTSMC's output voltage is equal to zero, as it is shown in Figs 5.7a and 5.7b. The goal of the derivation of the modulation is to determine time values $t_1, t_2, t_3, t_{z1}, t_{z2}, t_{z3}$ in for the modulation to accomplish two task stated in the beginning of this section. Without loss of generality, we shall derive the mentioned time values for Sector I, Section 1 of the grid period. Due to symmetricity of the grid voltage waveforms, it is sufficient to calculate given time values in only one Section of one Sector, and then, it is possible apply them to other Sections and Sectors by correctly connecting them with the adequate grid voltages.

Fig. 5.8 shows switching states during one period of the RTSMC's output voltage for Sector I, Section 1. From the given switching states it is possible to notice that during one period of the RTSMC's output voltage, switch S_4 performs two commutations, meaning that it is switching at double the frequency of the shown voltage. This fact, together with the fact that the maximum RMS value of the output voltage is $\sqrt{3}$ times less than the one of the TSMC as it was shown in Table 5.2, can be considered trade-offs for the RTSMC having 2/3 of the total semiconductor devices of the TSMC topology.

Voltage levels V_1, V_2, V_3 that are marked in Fig. 5.7b, that correspond to Sector I, Section 1 are given by the following equations:

$$V_1 = U_c = U_L \sin(2\pi/3 + \theta) \quad \theta \in [0, \pi/6] \quad (5.15)$$

$$V_2 = U_a = U_L \sin(\theta) \quad \theta \in [0, \pi/6] \quad (5.16)$$

$$V_3 = U_b = U_L \sin(-2\pi/3 + \theta) \quad \theta \in [0, \pi/6] \quad (5.17)$$

where U_L is amplitude of the grid line voltage and θ is the angle that describes the used voltages in each instant of the considered Section. Having in mind the order of magnitude of the switching frequency (85 kHz) and the grid frequency (50 Hz), it is possible to consider these voltage values constant over a single period of the RTSMC's output voltage. Similar to the derivation in Chapter 4, the considered interval of θ can be discretized into n small segments $[\theta_0, \theta_1, \dots, \theta_i, \dots, \theta_n]$, $\theta_i = i\pi/6n$, where the grid voltages can be considered constant. In order to obtain the six unknown time values $t_1, t_2, t_3, t_{z1}, t_{z2}, t_{z3}$, system will be analyzed on one of the segments θ_i of the previously mentioned interval.

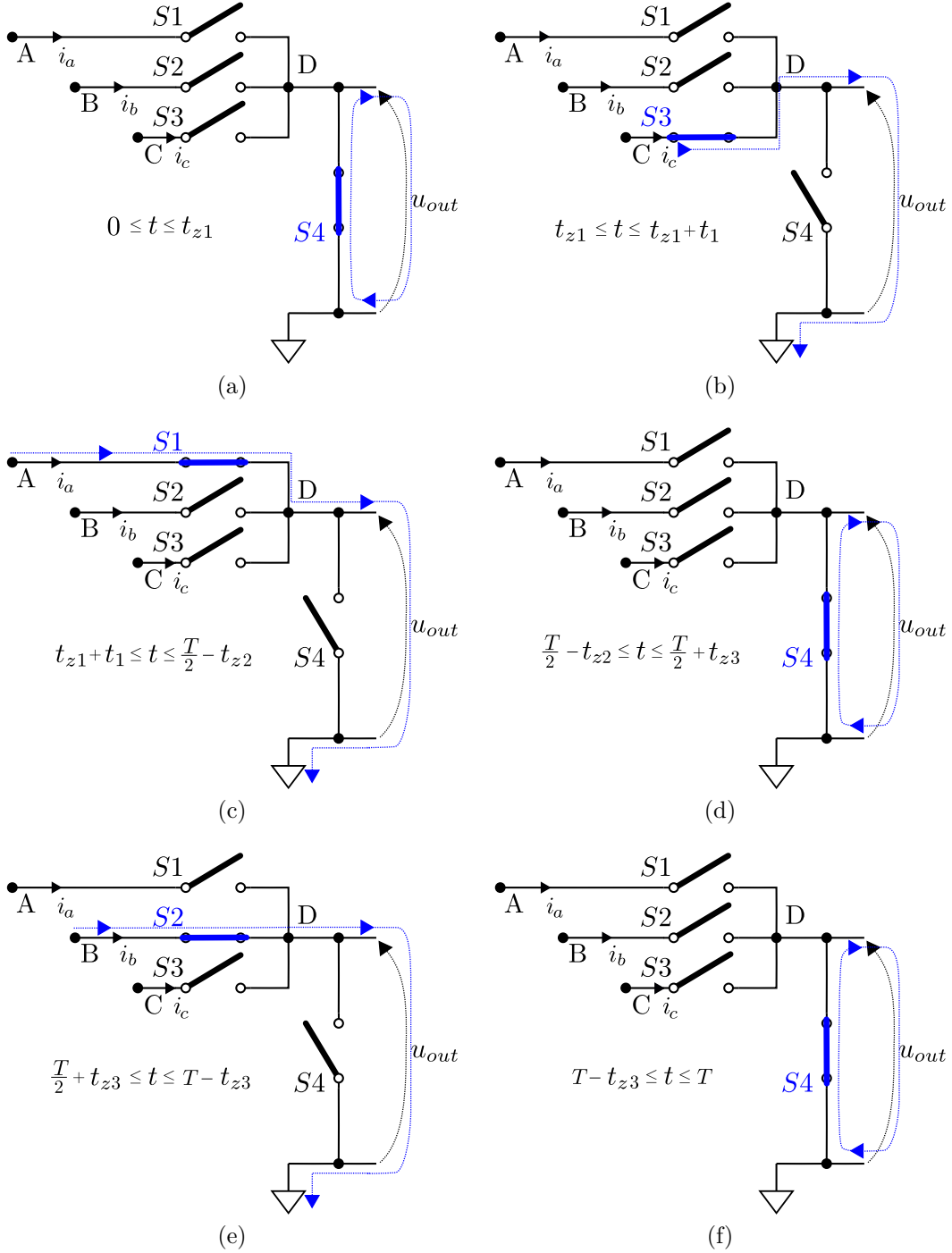


Figure 5.8: Switching states during one period of the RTSMC's output voltage for Sector I, Section 1

Based on the converter switching states that are given in Fig. 5.8, it is possible to write equations relating the grid currents to the output current of the RTSMC, and the output voltage of the RTSMC to the grid voltages:

$$\left. \begin{array}{l} i_a = i_b = i_c = 0 \\ u_{out} = 0 \end{array} \right\} t \in [0, t_{z1}] \cup [T/2 - t_{z2}, T/2 + t_{z3}] \cup [T - t_{z3}, T] \quad (5.18)$$

$$\left. \begin{array}{l} i_a = i_b = 0 \\ i_c = i_o \\ u_{out} = U_c \end{array} \right\} t \in [t_{z1}, t_{z1} + t_1] \quad (5.19)$$

$$\left. \begin{array}{l} i_b = i_c = 0 \\ i_a = i_o \\ u_{out} = U_a \end{array} \right\} t \in [t_{z1} + t_1, T/2 - t_{z2}] \quad (5.20)$$

$$\left. \begin{array}{l} i_a = i_c = 0 \\ i_b = i_o \\ u_{out} = U_b \end{array} \right\} t \in [T/2 + t_{z3}, T - t_{z3}] \quad (5.21)$$

From the previous equations it is possible to calculate the average values of the grid currents during one period of the RTSMC's output voltage:

$$i_a = (1/T) \int_{t_{z1}+t_1}^{t_{z1}+t_1+t_2} i_o(t) dt \quad (5.22)$$

$$i_b = (1/T) \int_{T/2+t_{z3}}^{T-t_{z3}} i_o(t) dt \quad (5.23)$$

$$i_c = (1/T) \int_{t_{z1}}^{t_{z1}+t_1} i_o(t) dt \quad (5.24)$$

In order to be able to calculate the grid currents, it is necessary to have knowledge about the output current of the RTSMC. For this derivation, we shall assume that it is sinusoidal and purely active, i.e, in phase with the first harmonic of the RTSMC's output voltage as it is shown in Fig. 5.7.

$$i_o = I \sin(\omega t) \quad (5.25)$$

To achieve low THD of the grid currents it is required that each of them is proportional to its corresponding grid voltage. From this fact following equations are obtained:

$$U_a(\theta_i)/U_b(\theta_i) = i_a/i_b \quad (5.26)$$

$$U_a(\theta_i)/U_c(\theta_i) = i_a/i_c \quad (5.27)$$

Contrary to the derivation from the last Chapter, previous two equations are not equivalent as, in the case of the considered system, equation:

$$i_a + i_b + i_c = 0 \quad (5.28)$$

is not necessarily satisfied as the connection to the neutral exists and is utilized for achieving the desired system operation.

Two equations are defined with the given tasks of the modulation that are related to the RMS of the 1st harmonic of RTSMC's output voltage and its phase. These conditions can be expressed in the best way using the sine and cosine arguments of the Fourier transform of the TSMC's output voltage that is shown in Fig. 5.7.

$$V_{RMS} = (1/\sqrt{2}T) \int_0^T u_{out}(t) \sin(\omega t) dt \quad (5.29)$$

$$0 = (1/\sqrt{2}T) \int_0^T u_{out}(t) \cos(\omega t) dt \quad (5.30)$$

V_{RMS} is the desired RMS value of the output voltage of the RTSMC. The equation (5.30) basically means that the phase of the RTSMC's output voltage is always kept constant and equal to 0, as it was mentioned earlier in this Chapter.

There is a total of 6 unknown time values $t_{z1}, t_1, t_2, t_{z2}, t_{z3}$ and t_3 . Two more equations determine the correlation between these time values:

$$t_{z1} + t_1 + t_2 + t_{z2} = T/2 = 1/2f_{sw} \quad (5.31)$$

$$2t_{z3} + t_3 = T/2 = 1/2f_{sw} \quad (5.32)$$

Equations (5.26), (5.27), (5.29), (5.30), (5.31) and (5.32) form a complete system of equations. Due to its complex form, an analytical solution of the given system of equations is almost impossible to find. Using MATLABs numerical solver it is possible to obtain the wanted solution of the system.

Sector	I		II		III		IV		V		VI	
Section	1	2	3	4	5	6	7	8	9	10	11	12
V_1	S_3	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2
V_2	S_1	S_3	S_3	S_2	S_2	S_1	S_1	S_3	S_3	S_2	S_2	S_1
V_3	S_2	S_2	S_1	S_1	S_3	S_3	S_2	S_2	S_1	S_1	S_3	S_3
V_z	S_4	S_4	S_4	S_4	S_4	S_4	S_4	S_4	S_4	S_4	S_4	S_4

Table 5.3: Switches used for generating output voltage of the RTSMC across all Sectors and Sections

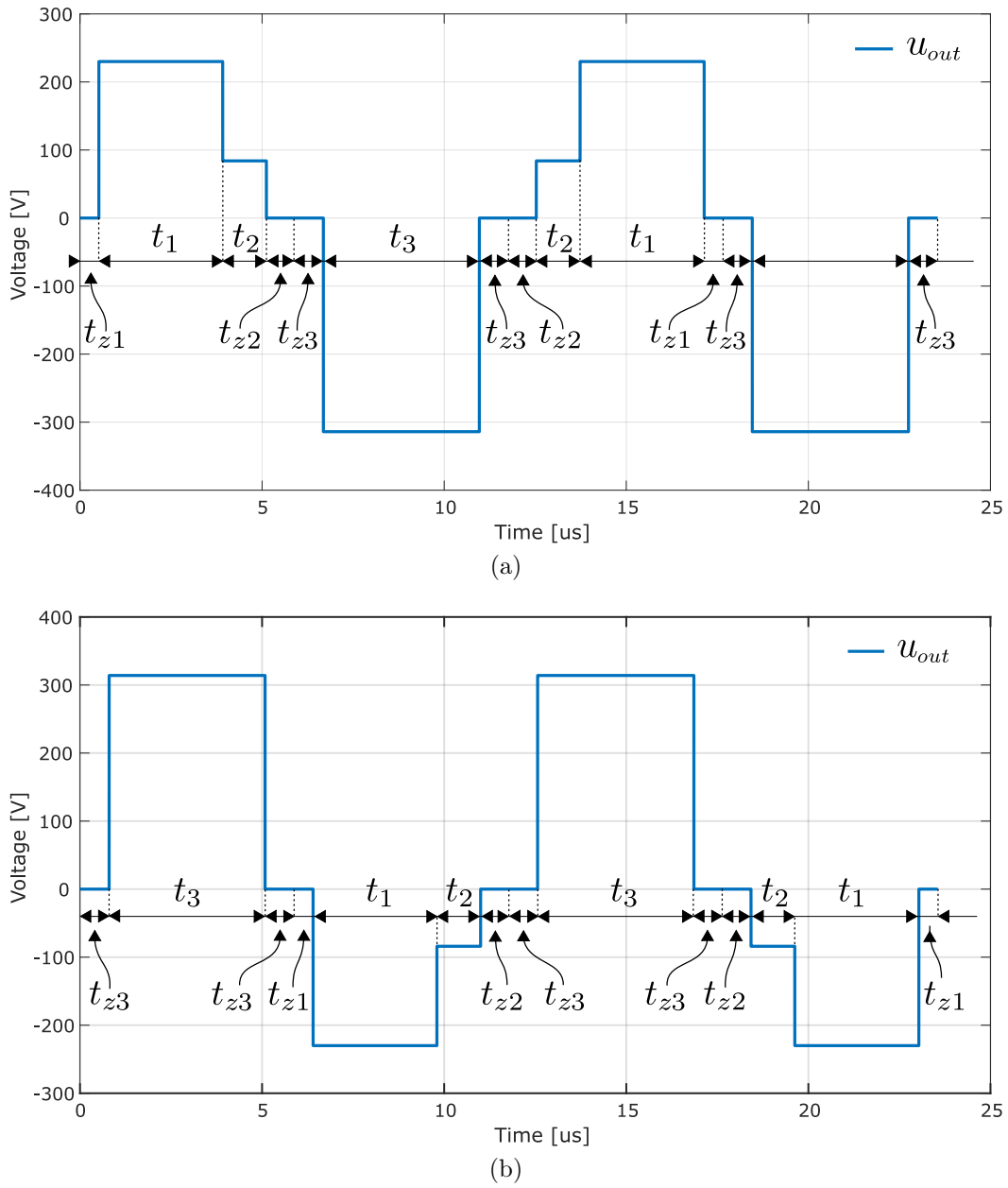


Figure 5.9: Voltage waveforms in two consecutive switching cycles a) Odd Sectors b) Even Sectors

The equations are solved for all of the discrete values of θ and a look-up table is formed from this data, that is later used in the control algorithm. Table 5.3 shows the combination of switches that are used for generating the output voltage of the TSMC throughout all Sectors and Sections.

In the previous derivation it was assumed that the output current of the RTSMC is sinusoidal and purely active. In general case, the output current does contain a certain reactive component. This reactive component, once processed by the proposed switching algorithm, would be transformed into higher order harmonics of the grid frequency, thus increasing THD of the

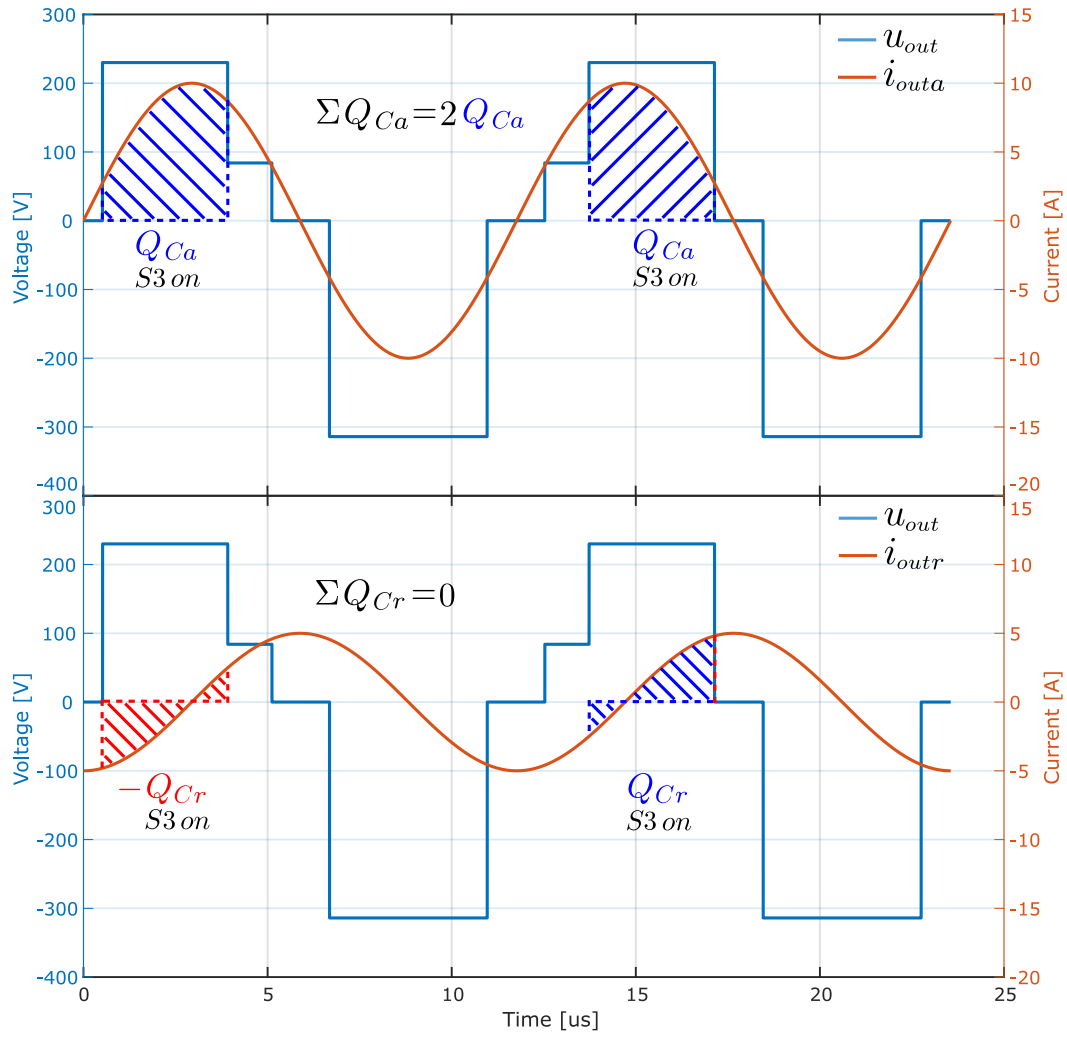


Figure 5.10: Influence of the flipping pattern on the active and reactive parts of the RTSMC's output current in Odd Sectors - example grid phase C, Sector I, Section 1

grid currents. This is completely analogous to the case from the previous Chapter. Because of this, the same trick of consecutively applying normal and flipped waveform will be applied here in order to tackle this challenge, as it was done in the previous Chapter. The waveforms used are given in Fig. 5.9. It is possible to show that applying these waveforms in the given manner does not influence the previously calculated phase nor the RMS value of the first harmonic of the RTSMC's output voltage. The mathematical proof will be omitted in this Chapter as it is similar to the one that is derived in the previous Chapter. Figures 5.10 and 5.11 are given in order to visualize the effect of the flipping pattern on the active and reactive components of the output current. Both Figures have 2 graphs, where the upper graph depicts the influence of the proposed switching pattern on the active component of the RTSMC's output current, while the bottom one shows the influence on the reactive component. Fig. 5.10 shows the overall charge distribution over the

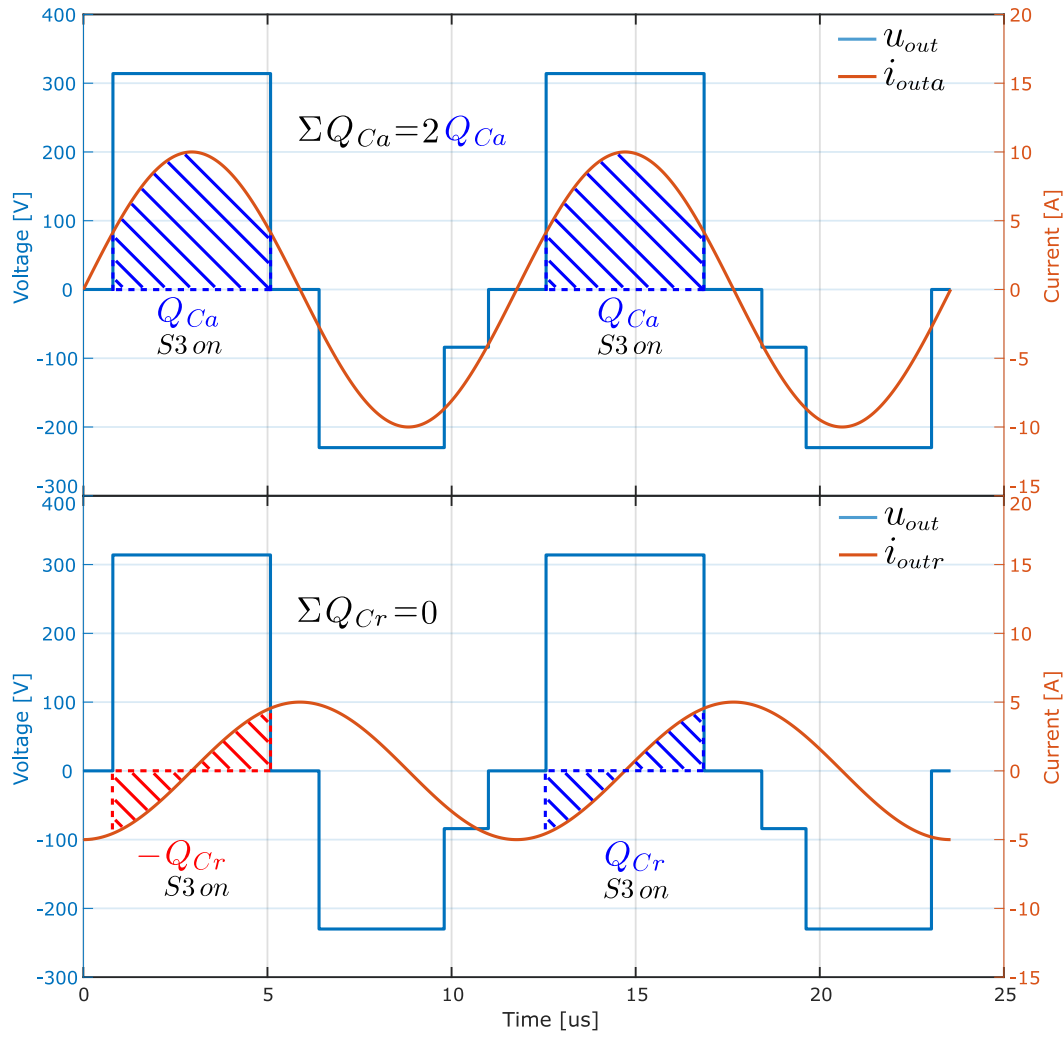


Figure 5.11: Influence of the flipping pattern on the active and reactive parts of the RTSMC's output current in Even Sectors - example grid phase C, Sector VI, Section 12

two consecutive switching period for phase C of the grid that corresponds to Sector I, Section 1. As it can be seen, flipping the switching pattern does not influence the charge distribution of the active component of the output current, as it is desired. As for the reactive component, the average charge over the two switching periods is equal to zero. This means that the reactive component of the RTSMC's output current is transformed into a high frequency ripple, with frequency equal to half of the switching frequency. This ripple is filtered out by the input LC filter, thus ensuring low THD of the grid currents. With this said, we conclude the part related to the modulation of the RTSMC.

5.5 Control of the system

To analyze the considered system, it is necessary to analyze the impedance matrix of the IPT link, that in this case is 6x6. The only input that the proposed control method requires is the impedance matrix that characterizes the inductive link. The impedance matrix of the system $\mathbf{M}$ is given with:

$$\mathbf{M} = \begin{bmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{B}^T & \mathbf{C} \end{bmatrix} \quad (5.33)$$

where $\mathbf{A}$ is the inductance matrix of the transmitter, $\mathbf{C}$ is the inductance matrix of the receiver and $\mathbf{B}$ is the coupling inductance matrix between the transmitter and receiver.

$$\mathbf{A} = \begin{bmatrix} L_Q & M_{QDD1} & M_{QDD2} \\ M_{QDD1} & L_{DD1} & M_{DD1DD2} \\ M_{QDD2} & M_{DD1DD2} & L_{DD2} \end{bmatrix} \quad (5.34)$$

$$\mathbf{B} = \begin{bmatrix} M_{Qq} & M_{Qdd1} & M_{Qdd2} \\ M_{DD1q} & M_{DD1dd1} & M_{DD1dd2} \\ M_{DD2q} & M_{DD2dd1} & M_{DD2dd2} \end{bmatrix} \quad (5.35)$$

$$\mathbf{C} = \begin{bmatrix} L_q & M_{qdd1} & M_{qdd2} \\ M_{qdd1} & L_{dd1} & M_{dd1dd2} \\ M_{qdd2} & M_{dd1dd2} & L_{dd2} \end{bmatrix} \quad (5.36)$$

When transmitter and receiver structures are manufactured correctly, $\mathbf{A}$ and $\mathbf{C}$ are equal to:

$$\mathbf{A} = \begin{bmatrix} L_Q & 0 & 0 \\ 0 & L_{DD1} & 0 \\ 0 & 0 & L_{DD2} \end{bmatrix} \quad (5.37)$$

$$\mathbf{C} = \begin{bmatrix} L_q & 0 & 0 \\ 0 & L_{dd1} & 0 \\ 0 & 0 & L_{dd2} \end{bmatrix} \quad (5.38)$$

If transmitter and receiver structures are aligned, the coupling inductance matrix $\mathbf{B}$ is diagonal:

$$\mathbf{B} = \begin{bmatrix} M_{Qq} & 0 & 0 \\ 0 & M_{DD1dd1} & 0 \\ 0 & 0 & M_{DD2dd2} \end{bmatrix} \quad (5.39)$$

In the case when the system is not aligned, matrix $\mathbf{B}$ is not diagonal. System is compensated using double-sided LCC compensation strategy. The system compensated in this way behaves as a triple cascaded gyrator, experiencing the current source behavior at the output, for voltage excitation at the input. Input voltage vector is defined with:

$$\underline{\mathbf{U}}_p = \begin{bmatrix} \underline{U}_{pq} \\ \underline{U}_{pdd1} \\ \underline{U}_{pdd2} \end{bmatrix} = \begin{bmatrix} U_{pq}e^{j0} \\ U_{pdd1}e^{j\varphi_{pdd1}} \\ U_{pdd2}e^{j\varphi_{pdd2}} \end{bmatrix} \quad (5.40)$$

When the system is excited with this input vector, vector of the secondary currents can be calculated using the following equation:

$$\underline{\mathbf{I}}_s = \begin{bmatrix} \underline{I}_{sq} \\ \underline{I}_{sidd1} \\ \underline{I}_{sidd2} \end{bmatrix} = -j\omega^3 C_{fp} C_{fs} \mathbf{B} \underline{\mathbf{U}}_p \quad (5.41)$$

From here it is possible to deduce that in case that $\mathbf{B}$ is diagonal, the power will be exchanged only between corresponding phases. This means if coupling between non-corresponding phases exists, i.e., the receiver and transmitter are not aligned, each of the phases of the transmitter will send power to each of the phases of the receiver, if excited with symmetrical voltages at the input. This problem exists in all of the compact three-phase IPT systems. In this article we propose a control strategy devised to achieve equal power transfer per-phase on both primary and secondary sides of the considered system. As it was stated previously, to implement the proposed control, it is necessary to have determined the matrix $\mathbf{M}$.

Once the secondary currents are determined, it is possible to determine the secondary voltages:

$$\underline{\mathbf{U}}_s = \begin{bmatrix} \underline{U}_{sq} \\ \underline{U}_{sdd1} \\ \underline{U}_{sdd2} \end{bmatrix} = f(\underline{\mathbf{I}}_s) \quad (5.42)$$

Function f that determines the relation between the secondary voltages and currents depends on the parameters of the electrical circuit. In order to determine this relation precisely, due to the non-linear behavior of the diode, we recommend establishing it based on tests performed on the actual prototype.

Once secondary voltages are determined, it is possible to calculate primary currents:

$$\underline{\mathbf{I}}_p = \begin{bmatrix} \underline{I}_{piq} \\ \underline{I}_{pidd1} \\ \underline{I}_{pidd2} \end{bmatrix} = -j\omega^3 C_{fp} C_{fs} \mathbf{B}^T \underline{\mathbf{U}}_s \quad (5.43)$$

Apparent powers at the primary and secondary sides are, respectively:

$$\underline{\mathbf{S}}_p = \begin{bmatrix} \underline{S}_{pq} \\ \underline{S}_{pdd1} \\ \underline{S}_{pdd2} \end{bmatrix} = \begin{bmatrix} \underline{U}_{pq} \underline{I}_{piq}^* \\ \underline{U}_{pdd1} \underline{I}_{pidd1}^* \\ \underline{U}_{pdd2} \underline{I}_{pidd2}^* \end{bmatrix} \quad (5.44)$$

$$\underline{\mathbf{S}}_s = \begin{bmatrix} \underline{S}_{sq} \\ \underline{S}_{sdd1} \\ \underline{S}_{sdd2} \end{bmatrix} = \begin{bmatrix} \underline{U}_{sq} \underline{I}_{siq}^* \\ \underline{U}_{sdd1} \underline{I}_{sidd1}^* \\ \underline{U}_{sdd2} \underline{I}_{sidd2}^* \end{bmatrix} \quad (5.45)$$

Active powers are real part of the apparent powers:

$$\underline{\mathbf{P}}_p = \begin{bmatrix} P_{pq} \\ P_{pdd1} \\ P_{pdd2} \end{bmatrix} = \text{real}(\underline{\mathbf{S}}_p) \quad (5.46)$$

$$\underline{\mathbf{P}}_s = \begin{bmatrix} P_{sq} \\ P_{sdd1} \\ P_{sdd2} \end{bmatrix} = \text{real}(\underline{\mathbf{S}}_s) \quad (5.47)$$

Now, that all of the values of interest of the system are determined, it is possible to start the process of determining the required excitation vector $\underline{U}_p$ to obtain desired system functionality. In the case of this work, we will seek $\underline{U}_p$ to achieve equal power distribution on both primary and secondary sides, i.e.:

$$\begin{aligned} P_{pq} &= P_{pdd1} = P_{pdd2} \\ P_{sq} &= P_{sdd1} = P_{sdd2} \end{aligned} \quad (5.48)$$

Equation (5.40) has total of 5 variables - U_{pq} , U_{pdd1} , U_{pdd2} , φ_{pdd1} , φ_{pdd2} while the system in (5.48) has total of 4 equations. This means that there is 1 degree of freedom, that can be used to set the exact power that will be exchanged between the primary and secondary sides. Considering that the previous system is pretty complex and nonlinear due to equation (5.42), it is hard to solve it analytically. Rather, it is more convenient to apply false assumption method for solving, first by defining the upper and lower limits for each of the 5 previously mentioned variables, and dividing the ranges into n equally sized parts. After this, by trying all of the combinations by varying each of the variables between its n previously established discrete values, having total of n^5 iterations, it is possible to find certain number of combinations that will fulfill the requirement of equation (5.48). Since the domain was discretized, there will be certain tolerance, thus the previous algorithm will give solutions in vicinity of which the exact solutions are located. The unbalance in power distribution across the phases obtained by applying the discretized solutions

will depend on the tolerance set on equation (5.48) during the execution of the process, and on the number of considered discrete values n , and it is realistic to expect this unbalance in range between $[-5\%, 5\%]$. If one wants to obtain the exact solution, it is necessary to do the following:

1. Determine the starting point from the pool of obtained discrete solutions $[U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd2}^0, \varphi_{pdd1}^0]$
2. For each of the per-phase powers in the given operating point $P_{pq}^0, P_{pdd1}^0, P_{pdd2}^0, P_{sq}^0, P_{sdd1}^0, P_{sdd2}^0$ determine the values of partial derivatives:
 - a) $\frac{\partial P_x}{\partial U_{pq}}(U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd1}^0, \varphi_{pdd2}^0)$
 - b) $\frac{\partial P_x}{\partial U_{pdd1}}(U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd1}^0, \varphi_{pdd2}^0)$
 - c) $\frac{\partial P_x}{\partial U_{pdd2}}(U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd1}^0, \varphi_{pdd2}^0)$
 - d) $\frac{\partial P_x}{\partial \varphi_{pdd1}}(U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd1}^0, \varphi_{pdd2}^0)$
 - e) $\frac{\partial P_x}{\partial \varphi_{pdd2}}(U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd1}^0, \varphi_{pdd2}^0)$.

for $x \in \{pq, pdd1, pdd2, sq, sdd1, sdd2\}$. These derivative values are best to be taken by measuring the given values on the real-life setup, not by simulation.

3. It is necessary to find a delta vector $(\Delta U_{pq}, \Delta U_{pdd1}, \Delta U_{pdd2}, \Delta \varphi_{pdd1}, \Delta \varphi_{pdd2})$ that is to be added to the vector of discrete solutions in order to perfectly equalize all of the powers across the phases. The system of equations that has to be solved is defined in equation (5.49). Values P_{pavg} and P_{savg} are the average active power values that are being transferred via primary and secondary, respectively, for the case given by the initial solution $[U_{pq}^0, U_{pdd1}^0, U_{pdd2}^0, \varphi_{pdd2}^0, \varphi_{pdd1}^0]$. Solving this system of linear equations, one obtains the final values of the 5 variables $U_{pq}, U_{pdd1}, U_{pdd2}, \varphi_{pdd1}, \varphi_{pdd2}$ that allow for equal power sharing between the phases of the system. As the given system has one more variable than the number of equations, it is possible to consider one of the delta values equal to 0.

In the previously described way, we have calculated the necessary excitation voltage vector that, as a result, leads to equal distribution of power levels across the phases of the considered system. As it was stated before, the discrete solution for achieving a certain power at a certain misalignment is not unique. This opens space for further improving of the presented control methodology, through analyzing the per-phase losses, and balancing them through applying different solutions that allow for the same power to be transferred, however that are producing different losses in different phases, thus balancing the system thermally over longer time spans. However, this will not be in the scope of this work.

$$\begin{aligned}
 P_{pavg} &= P_{pq}^0 + \frac{\partial P_{pq}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{pq}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{pq}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{pq}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{pq}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2} \\
 P_{pavg} &= P_{pdd1}^0 + \frac{\partial P_{pdd1}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{pdd1}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{pdd1}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{pdd1}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{pdd1}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2} \\
 P_{pavg} &= P_{pdd2}^0 + \frac{\partial P_{pdd2}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{pdd2}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{pdd2}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{pdd2}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{pdd2}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2} \\
 P_{savg} &= P_{sq}^0 + \frac{\partial P_{sq}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{sq}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{sq}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{sq}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{sq}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2} \\
 P_{savg} &= P_{sdd1}^0 + \frac{\partial P_{sdd1}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{sdd1}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{sdd1}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{sdd1}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{sdd1}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2} \\
 P_{savg} &= P_{sdd2}^0 + \frac{\partial P_{sdd2}}{\partial U_{pq}} \Delta U_{pq} + \frac{\partial P_{sdd2}}{\partial U_{pdd1}} \Delta U_{pdd1} + \frac{\partial P_{sdd2}}{\partial U_{pdd2}} \Delta U_{pdd2} + \\
 &\quad + \frac{\partial P_{sdd2}}{\partial \varphi_{pdd1}} \Delta \varphi_{pdd1} + \frac{\partial P_{sdd2}}{\partial \varphi_{pdd2}} \Delta \varphi_{pdd2}
 \end{aligned} \tag{5.49}$$

5.6 Experimental results

In order to verify the ideas that are proposed in this Chapter, an experimental setup was built. Fig. 5.12 depicts the prototype of a single RTSMC. Silicon-carbide modules MSCSM70DUM10T3AG, 700 V, 7.5 mΩ, were used as building blocks for this converter. A total of three of these converters were constructed in order to energize the considered system. DD²Q structures of the transmitter and receiver are shown in Fig. 5.13. Parameters of the system are given in the Table 5.4. Secondary side rectifier was built using MSC2X50SDA120J silicon-carbide diode modules, 1.2 kV, 50 A.

Several different tests were conducted to verify the functionality of the proposed ideas:

1. Aligned system, clearance 200 mm, power transfer 12 kW.

2. Misaligned system, $[\Delta x, \Delta y] = [100, 75]$ mm, clearance 200 mm, no balancing.
3. Misaligned system, $[\Delta x, \Delta y] = [100, 75]$ mm, clearance 200 mm, balancing relying on the false assumption method from Section 5.5.
4. Misaligned system, $[\Delta x, \Delta y] = [100, 75]$ mm, clearance 200 mm, balancing improved by small variation method from Section 5.5.
5. Aligned system, clearance 140 mm, power transfer 24 kW

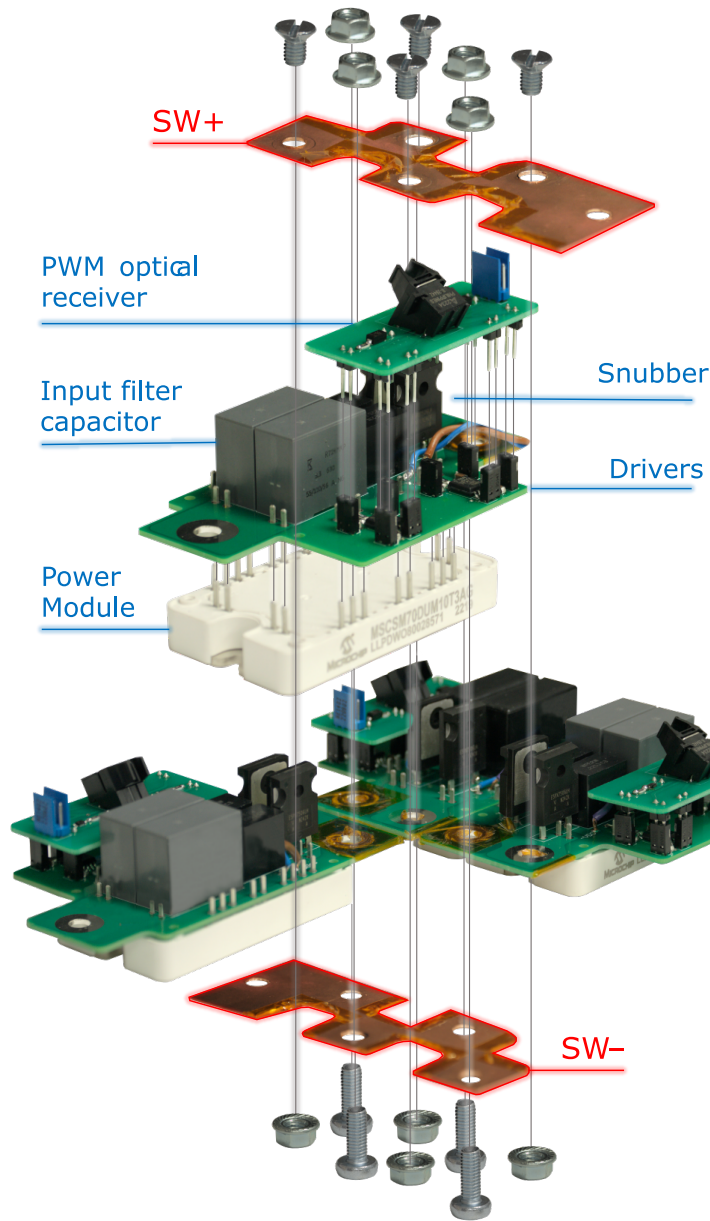


Figure 5.12: Exploded view of the RTSMC prototype

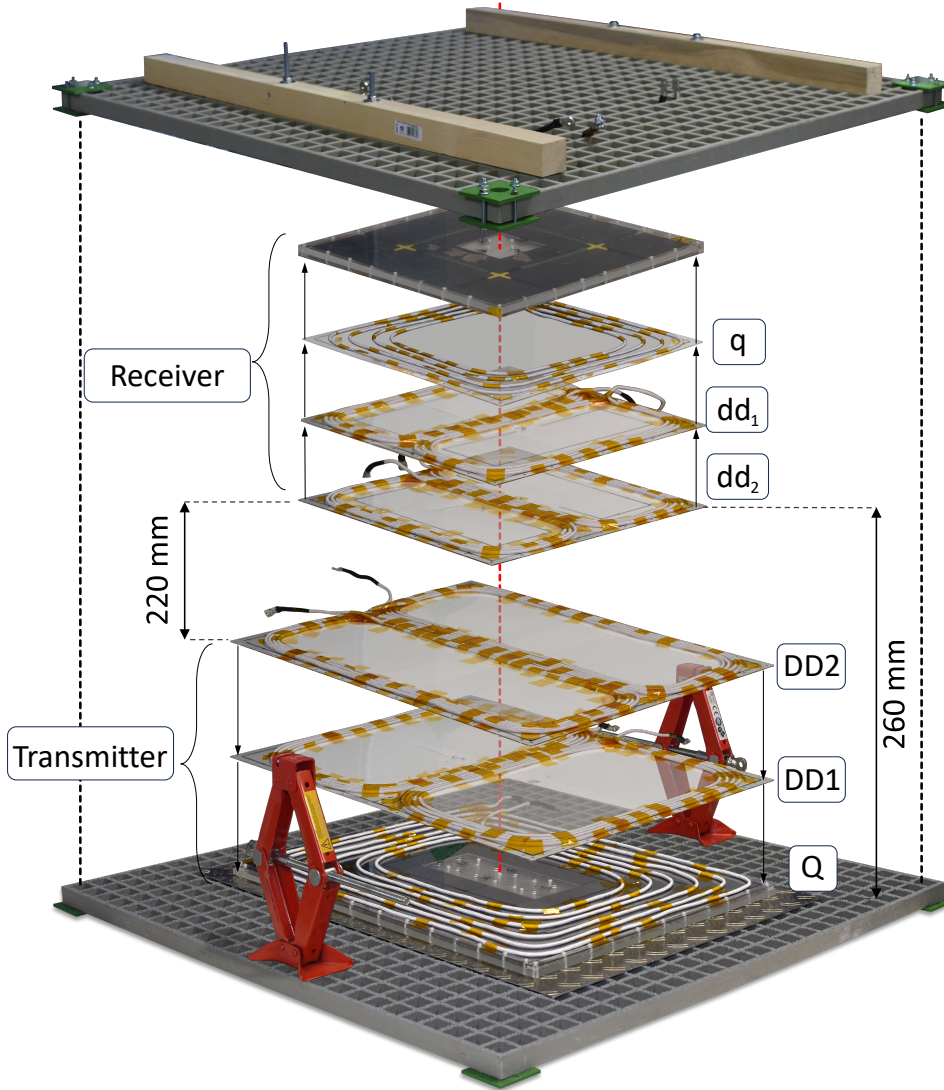


Figure 5.13: Exploded view of the considered DD^2Q system

Parameter	Value	Parameter	Value
L_{pq}	32 μH	L_{sq}	14.36 μH
L_{pdd1}	47.05 μH	L_{sdd1}	20.04 μH
L_{pdd2}	50.11 μH	L_{sdd2}	18.58 μH
C_{pq}	135 nF	C_{sq}	783 nF
C_{pdd1}	83.6 nF	C_{sdd1}	352 nF
C_{pdd2}	79.2 nF	C_{sdd2}	418 nF
C_{fp}	567 nF	C_{fs}	364.5 nF
L_{fp}	6.77 μH	L_{fs}	9.67 μH

Table 5.4: Measured parameters of the considered IPT system

	q	dd_1	dd_2
Q	$3.52 \mu\text{H}$	$-0.03 \mu\text{H}$	$0.09 \mu\text{H}$
DD_1	$0.19 \mu\text{H}$	$3.76 \mu\text{H}$	$0.06 \mu\text{H}$
DD_2	$0.04 \mu\text{H}$	$0.03 \mu\text{H}$	$3.5 \mu\text{H}$

Table 5.5: Mutual inductances between primary and secondary coils for the aligned system, clearance 200 mm

First, test results of the aligned system with 200 mm clearance between the transmitter and receiver structures will be analyzed. Power transfer of 12 kW is chosen as it is the one for which the coils are designed. System is excited with a symmetrical voltage system, where all voltages have the same RMS value of 205 V and are delayed by a third of a period. Operating frequency is 85 kHz. The mutual inductance matrix of the system is given in the Table 5.5. Fig. 5.14 shows high-frequency waveforms of the system. Fig. 5.14a shows

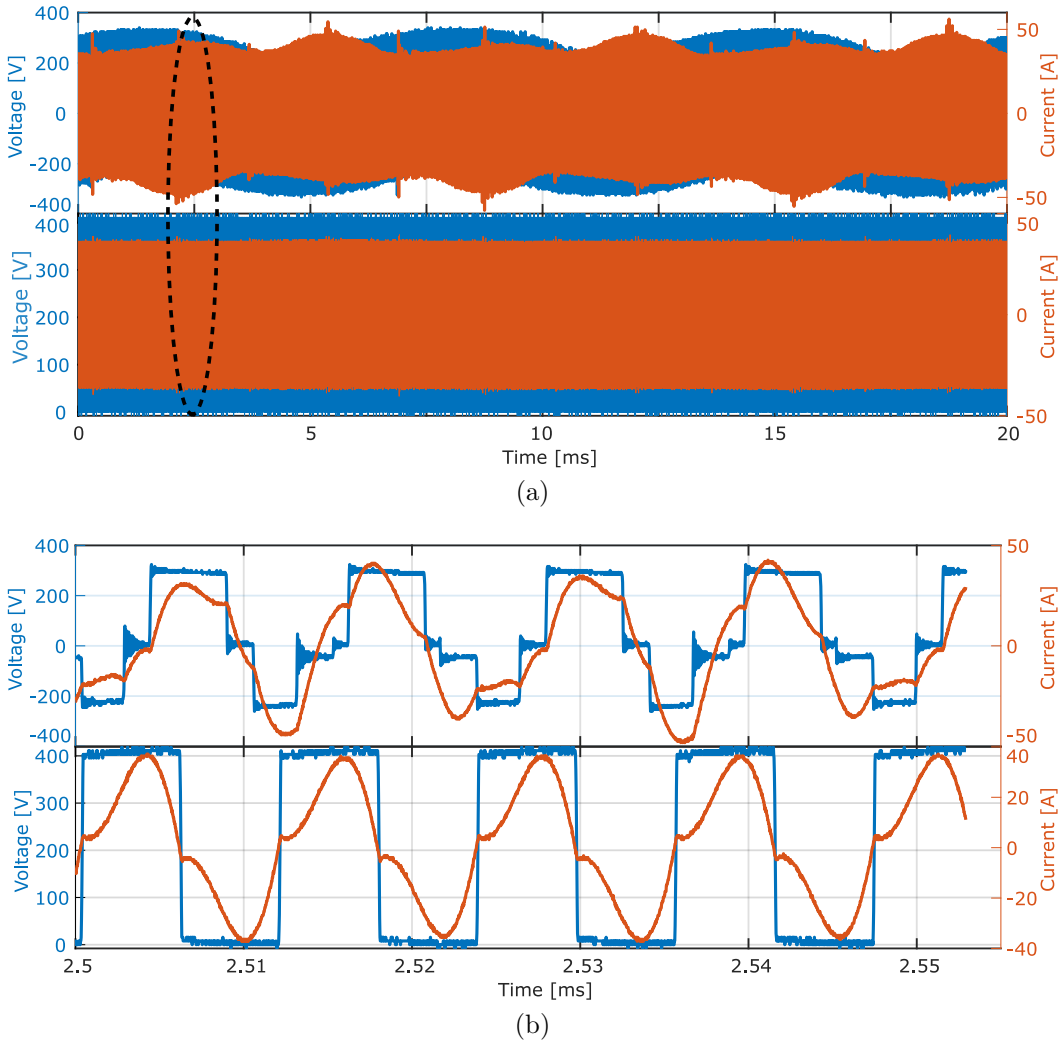


Figure 5.14

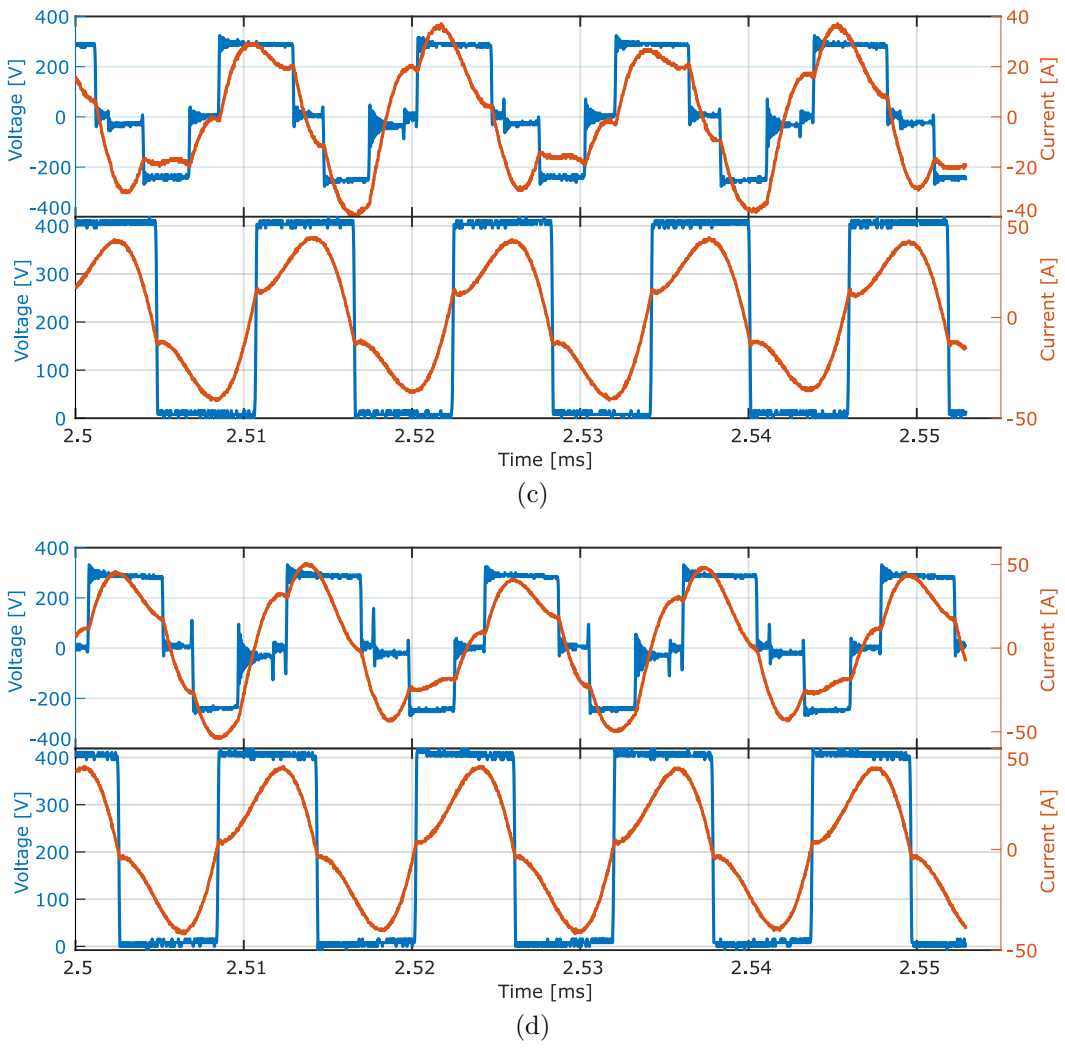


Figure 5.14: Aligned system a) Voltage and current of DD_1 coil over one grid period - primary (top) and secondary (bottom) b) Voltage and current of DD_1 coil in zoomed region c) Voltage and current of Q coil in zoomed region d) Voltage and current of DD_2 coil in zoomed region

the output voltage and current of the RTSMC (top waveforms) that energizes DD_1 coil, and the voltage and current of the half-wave diode rectifier (bottom waveforms) corresponding to the dd_1 secondary coil, over an entire grid period. Zoomed part of these graphs are given in Fig. 5.14b. Fig. 5.14c and 5.14d show the corresponding waveforms of the Q (q) and DD_2 (dd_2) phases, respectively. As it can be seen, system is excited with symmetrical voltage system and is rather balanced. Phase unbalance can be seen in the currents of different phases and it exists as a consequence of difference in coupling coefficient between the phases, tolerance in manufacturing of the compensation circuit and manufacturing tolerance of the coupler coils leading to non-zero coupling coefficient between the phases of the coupler. Additionally, due to the low values of coil self-inductances, currents will contain higher harmonic

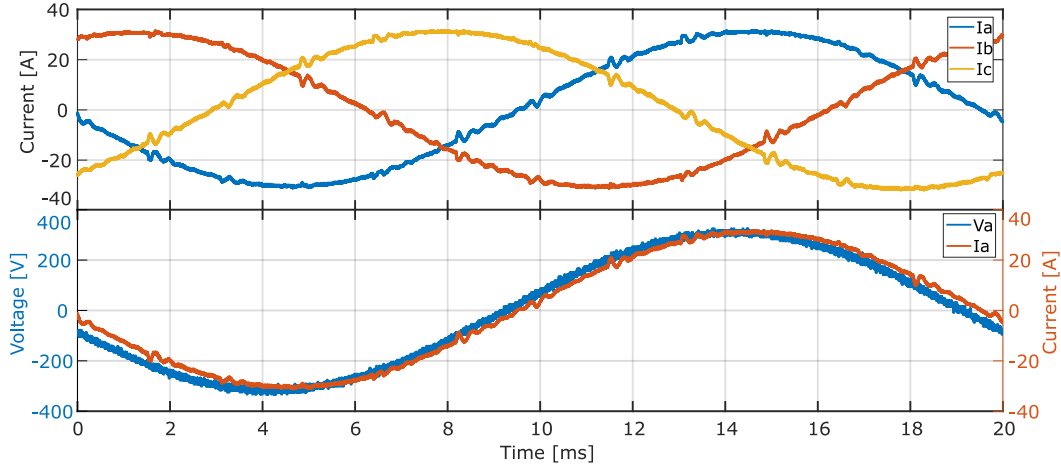


Figure 5.15: Grid currents (top); Voltage and current of the phase A of the grid (bottom)

Parameter	Phase A	Phase B	Phase C
V_{rms} [V]	220.77	221.3	221.06
I_{rms} [A]	21.858	22.069	22.098
P [kW]	4.791	4.849	4.851
Q [kvar]	0.578	0.580	0.579
I_{thd} [%]	2.459	2.399	2.317
PF	0.993	0.993	0.993

Table 5.6: Relevant parameters of the grid with 12.3 kW of output power

components. Processing of the these higher harmonics by the proposed modulation is described in Appendix B. Voltage waveforms are generated with the flipping pattern that was explained in Chapter 5.4. Difference in current waveforms that can be noted for all three RTSMCs in consecutive switching cycles comes from the different phases of higher harmonic components that exist in the excitation voltage. Also, voltage spikes can be seen in the moments of commutation and that are the consequence of the previously explained diode snubber. Grid waveforms are given in Fig. 5.15 and the parameters of the grid are given in Table 5.6. Power at the output of the secondary diode rectifier is equal to 12.3 kW, meaning that the system efficiency is equal to 84.89%.

A short discussion on the system efficiency will be given here. Losses breakdown is given in Fig. 5.16. Dominant losses are the ones in the inductive link and the compensation circuit. The reason for this are high resonant currents circulating through the coils, as the design process was done in the way to minimize the weight of the system and maximize the usage of the Litz wire cross section utilizing 5 A/mm². In this way, less Litz wire was used to build the system at the expense of higher losses. Second biggest contributor to the system losses are the ones coming from switching the RTSMC. Here it is important to note three things:

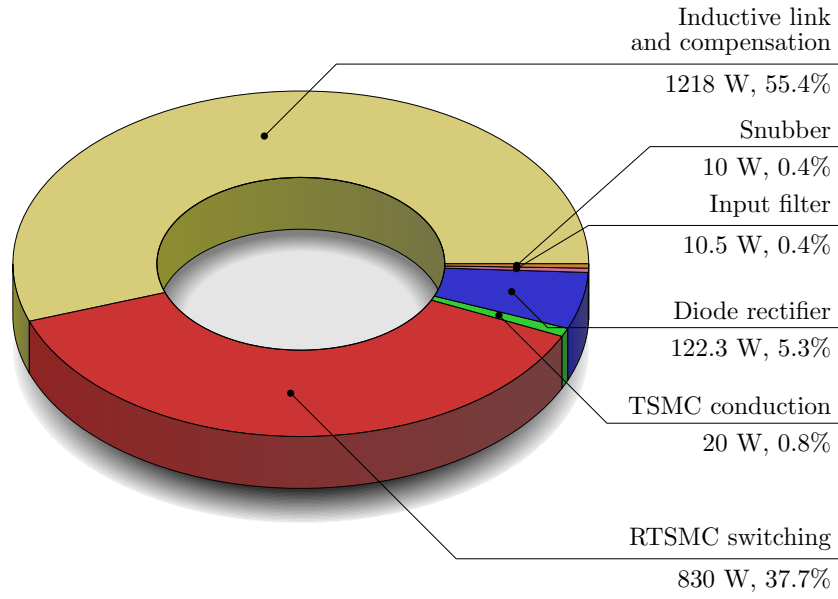


Figure 5.16: Losses breakdown of the system for the case of 12.3 kW of output power

1. Three of the RTSMC switches block the line-to-line voltage, the same as the switches of the TSMC topology. RMS value of the RTSMC's output voltage is $\sqrt{3}$ times smaller than the one of the TSMC, meaning that to achieve the same power transfer, more current is required in the case of RTSMC than in the case of TSMC, leading to higher switching losses.
2. One of the switches is commutating at twice the fundamental frequency, i.e. 170 kHz.
3. Modules used for making the RTSMC have very low resistance, meaning that they have a high capacitance and, by that, high switching losses in hard-switching applications.

These are the main reasons why the converter switching loss in the case of RTSMC is higher than the one of the TSMC from the previous Chapter, considering it relatively, respective to the power that is being transferred. Trade-off in this case is that RTSMC has 50% less semiconductors than the TSMC and design of the converter was much simplified with the use of modules instead of discrete transistors, enabling for much more optimal design in terms of parasitic inductances, which is a very important parameter in the case of matrix converter topology.

It is well known from the current state-of-the-art [130] that it is possible to achieve ZVS with matrix topology and by those means significantly reduce switching losses of the converter. The main requirement for the soft turn-on to occur is that the converter has negative output current whenever the output is transitioning from lower to higher voltage level, and vice versa, that the output current is positive whenever the output is transitioning from

higher to lower voltage level. From this fact, it is clear that it is impossible to achieve soft-switching when flipping pattern is applied, i.e., it is possible to be achieved in one half of all switching periods. Also, the ability to achieve ZVS comes at a cost:

1. Number of driver circuits would need to be twice as high as there would be one driver per transistor, not per four-quadrant switch.
2. Previous point leads to having twice the number of required PWM channels, meaning that the controller requirements are increased. Just for comparison, TSMC from the previous Chapter was controlled using Texas Instruments LAUNCHXL-F28379D that has 6 independent PWM channels available. Entire system from this Chapter was controlled using TMDSCNCD28379D ControlCard that has 12 independent PWM channels.

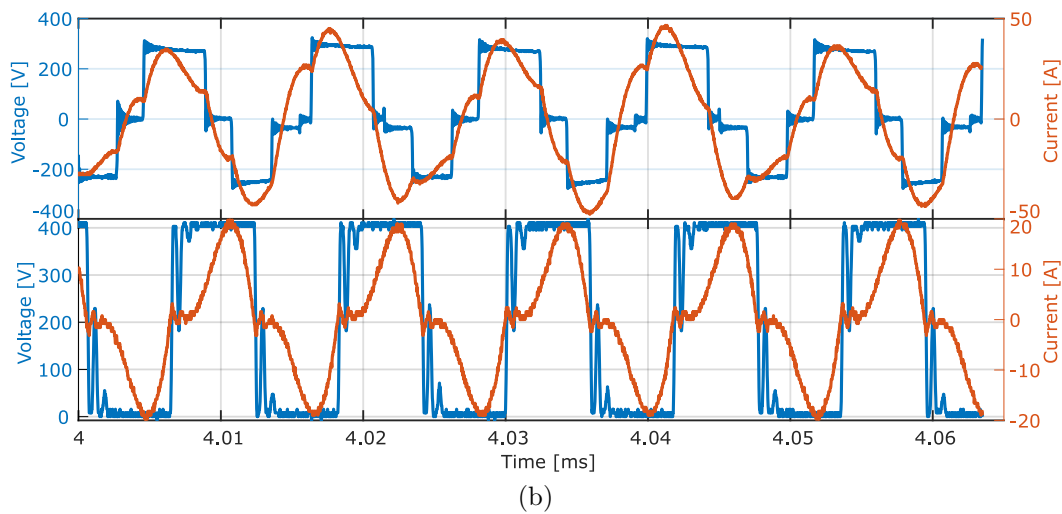
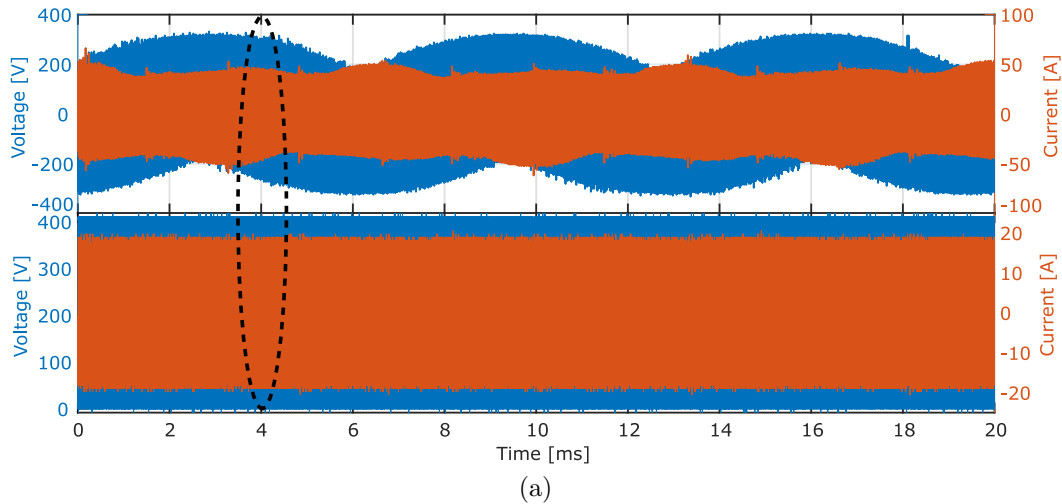


Figure 5.17

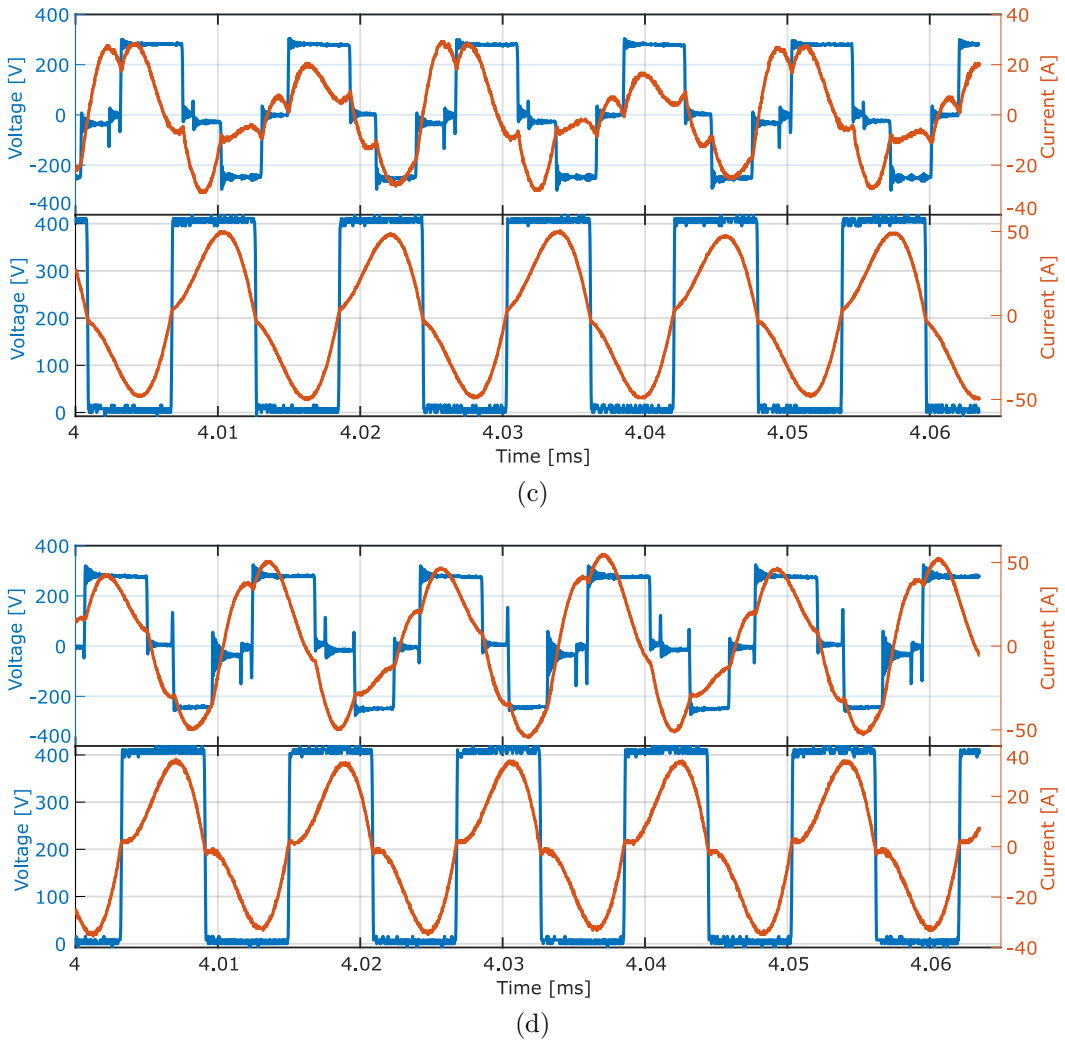


Figure 5.17: Misaligned system without control a) Voltage and current of DD_1 coil over one grid period - primary (top) and secondary (bottom) b) Voltage and current of DD_1 coil in zoomed region c) Voltage and current of Q coil in zoomed region d) Voltage and current of DD_2 coil in zoomed region

In this work we wanted to demonstrate the functionality of the proposed ideas, and therefore we have not considered efficiency optimization. Optimization of the converter design is part of the future work. Further discussion on the proposed RTSMC modulation is given in the Appendix of this Chapter, allowing for potential ZVS implementation in the future.

Next test that was performed is under maximum standard predicted misalignment $[\Delta x, \Delta y] = [100, 75]$ mm. Clearance between transmitter and receiver in this case is 200 mm. Mutual inductance matrix for this case is given in Table 5.7. Comparing the values from this Table to the ones from the aligned system, it is possible to see that there is significant coupling between the non-corresponding phases that will lead to the non-balance in power transfer between the phases.

Fig. 5.17 shows the high-frequency waveforms for the misaligned system

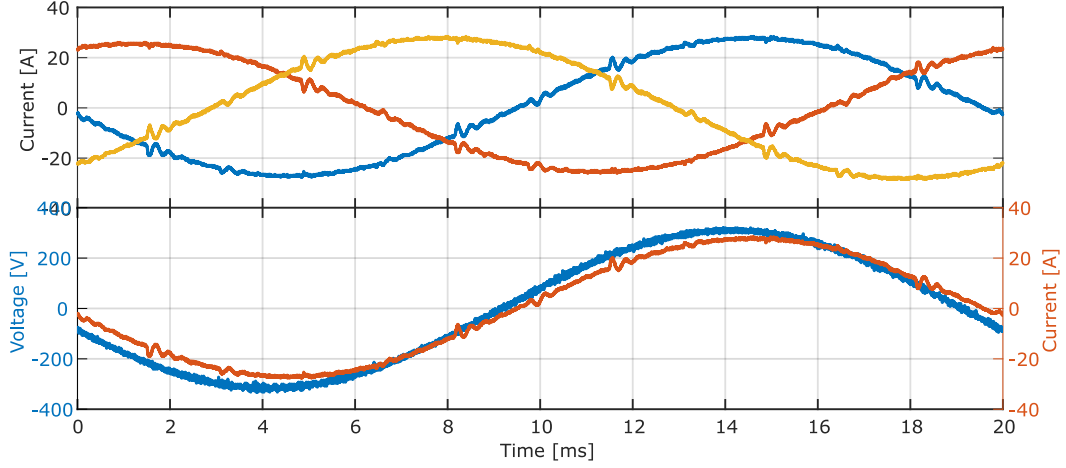


Figure 5.18: Grid currents (top); Voltage and current of the phase A of the grid (bottom) for the misaligned system excited with a symmetrical voltage system

	q	dd_1	dd_2
Q	$2.94 \mu\text{H}$	$1.05 \mu\text{H}$	$-1.5 \mu\text{H}$
DD_1	$-2.66 \mu\text{H}$	$2.39 \mu\text{H}$	$0.44 \mu\text{H}$
DD_2	$1.61 \mu\text{H}$	$0.13 \mu\text{H}$	$2.84 \mu\text{H}$

Table 5.7: Mutual inductances between primary and secondary coils for the misaligned system $[\Delta x, \Delta y] = [100, 75]$ mm, clearance 200 mm

Phase	Power Transmitting [kW]	Phase	Power Receiving [kW]
Q	2.06	q	5.52
DD_1	5.39	dd_1	1.75
DD_2	5.65	dd_2	3.62

Table 5.8: Power distribution between the phases for a misaligned system without control

excited with symmetrical voltage system. As it can be seen, there is significant difference between the currents and in the power transfer. Table 5.8 shows the power that is being transferred and received by each of the phases of the system. Total power that is being taken from the grid is equal to 13.03 kW, while the grid waveforms are given in Fig. 5.18, and the power at the output of the secondary rectifier is equal to 10.89 kW, yielding system efficiency of 83.58%. Average absolute relative deviation from the average transmitted and received power per phase in this case is 35.58% and 34.53%. In order to reduce these deviations and equalize the power distribution per phase control methods from the Chapter 5.5 are applied. From the figure that shows relevant grid waveforms, it is notable that from the point of view of grid, the misalignment between the transmitter and receiver is not seen, and grid currents are perfectly balanced, as it is expected.

First, the basic balancing method (false assumption), relying only on the simulation results is applied. As it was explained in the previous Sec-

tion, it is necessary to characterize the system, i.e., determine the function f from the equation (5.42) that shows dependence between the high-frequency voltage (U_{sq} , U_{sdd1} , U_{sdd2}) and the corresponding current of the diode rectifier (I_{siq} , I_{sidd1} , I_{sidd2}). This was done experimentally, by measuring the mentioned voltages and currents for different values of the secondary current and determining the RMS values for their 1st harmonic and phase-shift between the 1st harmonic components of the given signals. Only example for phase dd_1 is given here as the results for the other two phases are similar and are analogously derived. Fig. 5.19 shows the waveforms that were measured for different values of the secondary current while the Fig. 5.20 shows the processed results and curves that were obtained by interpolating the obtained results with a third order polynomial. As it can be seen from Fig. 5.19a and

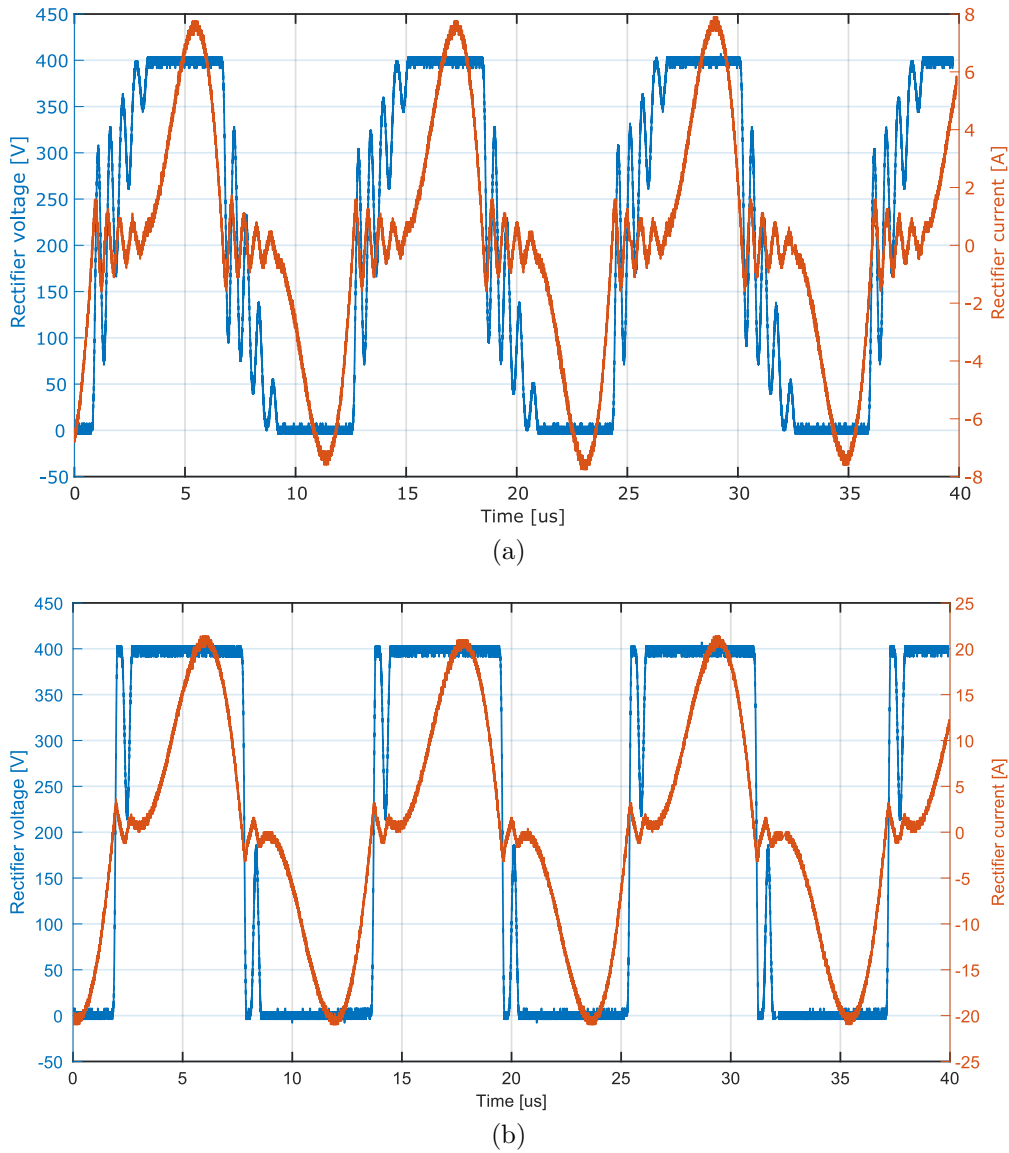


Figure 5.19

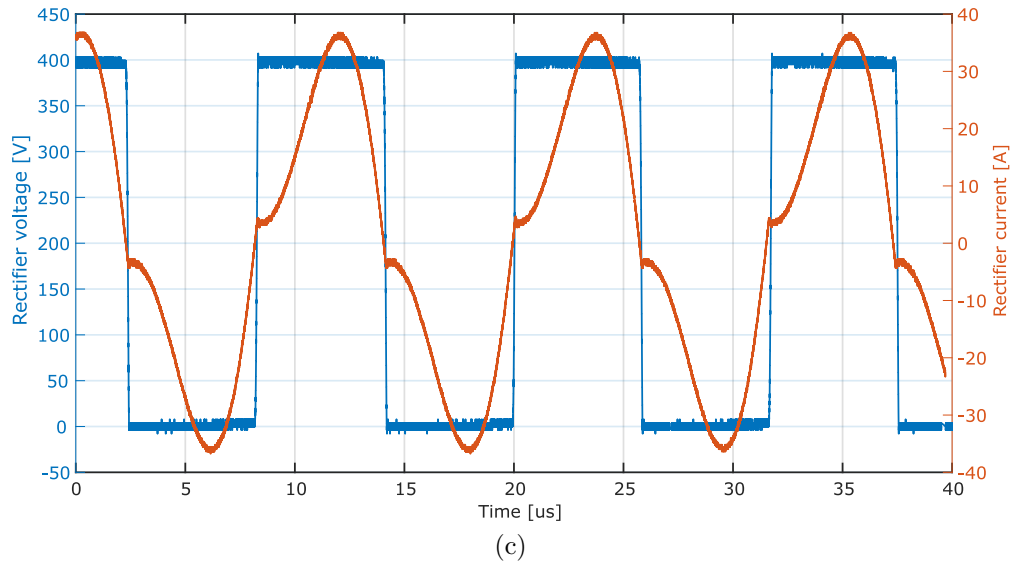


Figure 5.19: Voltage and current of the diode rectifier of the dd_1 phase a) Low secondary current b) Medium secondary current c) High secondary current

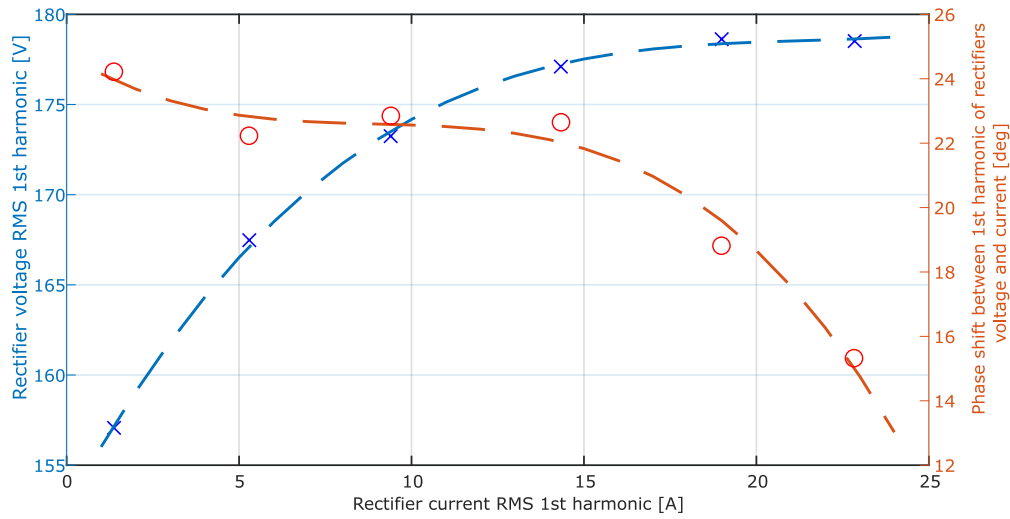
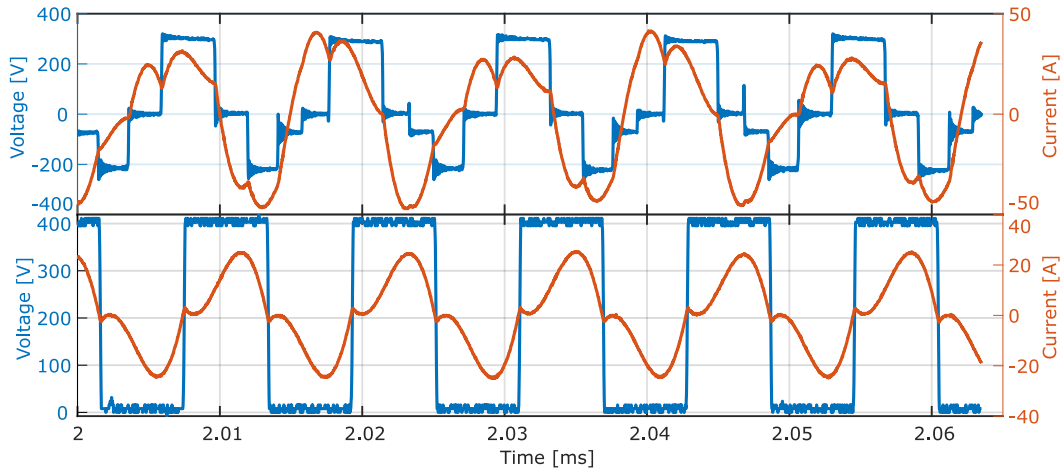


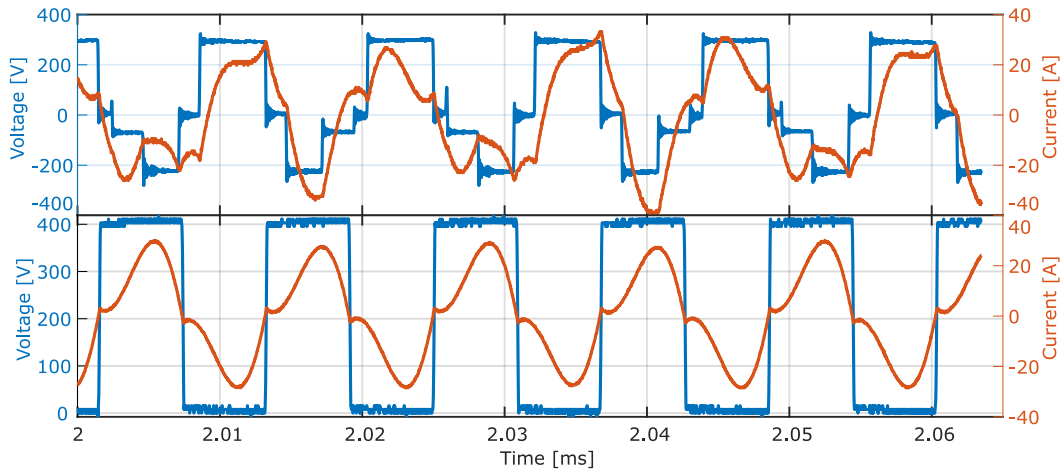
Figure 5.20: Measured dependence between the rectifier current and voltage of the phase dd_1

5.17a, for low values of the secondary current a significant oscillation in both the voltage and current is present. This is due to the oscillation caused by parasitic capacitances of the diodes with the parasitic inductances of the secondary. The results from the Figure 5.20 were used for solving the system (5.48). The solution of this system that was obtained is $[U_{pq}, U_{pdd1}, U_{pdd2}, \varphi_{pdd1}, \varphi_{pdd2}] = [198 \text{ V}, 220 \text{ V}, 181.5 \text{ V}, -45^\circ, -175^\circ]$.

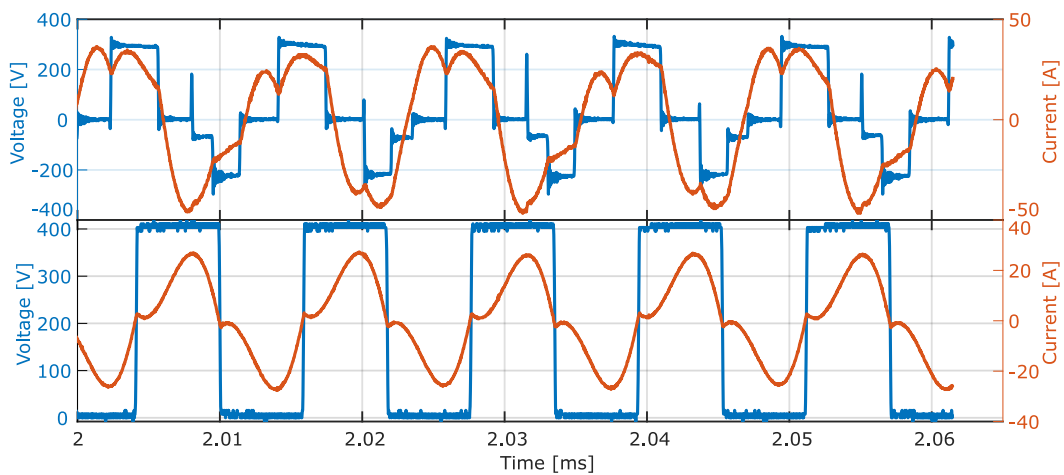
The system is now tested with applying the excitation given excitation vector of input voltages. Voltage and current waveforms are depicted in Fig. 5.21 for all the three phases of the inductive link. Power that is being transmitted and received by each of the phases is given in Table 5.9. Total input



(a)



(b)



(c)

Figure 5.21: Misaligned system with balancing method "false assumption" a) Voltage and current of DD_1 coil b) Voltage and current of Q coil c) Voltage and current of DD_2 coil

Phase	Power Transmitting [kW]	Phase	Power Receiving [kW]
Q	3.05	q	2.74
DD_1	3.5	dd_1	3.1
DD_2	3.88	dd_2	2.35

Table 5.9: Power distribution between the phases for a misaligned system with excitation obtained using false assumption method

power is 10.43 kW and the charging power is 8.59 kW yielding the system efficiency of 82.36%. Average absolute relative deviation from the average transmitted and received power per phase in this case is 8.2% and 9.3%, which is significantly better than the deviation in power distribution if the symmetrical voltage excitation is applied. Slightly lower system efficiency comes from the lower power that is being transferred in the system.

In order to prove the small variation method for enhancing and refining the power distribution across the phases additional test is performed. As it was explained in the previous Chapter, it is necessary to determine the values of change in power levels when applying small variations in each of the system control variables. The measured values are given in the Table 5.10. Solving the system (5.49) with the values from the previous two tables, one obtains the differential step of each of the system variables, applying which, system goes towards power equilibrium. The solution of the system for the given values is $[\Delta U_{pdd1}, \Delta U_{pdd2}, \Delta \varphi_{pdd1}, \Delta \varphi_{pdd2}] = [0 \text{ V}, -24.6 \text{ V}, -8.28^\circ, 7.96^\circ]$. Adding this vector to the excitation vector obtained by the false assumption method and applying the resultant excitation to the system, power levels that are being transmitted and received by each of the phases are given in Table 5.11.

Phase	$\partial P / \partial U_{pdd1}$	$\partial P / \partial U_{pdd2}$	$\partial P / \partial \varphi_{pdd1}$	$\partial P / \partial \varphi_{pdd2}$
Q	-10.12 W/V	-6.93 W/V	3.6 W/ $^\circ$	1.3 W/ $^\circ$
DD_1	23.79 W/V	6.56 W/V	17.3 W/ $^\circ$	2.9 W/ $^\circ$
DD_2	4.1 W/V	17.69 W/V	6.3 W/ $^\circ$	-19.3 W/ $^\circ$
q	3.28 W/V	1.82 W/V	51.6 W/ $^\circ$	-26.4 W/ $^\circ$
dd_1	7.29 W/V	-3.64 W/V	-14 W/ $^\circ$	-6.8 W/ $^\circ$
dd_2	4 W/V	22.21 W/V	-7.2 W/ $^\circ$	23.2 W/ $^\circ$

Table 5.10: Change in power levels with small variations in system control variables

Phase	Power Transmitting [kW]	Phase	Power Receiving [kW]
Q	3.21	q	2.71
DD_1	3.24	dd_1	2.57
DD_2	2.95	dd_2	2.51

Table 5.11: Power distribution between the phases for a misaligned system where excitation obtained using false assumption method is corrected using small variation method

Total power entering the system is 9.4kW and the total charging power is 7.79 kW yielding overall system efficiency of 82.87%. Average absolute relative deviation from the average transmitted and received power per phase in this case is 3.94% and 2.95%. Applying the proposed balancing methods reduces the power transfer because in the initial condition system was operating with maximal duty cycle, so the only possibility was to decrease it during the balancing process. This could be overcome by operating with duty cycle lower than 1 in the case of aligned transmitter and receiver, leaving space for increasing the duty cycle in the case of misalignment. High frequency primary and secondary waveforms are omitted as they are very similar to the ones from the previous case. Same conclusion is valid for the grid currents as they are well balanced with high power factor and low THD.

Last test that was performed was the one with 24kW output power. This test is done in order to demonstrate the capabilities of the proposed converter topology. The clearance between transmitter and receiver in this case is 15 cm. High frequency waveforms of all the three phases of the inductive link are given

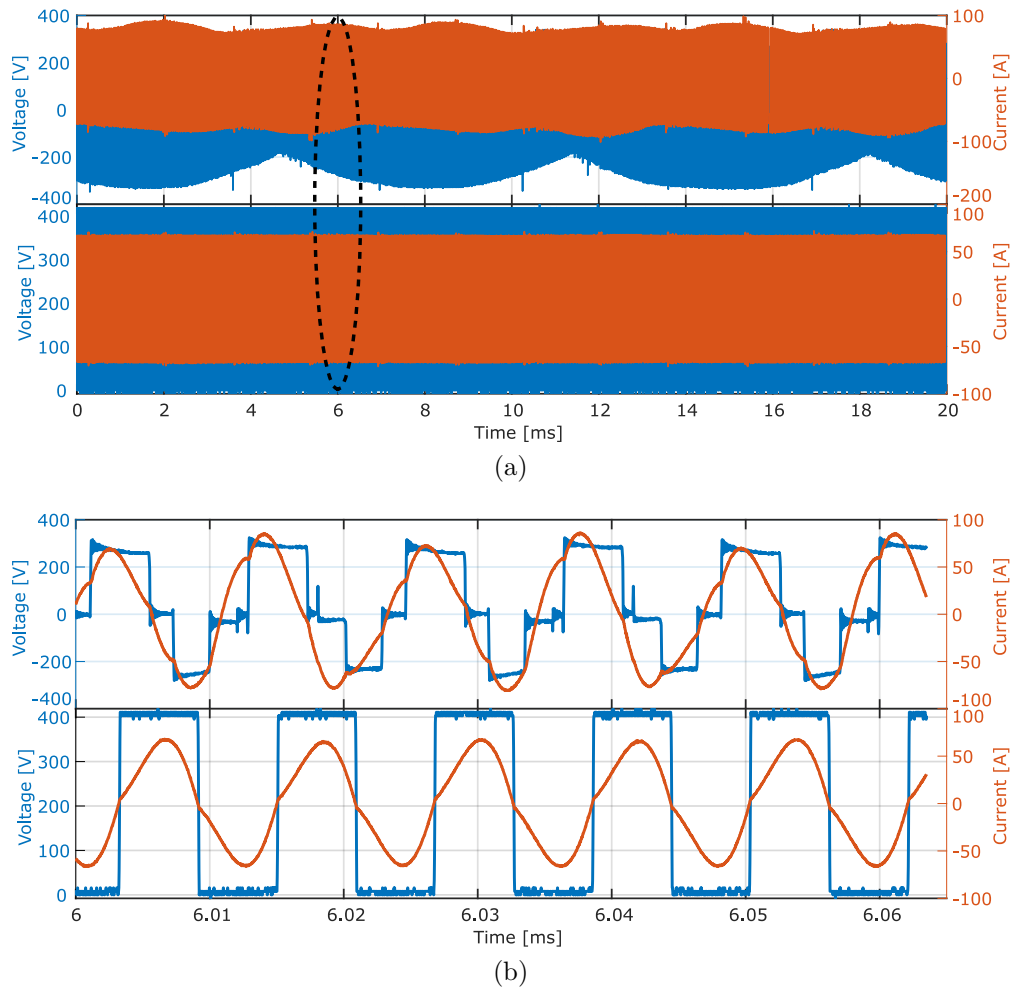


Figure 5.22

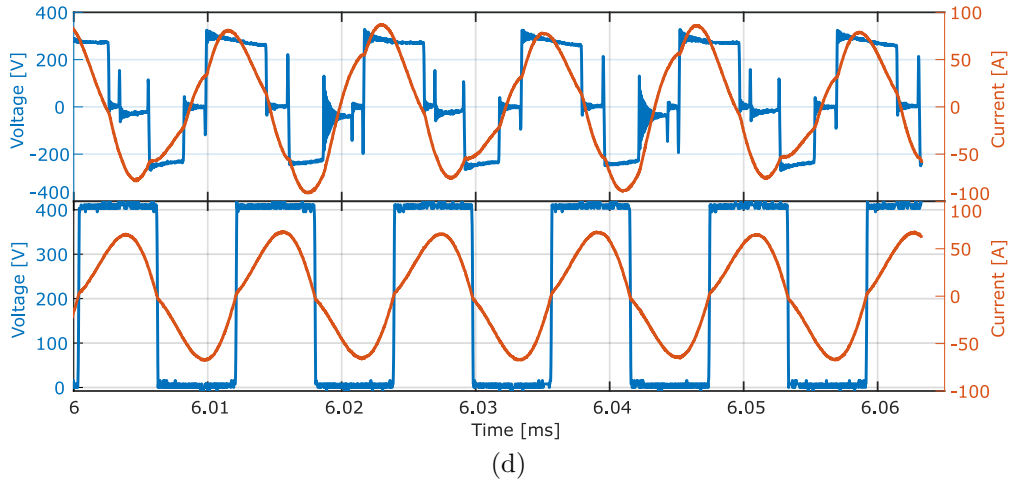
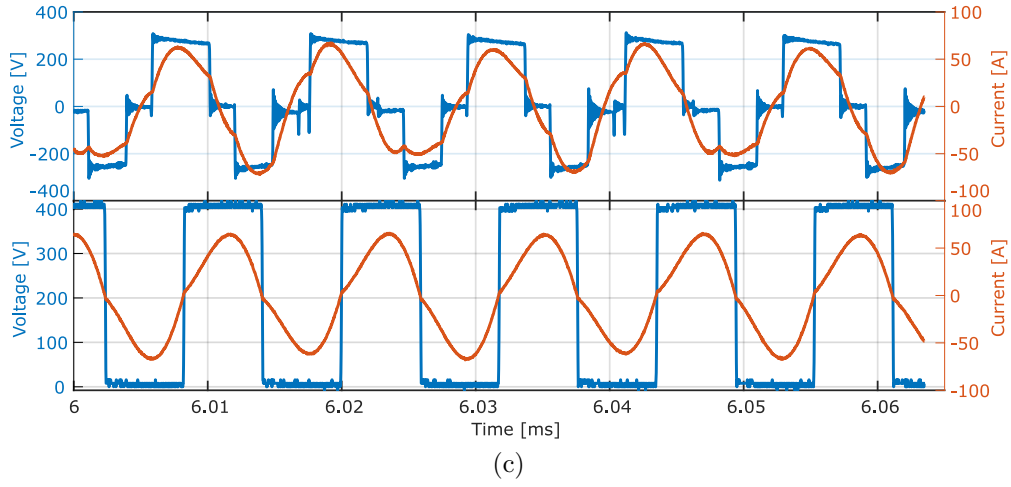


Figure 5.22: Aligned system with 23.87 kW of charging power a) Voltage and current of DD_1 coil over one grid period - primary (top) and secondary (bottom) b) Voltage and current of DD_1 coil in zoomed region c) Voltage and current of Q coil in zoomed region d) Voltage and current of DD_2 coil in zoomed region

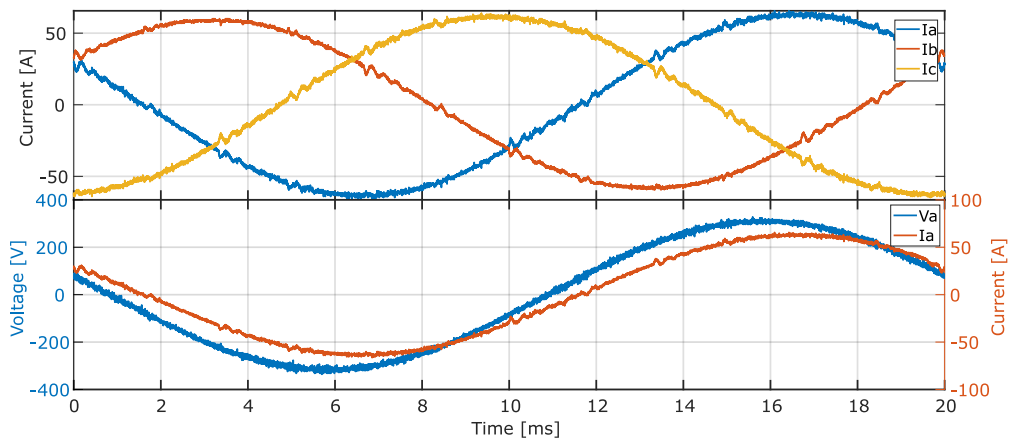


Figure 5.23: Grid currents (top); Voltage and current of the phase A of the grid (bottom) for the 23.87 kW of EV battery charging power

Parameter	Phase A	Phase B	Phase C
V_{rms} [V]	221.30	220.58	220.77
I_{rms} [A]	41.822	41.971	41.865
P [kW]	9.126	9.125	9.110
Q [kvar]	1.538	1.563	1.559
I_{thd} [%]	2.1	2.234	2.118
PF	0.986	0.986	0.986

Table 5.12: Relevant parameters of the grid with 23.87 kW of output power

Topology	Compensation strategy	Output Power	Efficiency	THD	PF
This work	Double-sided LCC	24 kW	86.42%	2.1%	0.986
Integrated [95]	Double-sided LCC	1.6 kW	91.5%	3.2%	1.0
Oak Ridge [94]	Double-sided LCC	20 kW	93%	9-10%	0.98-0.99

Table 5.13: Comparison with other single-stage Three-phase IPT chargers

in Fig. 5.22. Power that is being taken from the grid equals 27.62 kW while the power that is being delivered to the EV battery is 23.87 kW, resulting the system efficiency 86.42%. Grid currents and phase and current in phase A are given in 5.23. Parameters of the grid are given in Table 5.12.

Finally, it remains to give comparison of the presented work with the relevant solutions that already exist in the state-of-the-art. This is shown in Table 5.13. There are not many single-stage three-phase IPT chargers that can be encountered in the state-of-the-art. Both of them were discussed in Chapter 2 of this Thesis. Strictly speaking, only one of them [94] is completely three-phase, since the other one [95] has a three-phase transmitter but only a single-phase receiver, meaning that this work is one of the pioneering works in the area, dealing with single-stage three-phase IPT chargers. The power level of the presented solution is the highest one that can be encountered, accounting also the single-phase solutions that are presented in Table 4.5. THD and PF of the grid currents for the presented solution are fulfilling the grid code. Speaking about efficiency, as it was explained before in this Section, the utilized switches are not optimized for the application. Also the IPT link was not optimized for high efficiency, rather for low weight. Accounting for this information, and the proposed control methodology, it is clear that the idea presented in this Chapter of the Thesis presents a promising candidate for high-power AC/DC IPT charger for EV applications.

5.7 Conclusions

Key points of this Chapter are:

1. In order to increase power transfer capability and power density, a single-stage, compact, three-phase IPT charger based on DD²Q coil topology is proposed, where the IPT link is energized using a matrix converter (RTSMC) topology. Design methodology for the IPT coupler structure focusing on minimizing the system size and weight and maximizing the utilization of the employed materials is proposed. Modulation of the utilized converter is proposed, ensuring compliance of the system with the grid code.
2. Another key challenge that was addressed in this Chapter is the unbalance of the compact three-phase IPT chargers under misalignment conditions, where a control strategy is proposed based on balancing the power sharing of the phases, ensuring load equilibrium on both transmitter and receiver sides.

All of the proposed ideas were verified on a 24 kW prototype, resulting in overall system efficiency of 86.42%, achieving very low THD of the grid currents of 2.1% and near unity power factor of 0.986. It is also important to note that this work is one of the pioneering works in the domain of complex single-stage three-phase IPT systems, where it proposes original solutions to the existing challenges in the area, opening further research possibilities and path to industrial implementation of such systems.

Conclusions and Future Research Lines

His master replied, ‘Well done, good and faithful servant!...’

Matthew 25:23

6.1 Conclusions

THE topic of this Thesis are the wireless EV chargers that utilize principles of inductive power transfer. Three main areas were discussed including compensation strategies of the IPT link, single-stage converter topology solutions and three-phase IPT chargers. Focus was pointed at achieving high system efficiency and seamless control.

First of the ideas that is presented in this Thesis is an S-S-S compensated three-coil bidirectional EV charger with an intermediate coil that is presented in Chapter 3. The proposed topology and compensation method are convenient for high power applications due to the high efficiency of the system over the entire range of operating conditions.

Chapter 4 disseminates a single-stage bidirectional IPT charger that employs a Three-phase to Single-phase Matrix Converter. Challenges regarding utilization of the given converter are outlined and solutions are proposed.

IPT charger with a compact three-phase inductive link is the topic in Chapter 5. A single-stage solution utilizing Reduced Three-phase to Single-phase Matrix Converter for energizing each of the phases of the three-phase inductive link that is realized using DD²Q coil topology is presented.

All of the ideas and solutions that are proposed in this Thesis are thoroughly verified via extensive experiments. Three functional prototypes incor-

porating advanced converter topologies were developed for this cause. Power levels of the designed chargers vary from 3.3 kW to 30 kW. Efficiency of the proposed solutions is in the range of the highest efficiencies from the current state-of-the-art works, as it can be seen from the comparisons that are given in the Thesis. This makes the proposed ideas possible for potential use in the future EV applications.

Main contributions of this Thesis are:

1. A compensation technique based on the intermediate coil, that allows high system efficiency due to compensation of the magnetizing inductance, and seamless control of the system as the entire system is taken down to an equivalent inductor seen between the two voltage sources.
2. Control technique for achieving synchronous operation of the primary and secondary converters, that is independent on any communication between the two controllers that control the mentioned converters.
3. A single-stage IPT charger that utilizes matrix converter topology. A novel modulation technique for the employed converter is proposed and control methodology for the entire charger is devised.
4. A control technique for compact three-phase IPT charger that ensures power balancing across the phases of the system in the case of misalignment.

The previously listed innovations that are presented in this Thesis, are the solutions that we have proposed to the current challenges in the area of inductive charging of electric vehicles. Presented solutions tackle difficulties from different domains that are related to IPT charging. Designing an IPT EV charger is a multidisciplinary task, where challenges from several different engineering areas need to be considered in order to develop such a device. Another important aspect of this Thesis, is that it addresses problems related to different domains such as compensation of the system, converter topology and modulation, control of the system and topology of the inductive link, and it proposed innovative solutions to these problems. The proposed solutions allow for possible wider adoption of the advanced system topologies, both regarding topologies of converter and inductive link. When combined with presented control and modulation techniques, this Thesis shows a path towards enhancing the efficiency, reliability, control seamlessness and power density of the IPT EV charger, leading to its lower cost and higher availability for mass usage.

6.2 Future Research Lines

There are topics that are mentioned in this work that could be subject to the further research:

- In the Appendix A, a way to increase the power transfer capability of an IPT charger with an intermediate coil is presented. It relies on displacing the intermediate coil across one axis, in the direction of the expected misalignment. Further research in this direction can be conducted, investigating the optimal design of the intermediate coil in this case, analyzing the trade-off between the displacement of the coil and its current and varying the coil shape in order to achieve best coupling conditions between the intermediate coil and both transmitter and receiver structures.
- In Chapter 4 a modulation of the TSMC is presented. As it can be seen from the loss breakdown that is presented in the Experimental result section of the given Chapter, dominant losses are the switching losses of the TSMC. This is due to the fact that for driving each 4-quadrant switch, only one driver was used, simplifying the converter design and structure, however, disabling the possibility to achieve soft switching. One of the ways to enhance the proposed idea would be to utilize 12 drivers instead of 6, thoroughly analyze the current waveforms and improve the switching pattern in order to achieve soft switching transitions and improve system efficiency.
- Synchronization strategy between microcontrollers that is independent on any wireless communication between them is proposed in Chapter 4. In the future, it would be beneficial to examine the dynamic response characteristics of the proposed synchronization method, by analyzing the transient waveforms during changes in power/current reference and to implement a protection algorithm in case that the synchronization between the converters is lost, preventing any potential hardware failure.
- In the modulation strategy of the RTSMC that is utilized in Chapter 5, one of the switches exhibits two commutations over a single switching period. Detailed analysis to this issue is provided in the Appendix B. Future investigation on this topic would encompass analyzing the proposed alternative switching patterns that are proposed in this Appendix, focusing on the one based on having n consecutive normal patterns that are followed by n flipped patterns, disseminating the relation between n and the THD of the grid currents.

6.3 List of Publications

Several parts of this Thesis have already been published or are being submitted in international journals or conference proceedings.

6.3.1 Conference Papers

1. **N. Mirković**, Đ. Stojić, A. D. Exposito, P. Alou Cervera and M. Vasić, "Electric Vehicle Battery Charger Based on a Three-Phase to Single-Phase Matrix Converter for Inductive Power Transfer," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 1223-1228, doi: 10.1109/APEC48139.2024.10509262.
2. **N. Mirković**, A. D. Exposito, P. Alou Cervera and M. Vasić, "Design of a 11kW Three-Phase Inductive Power Transfer System Based on DD2Q Coil Structure," 2024 IEEE Applied Power Electronics Conference and Exposition (APEC), Long Beach, CA, USA, 2024, pp. 2893-2898, doi: 10.1109/APEC48139.2024.10509245.
3. **N. Mirkovic**, A. Delgado, P. Alou and M. Vasic, "Increasing Power Transfer Capability of Wireless Battery Charger Under Misalignment Conditions," PCIM Europe 2023; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 2023, pp. 1-8, doi: 10.30420/566091236.
4. **N. Mirkovic**, A. Delgado, P. Alou and M. Vasic, "Control of a Three-Phase Inductive Power Transfer System Based on DD(exp 2)Q Coil Topology," PCIM Europe 2024; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nürnberg, Germany, 2024, pp. 2483-2488, doi: 10.30420/566262349.

6.3.2 Journals Papers

1. **N. R. Mirković**, Đ. M. Stojić, A. Delgado, P. Alou and M. Vasić, "Novel Three-Phase to Single-Phase Matrix Converter Modulation Strategy for Bidirectional Inductive Power Transfer," in IEEE Transactions on Power Electronics, vol. 38, no. 12, pp. 14830-14846, Dec. 2023, doi: 10.1109/TPEL.2023.3309875.
2. **N. Mirković**, L. R. Chamorro, A. Delgado, P. Alou and M. Vasić, "30 kW Bidirectional Inductive Power Transfer Charger With Intermediate Coil for EV Applications," in IEEE Transactions on Power Electronics, vol. 39, no. 7, pp. 9007-9024, July 2024, doi: 10.1109/TPEL.2024.3389129.

Part I

Appendices

Adjusting the position of the auxiliary winding - a way to enhance the power transferring capability of the system

In Chapter 3, it was assumed that the tertiary winding has the same dimensions as the primary winding and that it is positioned on top of the primary, in the aligned position as it is shown in Fig. 3.4. In this appendix we will briefly discuss a possibility to enhance the power transferring capability of the system in the case of misalignment between the VA and GA.

In Fig A.1 it is depicted a position of the car at a parking lot, with the given GA and VA placement. If the placement of the GA and VA is done in such a way, that when the EV is at its right-most position GA and VA are aligned, it is clear that, along the x-axis, only possible and expected direction of misalignment would be alongside its negative part. In this Appendix we will analyze displacing of the auxiliary coil respective to the primary coil, in

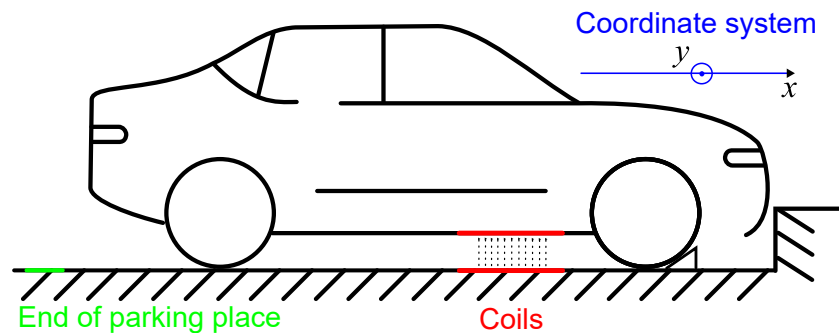


Figure A.1: Desired coil positions in a parking lot - expected misalignment to the negative side of the x-axis

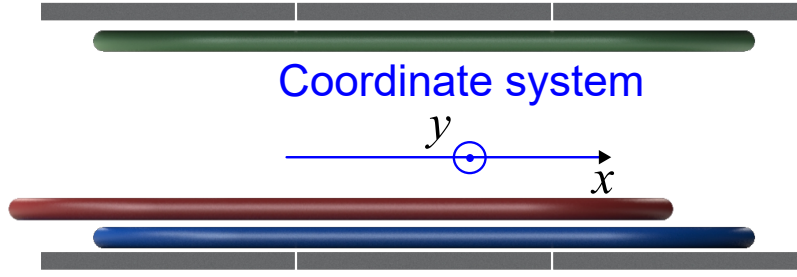


Figure A.2: Displacement of the tertiary winding along x-axis

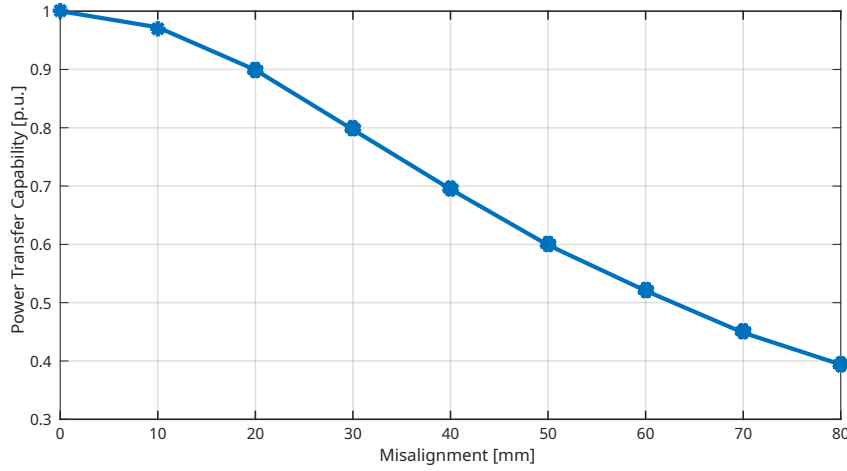


Figure A.3: Simulated change in the power transfer capability of the system with misalignment of the secondary in one axis while auxiliary winding is aligned with the primary

the same direction as is the expected misalignment of the secondary coil, and its effect on the power transfer capability of the system. 3D placement of the displaced auxiliary coil and secondary coil that is aligned with the primary is given in Fig. A.2. Misalignment of the secondary coil and displacement of the auxiliary coil are analyzed only alongside x-axis in this Appendix.

First question that arises is: How does the misalignment influence the parameters of the equivalent circuit of the system shown in Fig. 3.2b. In order to contemplate on this issue, it is necessary to analyze equations (3.7) - (3.12), that represent the correlation between the three coupled inductors, and the proposed equivalent circuit. By increasing the misalignment between the secondary coil and the GA, mutual inductances L_{ps} and L_{st} will start to decrease. This will lead to increase in the secondary leakage inductance and increase in the n_p/n_s transfer ratio. As the consequence, power transferring capability of the system that is determined by the equation (3.16), will be reduced. Fig. A.3 gives the dependence of the power transferring capability of the system and the misalignment, for a fixed value of clearance between the GA and VA.

A way to enhance the systems power transferring capability is to displace the auxiliary winding in the same direction as the secondary winding is mis-

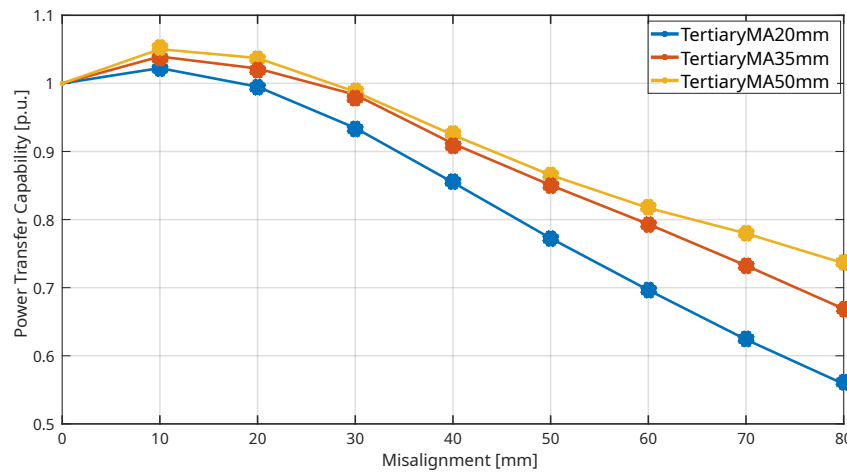


Figure A.4: Simulated change in the power transfer capability of the system with misalignment of the secondary in one axis while auxiliary winding is displaced respective to the primary

aligned. In that way the change in transfer ratio n_p/n_s is lower with the increase in misalignment, leading to higher power transferring capability of the system. This is depicted in Fig. A.4, where power transferring capability in dependence on the misalignment is given, for the 3 different systems, corresponding to the displacement of the tertiary coil of 20 mm, 35 mm and 50 mm. It can be seen that - larger the displacement of the tertiary coil - the power curve drops slower. For the displacement of 50 mm, the system is able to transfer around 74% of the nominal power, which comparing to 40% nominal power transfer given by the system where the auxiliary winding is centered, gives an increase of 85% in power transferring capability of the system. However, this comes at the prices of increased tertiary current, as displacing the tertiary coil reduces the mutual coupling between the primary and tertiary, L_{pt} , which, according to the equation (3.22), leads to the increase in the tertiary current, meaning more turns at the tertiary will be required for achieving the same current as before. Overall result is that the power transferring capability of the system is increased at the cost of having the VA rating of the auxiliary winding is increased.

Further Considerations on the Modulation of the RTSMC

The proposed modulation of the RTSMC fulfills all the given requirements, however it has one big drawback, and that is that one of the switches is commutating at double the fundamental frequency. This comes as a result of a trade-off between performance and number of employed semiconductor devices, as it was explained before in this Chapter. The question that we would like to discuss here is whether it is possible to avoid this switching at double the fundamental frequency.

There are 4 switches and 4 voltages at ones disposal for generating the output voltage of the RTSMC - U_a, U_b, U_c and 0. One thing is certain - in order to achieve current distribution across the phases of the grid that is required for low THD it is necessary to use all switches connecting the phases of the grid to the output. If any of them is not used there will be no current supplied to/from the given phase. This fact will be utilized only for brief periods of time, when a certain grid voltage is equal to zero, as during this time period, the current of that phase is supposed to be zero. Possibility of a repeatable sequence of a certain number of non-equal switching cycles is also discarded as there would be periods, where not utilizing one or two grid voltages during a certain switching period, would cause an unavoidable abrupt change in the phase of the RTSMC's output voltage. For these reasons, two cases will be analyzed in this Appendix:

1. RTSMC's output voltage is generated only using voltages U_a, U_b, U_c .
2. RTSMC's output voltage is generated using all available voltages, without repeating any of them two times within a switching period.

First, let us assume that the output voltage is generated without using the zero voltage. This waveform is given in Fig. B.1. The main problem with this

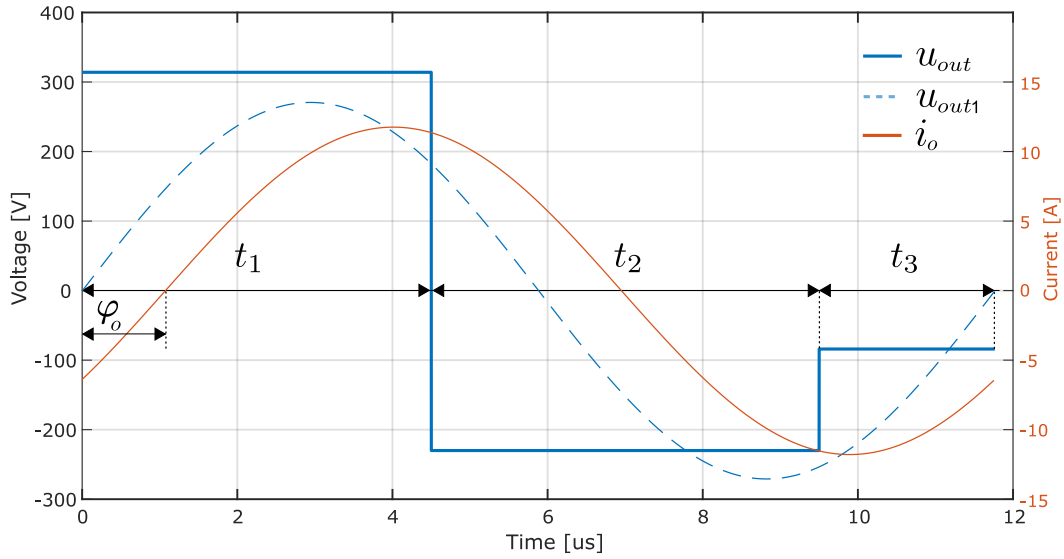


Figure B.1: Assumed waveform without utilization of the zero voltage

approach and why it is not applicable is that there are only two independent time variables - third one is determined by the switching period:

$$t_1 + t_2 + t_3 = 1/f_{sw} \quad (\text{B.1})$$

This means that there is a total of two variables for achieving all the tasks of the modulation - desired RMS and phase of the first harmonic of the output voltage as well as the distribution of the output current over the phases of the grid in the way that grid currents are proportional to the grid voltages. These requirements are defined by 4 equations (5.26), (5.27), (5.29) and (5.30). It is possible to demonstrate that if these time values are determined in the way to satisfy the tasks of having the desired RMS and phase of the first harmonic, the grid currents are not proportional to the grid voltages. In order to obtain sufficient variables for fulfilling all of the required tasks it is clear that it is necessary to use the zero voltage together with the grid voltages for generating the output voltage.

The voltage waveform where all four available voltage levels are used is given in Fig. B.2. In order to obtain 4 independent time variables it was necessary to split the zero sequence into two parts as it is shown in the mentioned Figure. However, this splitting does not affect the switching frequency of the switch used for obtaining the zero voltage as there is only a single commutation of this switch over a single period. The sum of all of the time values equals to a switching period:

$$t_1 + t_2 + t_3 + t_{z1} + t_{z2} = 1/f_{sw} \quad (\text{B.2})$$

This equation together with equations (5.26), (5.27), (5.29) and (5.30) forms

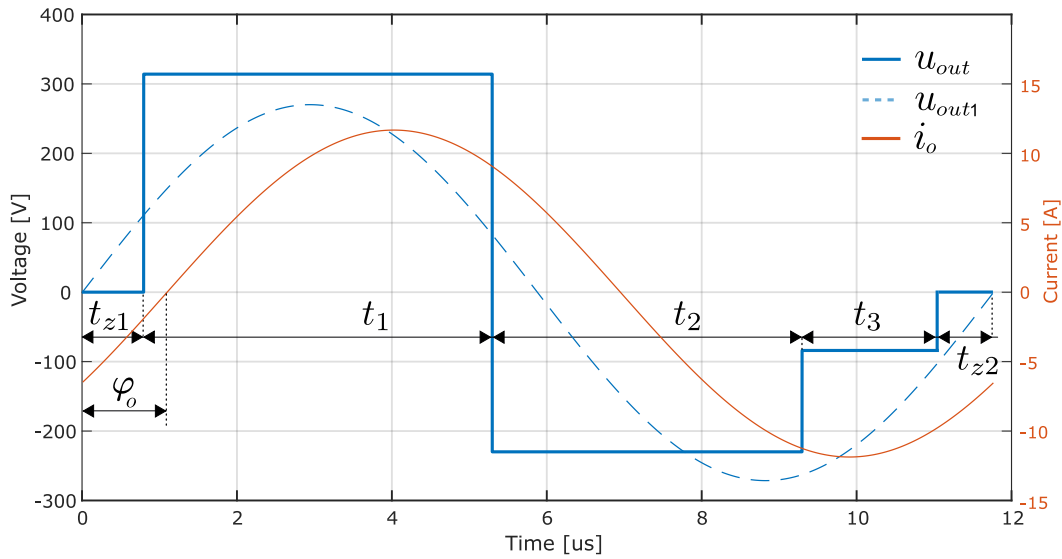


Figure B.2: Assumed waveform with utilization of the zero voltage

a complete system that is possible to solve using a software with a numerical solver such as MATLAB.

Now comes the question of dealing with active and reactive parts of the output current. There are two possible solutions to this problem:

1. Apply the flipping pattern in the way demonstrated previously Chapter 5.
2. Based on the measured phase delay of the output current φ_0 , respective to the first harmonic of the output voltage, determine the unknown time values t_1, t_2, t_3, t_{z1} and t_{z2} . This would require forming an array of solutions of the given times for different values of the phase delay φ_0 .

Instead of applying consecutively normal and flipped pattern, switching sequence is changed to applying normal - flipped - flipped - normal (i.e. normal - normal - flipped - flipped). This is depicted in Fig. B.4. Due to the properties of the normal and flipped patterns all of the tasks of the modulation would not be affected by this change in modulation. As it can be seen from the mentioned Figure, in the shown 4 switching cycles, switch that is commutating more than once per period would make a total of 5 commutations, further reducing the effective switching frequency of the given switch from 1.5 commutations per period to 1.25 commutations per period. This would lead to further improvement of the efficiency of the system and reduction of switching losses. This enhancement would come at a price. Namely, as it was stated before, reactive component of the RTSMC's output current is transformed into a high-frequency ripple with frequency equal to half of the fundamental frequency (42.5 kHz in our case) and this ripple is filtered out by the input LC filter. This was due to the fact that the average charge going to any of

the phases of the grid and that is consequence of the reactive component of the output current is equal to zero, as it is shown in Figs. 5.10 and 5.11. In the case of newly proposed switching pattern, average charge would be zero over 4 switching cycles instead of 2, reducing the frequency of the unwanted ripple to 21.125 kHz, meaning that better input filter is required in order to achieve same filtering effect as before. However, the frequency of this ripple is still high enough and easy to be filtered out by the input filter. On the other hand, improvement in the effective switching frequency is out of the highest importance, so there is a trade-off that one must consider.

Fig. B.3 shows the case of applying the flipping pattern to the waveform from the Fig. B.2. Because of the manner in which the flipping is performed - waveforms of each half-cycle are flipped around the central point of that half-period, in two consecutive switching period, the one with the flipped waveform would contain a double commutation of one of the switches. This means that one of the switches - which one depends on the Sector and Section, would commute in average 1.5 times per period (3 commutations per 2 fundamental periods). This is an improvement comparing to the main modulation that is analyzed in this Chapter as it reduces the effective switching frequency of one of the switches from 2 to 1.5, and it distributes this phenomenon across three switches instead of one, improving the loss distribution and thermal behavior of the system. However, there is one more way of enhancing the flipping pattern in this case and it is shown in Fig. B.4.

Previous analysis for applying normal - flipped or normal - normal - flipped - flipped patterns for generating RTSMC's output voltage can be generalized. Namely, it is possible to apply n times the normal pattern and then another n times the flipped pattern. Analogously to the previously outlined analysis, it is possible to show that this modulation pattern fulfills all the required

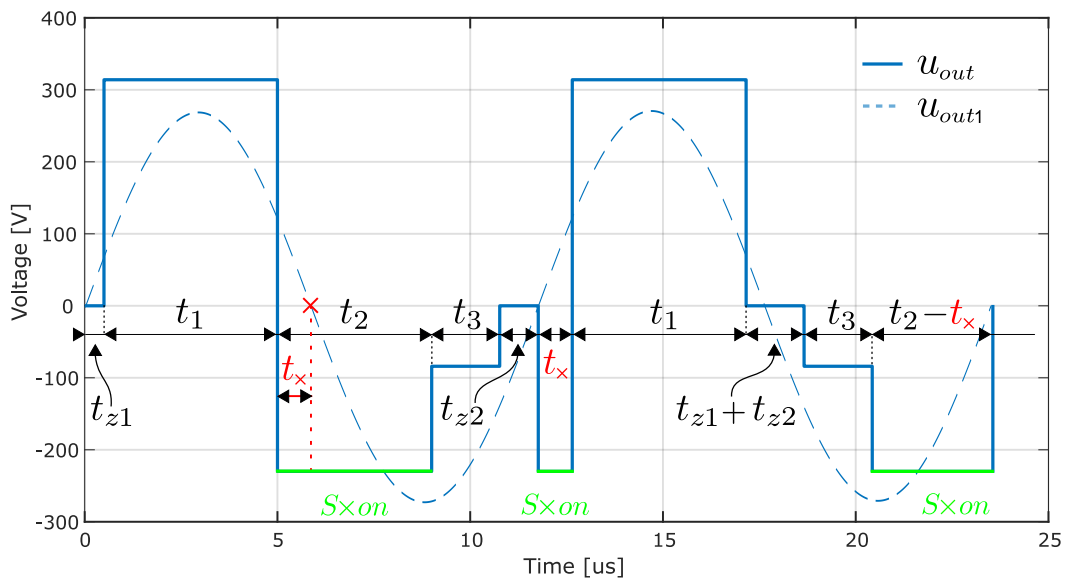


Figure B.3: Flipped waveform with utilization of the zero voltage - Mode 1

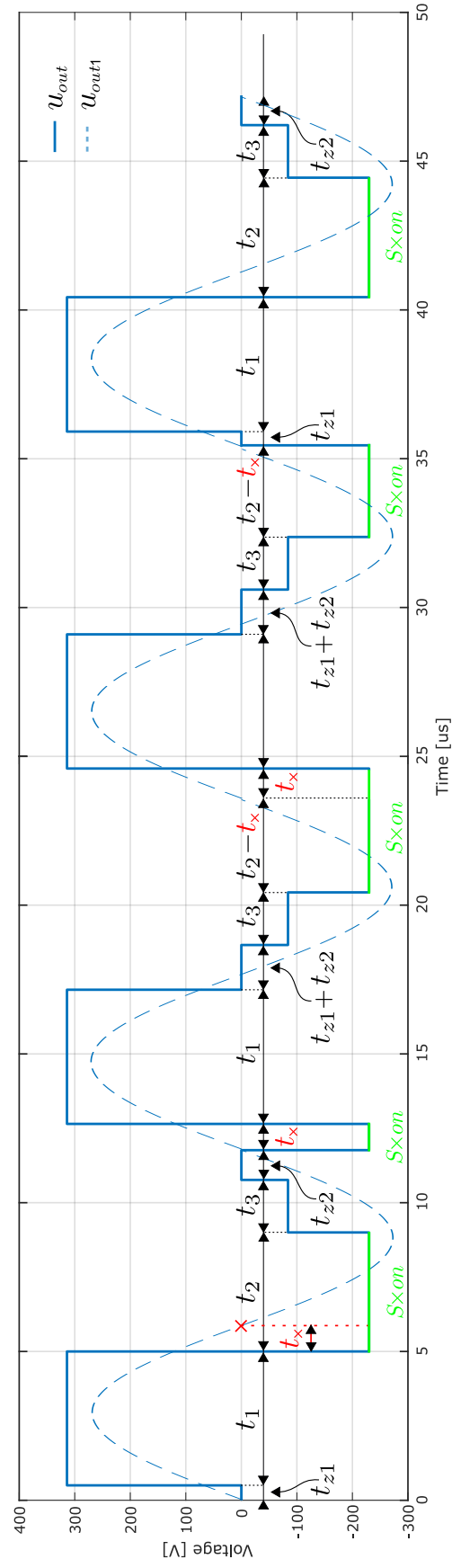


Figure B.4: Flipped waveform with utilization of the zero voltage - Mode 2

modulation tasks. The effective switching frequency of the switch with higher number of commutations would be equal to $(2n + 1)f_{sw}/2n$. Frequency of the ripple current obtained by processing the reactive component of the RTSMC's output current is equal to $f_{sw}/2n$. By increasing the number n , change in grid voltages over the entire repeating sequence that contains $2n$ fundamental periods becomes more and more expressed. For this reason, it would be necessary to analyze the impact of increasing number n on the modulation tasks. This analysis is out of the scope of this Thesis, and it is intended to be investigated in the future. With this said we conclude the analysis of the switching methodology that relies on flipping the normal waveform.

Second possibility for processing the active and reactive parts of the output current of the RTSMC is to measure the phase shift between the voltage and current of the RTSMC and to apply the time values t_1, t_2, t_3, t_{z1} and t_{z2} for the measured phase shift. This would require solving the system equations for different phase delays and storing this data in the memory of the employed microcontroller. Measuring of the phase shift between high frequency voltage and current may be challenging, although not impossible for the considered frequency range. A possibility to avoid measuring this phase-shift would be by measuring the grid current and calculating its THD. First, a certain value of the phase-shift of the RTSMC's output current is assumed. Then, a perturbation and observe method would be used, varying the assumed phase until the minimal THD is reached. This is a valid method as the function relating THD of the grid current to the assumed phase-shift of the RTSMC's output current to its voltage is monotonous function over the entire interval of considered phase-shifts $[-\pi/2, \pi/2]$. This solution is a good choice when the output current of the RTSMC is sinusoidal with low THD, i.e. when there is a little influence of the higher-order harmonics. The explanation to this is given in the following subsection.

B.0.1 Influence of the flipping pattern on the distribution of the higher-order harmonics of the RTSMC's output current over the phases of the grid

Both in this and in the previous Chapter, when deriving the modulation for the considered converters, it was assumed that their output current is sinusoidal and its higher-order harmonic content was neglected. However, this is not completely accurate as these harmonics exist due to the fact that they exist in the excitation voltages. Their presence can be seen in the presented experimental waveforms. The amount of higher-order harmonics in the matrix converter's output current, expressed through its THD, depends on the several operating conditions and system properties:

1. Active power that is being transferred - lower the power transfer, the

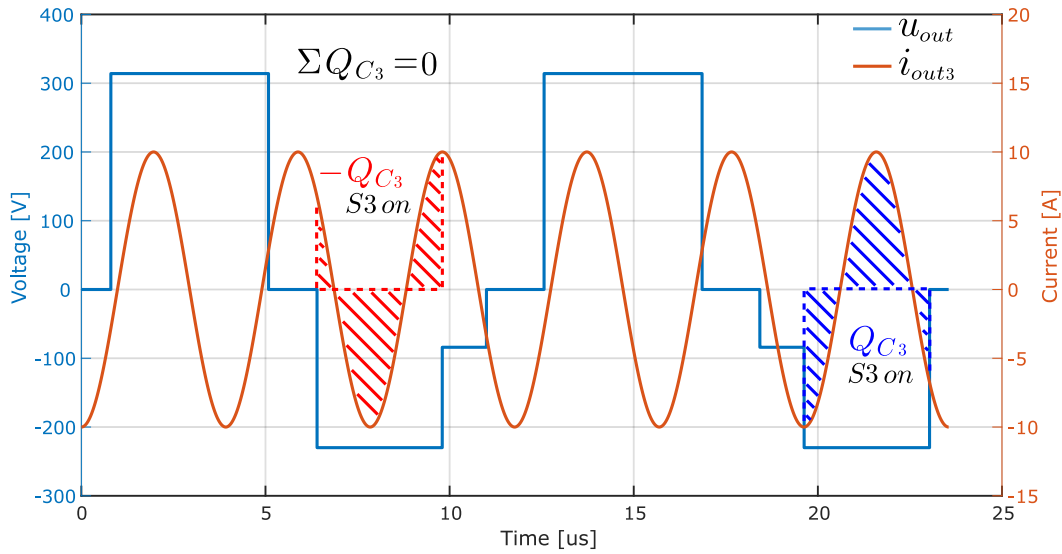


Figure B.5: Influence of the flipping pattern on third harmonic of the RTSMC's output current in Even Sectors - example grid phase C, Sector VI, Section 12

higher the THD

2. Excitation voltages
3. Compensation strategy and parameters of the resonant circuit

The precise calculation of the higher-order harmonic components in the output current of the considered matrix converters, whether TSMC or RTSMC, is not a trivial task and would include a lot of thorough mathematical analysis of the system. For the reasons mentioned above, we know that these harmonics exist, and what we want to analyze is their influence on the THD of the grid currents, once that they are processed by the proposed converter modulations that includes the flipping pattern. The analysis will be given for the modulation of the RTSMC, while in the case of TSMC it is completely analogous.

The dominant nature of the higher-order harmonics in the current is reactive, respective to the same higher-order harmonic in the voltage that they correspond to. This comes as the consequence of the frequency characteristics of the resonant network, thus allowing for the first-order harmonic approximation that was utilized for calculating the active power transfer through the entire Thesis. This means, that the proposed flipping pattern will have the same effect on the higher-order harmonics in the RTSM's output current as it has on the reactive part of the same current. Mathematical proof to this claim is similar to the one provided in Section 4.3, where instead of frequency ω there should be $\eta\omega$, where η is the order of the analyzed odd higher harmonic. For this reason, the strict mathematical proof is omitted and only a relevant figure is presented, in order to visualize this effect. The Figure B.5

provides this visualization. In this figure, the influence of the flipping pattern on the third harmonic of the RTSMC's output current is depicted. As the total charge over two switching periods is equal to zero, this means that the proposed flipping pattern successfully processes the third harmonic in the output current, transforming it into a high frequency ripple. This conclusion is valid for all of the higher-order harmonics in the output current.

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