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A GaN-on-SiC Transmit/Receive MMIC Frontend for 6-to-18-GHz Phased Array Transceivers

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***Abstract*—This work presents a monolithic transmit/receive (T/R) frontend for the 6–18-GHz band, implemented in 150-nm gallium-nitride (GaN) technology. Single-die integration is leveraged by co-designing all subcircuits: the T/R asymmetric switch simplifies the transmit (Tx) path to save for Tx output power and efficiency, while its receive (Rx) branch merges into the low-noise amplifier input matching network for compactness and reduced noise. On-wafer measurements show an average Tx output power of 9.5 W (minimum 5.6 W) with 19.4% efficiency (minimum 13.5%) across the band. In Rx mode, the prototypes exhibit over 21 dB gain with an average noise figure of 3 dB (maximum 3.3 dB). These metrics compete with the state of the art of ultrawideband GaN-based single-chip T/R frontends.**

***Index Terms*—Gallium nitride, HEMTs, III-V semiconductor, low-noise amplifiers, power amplifiers, ultra wideband radar.**

I. Introduction

MONOLITHIC microwave integrated circuits (MMICs) compacting the most critical radiofrequency (RF) functions of a transceiver frontend (FEM)—such as high-power amplification (HPA), low-noise amplification (LNA), and RF path selection—are key for advancing next-generation active phased array systems. Compared to prevailing gallium-arsenide (GaAs) solutions, gallium-nitride (GaN) high-electron-mobility transistors (HEMT) offer superior power density and breakdown voltage. These features lead to efficient HPAs with smaller footprints and robust LNAs without additional protection circuitry, enabling compact FEMs delivering higher power and similar noise figure (NF) to GaAs [1]–[6].

While several GaN MMIC FEMs have been reported for S-, C-, X- and Ku-bands [5]–[9], literature on ultrawideband FEMs spanning the C-to-Ku band remains limited. To date, only [2], [4], [10] describe such MMIC designs. In contrast, C-to-Ku GaN HPA, LNA and switch are well-documented as isolated MMICs [11]–[16]. However, co-integrating these subcircuits into a single die poses additional challenges, including tradeoffs in die size, circuit complexity, and transmit/receive (T/R) isolation.

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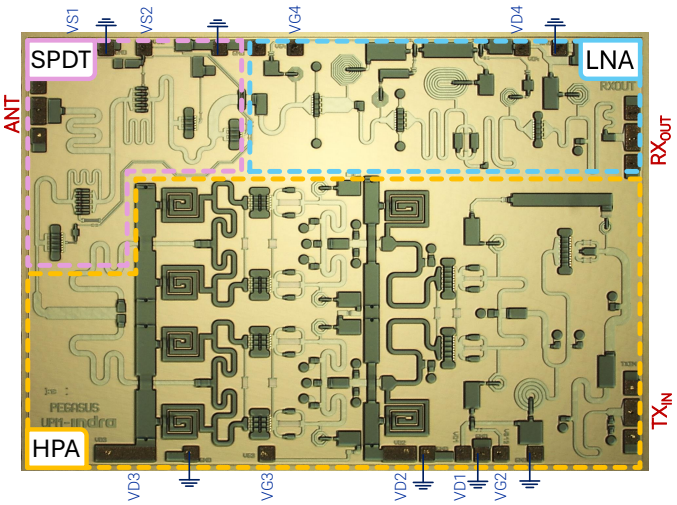

Fig. 1. Photograph of the prototyped MMIC with area of 5×3.5 mm^2.

This work presents a T/R FEM MMIC implemented in a 150-nm GaN-on-SiC process by United Monolithic Semiconductors. The FEM design targets half-duplex operation from 6 GHz to 18 GHz, comprising an HPA for transmission (Tx), an LNA for reception (Rx), and a single-pole double-throw (SPDT) switch for T/R commutation (see Fig. 1).

II. Design

The MMIC was specified in the 6-to-18-GHz band, targeting a Tx power and gain higher than 37 dBm and 18 dB, respectively, and a Rx gain of 20 dB with NF above 3 dB. It was developed using Advanced Design System and its associated electromagnetic solver, Momentum.

A. SPDT Design

The proposed SPDT switch, presented in Fig. 2, exploits the fully integrated approach by adopting an asymmetric topology, which saves for Tx output power, power-added efficiency (PAE), and die space as compared to symmetric designs [4], [6]. The Rx path includes an inductively resonated series device (S1 = 8×40 µm wide) cascaded to two shunt HEMTs (S2 = 6×68 µm, S3 = 6×75 µm), which are co-designed with the LNA to reduce noise and provide over 30-dB isolation (see Sec. II-B). The Tx path is simpler, comprising an inductively

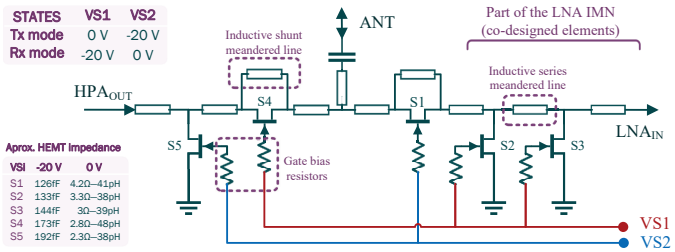

Fig. 2. Circuit schematic of the asymmetric SPDT switch. Ports LNA_{IN} and HPA_{OUT} are connected to the input port of the LNA (Fig. 3a) and the output port of the HPA (Fig. 4a), respectively.

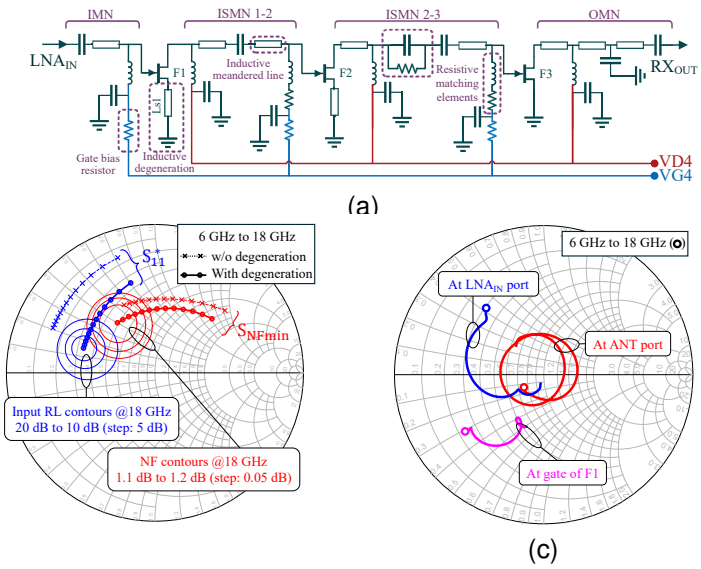

Fig. 3. LNA design: (a) circuit schematic of the three-stage LNA, (b) maximum gain (G_{max}), minimum noise figure (NF_{min}), and return loss referred to Z_{opt} (NRL) of F1 at 18 GHz with and without source degeneration (L_{s1}), and (c) input reflection coefficient throughout the receiver. Biased at VD4 = 7.5 V and 190 mA/mm. Port LNA_{IN} connects directly to the SPDT switch (Fig. 2).

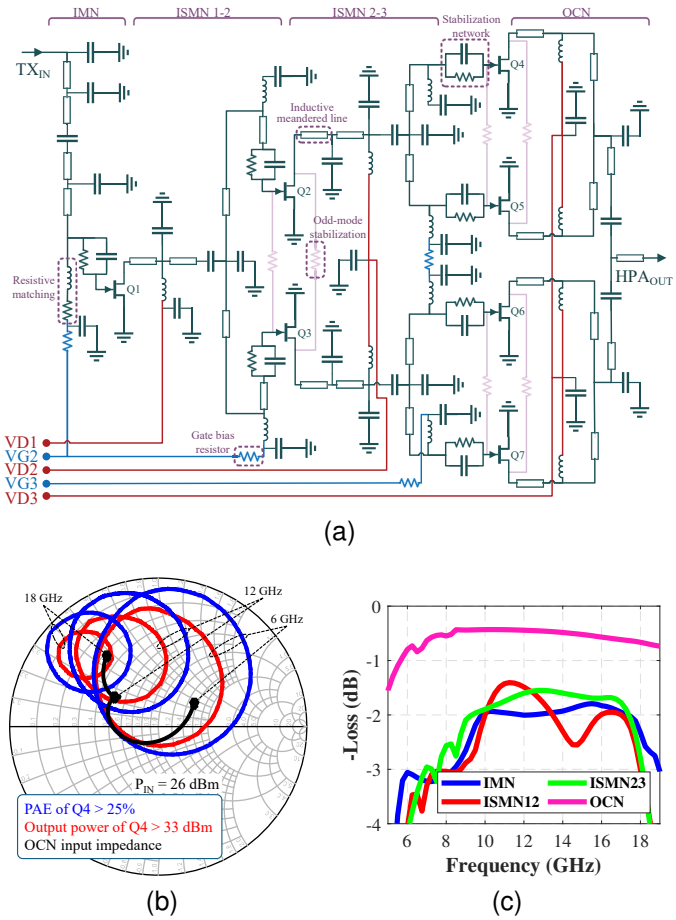

Fig. 4. HPA design: (a) circuit schematic of the three-stage corporate HPA, (b) load-pull and synthesized load impedance for a stabilized third-stage transistor biased at VD3 = 25 V and 14 mA/mm, and (c) additional loss of the input matching, interstage matching and output combining networks (IMN, ISMN, OCN). Port HPA_{OUT} connects directly to the SPDT switch in Fig. 2.

resonated series device (S4 = 8×60 µm) and a shunt HEMT (S5 = 8×75 µm), which are sized for an input 1-dB compression point over 42 dBm—higher than the expected power at the HPA_{OUT} port. The SPDT achieves small-signal insertion loss below 1 dB in Tx mode and 1.2 dB in Rx mode. The active path is set by the DC control voltages VS1 and VS2.

B. LNA Design

Considering the switch insertion loss, the LNA shall achieve an NF below 1.8 dB, with an associated linear gain of at least 21.2 dB. To meet these targets, the LNA adopts the three-stage cascaded topology illustrated in Fig. 3a. It operates with a drain voltage of 7.5 V and DC current density of 190 mA/mm.

Special design emphasis is placed on the first stage, which here employs inductive source degeneration (L_{s1}) to bring the input impedance (Z_{in}) closer to the conjugate of the optimum source impedance for noise (Z_{opt}) [17]–[19]. As shown in Fig. 3b, F1 device (8×36 µm) and L_{s1} (85 pH) are chosen to deliver simultaneous noise and input impedance matching, with realizable NF below 1 dB and available gain above 10 dB.

Another key focus to achieve a low-noise design is to keep a simple input matching network (IMN) with minimal loss [11]. Here, this is attained by removing the arbitrary constraint of a 50-Ω impedance at the switch-to-LNA interface. Fig. 3c illustrates how the off-state capacitances of the shunt devices of the switch (S2, S3) play a significant role in matching the receiver input to 50 Ω at mid-to-high frequencies, while the gate bias inductor of F1 supports the low-frequency matching.

Resistive elements are avoided both in the IMN and the F1-to-F2 interstage matching network (ISMN) to maintain low noise. The second and third stages are designed to meet the Rx gain, linearity, and DC consumption goals of the receiver.

C. HPA Design

The HPA circuit topology is presented in Figure 4a. It implements a three-stage corporate scheme with four parallel, common-source transistors at the last stage. Accounting for the switch loss (∼1 dB) and assuming a 1-dB insertion loss for the output combining network (OCN), each last-stage transistor should output at least 33 dBm across the band of interest, to ensure the target Tx output power of 37 dBm. With this goal, the last stage comprises four devices (Q4-7) with 6×142 µm periphery, biased for optimal power dissipation and PAE at VD3 = 25 V and 14 mA/mm. Fig. 4b illustrates

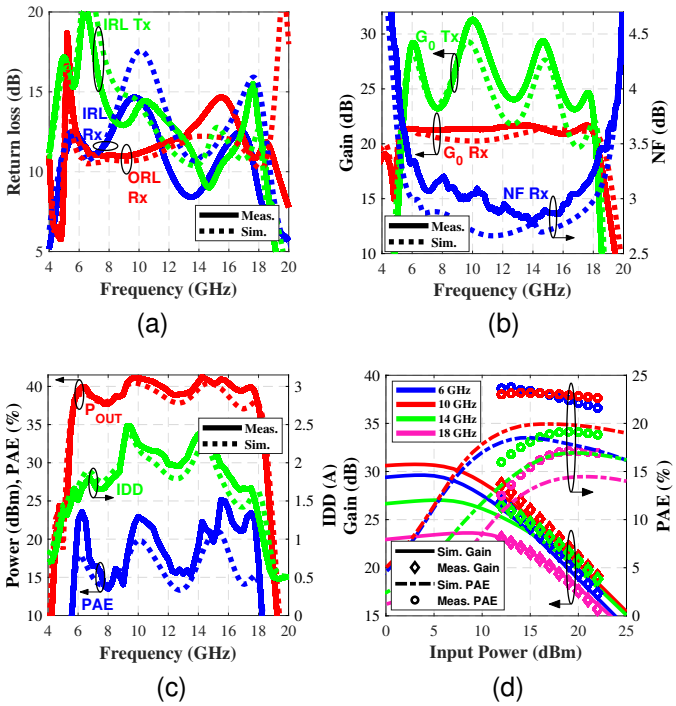

Fig. 5. Measured on-wafer performance (typ.) vs. simulations: (a) small-signal input/output return loss (IRL/ORL), (b) small-signal gain (G_0) and Rx noise figure (NF), (c) Tx large-signal performance for input power P_{IN}=19 dBm, and (d) Tx PAE and gain as a function of P_{IN}. DC bias for the Tx mode: VD1 = VD2 = VD3 = 25 V and $ID_{Q,Tx}$ = 525 mA. DC bias for the Rx mode: VD4 = 7.5 V and $ID_{Q,Rx}$ = 190 mA. Large-signal meas.: 30 µs/300 µs pulses.

the optimum load impedance region for a final-stage transistor, stabilized with an input RC circuit. The OCN input impedance is designed to lie within this region. To meet the gain specification, two driver stages are also implemented to deliver about 26 dBm to the third stage. They comprise one and two parallel transistors (Q1 = 12×56 µm, Q2-3 = 10×65 µm), respectively, and require a DC bias of VD1 = VD2 = 25 V and 250 mA/mm.

The simulated additional losses by the IMN, ISMN, and OCN networks are depicted in Fig. 4c. These networks include the reactive effects of all elements required for DC biasing.

III. Results

Figures 5a and 5b depict the small-signal performance of the MMIC. In Rx mode, it achieves a linear gain (G_0) higher than 21 dB with fluctuation below ±0.4 dB across the target bandwidth, and input and output return losses (IRL, ORL) better than 8.5 dB and 10.8 dB, respectively. In Tx mode, IRL and G_0 exceed 9 dB and 23 dB, respectively. Overall, the measured curves align closely with the simulations, with the exception of the IRL for the Rx mode, which has shifted at high frequencies, thereby reducing the bandwidth.

Figure 5b presents the noise figure of the receiver, including the switch. When measured at room temperature, the prototypes feature an average NF of 3 dB across the 6-to-18-GHz band, with a maximum of 3.3 dB at low frequencies. This is about 0.1 dB to 0.2 dB higher than expected from simulation.

Figure 5c presents the large-signal performance in Tx mode for an available input power (P_{IN}) of 19 dBm at the TX_{IN} port.

TABLE I
Literature on single-die GaN-based T/R frontends.

Parameter [a]	[2]	[4]	[10]	This work [b]
Freq. range [GHz]	5.5 – 18	2 – 18	4 – 18	6 – 18
Tx P_{OUT} [dBm]	∼36 {37.4}	38.2	34 {35.1}	37.5 {39.8}
Tx PAE [%]	∼8 {9.1}	7	16.6 {22.1}	13.5 {19.4}
Tx sat. gain [dB]	10 {11.4}	9.5	21 {22.1}	18.5 {20.8}
Rx NF [dB]	—	3.5	3.5 {3.15}	3.3 {3}
Rx lin. gain [dB]	-4	∼17 {18}	24 {24.6}	21 {21.4}
Tx P_{DC} [W]	{50}	—	17.4 {14.6}	62 {49}
Size [mm×mm]	6.3×4.3	3.2×2.5	5×3.5	5×3.5
Technology	250 nm GaN/SiC	100 nm GaN/Si	150 nm GaN/SiC	150 nm GaN/SiC

[a] The parameters listed denote the minimum values within the published bandwidth, with the exception of "Rx NF" and "Tx P_{DC}" which indicate the maximum values. The typical or average values across the band are shown inside curly brackets. Symbol "∼" indicates an estimate from reported graphs.
[b] Tx values for an input power of 19 dBm at the TX_{IN} port.

The results are better than expected from simulation, especially at the upper edge of the band: average output power at the ANT port is 39.8 dBm (9.5 W) across the target bandwidth from 6 GHz to 18 GHz, with a minimum of 37.5 dBm (5.6 W) at 18 GHz. This corresponds to a saturated transducer gain exceeding 18.5 dB. The DC current consumption under RF operation is 1.95 A, yielding an average PAE of 19.4% across the 6-to-18-GHz band, with a minimum of 13.5% at 8 GHz.

Figure 5d presents the measured and simulated Tx saturation performance. On average, the PAE peaks for a P_{IN} level between 19 dBm and 20 dBm (see Fig. 5c for performance at P_{IN} = 19 dBm). Dynamically optimizing P_{IN} for each frequency point would further increase the average and minimum PAE to 19.7% and 14.2%, respectively. At P_{IN} = 19 dBm, the average gain compression is 5.5 dB, exceeding the simulated value of of 4.8 dB.

IV. Conclusion

A 6-to-18-GHz GaN-on-SiC MMIC has been presented which integrates both high-power and low-noise amplification within a single-chip solution, as well as Tx–Rx switching. On-wafer measurements demonstrate competitive performance compared to the reported literature detailed in Table I. Notably, this work exhibits an average output power of 39.8 dBm (9.5 W), exceeding 37.5 dBm (5.6 W) across the entire target bandwidth. This is 4.7 dB higher than a previous design by the authors [10]. The lower Tx efficiency with respect to [10] can be attributed to the addition of a protection polymer film for low-cost encapsulation. This film also degrades the Rx noise figure. Comparative analysis with other documented works [2], [4] reveals a similar output power for the Tx mode, but a significantly higher efficiency and gain in this design. Furthermore, the prototypes exhibit a remarkable sensitivity for the Rx mode, with NF below 3.3 dB over the entire band (average of 3 dB), representing the lowest reported NF value among comparable all-GaN single-die frontends.

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