electronics

MDPI

Article

A Simple Single-Ended Post-Fault Location Technique for DC Lines Based on Controlled Re-Energizations

Kumar Mahtani [1,*], José M. Guerrero [2], Julien Decroix [3] and Carlos A. Platero [1]

[1] Department of Automation, Electrical and Electronic Engineering and Industrial Informatics, Escuela Técnica Superior de Ingenieros Industriales, Universidad Politécnica de Madrid, 28006 Madrid, Spain; carlosantonio.platero@upm.es
[2] Department of Electrical Engineering, Escuela de Ingeniería de Bilbao, Universidad del País Vasco, 48013 Bilbao, Spain; josemanuel.guerrerog@ehu.eus
[3] Interdisciplinary Research Group in Energy Modeling, Paris-Saclay University, 91190 Gif-sur-Yvette, France
* Correspondence: kumar.mahtani@upm.es

Abstract: Fault location in medium-voltage direct current (MVDC) systems is an essential yet underexplored area compared to high-voltage (HVDC) and low-voltage (LVDC) systems. MVDC systems, characterized by intermediate line lengths and fault resistances, as well as rapid fault clearance requirements, demand specialized solutions. This paper proposes a novel single-ended, offline fault location method based on controlled re-energizations after fault clearance. This approach employs a switched grounding resistor and a bypass connection through the current-limiting inductor to extract fault parameters from the discharge curves of two re-energization cycles. By analyzing the time constants derived from these curves, the method estimates fault location and resistance with high accuracy. The proposed method eliminates the need for additional active injection sources and circuit breaker modifications, ensuring seamless integration into existing MVDC infrastructure. Furthermore, the method avoids inter-terminal communication delays and sampling delays before fault clearance. Validation through electromagnetic transient simulations demonstrates fault location errors below 5% for fault resistances up to 50 Ω. Results show that the method performs better for faults farther from the active terminal, with the higher errors seen for short distances and elevated resistances. The proposed technique offers a robust and practical solution for post-fault location in DC lines.

Keywords: DC lines; fault location; inductance; injection; impedance; medium-voltage direct current; reclosing; single-ended; time constant

Academic Editor: Nilanjan Ray Chaudhuri

Received: 18 December 2024
Revised: 7 January 2025
Accepted: 10 January 2025
Published: 11 January 2025

Citation: Mahtani, K.; Guerrero, J.M.; Decroix, J.; Platero, C.A. A Simple Single-Ended Post-Fault Location Technique for DC Lines Based on Controlled Re-Energizations. *Electronics* **2025**, *14*, 275. https://doi.org/10.3390/electronics14020275

1. Introduction

The increasing adoption of direct current (DC) lines in modern power systems highlights their critical role in achieving efficient and reliable energy transmission [1]. DC lines can be broadly classified into three main categories based on their voltage levels: high-voltage DC (HVDC), medium-voltage DC (MVDC), and low-voltage DC (LVDC). Each category serves distinct applications and exhibits unique technical characteristics.

HVDC systems [2], operating at voltage levels typically above 100 kV, are primarily used for long-distance power transmission and to interconnect asynchronous grids. Their ability to minimize power losses over extended distances makes them an optimal choice for bulk energy transfer. The technical intricacies of HVDC systems include the use of complex control schemes for power flow, the employment of sophisticated converter technologies (e.g., line-commutated converters and voltage-source converters), and the need for robust insulation to handle high voltages.

LVDC systems [3], operating at voltages below 1 kV, are predominantly used for localized applications. These applications include residential and commercial systems, microgrids that enable decentralized power generation and consumption, and the charging and operating of electric vehicles and other transportation systems. The main advantages of LVDC systems include reduced energy losses in conversion processes and compatibility with renewable energy sources such as solar photovoltaics. However, the relatively low voltage levels require careful design to mitigate issues such as voltage drops and to ensure safe operation.

In recent years, systems operating at voltage levels ranging from 1 kV to 100 kV, known as MVDC systems, have gained attention due to their flexibility and efficiency in medium-scale power distribution [4,5]. MVDC systems are particularly suited for distributed renewable energy integration [6], ensuring power distribution as support for microgrids and smart grids [7], and for marine and other off-shore distribution and subsea applications [8]. MVDC systems bridge the gap between HVDC and LVDC applications, offering flexibility and efficiency for medium-scale power distribution. However, they pose unique challenges, such as the need for fast and reliable protection systems, or compact and cost-effective converters.

Across all categories of DC systems, faults can occur due to insulation breakdown, external interference, or the aging of components [9]. Faults systems propagate more rapidly in DC than in AC systems owing to the absence of zero crossings in the current waveform, which complicates current interruption. Consequently, effective fault detection, isolation, and location are vital for maintaining system integrity and minimizing downtime. In particular, fault location ensures the rapid restoration of the isolated faulty line into the DC system. However, the literature has mainly covered fault location for LVDC and HVDC lines, while fault location for MVDC lines remains a relatively underexplored area [7].

Generally, LVDC systems are characterized by short lines (<1 km) and low fault resistance values (<5 Ω). Fault location in LVDC systems often focuses on cost-effective single-terminal methods. These methods operate without requiring data exchange between terminals, thereby eliminating the need for communication infrastructure. Nevertheless, the accuracy of single-terminal fault location techniques is intrinsically affected by the fault resistance. Passive methods based on local measurements in protective devices have been extensively proposed, using the attenuation characteristics of current, related to the inductance, as a marker of the fault distance [10–12]. Conversely, the most widespread active technique involves the use of probe power units, which are utilized as external injection devices [13–15]. This impedance-based technique is based on the use of the discharge of a probe capacitor in the faulty RLC circuit to locate a fault. Alternatively, fault location modules, consisting of a simple RL circuit, two switches, and two thyristors, have been proposed to achieve accurate fault location [16]. Another area of research in single-ended fault locations methods is centered on modifications of the DC circuit breaker technology, either to add additional passive elements to form a fault location loop [17], or to include active elements for current injection [18].

On the other hand, HVDC lines are related to long transmission distances (>100 km) and the possibility of high fault resistances (>50 Ω), necessitating the use of more advanced methods. Accordingly, connected to greater investment costs into these infrastructures, double-terminal or multi-terminal methods are more suitable for fault location. However, some single-ended fault location methods exist in the field of HVDC to avoid communication delays, and are the predominant techniques related to traveling wave analysis [19–23]. These techniques are highly accurate and effective for long-distance HVDC lines, but require sophisticated high-speed measurement systems and significant computational resources. Also, time-domain reflectometry, which involves injecting a signal into the line and

analyzing the reflected waveform to identify fault characteristics, is particularly effective for offline analysis [24]. The requirement for specialized costly equipment for detecting and measuring the high frequency waves and calculating their reflections is the main drawback of these methods. Furthermore, impedance-based methods involving active signal injection have been proposed for single-ended fault location in HVDC lines [25,26], although these require changes in the control strategy of the converter during the reclosing stage.

The mentioned methods address LVDC and HVDC. In contrast, MVDC lines have the following intricacies [7,27]:

- They have shorter lines than HVDC (between 1 and 100 km) systems, which jeopardizes the use of traveling-wave-based methods as wave propagation times are reduced.
- They have higher fault resistances than in LVDC (generally up to 50 Ω), which hinders the use of passive and active impedance-based methods.

In this regard, MVDC systems, with intermediate line lengths and fault resistances, and stringent requirements for rapid fault clearance, present unique challenges that require tailored solutions. A research gap exists in this field [28]. In fact, a limited number of references have addressed fault location in DC lines in the length range of 1–100 km and fault resistances in the range of 0–50 Ω. The first attempts involved communication links between relays [6], which necessarily introduce a communication lag and an additional source of contingencies. In recent years, active impedance estimation has been applied for fault location [29]. An additional unit is used to inject sinusoidal signals at two distinct fundamental frequencies before fault clearance. This method introduces a delay in fault clearance and relies on the wavelet packet decomposition of the voltage and current signals, resulting in a computational burden. In [30], a highly accurate method is proposed based on the evaluation of the line inductance provided from fault current fitting. However, this technique requires additional voltage sensors and several calculations steps, and also introduces a delay in fault clearance in order to capture enough points for fitting.

On the other hand, offline methods present an opportunity for detailed fault analysis without interfering with real-time operations. Several offline methods, suitable for the length and fault resistance values typical of MVDC lines, have been proposed. These methods are related to the reclosing of DC lines, which is a usual operation in distribution lines. As stated in [31], most of the reclosing schemes are based on traveling-wave analysis. These methods require high-performance equipment and are affected by a dead zone in the case of near-end or remote end. These methods can be categorized according to the source of the active signals: modified DC circuit breaker or other additional active equipment. In the first case [32,33], electronic components or voltage sources need to be integrated into the branches of the circuit breaker for active signal injection. In the second case, additional elements are required, such as in [34], where the fault energy of current-limiting inductors is stored in a parallel IGBT-based absorption module, from which the reclosing is fed, instead of reclosing the line through the breaker and provoking a new fault current strike. However, this method requires the installation of an additional power electronics module for the injection.

A summary of the single-ended fault location methods employed in LVDC, HVDC, and MVDC systems is provided in Table 1.

Table 1. Summary of single-ended fault location methods for LVDC, HVDC, and MVDC systems.

System	Line Length	Fault Resistance	Fault Location Methods	Advantages	Limitations
LVDC (<1 kV)	<1 km	<5 Ω	Passive methods [10–12]: utilize local measurements, leveraging current attenuation related to inductance.	✓ Cost-effective ✓ Simple implementation	✗ Accuracy highly affected by fault resistance ✗ Limited to short lines
			Active impedance-based methods [13–15]: use probe capacitors to inject signals into the faulty RLC circuit.	✓ Simple design and modularity ✓ Accurate for localized applications	✗ Limited performance for long lines ✗ Requires external injection devices ✗ Additional equipment increases costs
			Active fault loop-based methods [16–18]: eventually add passive or active components to the circuit breaker to form fault location loops.	✓ Can achieve precise fault location ✓ Integrates with existing protection infrastructure	✗ Increases equipment complexity and cost ✗ May require redesign of circuit breakers
HVDC (>100 kV)	>100 km	>50 Ω	Traveling-wave analysis [19–23]: analyze wavefronts created by fault-induced disturbances.	✓ Highly accurate over long distances ✓ Effective for fast fault detection ✓ Robust for high fault resistance	✗ High-speed measurement and recording systems required ✗ High computational burden
			Time-domain reflectometry [24]: inject signals into the line and analyze reflected waveforms for fault characterization.	✓ Effective for offline analysis ✓ Suitable for long cables	✗ Requires specialized and costly equipment ✗ Ineffective for high resistance faults
			Active impedance injection methods [25,26]: inject sinusoidal signals to estimate fault impedance before fault clearance.	✓ Highly accurate ✓ Effective for complex HVDC systems	✗ Introduces delays in fault clearance ✗ Requires changes to converter control strategies
MVDC (1–100 kV)	1–100 km	0–50 Ω	Active impedance estimation methods [29,30]:inject sinusoidal signals at multiple frequencies before fault clearance.	✓ Highly accurate for complex fault scenarios ✓ Adaptable to different system configurations	✗ Computationally intensive ✗ Requires additional sensors ✗ Delays fault clearance
			DC breaker-based signal injection [32]: use modified circuit breakers to inject fault identification signals during reclosing.	✓ High accuracy ✓ Can leverage existing protection hardware	✗ Requires additional modifications of breaker configuration or power electronics ✗ Increases cost and system complexity

Table 1. *Cont.*

System	Line Length	Fault Resistance	Fault Location Methods	Advantages	Limitations
MVDC (1–100 kV)	1–100 km	0–50 Ω	Offline reclosing methods [34]: use ordinary or power electronics-fed reclosing to analyze faults after fault clearance.	✓ Allows detailed post-fault analysis ✓ Avoids interference with real-time operations	✗ Can require high-performance equipment if traveling waves are analyzed ✗ May require additional electronic elements ✗ Accuracy highly influenced by fault distance
			Impedance-based reclosing methods (proposed): perform bus-fed re-energizations and analyze transient responses.	✓ High accuracy ✓ Eliminates need for active signal injection devices ✓ Integrates easily ✓ Avoids fault clearance delays	✗ Accuracy reduces for faults near the active terminal ✗ Limited effectiveness for very high fault resistance values ✗ May require high-sampling-frequency devices

This paper proposes a simple alternative for fault location in DC lines, particularly one conceived for MVDC lines, which is categorized as an impedance- and reclosing-based offline fault location method. The proposed method utilizes a switched grounding resistor at the converter station and a bypass connection through the current-limiting inductor. Once the fault is cleared, the fault characterization process is conducted, which includes two re-energizations. By fitting the transient discharge curves, the fault parameters are extracted.

The contributions of the proposed method are as follows:

1. Seamless integration: The fault location method does not require modifications to the DC circuit breaker topology, ensuring integration into any type of breaker technology (mechanical, solid-state, or hybrid). The method does not need any additional electronic component or voltage source for active injection, as the reclosings are fed from the DC bus.
2. Novel and simple configuration: The system only requires a single-ended switched grounding resistor and bypass connection through the limiting inductor. The grounding resistor allows us to limit the injected current, avoiding further spikes affecting the system. The bypass connection allows us to leverage the transient response of the faulty equivalent circuit.
3. Single-ended and offline: The method eliminates the need for inter-terminal communication. Furthermore, it does not introduce any delays for sampling before disconnecting the line, ensuring rapid fault clearance.

The paper is organized as follows. In Section 2, the operational principles of the proposed system are detailed. Section 3 discusses the research methodology, which is based on electromagnetic transient simulations, and presents and analyzes the results. Section 4 provides a broader discussion of the findings. Finally, Section 5 summarizes the main conclusions and prospects for potential future work.

2. Operational Principles of the Proposed Method

2.1. System Topology and Configuration

A general multi-terminal system topology is utilized to introduce the operating principles of the proposed method, as shown in Figure 1. A fully selective protection scheme is considered, where the DC grid is partitioned into protection zones corresponding to end-to-end lines. In the case of faults, the faulty line is disconnected to interrupt the fault current and isolate the fault, while the rest of the network continues in operation. This fully selective philosophy necessarily requires the installation of DC circuit breakers at both ends of each line.

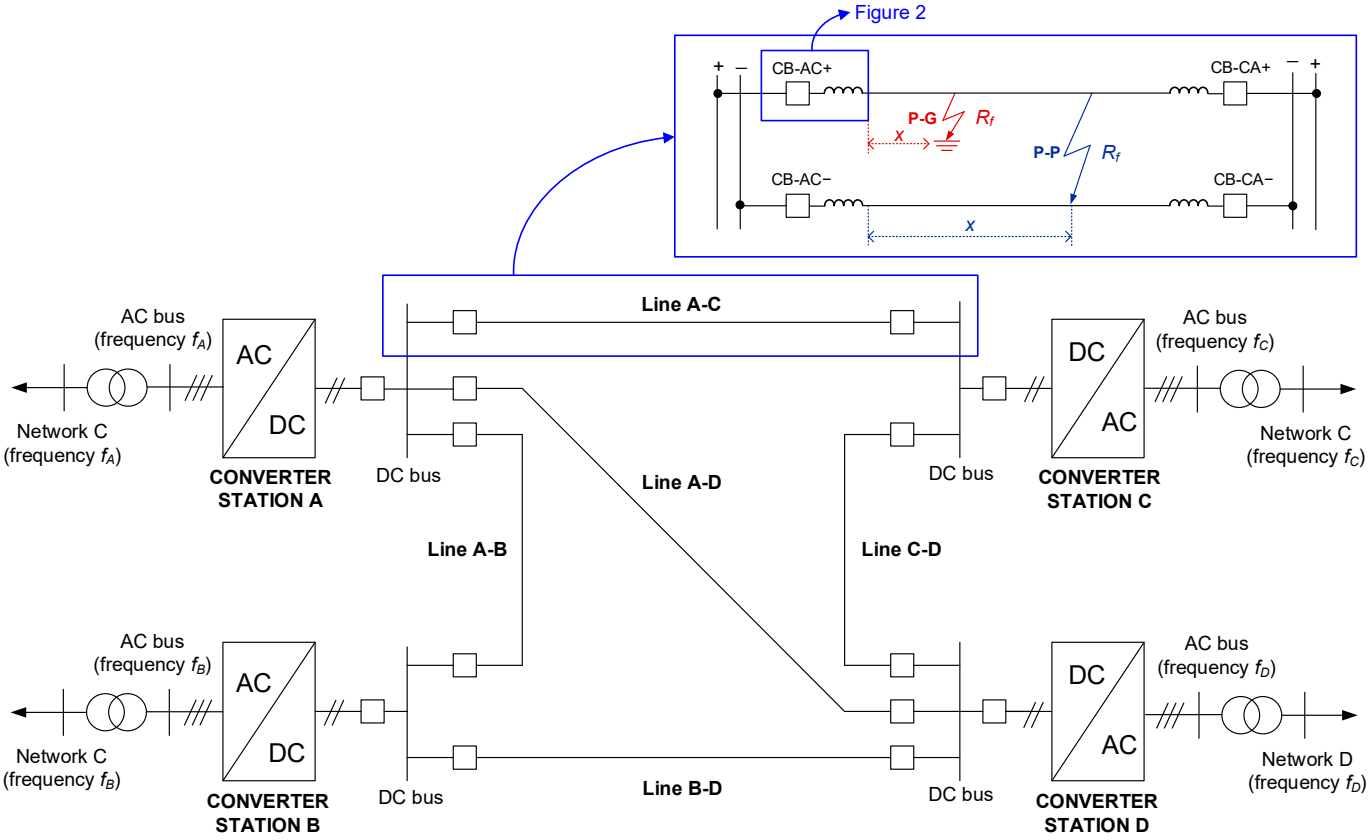


Figure 1. Multi-terminal fully selective DC network based on bipolar links.

In Figure 1, two common types of faults are represented: pole-to-ground faults (P-G) and pole-to-pole faults (P-P). These faults are represented at location x, with $x = 0$ at the near end of the line and $x = 100\%$ at the opposite end of the line, and fault resistance R_f. As also shown in Figure 1, current-limiting inductors are usually used in series with the circuit breakers in order to improve the selectivity and set the protection zones in the network. Limiting inductors also help to reduce the peak value of fault currents, allowing for a reduction in the current ratings of the breaker.

The fault location process is conducted once the fault has been detected through any of the existing state-of-the-art methods, and after the fault clearance process has been completed by the breaker. In this situation, either a P-G or a P-P fault is present on the DC line and the line is out of service. Most state-of-the-art methods for fault detection are capable of identifying the type of fault between P-G and P-P, as well as the faulty pole in the case of P-G faults, although this is evident when analyzing the fault current distribution and its polarity. Thus, the faulty line and pole are known. In this section, we assume that there are faults on the positive pole of the A-C line.

In the proposed approach, fault resistance R_f is treated as a variable alongside the fault location x, and these features jointly characterize the fault. The proposed fault location method outputs an estimation of x and R_f. The configuration required for the method is illustrated in Figure 2. The system includes a bypass branch in parallel with the circuit breaker, featuring a grounding resistor (R_g) as the key element. The branch is fed from the DC bus side of the breaker through switch S_1. Furthermore, switch S_2 consists of a relay with one pole and two throws (A and B). Position A allows us to feed the branch from the DC bus, while position B allows us to connect the branch to the ground. The grounding system is electrically coupled to the converter ground. Lastly, the limiting inductor L_{dc} is provided with a bypass connection through switch S_3. All the switches (S_1, S_2, and S_3) are initially open. The same configuration should be developed at the same end on the opposite pole.

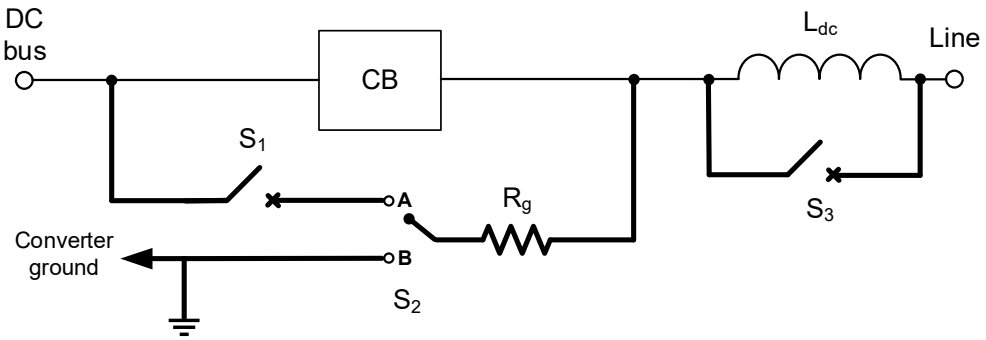


Figure 2. An electrical diagram of the proposed configuration.

2.2. Location of P-G Faults

If the reported fault on the positive pole is a P-G fault, then S_1 is closed and S_2 is thrown into position A. The line is energized, acting as a closed RL loop that is progressively charged. This closed loop includes the grounding resistor R_g, the limiting inductor L_{dc}, the RL line components corresponding to the section that extends from the circuit breaker to the fault location (x), and the fault resistance R_f. Subsequently, once the circuit is charged, switch S_2 is commuted to position B. The closed circuit is then progressively discharged. The discharging current of the first energization should be monitored: $I_1(t)$. Then, the first energization process is over. At this stage, the limiting inductor is bypassed by closing S_3, and a second energization is carried out via charging and discharging cycles. For this, switch S_2 is newly thrown to position A to charge the circuit, and afterward shifted to position B to discharge the circuit. The discharging current of the second energization should also be monitored: $I_2(t)$. Throughout the fault location process, no action is taken on the configuration deployed on the opposite pole.

The switching sequences for the charging and discharging cycles, for both the first and second energizations, are presented in Figure 3. Based on the system topology and the proposed switching scheme, the equivalent circuit of the closed RL loop, during the discharging cycles for the first and second energizations, are represented in Figures 4 and 5, respectively, for a P-G fault. The line is supposed to have a per-unit length inductance l, and a per-unit length resistance r.

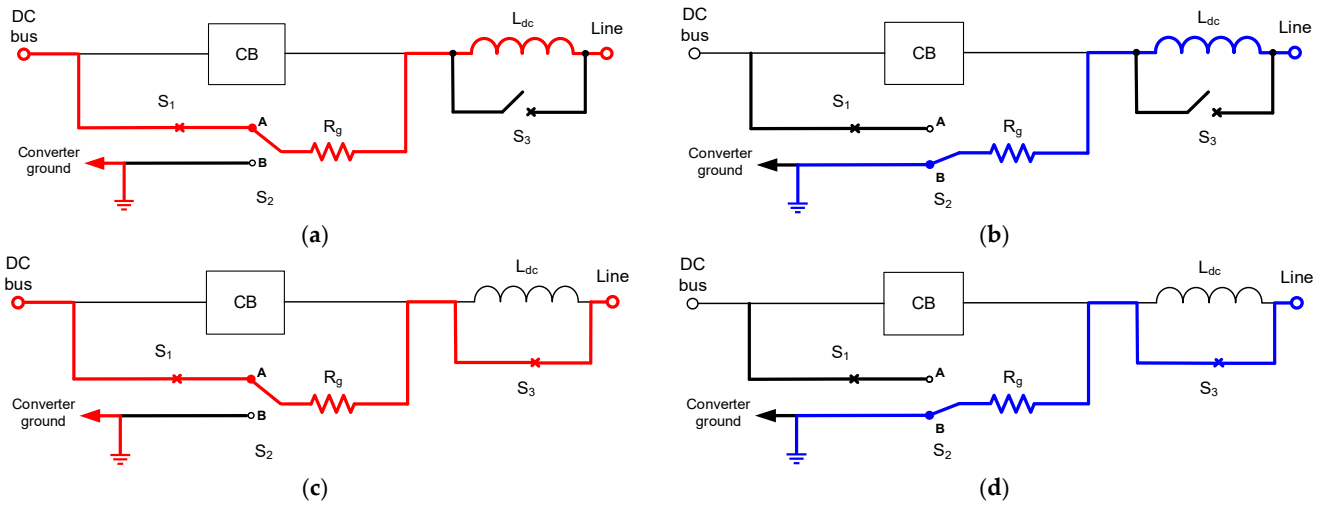


Figure 3. Re-energization switching sequence: (**a**) first energization, charging; (**b**) first energization, discharging; (**c**) second energization, charging; (**d**) second energization, discharging.

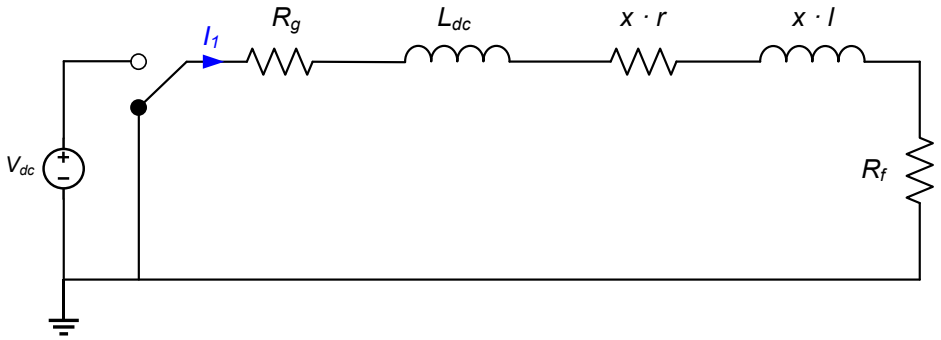


Figure 4. Equivalent circuit during discharging of first energization (P-G fault).

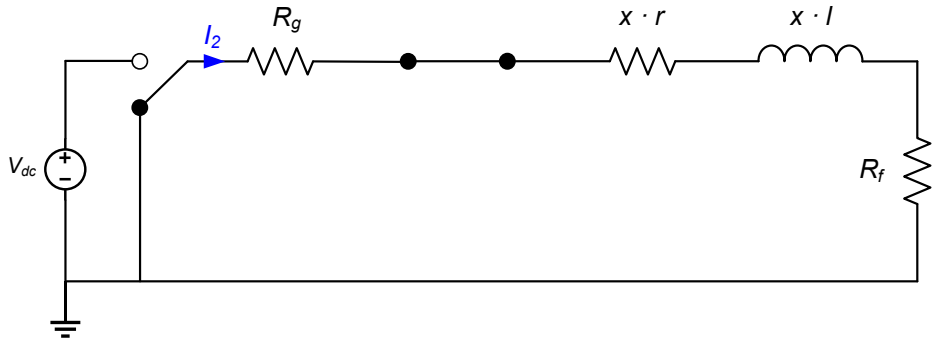


Figure 5. Equivalent circuit during discharging of second energization (P-G fault).

The expressions describing the discharging circuits for each energization are shown in Equations (1) and (2), respectively. The characteristic expressions for the discharge currents, $I_1(t)$ and $I_2(t)$, are given by Equations (3) and (4), respectively, where I_{1max} and I_{2max} correspond to the initial values of each of the currents when measured before discharging. The discharging in the first energization (S_2 is thrown to position B) occurs at $t = t_1$, while the second energization occurs at $t = t_2 > t_1$. The time constants for each discharging circuit, τ_1 and τ_2, are presented in Equations (5) and (6), respectively.

$$(x \cdot l) \cdot \frac{dI_1}{dt} + \left(R_g + x \cdot r + R_f\right) \cdot I_1 = 0 \quad (1)$$

$$(L_{dc} + x \cdot l) \cdot \frac{dI_1}{dt} + \left(R_g + x \cdot r + R_f\right) \cdot I_1 = 0 \quad (2)$$

$$I_1(t) = I_{1max} \cdot e^{-\frac{t-t_1}{\tau_1}} \text{ for } t > t_1 \quad (3)$$

$$I_2(t) = I_{2max} \cdot e^{-\frac{t-t_2}{\tau_2}} \text{ for } t > t_2 > t_1 \quad (4)$$

$$\tau_1 = \frac{L_{dc} + x \cdot l}{R_g + x \cdot r + R_f} \quad (5)$$

$$\tau_2 = \frac{x \cdot l}{R_g + x \cdot r + R_f} \quad (6)$$

The time constants can be estimated from Equations (3) and (4) using any fitting technique for the exponential form, such as an exponential least-squares fitting, trust-regions algorithms, or Levenberg–Marquardt algorithms for non-linear fitting. Solving the system constituted by Equations (5) and (6), the fault distance x, and the fault resistance R_f, can be achieved as per Equations (7) and (8), respectively:

$$x = \frac{1}{l} \cdot \frac{\tau_2 \cdot L_{dc}}{\tau_1 - \tau_2} \quad (7)$$

$$R_f = \frac{r}{l} \cdot \frac{\tau_2 \cdot L_{dc}}{\tau_2 - \tau_1} - \frac{L_{dc}}{\tau_2 - \tau_1} - R_g \quad (8)$$

2.3. Location of P-P Faults

If the reported fault is a P-P fault on the positive pole, the procedure on the positive pole is analogous to the one described for the P-G fault. However, at the same end on the negative pole, the procedure should consist of keeping the switching positions, depicted in Figure 3d, throughout the fault location process. The equivalent discharging circuits for the first and second energizations are illustrated in Figures 6 and 7, respectively.

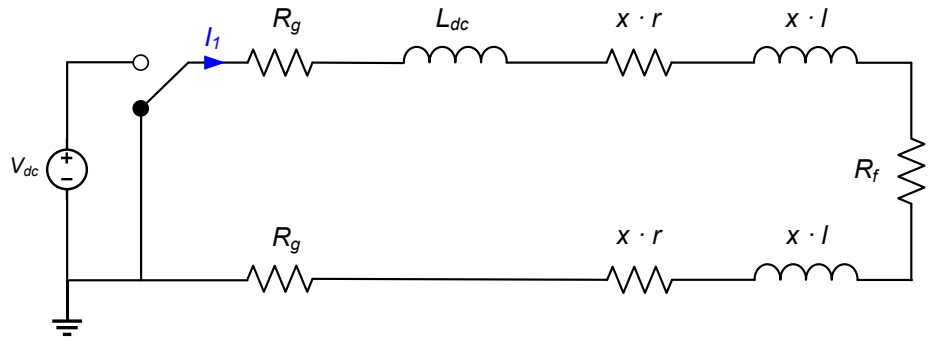


Figure 6. Equivalent circuit during discharging of first energization (P-P fault).

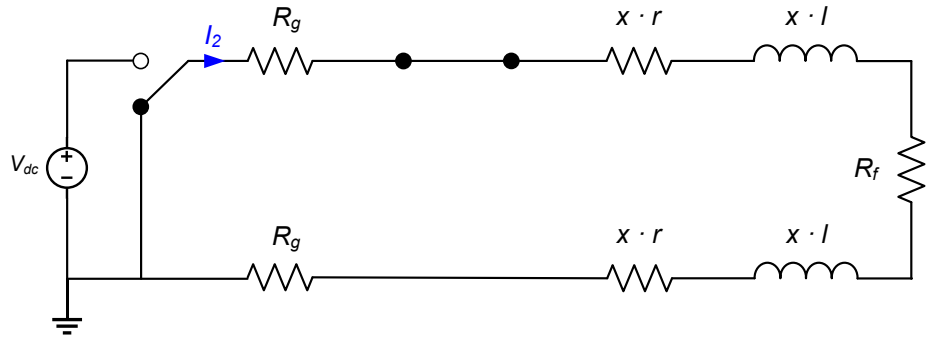


Figure 7. Equivalent circuit during discharging of second energization (P-P fault).

In this case, the expressions that define the discharge circuit during the first and the second energizations are expressed by Equations (9) and (10). The currents during the discharges are written in Equations (11) and (12), while the time constants for each circuit are presented in Equations (13) and (14). Finally, the fault distance x and the fault resistance R_f that stem from these equations are given in Equations (15) and (16), respectively:

$$(2 \cdot x \cdot l) \cdot \frac{dI_1}{dt} + \left(2R_g + 2 \cdot x \cdot r + R_f\right) \cdot I_1 = 0 \tag{9}$$

$$(L_{dc} + 2 \cdot x \cdot l) \cdot \frac{dI_1}{dt} + \left(2R_g + 2 \cdot x \cdot r + R_f\right) \cdot I_1 = 0 \tag{10}$$

$$I_1(t) = I_{1max} \cdot e^{-\frac{t-t_1}{\tau_1}} \text{ for } t > t_1 \tag{11}$$

$$I_2(t) = I_{2max} \cdot e^{-\frac{t-t_2}{\tau_2}} \text{ for } t > t_2 > t_1 \tag{12}$$

$$\tau_1 = \frac{L_{dc} + 2 \cdot x \cdot l}{2R_g + 2 \cdot x \cdot r + R_f} \tag{13}$$

$$\tau_2 = \frac{2 \cdot x \cdot l}{2R_g + 2 \cdot x \cdot r + R_f} \tag{14}$$

$$x = \frac{1}{2 \cdot l} \cdot \frac{\tau_2 \cdot L_{dc}}{\tau_1 - \tau_2} \tag{15}$$

$$R_f = \frac{r}{l} \cdot \frac{\tau_2 \cdot L_{dc}}{\tau_2 - \tau_1} - \frac{L_{dc}}{\tau_2 - \tau_1} - 2R_g \tag{16}$$

2.4. Summary and Remarks

2.4.1. Summary

The complete wrap-up of the post-fault characterization process is depicted in Figures 8 and 9.

The process flow for fault characterization, as depicted in Figure 8, involves a sequence of operations designed to extract fault parameters accurately. Initially, the fault type is identified by the protection system (P-G or P-P). If a P-G fault is reported, e.g., on the positive pole in this description, actions are only required on this pole. In contrast, if a P-P fault is reported, actions are required on both poles. The theoretical basis for these actions is detailed in Sections 2.2 and 2.3. for P-G and P-P faults, respectively.

In the positive pole, switches S_1, S_2, and S_3 are engaged for the re-energizations. First, S_1 is closed to allow the faulty circuit to be fed from the DC bus. The first re-energization is conducted by charging the circuit (throwing S_2 to A) and then discharging it (throwing S_2 to B) through the grounding resistor and the limiting inductor. During the discharge phase, the current (I_1) is monitored for subsequent analysis. After this, S_3 is closed to bypass the limiting inductor, preparing the circuit for the second re-energization. As with the first re-energization, the faulty circuit is charged (S_2 to A) and discharged (S_2 to B), but this time only through the grounding resistor. The discharge current (I_2) is also monitored for further analysis.

For the negative pole, switches S_2 and S_3 are only engaged in the case of a P-P fault. S_1 remains open under the assumption that the circuit is fed from the positive pole. The actions here involve ensuring electrical continuity through the ground by throwing S_2 to B and bypassing the limiting inductor by closing S_3. These settings should be established before the first re-energization on the positive pole and maintained throughout both re-energizations.

Finally, as illustrated in Figure 9, the discharge currents from both cycles (I_1 and I_2) are processed using exponential fitting to calculate the time constants (τ_1 and τ_2). These

constants are then used to determine the fault location (x) and resistance (R_f) using the applicable expressions provided in Sections 2.2 and 2.3. for P-G and P-P faults, respectively. This systematic process ensures reliable and precise fault parameter extraction.

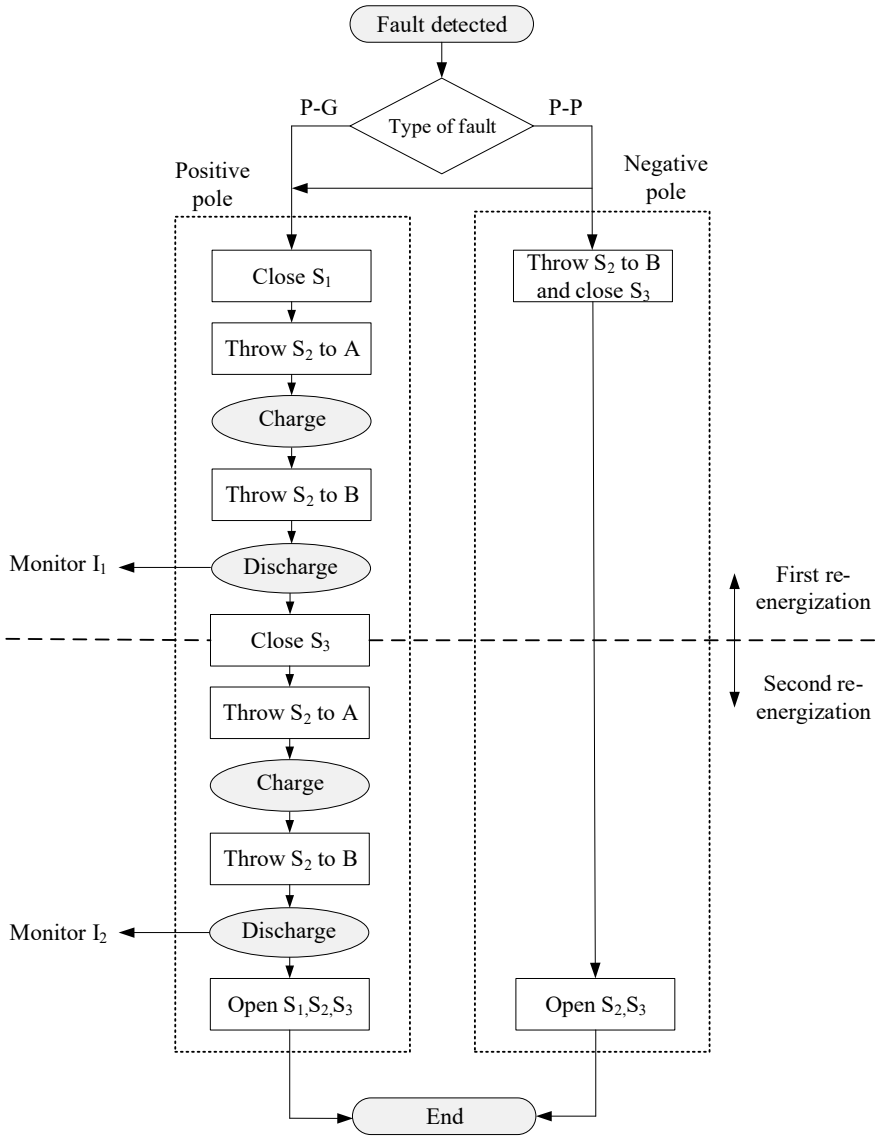


Figure 8. Proposed operation flowchart.

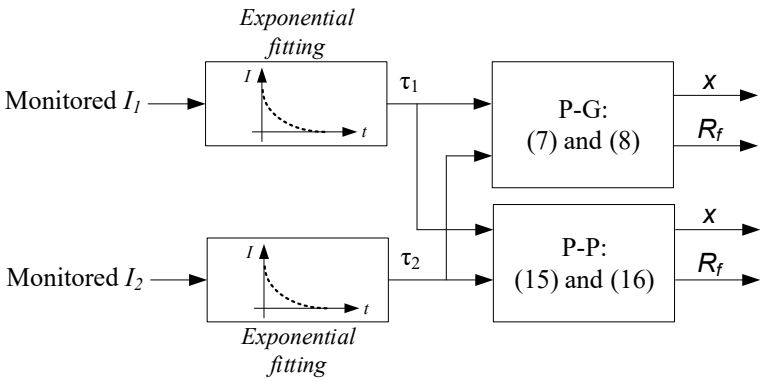


Figure 9. Fault characterization process (obtention of x and R_f).

2.4.2. Remarks

In the method described, the branch is fed from the DC bus at the corresponding bus voltage (V_{dc}). Thus, no additional voltage source is necessary. However, voltage dividers may be used in order to conduct the process at a lower voltage.

According to the switching logic based on the configuration depicted in Figure 2, switch S_1 is redundant, with switch S_2 serving as an additional measure to avoid inadvertent feeding of the line whenever the fault characterization method is not being used. Furthermore, switch S_2 can be replaced with two individual switches. However, the configuration of one pole and two throws is preferred to ensure efficient commutation between the charging and discharging cycles.

The method has been described for a fault on the positive pole, but its application to faults on the negative pole is analogous and immediate. For P-G faults, the re-energization process is conducted at any end of the faulty pole. For P-P faults, the re-energization process is also conducted at any end of one of the poles, while electrical continuity to the ground should be ensured at the same end of the opposite pole. Thus, the method can be applied in each line of the DC network by installing the proposed system at the same side end of each pole.

The method requires parameters L_{dc}, r, and l as inputs, and these are known in industrial applications. Furthermore, currents I_1 and I_2 can be measured with conventional DC transducers such as those based on the Hall effect. The key parameter to be adequately selected is the grounding resistor R_g. Also, the sampling window (Δt) and the sampling frequency (f_s) should be accurately set according to the following principles.

(a) The limitation of the energization current (action on R_g).

To avoid excessive energization currents from being injected into the faulty line and recirculated through the converter during the re-energizations, the minimum value of R_g should be computed while considering the value of the energization current for a direct P-G fault ($R_f = 0$) at the breaker terminals ($x = 0$). The energization current achieves its maximum value at the end of the charging process, i.e., at the start of the discharging process. This value should not exceed the overcurrent protection setting of the line, which is usually $n = 1.2$–2 times the rated current I_n. Accordingly, the condition is expressed by Equation (17):

$$R_g > \frac{V_{dc}}{n \cdot I_n} \tag{17}$$

(b) The prevention of excessively large time constants (action on R_g) and the capture of the longest transient response (action on Δt).

Accurate estimations of the time constants τ_1 and τ_2 through the exponential fittings are essential for the accurate estimation of the fault location and resistance. As per Equations (5), (6), (13), and (14), τ_1 and τ_2 become significantly large for faults with low R_f values, as well as for faults located at the opposite end, i.e., those with high x values. This leads to excessively long discharging responses in the RL circuit, failing to capture representative variations in the energization current for fitting purposes. Therefore, sufficiently high values of R_g and/or Δt are needed.

Particularly, the longest time constant will be given for the first re-energization (τ_1) for a P-G fault, with $R_f = 0$ and $x = 100\%$. To ensure that at least 95% of the exponential decay fits within the sampling window (Δt), this parameter should be set hand in hand with R_g. The following conditions should be accomplished:

$$\Delta t = \Delta t_1 > 3 \cdot \frac{L_{dc} + L_{line}}{R_g + R_{line}} \tag{18}$$

However, as $\tau_1 > \tau_2$ for any R_f and x, if different sampling windows are selected for each re-energization, then Δt_1 will be set according to Equation (18), while a shorter value can be selected for the second re-energization as follows:

$$\Delta t_2 > \frac{3}{2} \cdot \frac{L_{dc} + 2L_{line}}{R_g + R_{line}} \tag{19}$$

where R_{line} and L_{line} are the resistance and inductance of the full DC line, respectively.

(c) The prevention of excessively short time constants (action on R_g) and sufficient sampling points for the shortest transient response (action on f_s).

On the opposite side, if the time constants τ_1 and τ_2 are excessively short, there is a risk of poor exponential fitting due to the limited number of available samples during the transient decay. As per Equations (5), (6), (13), and (14), τ_1 and τ_2 become significantly low for faults with high R_f and for faults located at the near end, i.e., with low x values. Therefore, R_g should not be excessively oversized, and/or f_s should be accordingly fixed at a sufficient level. The shortest time constant will be given for the second re-energization (τ_2) for a P-P fault with high R_f and low x values. Denoting the maximum detectable fault resistance by R_{fmax}, and the minimum detectable fault distance by x_{min}, the following condition should be met according to k times the Nyquist frequency:

$$f_s > k \cdot \frac{R_g + x_{min} \cdot R_{line} + R_{fmax}}{2 \cdot x_{min} \cdot L_{line}} \tag{20}$$

Typically, the oversampling factor should be set at k = 4 to 10. A high sampling frequency provides more valuable data for exponential fitting, reducing the risk of aliasing and improving the accuracy in estimating the fault parameters for the fastest transient responses. Modern systems can achieve f_s > 100 kHz with digital signal processors, although this requirement increases computational and storage demands for data processing. Therefore, it should be carefully selected.

3. Electromagnetic Transient Simulations

3.1. Simulation Model

To validate the premises described above, electromagnetic transient simulations were conducted using PSCAD-EMTDC (electromagnetic transient including DC) and MATLAB for data processing, calculations, and plotting. This choice was based on the proven effectiveness in handling the intricacies of DC systems, including detailed modeling of converters and line characteristics. Two half-bridge modular multilevel converter (MMC)-based voltage source converter (VSC) stations have been considered at the ends of a two-terminal bipolar medium voltage DC (MVDC) link. This choice was based on the prominence of VSCs based on insulated gate bipolar transistors (IGBTs) in modern practice. A simplified representation of the simulated system is provided in Figure 10.

The EMTDC simulation model comprises a 10 km DC line rated at ±10 kV and 20 MW. Table 2 presents the technical features of the system. The values in Table 2 were selected to represent typical MVDC system parameters. The AC grid and MVDC network designs were based on [35], while converter parameters were inspired by [36–38]. DC cable parameters were based on data from manufacturers' catalogs (NEXANS, Paris, France), ensuring alignment with standards and technical recommendations from IEC and CIGRE. The value of R_g, included in Table 2, was selected to limit the injected current to twice the rated current, i.e., n = 2 in Equation (17). We also ensured that this value allowed for proper exponential fitting of the slowest expected responses.

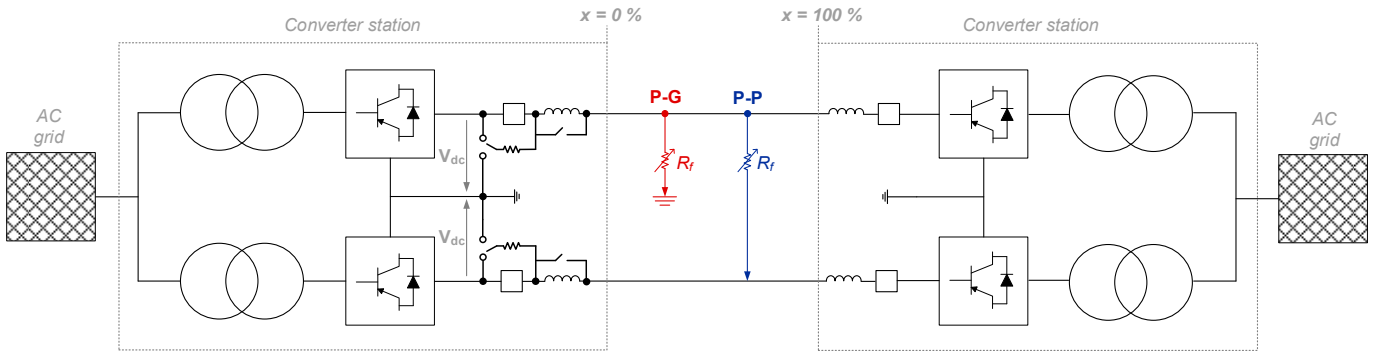


Figure 10. A representation of the EMTDC simulation model.

Table 2. Parameters of the system used for EMTDC simulations.

Subsystem	Parameter	Magnitude	Units
AC grids	Rated voltage	220	kV
	Short-circuit power	∞	
	Rated frequency	50	Hz
Converter station	Transformer rated voltage ratio	220/10	kV
	Transformer rated power	10	MVA
	Transformer short-circuit voltage	20	%
	Converter rated power	10	MW
	Number of submodules per bridge arm	12	
	Inductance per bridge arm	10	mH
	Submodule capacitance	10	mF
	Limiting reactor (L_{dc})	10	mH
	Circuit breaker opening time	10	ms
	Grounding resistor (R_g)	5	Ω
DC line	Length	10	km
	Voltage	±10	kV
	Rated current	1	kA
	Cable resistance at 20 °C (r)	0.2	Ω/km
	Cable inductance (l)	0.5	mH/km
	Cable phase capacitance	0.2	μF/km

Several fault characterization simulations were conducted for P-G and P-P faults at various locations (x = 1, 25, 50, 75, and 100%) and with various fault resistance values (R_f = 0.1, 1, 10, 20, and 50 Ω). Regarding the switches used, the fastest operation was achieved with solid-state switches, such as IGBTs, MOSFETs, or thyristors, in the range of 1–100 μs, while mechanical switches only achieved 20–150 ms. In these simulations, we utilized a trade-off value of 1 ms for hybrid switches. The simulations were performed in the time domain with a sampling frequency of f_s = 50 kHz. For charge and discharge cycles with values of Δt_1 = 10 ms for the first re-energization, and of Δt_2 = 5 ms for the second re-energization, a total of 500 and 250 current measurements, respectively, were consequently available along the discharge exponential curves of each re-energization to carry out the fittings.

3.2. Results

The line current for a P-G occurring at t = 1 s at location x = 50%, with a fault resistance of R_f = 1 Ω, is shown in Figures 11 and 12. Before the fault occurs, the system works near full-load conditions. After the fault occurs, the limiting inductor contains the current rise before the fault is completely cleared at t = 1.012 ms (2 ms for fault detection and 10 ms for circuit breaker opening). The first re-energization is performed after a dead time of 100 ms. The circuit is charged for 10 ms and discharged for an analogous time period. Then, the lim-

iting inductor is bypassed, and the second charging–discharging process is carried out with half the durations. It is observed that the circuit's response is notably faster in the second re-energization, with the limiting inductor bypassed, which is the factor enabling us to reduce the duration of the charging and discharging cycles of the second re-energization. The current throughout the re-energizations is limited by the grounding resistor. In this particular example, the time constants were found at $\tau_1 = 1.7776 \times 10^{-3}$ s and $\tau_2 = 1.1510 \times 10^{-3}$ s via exponential fitting, leading to an estimated location of x = 49.9945% and an estimated fault resistance of $R_f = 1.0319\ \Omega$.

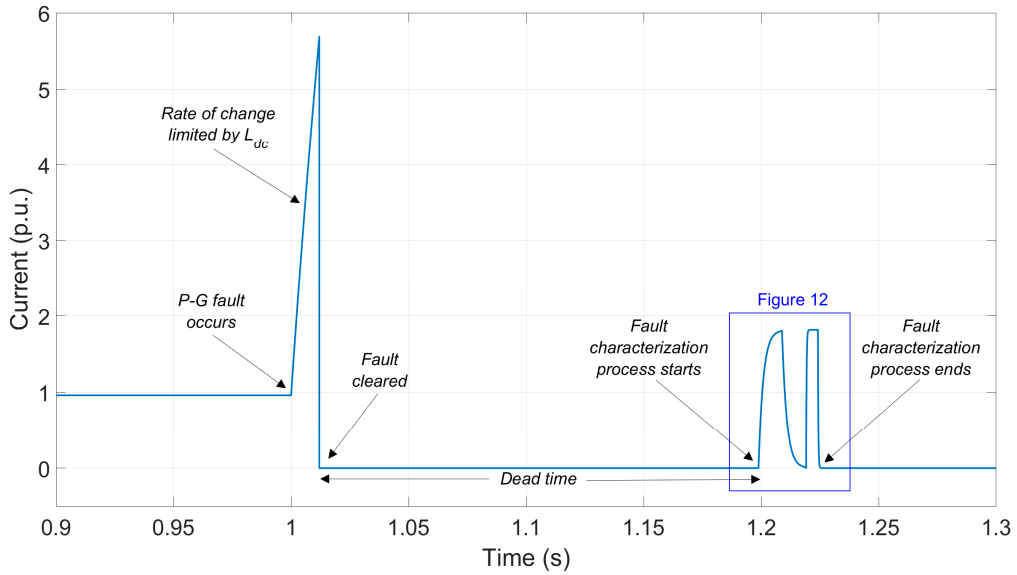


Figure 11. Current evolution from before the fault until the end of the fault characterization (P-G fault at location $x = 50\%$ with fault resistance $R_f = 1\ \Omega$).

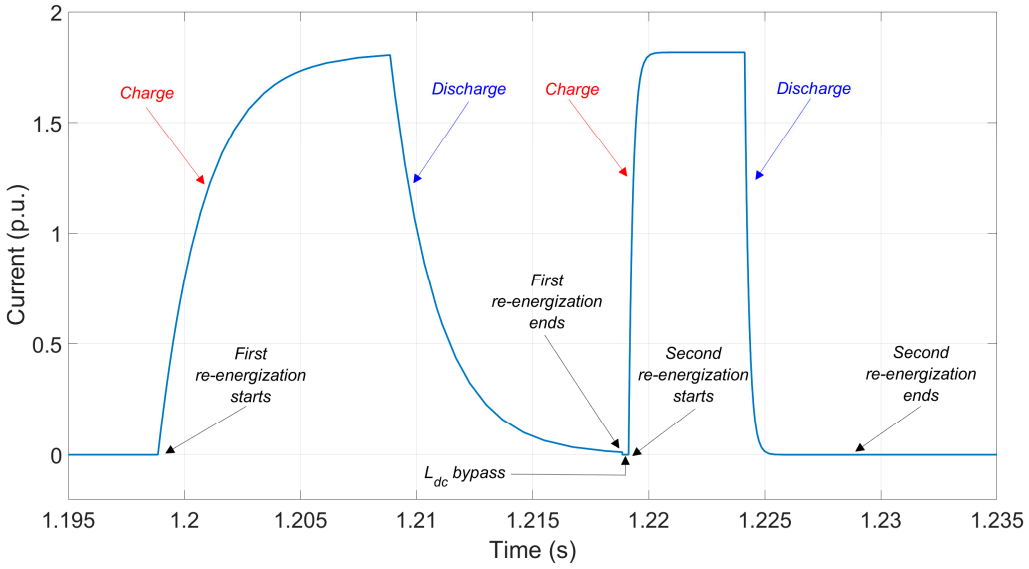


Figure 12. The current evolution throughout the fault characterization process (P-G fault at location $x = 50\%$ with fault resistance $R_f = 1\ \Omega$).

The current waveforms obtained for the simulated P-G and P-P faults are represented in Figures 13 and 14, respectively. For each type of fault, fault locations $x = 1$, 25, 50, 75, and 100% are studied, and for each fault location, different fault resistances $R_f = 0.1$, 1, 10, 20, and 50 Ω are considered. From these results, the influence of x and R_f on the exponential form of the discharge curve is derived. The time constants, which involve the behavior of

the transient responses of the RL loop following the re-energizations, decrease when x and R_f increase.

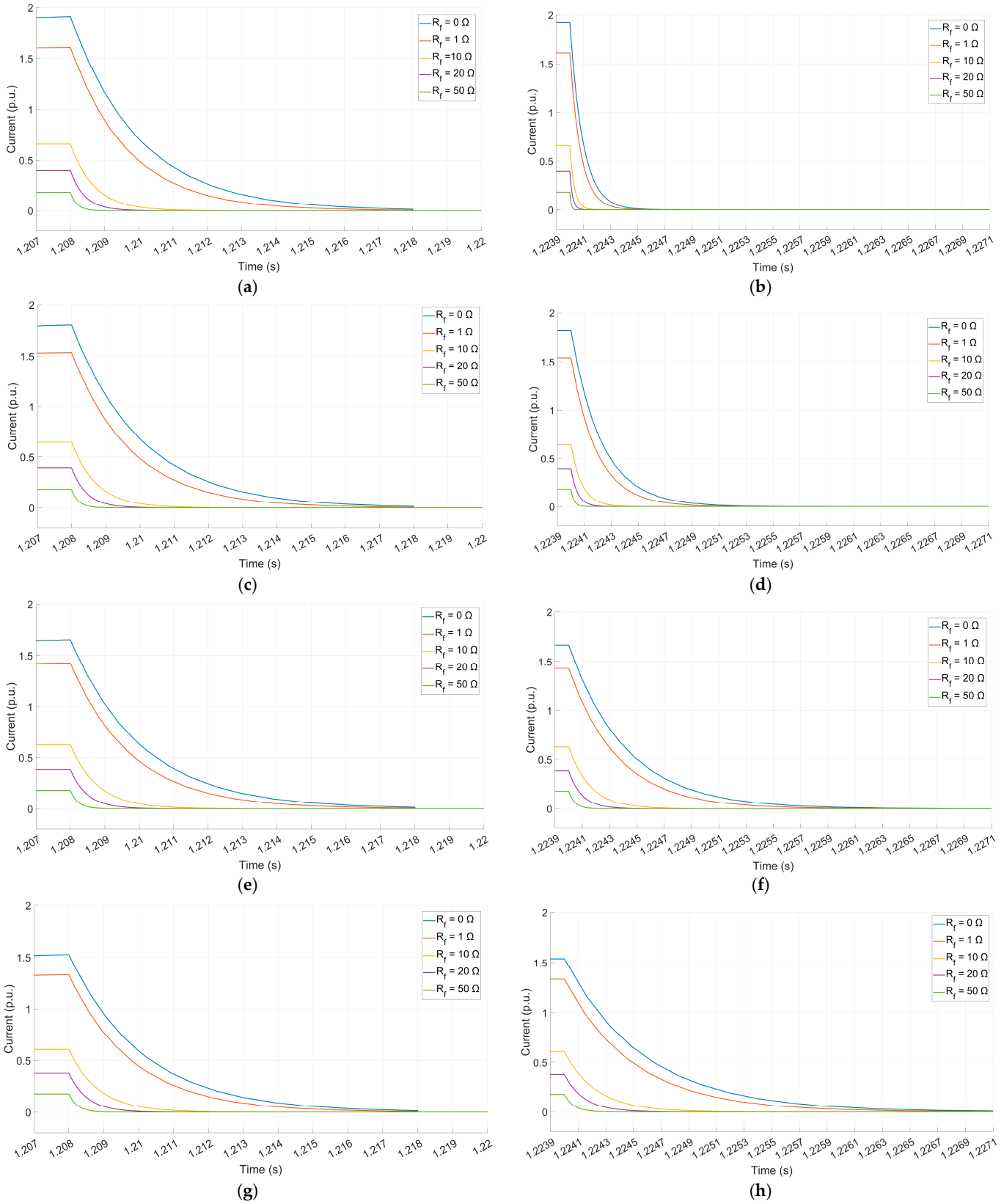
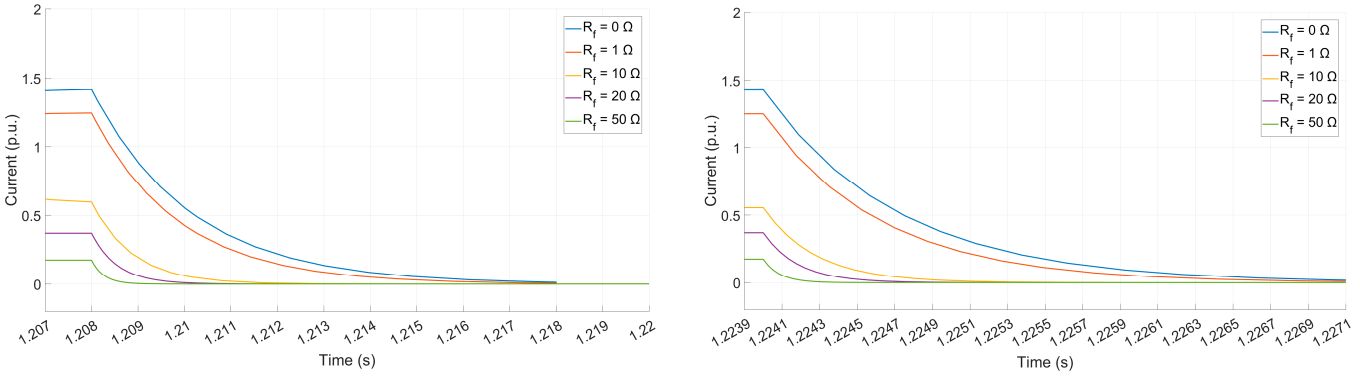
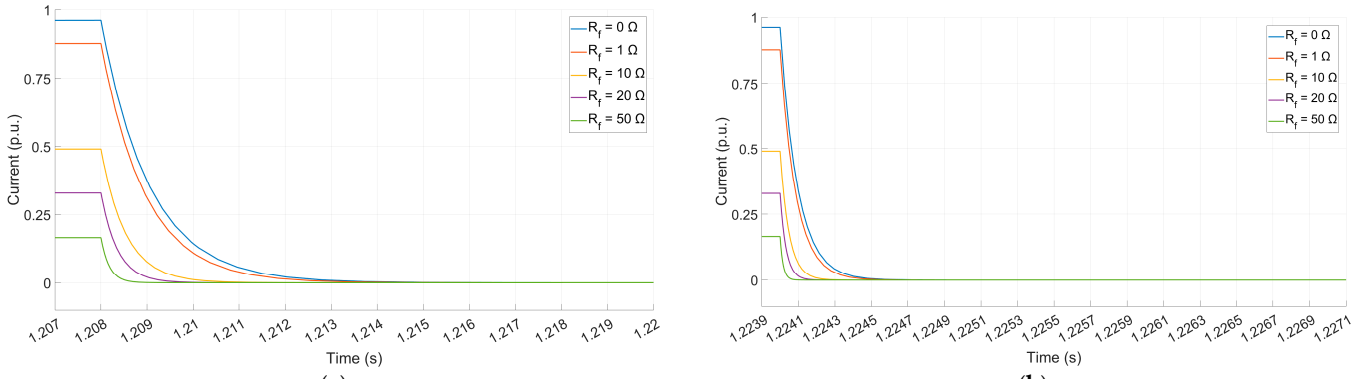


Figure 13. *Cont.*

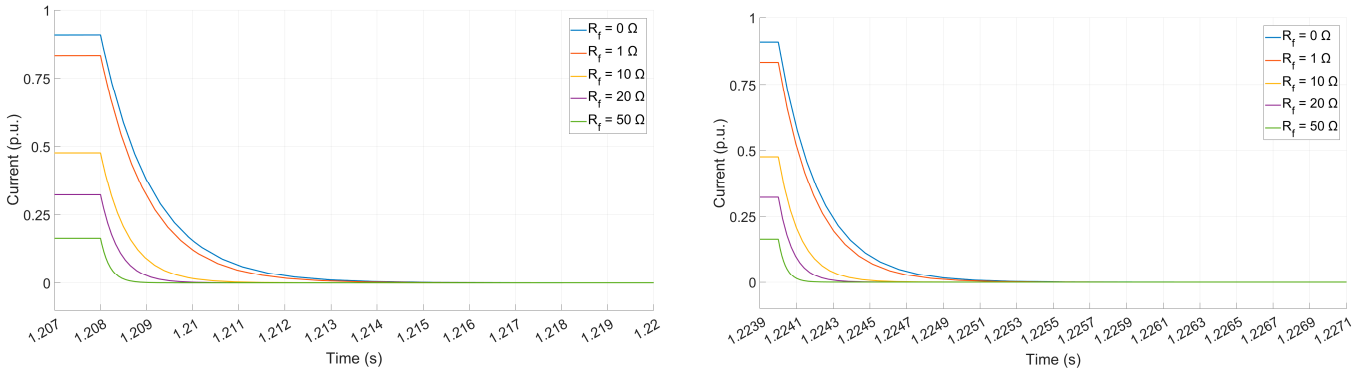


(**i**) (**j**)

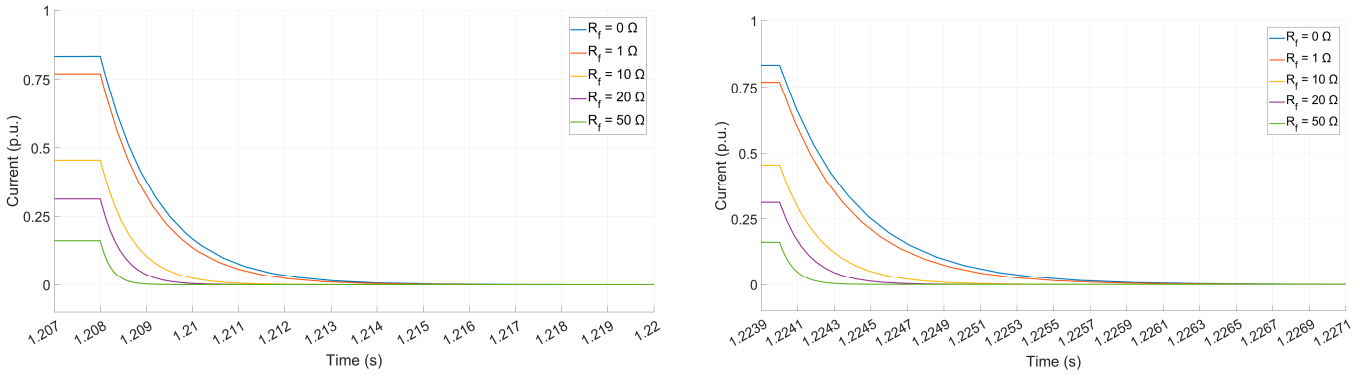
Figure 13. Current evolution throughout the circuit discharging cycles for P-G faults. (**a**) x = 1%, first re-energization; (**b**) x = 1%, second re-energization; (**c**) x = 25%, first re-energization; (**d**) x = 25%, second re-energization; (**e**) x = 50%, first re-energization; (**f**) x = 50%, second re-energization; (**g**) x = 75%, first re-energization; (**h**) x = 75%, second re-energization; (**i**) x = 100%, first re-energization; (**j**) x = 100%, second re-energization.



(**a**) (**b**)



(**c**) (**d**)



(**e**) (**f**)

Figure 14. *Cont.*

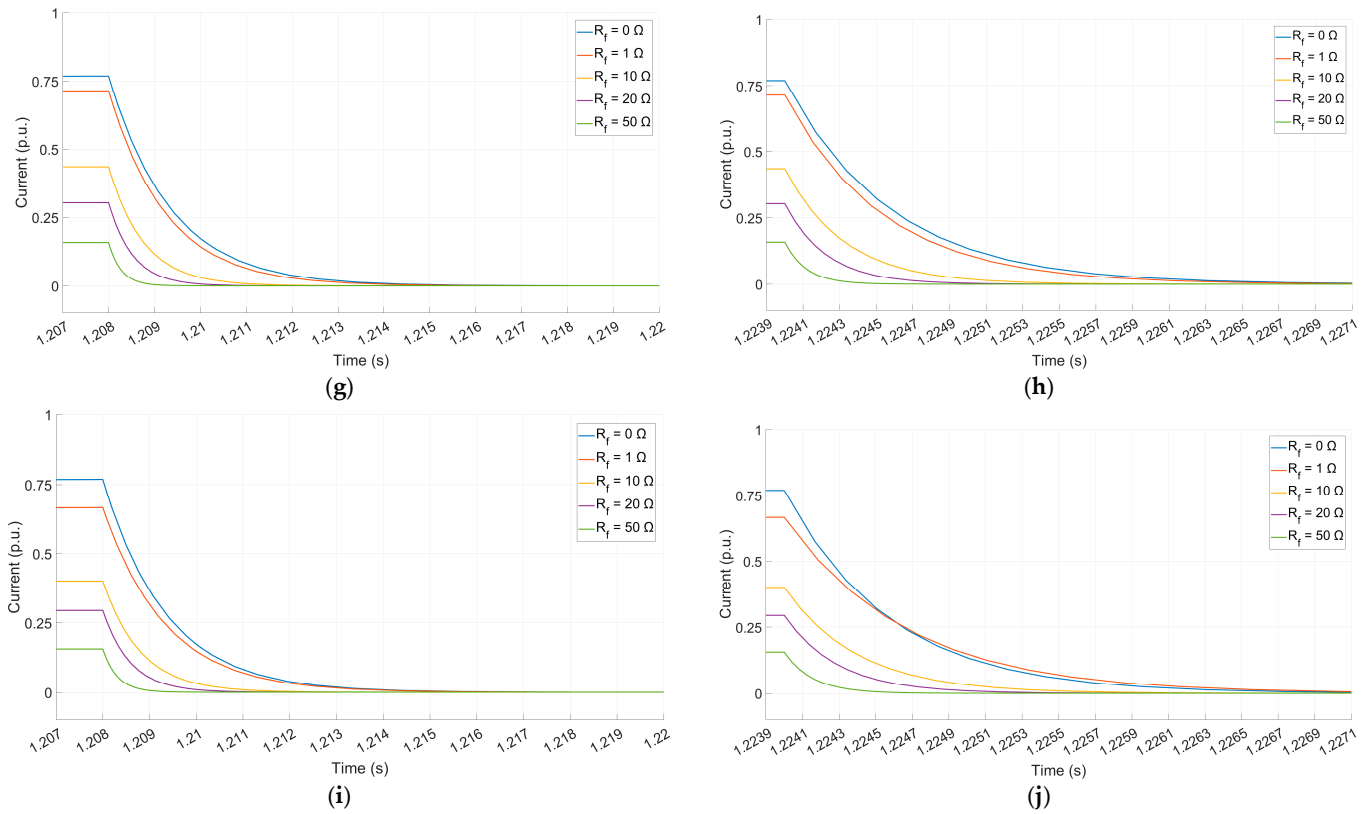


Figure 14. Current evolution throughout the circuit discharging cycles, for P-P faults. (**a**) x = 1%, first re-energization; (**b**) x = 1%, second re-energization; (**c**) x = 25%, first re-energization; (**d**) x = 25%, second re-energization; (**e**) x = 50%, first re-energization; (**f**) x = 50%, second re-energization; (**g**) x = 75%, first re-energization; (**h**) x = 75%, second re-energization; (**i**) x = 100%, first re-energization; (**j**) x = 100%, second re-energization.

In this context, two re-energizations are required to unequivocally obtain the correct [x, R_f] values, and a single re-energization would lead to an indeterminate system with infinite [x, R_f] solutions. Additionally, it is observed that $I_{max1} = I_{max2}$ for each fault characterization process. In fact, $I_{max1} = I_{max2}$ corresponds to the steady-state value acquired after the first re-energization (inverse exponential function) and thus to the initial value of the second energization (exponential decay). This value only depends on the resistive components of the energized circuit. Therefore, it only varies with x and R_f. Particularly, it is verified that it decreases with x and R_f as per the Equation (21) for P-G faults and as per Equation (22) for P-P faults:

$$I_{1max} = I_{2max} = \frac{V_{dc}}{R_g + x \cdot r + R_f} \tag{21}$$

$$I_{1max} = I_{2max} = \frac{V_{dc}}{2R_g + 2 \cdot x \cdot r + R_f} \tag{22}$$

The variation in the time constants τ_1 and τ_2 with x and R_f is plotted in Figure 15 for both P-G and P-P faults. It is observed that the time constants increase with x and decrease with R_f. Thus, the time windows should be selected based on the slowest expected response (ideally $x \to 100\%$ and $R_f \to 0$). In this case, the response for [x = 100%; R_f = 0] is considered. For [x = 100%; R_f = 0], the time window should allow us to cover the transient exponential evolution to achieve proper fitting. It is observed in Figures 13i and 14i that the time windows of 10 ms and 5 ms are sufficiently long for this purpose for the first and second re-energizations, respectively.

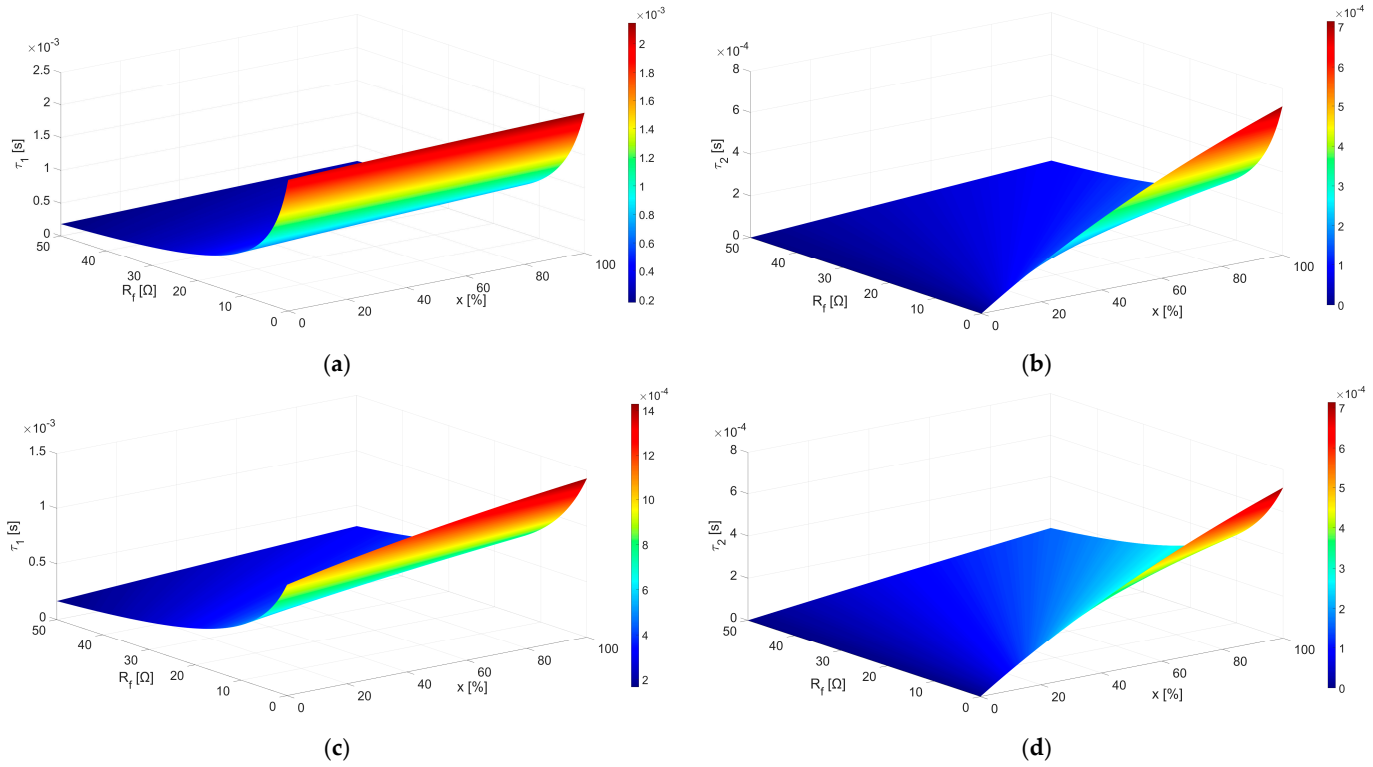


Figure 15. Time constants as function of the fault location (x) and fault resistance (R_f). (**a**) P-G faults, first re-energization (τ_1); (**b**) P-G faults, second re-energization (τ_2); (**c**) P-P faults, first re-energization (τ_1); (**d**) P-P faults, second re-energization (τ_2).

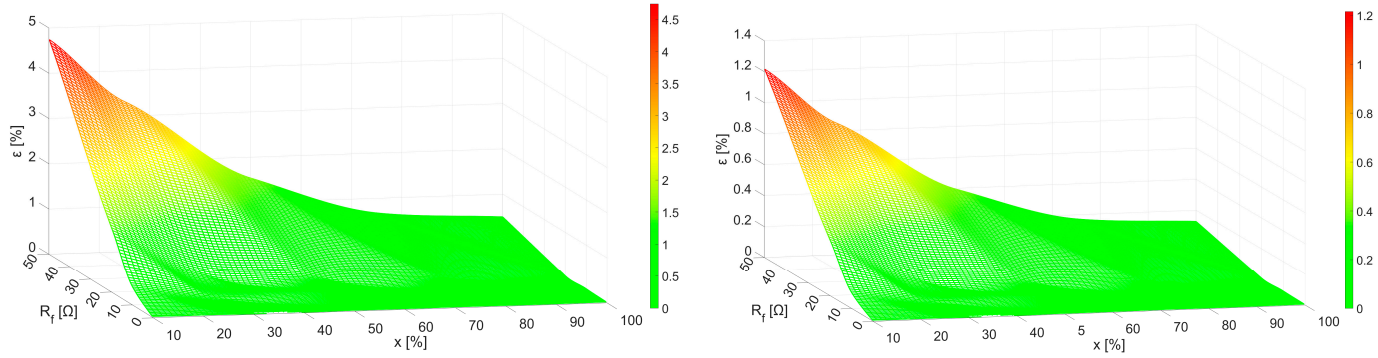
On the other hand, it should be ensured that the sampling frequency allows us to capture a significant number of points during the transient exponential evolution of the fastest expected response (ideally $x \rightarrow 0$ and $R_f \rightarrow \infty$). It is observed in Figures 13b and 14b, particularly for [x = 1%; R_f = 50 Ω], that the sampling frequency is critical to ensuring an accurate estimation of τ_1 and τ_2 and therefore an accurate estimation of x and R_f. Current technologies even allow for sampling frequencies above 100 kHz, which would notably increase the number of inputs required to carry out the fittings. Consequently, the error would decrease for the fastest responses, but it would not substantially enhance the accuracy of the proposed location method for all other responses on an overall basis.

The fault location method should be evaluated based on its accuracy in determining the fault position. Thereby, the relative fault location error (ε) is defined according to Equation (23), based on the estimated fault position (x_{est}) and the actual fault position (x_{act}). The relative fault location errors for faults at x = 1, 25, 50, 75, and 100%, with fault resistances R_f = 0.1, 1, 10, 20 and 50 Ω, are shown in Figure 16a,b for P-G and P-P faults, respectively. The maximum observed errors are ε = 4.82% for P-G faults and ε = 1.21% for P-P faults.

$$\varepsilon\,[\%] = \left| \frac{x_{est} - x_{act}}{x_{act}} \right| \cdot \frac{1}{100} \tag{23}$$

As shown in Figure 16, when the fault resistance is low, and the fault occurs farther from the measurement point, the fault location error is minimal. However, larger errors arise when these conditions are reversed. As the fault resistance increases, the time constants decrease, leading to greater errors. In fact, the proposed method is based on discriminating the line impedance from the measurement end to the fault point, with and without the limiting reactor. A high fault impedance diminishes the influence of the line's behavior on the exponential discharge curves, i.e., the influence of the distance-dependent impedance

parameters on the time constants, jeopardizing the differentiation process. Therefore, high values of R_f limit the fault location accuracy. Conversely, faults with larger x imply greater line-distance-dependent impedance, thus facilitating fault location with a lower error. Additionally, the location error for P-P faults is smaller, being approximately ¼ of that of P-G faults, as the doubled line-dependent impedance in the circuit outweighs the impact of the doubled grounding resistance.



(**a**) (**b**)

Figure 16. Errors as a function of the fault location (x) and fault resistance (R_f). (**a**) P-G faults; (**b**) P-G faults.

For a specific installation, L_{dc}, r, and l are fixed (smoothing inductor and cable parameters). Therefore, the method's tunable settings include the charging and discharging window durations, the sampling frequency, and the value of R_g. Considering that the charging and discharging window is correctly selected to provide an accurate curve fitting for the slowest response, further actions can then be taken on the sampling frequency and R_g. The value of R_g serves to modulate the speed of responses during re-energization. In this case, reducing R_g below 5 Ω would have particularly helped to slow down the fastest responses (higher R_f values) and reduce errors, but at the cost of increasing the injected currents during re-energization. This current, however, is already calculated at twice the rated value for the worst-case scenario. In this regard, R_g and R_f have similar mathematical effects on the response, and so low R_g values can compensate for large R_f values up to the mentioned limit. Finally, as observed in Figure 15, very large R_f values lead to significantly slower responses, reducing the number of inputs available to fit the exponential curves. This limitation increases the fault location error, as derived from Figure 16. Given the impracticality of further reducing R_g for this specific case, increasing the sampling frequency remains the most feasible option.

Overall, the described results demonstrate the proposed method's effectiveness in accurately characterizing P-G and P-P faults in DC lines, achieving errors below 5% for fault resistances under 50 Ω. These findings rely on a straightforward operating principle. Further analysis and discussion are provided in the next section.

4. Discussion

The proposed single-ended, offline fault location method demonstrates significant advantages over existing techniques, particularly in terms of simplicity, integration, and performance under varying fault scenarios. By focusing on MVDC systems, the method addresses a critical gap in fault location research, which has traditionally centered on HVDC and LVDC applications. MVDC systems present unique challenges, including intermediate line lengths (1–100 km), moderate fault resistances (up to 50 Ω), and stringent fault clearance requirements, all of which are effectively tackled by the proposed approach.

In comparison to impedance-based methods that rely on external active injection devices for fault characterization, the proposed method avoids the need for additional equipment by utilizing the existing DC bus voltage and a switched grounding resistor to induce and analyze the discharge transients. This reduces system complexity and the associated costs. On the other hand, unlike methods requiring double-terminal or multi-terminal measurements, which necessitate communication between terminals and time synchronization, the single-ended nature of this technique eliminates such dependencies, ensuring robustness and reduced operational delays. Moreover, while traveling wave-based methods achieve high accuracy over long distances, they are impractical for MVDC lines due to shorter wave propagation times and the need for high-speed sensors and processing systems. The proposed method circumvents these limitations by leveraging the inductive discharge transient characteristics of the fault circuit.

The method's novel configuration, comprising a bypass connection through a current-limiting inductor and a switched grounding resistor at the converter station, uniquely modifies the system's inductive behavior during controlled discharge transients. By analyzing the exponential decay of discharge currents across two re-energizations, the method accurately determines fault location and resistance. Key contributions include the avoidance of external voltage sources or active electronic modules, as well as the avoidance of circuit breaker topology modifications for active injection, ensuring seamless integration into existing DC systems.

The simulation results validate the method's effectiveness, achieving fault location errors of $\varepsilon < 5\%$ for fault resistances up to $R_f = 50\ \Omega$, and errors of $\varepsilon < 0.32\%$ for fault resistances up to $R_f \leq 10\ \Omega$, outperforming the accuracy of existing approaches in comparable fault resistance ranges. For instance, fault location modules achieve $\varepsilon = 6.25\%$ for $R_f \leq 10\ \Omega$ [16], while active impedance estimation methods report an improved accuracy of $\varepsilon = 2.23\%$ for $R_f \leq 10\ \Omega$ [30], albeit with added computational complexity and equipment requirements. Similarly, the modification in thyristor-based DC circuit breakers achieves $\varepsilon = 1.50\%$ for $R_f \leq 10\ \Omega$ and $\varepsilon = 2.50\%$ for $R_f \leq 100\ \Omega$ at the cost of increased system complexity [32]. The approach involving pulse injection and traveling wave analysis offers $\varepsilon = 2.70\%$ for $R_f \leq 10\ \Omega$ [34], demonstrating robustness but requiring advanced power electronics modules and sensors. Comparatively, based on the analysis provided in Table 1, and considering the accuracy level achieved, it is derived that the proposed method balances accuracy with simplicity.

For faults with high resistances or those closer to the active end, the error increases due to the reduced influence of distance-dependent impedance parameters on the discharge time constants. This emphasizes the sensitivity of the method to the cable's resistive (r) and inductive (l) properties. Particularly, for cables with lower impedance values, fault location errors are expected to increase, as the discharge responses become less distinct across different fault locations. Thereby, the influence of cable parameters is considered one of the limitations of the method. However, this limitation can be substantially mitigated by fine-tuning the grounding value to modulate the relative importance of R_g with respect to the distance-dependent cable impedance in the discharge responses. For each implementation of the method, the tuning of the sampling window and sampling rate should also consider cable parameters.

While the sampling window does not impose significant limitations, the sampling frequency plays a critical role. This is specifically relevant for faults at the near end or areas with high fault resistance, as faster responses require higher sampling rates to capture sufficient data points for accurate exponential curve fitting. While the chosen sampling rate of $f_s = 50$ kHz proved adequate in the simulations, higher frequencies can further improve accuracy, especially for rapid transients, and enhance robustness against noise.

In fact, the sampling frequency is considered the main practical limitation of the proposed method, as locating faults with values above R_{fmax} and below x_{min} would require higher f_s, which depends on the available resources. Therefore, the technical features of the measurement equipment and the availability of sufficient computational power are crucial for achieving reliable results. The current sensors required for the implementation of the proposed method must have a sampling frequency significantly higher than the expected transient response frequency in order to capture sufficient data points for accurate exponential fitting. Additionally, synchronization between the measurement system and the control logic must be precise to ensure accurate recording of the discharge currents.

Another key limitation of the proposed method is the effect of measurement noise on its accuracy, as noise in the current measurements can impact the exponential fitting process. To mitigate this, high-precision current transducers with high noise-filtering capability are required. For instance, Hall effect sensors or shunt resistors with high resolution and adequate bandwidth are suitable for capturing transient waveforms accurately. Digital signal processing techniques, such as filtering or smoothing, may also be necessary to reduce the impact of noise on the extracted time constants.

The selection of switches S_1, S_2, and S_3 is critical to the effective implementation of the proposed fault location method. These switches must operate at high speed and precision to enable accurate fault parameter extraction during the re-energization cycles. S_1 and S_3, which connect the faulty circuit to the DC bus and bypass the limiting inductor, respectively, are best implemented as solid-state switches, such as IGBT- or MOSFET-based devices. Solid-state switches are well suited for their fast actuation times, typically in the ms range, and their ability to handle repetitive switching without mechanical wear and with minimal loss. On the other hand, S_2, which alternates between connecting the circuit to the DC bus and ground, is ideally implemented as a solid-state relay or a hybrid switch, combining the high-speed operation of solid-state components and the high current-handling capacity and cost-effectiveness of mechanical components.

Moreover, switch selection should consider thermal constraints and transient current dynamics. Switches are required to possess sufficient thermal capacity to withstand the heat generated by the current surges and appropriate protection mechanisms to prevent thermal damage. The current rise time, in particular, can impose additional stress on the switches, necessitating designs with low on-state resistance and high transient current ratings. Furthermore, the switches must be rated for the full DC system voltage (e.g., $\pm$10 kV for the simulated MVDC system) and include adequate insulation and protection against overvoltage transients.

Moreover, the proposed method assumes the presence of a current-limiting inductor (L_{dc}) in the DC line, which plays a significant role in shaping a different discharge transient for each re-energization. In fact, the method is contingent on a sufficiently large value of L_{dc}, which is usually in the range of tens of mΩ in MVDC lines, and in the range of hundreds of mΩ in HVDC lines. The value of L_{dc} directly influences the time constant τ_1, thus affecting the decay in the first re-energization. Higher values of L_{dc} slow down the first discharge process, inducing a larger difference between the behavior of the first and second re-energization, and therefore facilitating fault location. However, excessively high L_{dc} values may lead to overly slow responses, requiring longer settings of Δt_1.

Utilizing a double-ended configuration instead of the proposed single-ended configuration represents a notable development of the proposed method. The higher errors associated with short fault distances from the active terminal (low x values) can be mitigated by the double-ended configuration. This approach involves applying the same switching procedure at the opposite terminal, inverting the active line end. By analyzing the fault from the furthest possible distance, the fault-dependent impedance is increased, leading to

significantly lower characterization errors. However, this dual-terminal approach necessitates the duplication of the required equipment, including switches, grounding resistor, and bypass connection, at both ends of the DC line. The additional material cost must we weighed against the improvements in fault location accuracy.

It should be noted that the method assumes fully selective fault isolation, requiring the faulty line to be disconnected from both ends. While this is standard in many MVDC applications, it restricts the method's applicability in non-fully selective systems, where partial isolation or overlapping protection zones exist. Future research could adapt the approach to such systems, integrating redundancy into switching configurations or introducing adaptive algorithms to account for partial isolation scenarios. Another avenue for future development involves adapting the method to real-scale systems, including the practical sizing and installation of additional equipment such as the grounding resistor and bypass connections. Exploring hybrid approaches that combine this method with various frequency signal injections may enhance its scalability.

5. Conclusions

This study focuses on fault location in medium-voltage direct current (MVDC) systems, an area of study that has received comparatively less attention than high-voltage (HVDC) and low-voltage (LVDC) systems. MVDC systems present unique challenges, including intermediate line lengths, higher fault resistances, and stringent requirements for rapid fault clearance.

This work proposes a single-ended, offline fault location method based on controlled re-energization. The method utilizes a novel configuration involving a switched grounding resistor and a bypass connection through the current-limiting inductor to extract fault parameters via two-line re-energization. By leveraging the bypass connection, the inductive behavior of the system is modified during discharge transients, and the resulting different discharge curves are analyzed to determine fault parameters.

The proposed impedance-based approach eliminates the need for additional voltage sources, active electronic modules, or modifications to existing circuit breaker topologies for active signal injection. It is seamlessly integrated with current DC circuit breaker systems and eliminates inter-terminal communication delays, ensuring practicality and compatibility with existing infrastructure.

The method's validity was demonstrated through electromagnetic transient simulations, with comprehensive testing performed across a range of fault locations and resistances. Results indicate that fault location errors remain below 5% for fault resistances up to 50 Ω. Critical insights reveal that the time constants derived from the exponential decay of re-energization currents are pivotal in accurately estimating fault location and resistance. The method performs best for faults farther from the active terminal, with higher errors observed for short fault distances and elevated fault resistances due to the limitations in sampling frequency.

The presented results validate the proposed fault location method through detailed simulations. However, experimental verification should be conducted in future work, on a scaled-down MVDC setup, in order to fully substantiate the effectiveness of the method.

Future developments of the proposed method will focus on adapting it for real-scale implementations, including the assessment of the sizing requirements and installation constraints of the additional switchgear. Furthermore, extensions of the proposed approach should be explored to manage more complex scenarios, such as non-fully-selective multi-terminal DC grids.

Author Contributions: Conceptualization, K.M.; methodology, K.M. and J.D.; software, K.M. and J.D.; validation, K.M., J.M.G. and C.A.P.; formal analysis, K.M., J.M.G. and C.A.P.; investigation, K.M. and J.D.; resources, K.M.; data curation, K.M.; writing—original draft preparation, K.M.; writing—review and editing, K.M., J.M.G., J.D. and C.A.P.; visualization, K.M.; supervision, C.A.P.; project administration, K.M.; funding acquisition, K.M. All authors have read and agreed to the published version of the manuscript.

Funding: This research was partially funded by the European Metrology Programme for Innovation and Research, grant 19ENG02 Future Energy.

Data Availability Statement: Datasets available on request from the authors.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. WG C6/B4.37 Cigre. *Medium Voltage DC Distribution Systems*; Ref. 875; CIGRE: Paris, France, 2022; ISBN 978-2-85873-580-8.
2. Wang, M.; Li, W.; Wang, S.; Xu, Q.; Zhang, X. Review and Outlook of HVDC Grids as Backbone of Transmission System. *CSEE J. Power Energy Syst.* **2021**, *7*, 797–810.
3. Mohan, F.; Sasidharan, N. Protection of Low Voltage DC Microgrids: A Review. *Electr. Power Syst. Res.* **2023**, *225*, 109822. [CrossRef]
4. Li, W.; Li, Y.; Yu, S.; Wei, T.; Chen, J.; Liu, Y.; Xu, S. State of the Art of Researches and Applications of MVDC Distribution Systems in Power Grid. In Proceedings of the IECON 2019—45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 14–17 October 2019; pp. 5680–5685.
5. Ciniello, V.; Loggia, R.; Martirano, L.; Lauria, S. A Review of MVDC Smart Grids Technologies and Components. In Proceedings of the 2024 IEEE/IAS 60th Industrial and Commercial Power Systems Technical Conference (I&CPS), Las Vegas, NV, USA, 19–23 May 2024; pp. 1–10.
6. Monadi, M.; Koch-Ciobotaru, C.; Luna, A.; Candela, J.I.; Rodriguez, P. A Protection Strategy for Fault Detection and Location for Multi-Terminal MVDC Distribution Systems with Renewable Energy Systems. In Proceedings of the 2014 International Conference on Renewable Energy Research and Application (ICRERA), Milwaukee, WI, USA, 27–30 October 2014; pp. 496–501.
7. Nougain, V.; Mishra, S.; Nag, S.S.; Lekić, A. Fault Location Algorithm for Multi-Terminal Radial Medium Voltage DC Microgrid. *IEEE Trans. Power Deliv.* **2023**, *38*, 4476–4488. [CrossRef]
8. Song, X.; Peng, C.; Huang, A.Q. A Medium-Voltage Hybrid DC Circuit Breaker, Part I: Solid-State Main Breaker Based on 15 kV SiC Emitter Turn-OFF Thyristor. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 278–288. [CrossRef]
9. Yang, J.; Fletcher, J.E.; O'Reilly, J. Short-Circuit and Ground Fault Analyses and Location in VSC-Based DC Network Cables. *IEEE Trans. Ind. Electron.* **2012**, *59*, 3827–3837. [CrossRef]
10. Feng, X.; Qi, L.; Pan, J. A Novel Fault Location Method and Algorithm for DC Distribution Protection. *IEEE Trans. Ind. Appl.* **2017**, *53*, 1834–1840. [CrossRef]
11. Bin Gani, M.; Brahma, S. A Closed-Form Mathematical Model and Method for Fast Fault Location on a Low Voltage DC Feeder Using Single-Ended Measurements. *IEEE Open Access J. Power Energy* **2022**, *9*, 523–536. [CrossRef]
12. Bhargav, R.; Bhalja, B.R.; Gupta, C.P. Novel Fault Detection and Localization Algorithm for Low-Voltage DC Microgrid. *IEEE Trans. Ind. Inform.* **2020**, *16*, 4498–4511. [CrossRef]
13. Park, J.; Candelaria, J.; Ma, L.; Dunn, K. DC Ring-Bus Microgrid Fault Protection and Identification of Fault Location. *IEEE Trans. Power Deliv.* **2013**, *28*, 2574–2584. [CrossRef]
14. Mohanty, R.; Balaji, U.S.M.; Pradhan, A.K. An Accurate Noniterative Fault-Location Technique for Low-Voltage DC Microgrid. *IEEE Trans. Power Deliv.* **2016**, *31*, 475–481. [CrossRef]
15. Aluri, V.R.K.; Samantaray, S.R. An Improved Probe Power Unit (PPU)-Based Fault Location Estimation in Low-Voltage DC Microgrids. *IEEE Trans. Smart Grid* **2024**, *15*, 5514–5525. [CrossRef]
16. Yang, Y.; Huang, C.; Xu, Q. A Fault Location Method Suitable for Low-Voltage DC Line. *IEEE Trans. Power Deliv.* **2020**, *35*, 194–204. [CrossRef]
17. Yang, Y.; Huang, C.; Zhou, D.; Li, Y. Fault Detection and Location in Multi-Terminal DC Microgrid Based on Local Measurement. *Electr. Power Syst. Res.* **2021**, *194*, 107047. [CrossRef]
18. Liu, W.; Liu, F.; Zha, X.; Huang, M.; Chen, C.; Zhuang, Y. An Improved SSCB Combining Fault Interruption and Fault Location Functions for DC Line Short-Circuit Fault Protection. *IEEE Trans. Power Deliv.* **2019**, *34*, 858–868. [CrossRef]
19. Zhang, C.; Song, G.; Wang, T.; Yang, L. Single-Ended Traveling Wave Fault Location Method in DC Transmission Line Based on Wave Front Information. *IEEE Trans. Power Deliv.* **2019**, *34*, 2028–2038. [CrossRef]

20. Song, G.; Wang, T.; Hussain, K.S.T. DC Line Fault Identification Based on Pulse Injection from Hybrid HVDC Breaker. *IEEE Trans. Power Deliv.* **2019**, *34*, 271–280. [CrossRef]
21. Farshad, M.; Karimi, M. A Signal Segmentation Approach to Identify Incident/Reflected Traveling Waves for Fault Location in Half-Bridge MMC-HVdc Grids. *IEEE Trans. Instrum. Meas.* **2022**, *71*, 3501209. [CrossRef]
22. Wang, D.; Hou, M. Traveling Wave Fault Location Principle for Hybrid Multi-Terminal LCC-VSC-HVDC Transmission Line Based on RECT. *Int. J. Electr. Power Energy Syst.* **2020**, *117*, 105627. [CrossRef]
23. Wang, J.; Zhang, Y. Traveling Wave Propagation Characteristic-Based LCC-MMC Hybrid HVDC Transmission Line Fault Location Method. *IEEE Trans. Power Deliv.* **2022**, *37*, 208–218. [CrossRef]
24. Kwon, G.-Y.; Lee, C.-K.; Lee, G.S.; Lee, Y.H.; Chang, S.J.; Jung, C.-K.; Kang, J.-W.; Shin, Y.-J. Offline Fault Localization Technique on HVDC Submarine Cable via Time–Frequency Domain Reflectometry. *IEEE Trans. Power Deliv.* **2017**, *32*, 1626–1635. [CrossRef]
25. Song, G.; Hou, J.; Guo, B.; Wang, T.; Masood, B.; Kazmi, S.T.H. Single-Ended Active Injection for Fault Location in Hybrid MMC-HVDC Systems. *Int. J. Electr. Power Energy Syst.* **2021**, *124*, 106344. [CrossRef]
26. Hou, J.; Song, G.; Fan, Y. Fault Identification Scheme for Protection and Adaptive Reclosing in a Hybrid Multi-Terminal HVDC System. *Prot. Control Mod. Power Syst.* **2023**, *8*, 23. [CrossRef]
27. Allam, M.A.; Saleh, K.A. A Novel DC Distance Relay for MVDC Microgrids. *IEEE Trans. Smart Grid* **2022**, *13*, 962–974. [CrossRef]
28. Kaharević, A.; Ramos, J.C.; Jahn, I.; Ponci, F.; Monti, A. A Review of HVDC and MVDC Grid Protection. In Proceedings of the 19th International Conference on AC and DC Power Transmission (ACDC 2023), Glasgow, UK, 1–3 March 2023; pp. 271–280.
29. Nourmohamadi, H.; Gohil, G.; Balsara, P.T. Fault Location and Classification for MVDC Networks. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 589–603. [CrossRef]
30. Li, D.; Ukil, A. Fault Location Estimation in Voltage-Source-Converter-Based DC System: The L Location. *IEEE Trans. Ind. Electron.* **2022**, *69*, 11198–11209. [CrossRef]
31. Hou, J.; Song, G.; Sun, Y.; Fan, Y.; Wu, X.; Chang, P.; Chang, N. Permanent Fault Identification and Location Scheme for MTDC Grid Based on Equivalent Impedance Phase Characteristics and Distributed Parameter Line. *Int. J. Electr. Power Energy Syst.* **2023**, *153*, 109326. [CrossRef]
32. Kamalinejad, K.; Iman-Eini, H.; Samimi, M.H. A Modification in Thyristor-Based Hybrid DC Circuit Breaker for DC-Side Fault Identification in Auto-Reclosing of MMC-HVDC Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2023**, *11*, 4119–4126. [CrossRef]
33. Zheng, S.; Kheirollahi, R.; Pan, J.; Xue, L.; Wang, J.; Lu, F. DC Circuit Breakers: A Technology Development Status Survey. *IEEE Trans. Smart Grid* **2022**, *13*, 3915–3928. [CrossRef]
34. Mei, J.; Ge, R.; Zhu, P.; Fan, G.; Wang, B.; Yan, L. An Adaptive Reclosing Scheme for MMC-HVDC Systems Based on Pulse Injection From Parallel Energy Absorption Module. *IEEE Trans. Power Deliv.* **2021**, *36*, 1809–1818. [CrossRef]
35. Dworakowski, P.; Páez, J.D.; Grieshaber, W.; Bertinato, A.; Lamard, E. Protection of Radial MVDC Electric Network Based on DC Circuit Breaker and DC Fuses. *Int. J. Electr. Power Energy Syst.* **2023**, *153*, 109398. [CrossRef]
36. Bose, J.; Martins, S.; Chaudhary, S.; Teodorescu, R. Analysis of Back-to-Back MMC for Medium Voltage Applications Under Faulted Condition. In Proceedings of the IECON 2017—43rd Annual Conference of the IEEE Industrial Electronics Society, Beijing, China, 29 October–1 November 2017; pp. 858–963.
37. Rao, N.P.; Shukla, A. Analysis of Capacitor Voltage Unbalance in Hybrid MMC and Its Novel Operation with Reduced Submodule Capacitance. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 7271–7284. [CrossRef]
38. Li, H.; Xie, X.; McDonald, A.; Chai, Z.; Yang, T.; Wu, Y.; Yang, W. Cost and Reliability Optimization of Modular Multilevel Converter with Hybrid Submodule for Offshore DC Wind Turbine. *Int. J. Electr. Power Energy Syst.* **2020**, *120*, 105994. [CrossRef]