A Fully Integrated 6–18 GHz Transmit/Receive MMIC Frontend Implemented in 150-nm GaN-on-SiC Technology

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***Abstract*—This work presents a monolithic transmit/receive (T/R) frontend covering the 6–18-GHz frequency band and implemented in 150-nm gallium-nitride (GaN) technology. The benefits of single-die integration are harnessed through a top-down, system-level co-design approach, where specifications and system tradeoffs are addressed directly at the die level: an asymmetric T/R switch simplifies the transmit path to save for output power and efficiency, while its receive branch is merged with the low-noise amplifier's input matching network for improved compactness and sensitivity; the floorplan is optimized from the start, implementing single-side biasing for all subcircuits to minimize T/R coupling. On-wafer measurements demonstrate an average transmit output power of 9.5 W (minimum of 5.6 W) with 19.4% efficiency (minimum of 13.5%) across the target bandwidth. In receive mode, the prototypes achieve over 21-dB gain with an average noise figure of 3 dB (maximum of 3.3 dB). These results are consistent with, and in some aspects exceed, those reported in the literature for ultrawideband GaN-based single-chip T/R frontends. Furthermore, the prototypes were also successfully tested in bare–die configuration on a custom evaluation fixture, confirming robust performance under realistic system conditions with only minor degradation compared with on-wafer measurements.**

***Index Terms*—Gallium nitride (GaN), high-electron-mobility transistors (HEMTs), III–V semiconductor, low-noise amplifiers, power amplifiers, transmit/receive (T/R) module, ultrawideband radar.**

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I. Introduction

MONOLITHIC microwave integrated circuits (MMICs) compacting the most critical radio frequency (RF) functions of a transceiver frontend—such as high-power amplification (HPA), low-noise amplification (LNA), and RF path selection—are key for advancing next-generation active phased-array systems. Compared with the prevailing gallium-arsenide (GaAs) solutions, gallium-nitride (GaN) high-electron-mobility transistors (HEMTs) offer superior power density and breakdown voltage. These features lead to efficient HPAs with smaller footprints and robust LNAs that do not require additional protection circuitry. This enables compact single-chip front-ends (SCFEs) that can deliver higher power and a comparable noise figure (NF) to GaAs solutions [1], [2], [3], [4], [5], [6].

While several GaN SCFE MMICs have been reported for the S-, C-, X- and Ku-bands [5], [6], [7], [8], [9], the literature on ultrawideband SCFEs spanning the C-to-Ku band remains limited. To date, only Palombini et al. [2], Lin et al. [4], and Antolinos et al. [10] describe such MMIC designs. In contrast, C-to-Ku GaN HPA, LNA, and switch are well-documented as standalone MMICs [11], [12], [13], [14], [15], [16]. Co-integrating these RF subcircuits into a single die would offer significant advantages over traditional hybrid implementations, such as a smaller footprint, enhanced performance, and improved robustness due to the elimination of high-frequency interconnections. However, the monolithic approach introduces additional challenges, including tradeoffs in die size, circuit complexity, and transmit/receive (T/R) isolation.

Understanding the strategic potential of GaN technology for the defense sector, the "European Innovative GaN Advanced Microwave Integration" (AGAMI_EURIGAMI) project is currently underway, aiming to establish a competitive European supply chain for the development of the high-performance GaN-based RF electronic components required in current and future military systems [17]. In the context of this project, several technology demonstrators have been developed, among which is the T/R SCFE MMIC reported in this work.

The proposed MMIC, shown in Fig. 1, was implemented in a 150-nm GaN-on-SiC process offered by the European

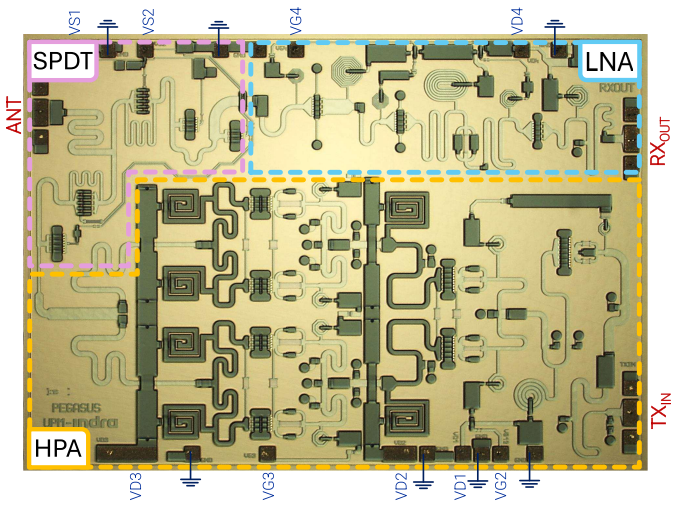

Fig. 1. Photograph of the prototyped MMIC with area of 4.9 × 3.4 mm^2.

foundry United Monolithic Semiconductors (UMS). The SCFE was designed to achieve half-duplex operation from 6 to 18 GHz. It comprises an HPA for transmission (Tx), an LNA for reception (Rx), and a single-pole double-throw (SPDT) switch for T/R mode selection. The novelty of the work lies not only in the individual subcircuit designs, but in their monolithic integration into a single GaN MMIC, which enables concurrent system-level optimization of the floorplan and the subcircuit interfaces. Distinctive features include the single-side biasing solution for the wideband HPA and the co-design of the switch-to-LNA interface, both of which are unconventional strategies directly linked to the monolithic approach. In particular, this manuscript builds upon our previous publication in [18] by providing a more comprehensive description of circuit-level design methods (see Sections II-A–II-C), by including system-level verification of the full MMIC (see Section II-D), and by presenting additional experimental results beyond on-wafer testing, with the MMIC prototypes wirebonded to a test fixture (see Section III), which validate the MMIC performance under realistic system operation conditions.

II. Design

The SCFE MMIC was implemented using UMS GH15-11 GaN-on-SiC monolithic process. This technology employs AlGaN/GaN HEMTs with a 150-nm gate length on a 70-μm-thick SiC substrate, offering a peak power density above 5 W/mm at 18 GHz. Key transistor parameters for this technology include a typical pinch-off voltage of −3.2 V, a maximum drain current (I_{DSS}) of 1400 mA/mm, and peak transconductance of 390 mS/mm. The process provides cut-off and maximum oscillation frequencies (f_T and f_{max}) of 35 GHz and 90 GHz, respectively. Two FET topologies are available in the process design kit (PDK): one with source-terminated field plates for high-power applications, and one without field plates, optimized for low-noise and switching designs [19].

The SCFE was designed to operate over the 6–18-GHz band, targeting a Tx output power (P_{OUT}) and gain above 37 dBm and 18 dB, respectively, and an Rx gain of 20 dB with NF below 3 dB and an input 1-dB compression point (IP1dB) better than 0 dBm. To meet these requirements, the design was carried out using the Keysight Advanced Design System (ADS) circuit design environment, along with its associated electromagnetic (EM) solver, Momentum.

A. SPDT Design

From a system perspective, the main performance metrics for switch design are the insertion loss, the Tx-to-Rx isolation, and the power-handling capability. In Tx mode, low insertion loss under power stress improves power and efficiency, while high isolation is essential to protect the LNA from damage. In Rx mode, a low insertion loss guarantees a better sensitivity. The key building blocks for implementing wideband SPDT switches are series and shunt drain-unbiased HEMTs, whose parasitic OFF-state capacitances are inductively resonated to form an *L–C* ladder structure with the required bandwidth. The switching state of each HEMT device is controlled by its respective gate voltage, which is applied through a high-ohmic resistor ensuring proper RF isolation [2], [16], [20], [21].

The proposed SPDT switch, presented in Fig. 2, exploits the fully integrated approach by adopting an asymmetric topology, which saves for Tx output power, power-added efficiency (PAE), and die area as compared with traditional symmetric designs [4], [6], [21]. The active signal path is selected by setting the dc control voltages VS1 and VS2 to either 0 or −20 V, as detailed in the inset table in Fig. 2. The Rx path consists of an inductively resonated series device (*S1* = 8 × 40-μm wide) cascaded to two shunt HEMTs (*S2* = 6 × 68 μm, *S3* = 6 × 75 μm). The size of these FETs has been co-designed with the LNA input (see Section II-B) to provide the best possible sensitivity for the receiver while maintaining more than 30-dB Tx-to-Rx isolation in Tx mode. On the other hand, the Tx path adopts a simpler configuration, comprising an inductively resonated series device (*S4* = 8 × 60 μm) and a single shunt HEMT (*S5* = 8 × 75 μm). These devices are sized to handle the expected output power from the HPA (target of 38 dBm) with margin: as a standalone device with 50-Ω termination, *S4* achieves an IP1dB of 42 dBm, while *S5* operates safely within the limits of breakdown for an input power up to 42.5 dBm.

The switch was initially matched to 50 Ω at all ports. However, the interfaces with the amplifiers were later fine-tuned to facilitate matching and improve the overall system performance. To exclude the effect of reflections, the simulations of the standalone switch are presented here with conjugate matching at the amplifier ports. The small-signal insertion loss [see Fig. 3(a)] stays below 1 dB in Tx mode and under 1.3 dB in Rx mode from 6 to 18 GHz. On the other hand, the small-signal Tx-to-Rx isolation [see Fig. 3(b)] is better than 35.5 dB and 26 dB in Tx and Rx modes, respectively. The Tx-mode insertion loss and isolation degrade to 1.15 dB and 33.7 dB, respectively, for the target output power from the HPA (~38 dBm).

To understand which devices determine the saturation performance of the switch, a dynamic loadline analysis was carried out under increasing input power. In Tx mode, devices

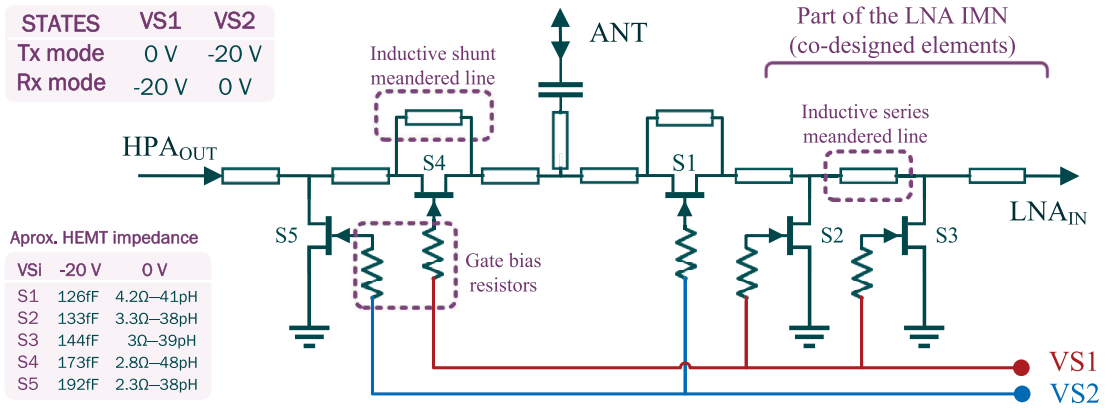

Fig. 2. Circuit schematic of the asymmetric SPDT switch. The internal ports of the switch interface directly with the input port of the LNA (see Fig. 5) and the output port of the HPA (see Fig. 8), respectively.

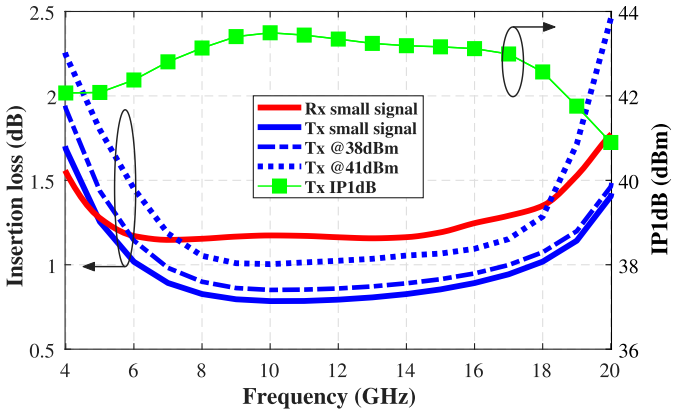

Fig. 3. Simulated performance of the switch. (a) Tx- and Rx-mode insertion loss and Tx-mode IP1dB. (b) Tx-mode isolation for the Tx-to-Rx path (from the HPA_{OUT} port to the LNA_{IN} port) and for the Ant-to-Rx path (from the ANT port to LNA_{IN} port). Insertion loss and isolation are calculated assuming conjugate matching at LNA_{IN} and HPA_{OUT} ports.

S2, *S3*, and *S4* are expected to operate ideally as short circuits ($I_{DS} \approx 0$), while *S1* and *S5* should act as open circuits ($V_{DS} \approx 0$). As the input power increases, these devices progressively deviate from their ideal operation. Fig. 4 illustrates the dynamic loadlines of the ON-state devices for an input power of 41 dBm (well above the expected 38 dBm). Devices

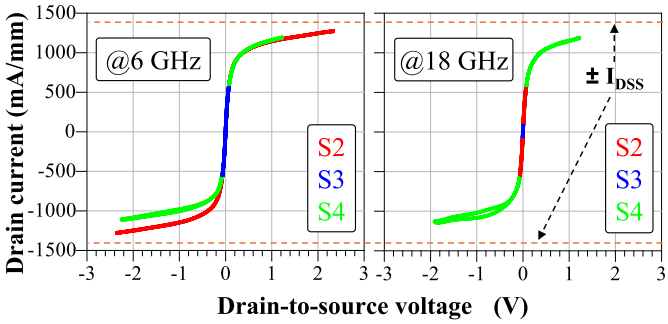

Fig. 4. Dynamic loadline analysis of the ON-state switch devices when the switch is biased in Tx mode. The HPA_{OUT} port is excited with 41 dBm (sinusoidal, 50-Ω power source). This input power level is 3 dB higher than expected from the HPA output.

S2 and *S4* exhibit clear signs of current saturation when the current swing approaches I_{DSS}. In fact, device *S2* exhibits significant saturation only at low frequencies, due to signal leakage through the inductive line in parallel with device *S1*. The leaked signals are absorbed by the shunt transistors in the Rx path (mainly *S2*), causing compression of the isolation curve at low frequencies [see Fig. 3(b)].

B. LNA Design

The Rx mode of the SCFE MMIC was specified to have a gain of 20 dB, NF better than 3 dB, and IP1dB of 0 dBm, all with a dc power consumption below 1.5 W. Considering the Rx-mode insertion loss expected from the switch [see Fig. 3(a)], the LNA has been designed to achieve an NF below 1.7 dB, with linear gain of at least 21.3 dB, and IP1dB better than −1.3 dBm. To meet these requirements, the LNA adopts the three-stage common-source cascaded topology illustrated in Fig. 5, which uses common dc gate- and drain-bias supply pads for all devices.

A drain supply voltage (VD4) of 7.5 V and a quiescent dc current density ($ID_{Q,Rx}$) of 195 mA/mm (VG4 ≈ −2.3 V) are selected to operate the LNA as a tradeoff to meet the required goals. Fig. 6 shows that the high bias point is necessary so that the input transistor (*F1*) achieves the best possible noise performance, which allows for an IP1dB

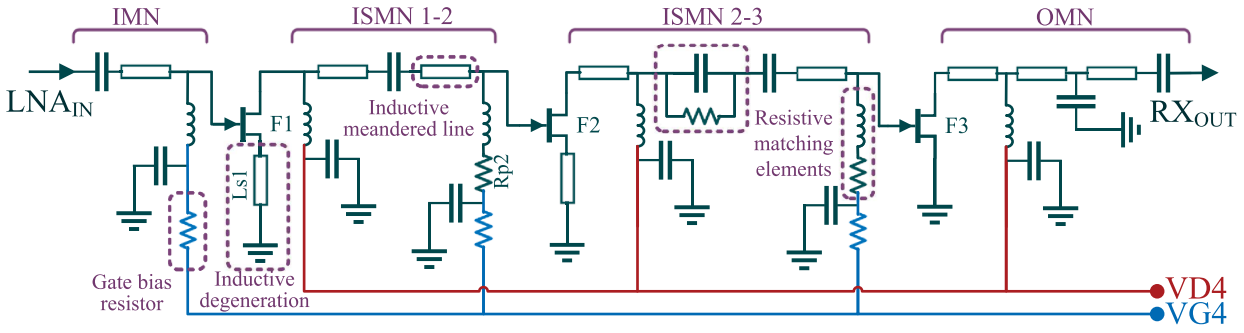

Fig. 5. Circuit schematic of the three-stage LNA. The LNA is nominally biased at VD4 = 7.5 V and $I_{DQ,Rx}$ = 195 mA/mm (VG4 ≈ −2.3 V). The LNA_{IN} port is directly connected to the SPDT switch (see Fig. 2).

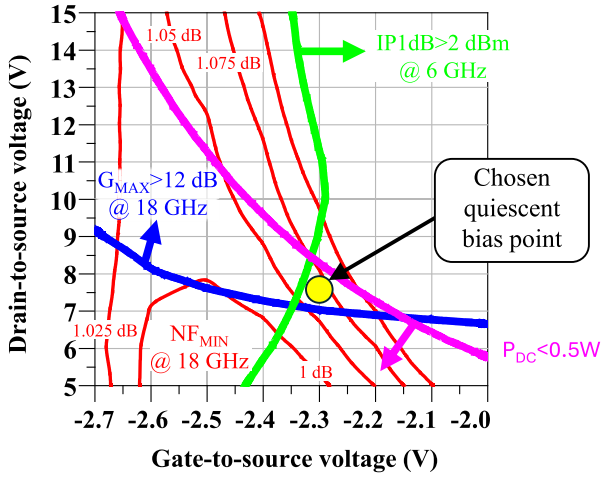

Fig. 6. Selection of the LNA quiescent bias point: contour plots of the key performance metrics for an 8 × 36 μm device without source-terminated field plates simulated across the drain- and gate-bias voltage planes (VD4, VG4). Arrows indicate the direction toward the optimum. The quiescent bias point is chosen at VD4 = 7.5 V and VG4 = −2.3 V, corresponding to ~195 mA/mm.

exceeding the LNA target by at least 3 dB, and an acceptable available power gain of at least ~12 dB. In fact, since the minimum NF is relatively flat across bias, the quiescent point and size are ultimately set by the gain and linearity requirements.

The first-stage device (*F1* = 8 × 36 μm) is a common-source transistor with inductive source degeneration implemented via the L_{s1} inductor. This topology shifts the gate input impedance (Z_{in}) of *F1* closer to the complex conjugate of the optimum source impedance for minimum noise (Z_{opt}) [22], [23], [24]. The shift in the target source impedance regions is illustrated in Fig. 7(a) for L_{s1} = 85 pH. The degree of alignment between those two impedances can be quantified by introducing a noise matching coefficient (Γ_{noise}), which leads to a corresponding definition of the noise-related return loss (NRL). Although not a standard term, the NRL, as defined below, provides a meaningful measure of how closely the input impedance of the device matches its optimum noise performance point:

$$\Gamma_{noise} = \frac{Z_{in} - Z_{opt}^{*}}{Z_{in} + Z_{opt}} \tag{1}$$

$$\mathrm{NRL\,(dB)} = -20\log\left(|\Gamma_{noise}|\right). \tag{2}$$

As shown in Fig. 7(b), the selected values for *F1* transistor size (8 × 36 μm) and source degeneration inductance (L_{s1} = 85 pH) yield a high value of NRL (above 8 dB), indicating that a source impedance exists which enables simultaneous noise and input impedance matching. With source degeneration, the minimum achievable NF (NF_{min}) for the stage remains below 1 dB, while its maximum transducer gain under stable, conjugate-matched conditions (G_{max}) still exceeds 10 dB.

Another key consideration in achieving a low-noise design is using a simple input matching network (IMN) with minimal loss [11]. This work addresses that goal by leveraging monolithic integration to relax the conventional arbitrary constraint of a fixed 50-Ω impedance at the switch-to-LNA interface (LNA_{IN} port). Furthermore, all required biasing components—choke inductors, bypass capacitors, and dc-blocking capacitors—are implemented as multifunctional elements that simultaneously serve as integral parts of the matching networks, thereby simplifying their design. Fig. 7(c) illustrates how the OFF-state parasitic capacitances of the shunt devices of the switch (*S2* and *S3* in Fig. 2) contribute significantly to achieving 50-Ω matching at the receiver input (ANT port of the MMIC) at mid-to-high frequencies, while the gate-bias inductor of *F1* facilitates impedance matching at lower frequencies.

The second and third stages are designed to meet the Rx gain, linearity, and dc power targets of the complete receiver. The output-stage device (*F3* = 8 × 41 μm) is sized to achieve an output 1-dB compression point (OP1dB) above 21 dBm. The intermediate-stage device (*F2* = 8 × 48 μm) was defined within the overall optimization process of the interstage matching networks (ISMNs). Its relatively large periphery prevents early compression of the low frequencies, as resistive gain-compensation is avoided at the IMN and the *F1*-to-*F2* ISMN (except for resistor R_{p2}) to preserve Rx sensitivity. In contrast, the *F2*-to-*F3* ISMN includes an *R–C* cell for gain flattening and low-frequency stabilization [23], [24].

Overall, the receiver design, including the SPDT switch and the LNA, meets all design targets with a quiescent dc power consumption of 1.46 W, which is consistent with the high IP1dB specification.

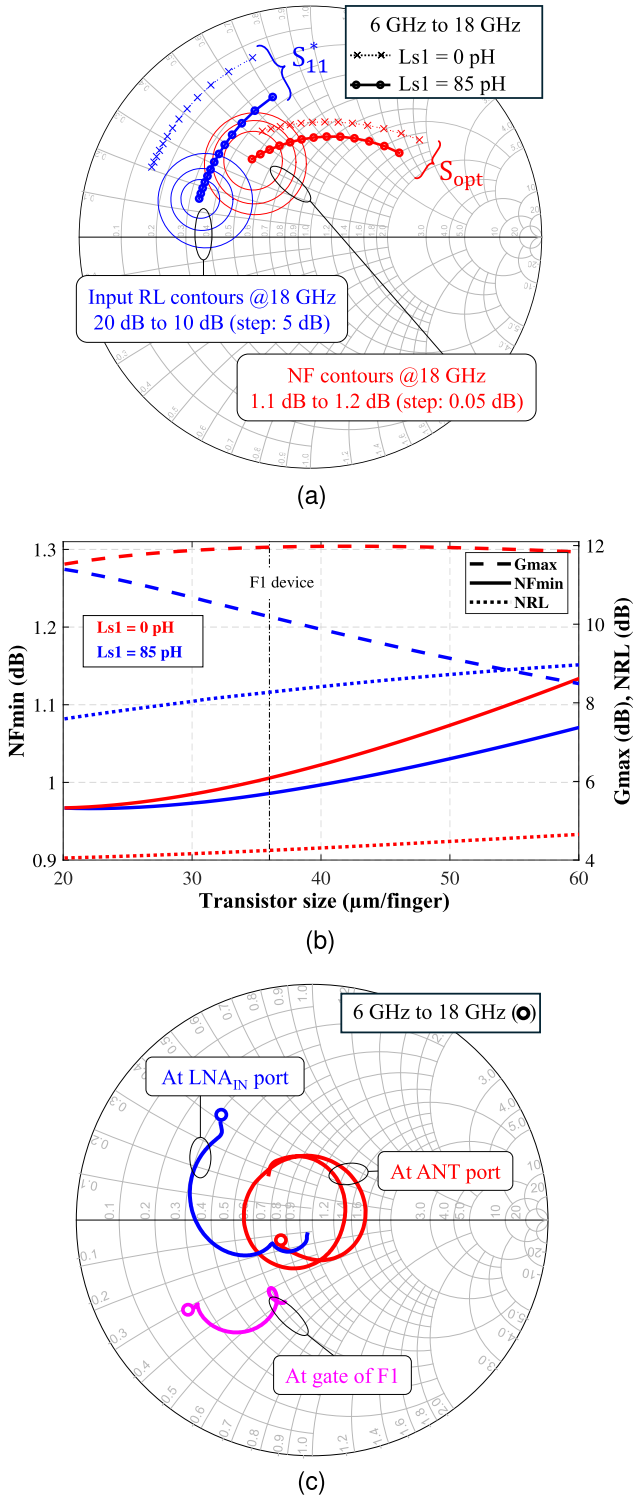

Fig. 7. Design of the LNA IMN. (a) Optimum source reflection coefficient targets (S_{opt} for best noise; S_{11}^* for best gain), with and without source degeneration at *F1* device. (b) Maximum transducer gain (G_{max}, NF_{min}), and NRL for different sizes of device *F1* at 18 GHz, with and without source degeneration. (c) Input reflection coefficient throughout the receiver interfaces. The LNA is biased at VD4 = 7.5 V and $I_{DQ,Rx}$ = 195 mA/mm. Source degeneration is applied to *F1* device via the L_{s1} inductor (see Fig. 5).

C. HPA Design

The Tx-mode performance targets for the SCFE MMIC are an output power of 37 dBm, PAE above 15%, and saturated gain greater than 18 dB. The HPA circuit topology, shown in Fig. 8, adopts a three-stage corporate architecture, with the final stage comprising four parallel common-source transistors. A key constraint is that the HPA must be biased from a single side of the die, which was considered from the start. The single-side bias network for ultrawideband operation is based on an earlier SCFE design [10], in which the drain-bias lines cross the RF paths via airbridges. Thus, in this design, the electromigration limit of a maximally wide airbridge (15 mA/mm) directly constrains the maximum dc current per HPA stage.

Considering the Tx-mode insertion loss introduced by the T/R switch [approximately 1 dB, Fig. 3(a)] and the output combining network (OCN, loss estimated at ~1 dB), each output-stage device must deliver at least 33 dBm with PAE better than 25% across the 6–18-GHz band. To meet this goal, the output stage employs four transistors (*Q4–Q7*), each with a gate periphery of 6 × 142 μm. They are biased at a drain supply voltage VD3 = 25 V (maximum recommended for this process) and a quiescent current density $I_{DQ,\,Q4–Q7}$ = 14 mA/mm (1% of I_{DSS}, class B). These values, determined from extensive load–pull analysis, represent a favorable trade-off between output power capability, efficiency, and thermal robustness of the devices (junction temperature, $T_j \ll 200$ °C). In addition, the low quiescent bias helps control the small-signal behavior during system start-up and testing.

Fig. 9(a) illustrates the optimal load impedance regions for one output-stage transistor, including its input stabilization network (*R–C* cell at gate). The load target for the HPA is the switch input impedance (nominally 50 Ω), which the OCN transforms into the target values inside the contours. Due to the broadband design (6–18 GHz), the most restrictive region occurs at 18 GHz, while the load–pull contours broaden at lower frequencies. As shown, the synthesized input impedance of the OCN network (solid black curve) remains within the frequency-dependent optimal regions for PAE > 25%, P_{OUT} > 33 dBm, and T_j < 150 °C, ensuring the target performance for the stage.

To meet the gain specification, the driver chain comprises two stages: the first consists of a single 12 × 56 μm transistor (*Q1*), while the second employs two parallel 10 × 62 μm transistors (*Q2–Q3*). Both stages are biased at VD1 = VD2 = 25 V with a quiescent current density $I_{DQ,\,Q1–Q3}$ = 250 mA/mm. They deliver around 25 dBm to each output-stage device.

The simulated additional losses introduced by the IMN, ISMN, and OCN networks are presented in Fig. 9(b). These networks incorporate the reactive effects of all components necessary for dc biasing the HPA, which are also integrated into the matching strategy. Notably, to achieve a flatter gain response across the target bandwidth (6–18 GHz), moderate attenuation is intentionally introduced at the lower frequencies of the band (6–9 GHz).

As noted above, the HPA is biased from one side only, which posed challenges for the drain-bias network design of the intermediate and output stages: to distribute dc current evenly among the parallel-combined transistors, a wide drain-bias line—incorporating bypass capacitors—crosses over the RF output Tx lines using airbridges; each transistor connects to the shared bias line through a dedicated drain-bias inductor

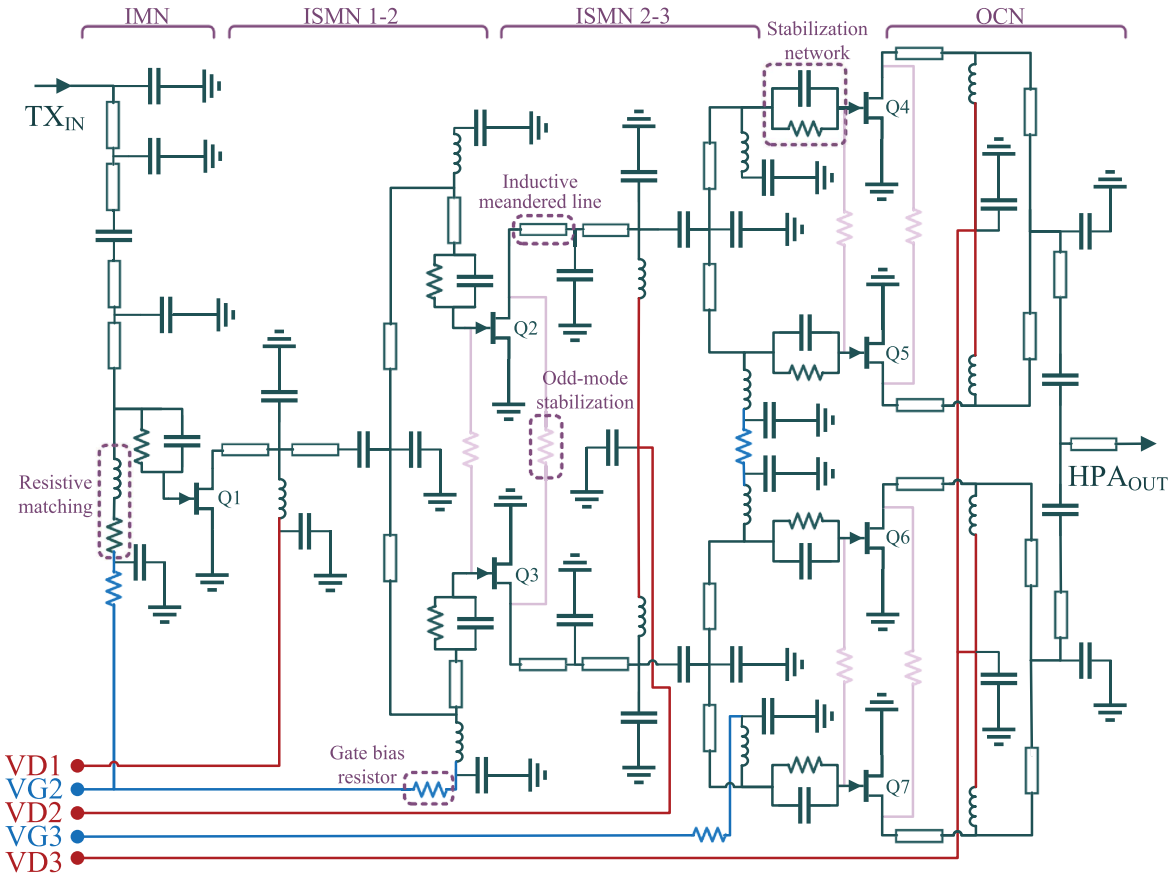

Fig. 8. Circuit schematic of the three-stage corporate HPA. The HPA is nominally biased at VD1 = VD2 = VD3 = 25 V, with $I_{DQ,\,Q1–Q3}$ = 250 mA/mm (VG2 ≈ −2.4 V) and $I_{DQ,\,Q4–Q7}$ = 14 mA/mm (VG3 ≈ −3.1 V). The HPA_{OUT} port is directly connected to the SPDT switch (see Fig. 2).

(see Fig. 1). This structure achieves a wideband response while preserving EM symmetry. Any residual odd-mode imbalances are mitigated using small-valued shunt resistors between adjacent parallel transistors, as illustrated in Fig. 8.

Overall, the designed HPA delivers more than 38.2 dBm to the SPDT switch for an input power of 19 dBm. Under this nominal drive, reliability constraints—such as electromigration, thermal robustness, and stability—were verified and satisfied with margin (more details in Section II-D).

D. Single-Chip Integration

The proposed T/R chip was conceived from the beginning as a fully integrated system, enabling a concurrent design of its functional blocks—LNA, HPA, and switch—at the die level. The layout floorplan was defined early in the design process to balance the available die area (4.9 × 3.4 mm^2) with the complexity of RF and bias circuits. As shown in Fig. 1, the switch was placed at one die corner to free horizontal space for the HPA, while both the LNA and the HPA were vertically compressed to fit the die height. This dense arrangement required extensive EM co-optimization of layout structures to preserve RF performance, especially at high frequencies. Fig. 10 shows the simulated load–pull contours for the load at the ANT port of the MMIC at three representative frequencies across the band. Solid contours indicate the target design goals for Tx and Rx operation, showing that the proposed design achieves a balanced compromise between all T/R constraints even in the presence of moderate load mismatch. Furthermore, both small- and large-signal stability were verified, including internal loop-gain analysis using probes at the internal nodes. No signs of instability were observed under any bias or mismatch condition.

Full-chip EM simulations with nominal Tx power (19 dBm) predict a TX_{IN}-to-RX_{OUT} isolation better than 26.4 dB with the LNA OFF and −3.5 dB with the LNA ON, as shown in Fig. 11. In such conditions, a maximum power of ∼9 dBm reaches the LNA input through the switch, which the LNA was designed to tolerate reliably (limited by metal electromigration to 17 dBm), even if left ON during continuous-wave (CW) Tx operation. When the LNA is OFF, the dominant Tx–Rx coupling mechanism is EM proximity of LNA and HPA on the layout, rather than the electrical isolation provided by the switch.

As previously commented in Section II-C, the single-die approach was leveraged by co-designing the shunt devices in the Rx path of the switch with the LNA, so that their OFF-state capacitances contribute significantly to matching the ANT port to 50 Ω (see Section II-B). This approach removed unnecessary elements in the IMN, improving Rx sensitivity. In contrast, the switch-to-HPA interface followed the traditional sequential approach: the switch was designed first at ∼50 Ω,

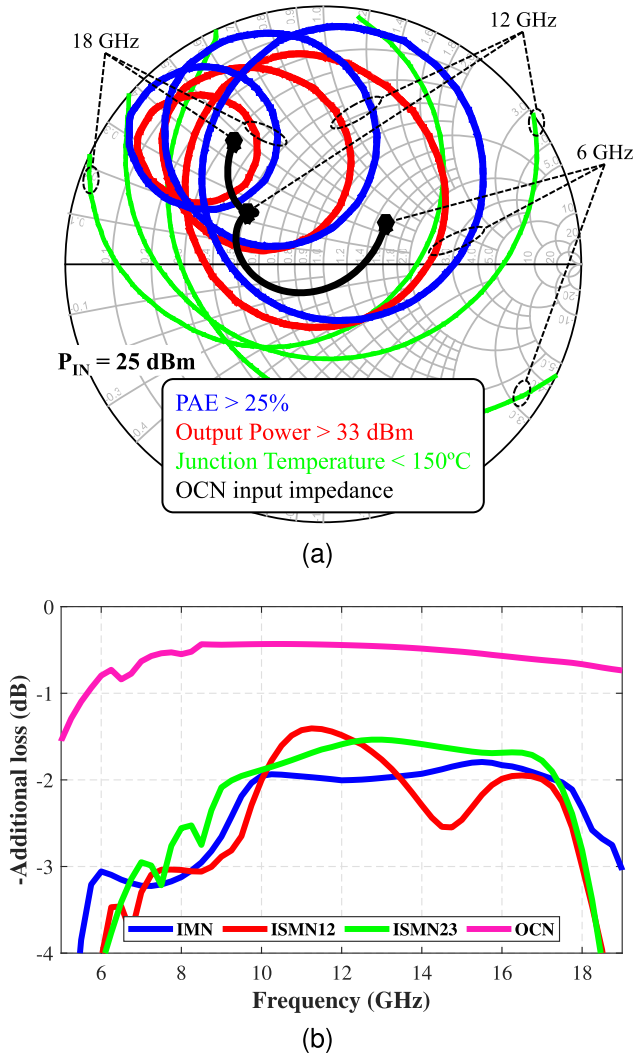

Fig. 9. Design of the HPA matching networks. (a) Load–pull contours and synthesized load impedance for a stabilized output-stage transistor (*Q4–Q7*) dc-biased at VD3 = 25 V and $I_{DQ,\,Q4–Q7}$ = 14 mA/mm with input power of 25 dBm. (b) Additional loss of the IMN, ISMN, and OCN networks.

and its input impedance was the load target for the HPA. Since 3-D integration options are unavailable for this process, both amplifiers are biased from a single side only, which added complexity to the drain-bias network design for parallel devices in the HPA (see Section II-C).

Transient simulations of the complete T/R chip indicate a switching time of around 7 ns, enabling fast T/R transitions in pulsed radar operation. This value is likely optimistic, as some dispersive effects are not modeled by the PDK switching device models [19], and an ideal driver was assumed.

Under nominal Tx drive in CW mode, the simulated average power dissipation across the 6–18-GHz band is 39.4 W, with a peak of 50 W near 9 GHz, as shown in Fig. 12. Under these conditions, the predicted peak junction temperature of the output-stage devices is below 164 °C, remaining well below the recommended process limit of 200 °C with an adequate margin for reliable operation. Finally, it was also essential to size the width of all conductor traces and resistors to comply with the foundry's electromigration and power

TABLE I
SUMMARY OF ELECTROMIGRATION ANALYSIS IN CW MODE

Stage	Peak total DC current (nominal)	Limiting component: rating	Max. input power
HPA 1	187 mA	Drain-bias inductor: <275 mA	25.5 dBm
HPA 2	556 mA	Drain-bias inductors: <417 mA	>30 dBm
HPA 3	1752 mA	Drain-bias capacitors: <2 A	>30 dBm
LNA 1	56 mA	Drain-bias inductor: <110 mA	17.5 dBm
LNA 2	75 mA	Drain-bias inductor: <165 mA	16 dBm
LNA 3	64 mA	Drain-bias inductor: <165 mA	>20 dBm

Note: Maximum current and input power ratings according to foundry recommendation on the maximum mean current density [19]. HPA currents correspond to Tx CW mode with input power at TX_{IN}; LNA currents correspond to Rx CW mode with input power at the ANT port.

dissipation guidelines for long-term reliability [19]. Table I reports the most critical component on each amplifier stage and their corresponding electromigration limit.[1]

III. RESULTS

The MMIC prototypes were fabricated and measured on-wafer prior to dicing. To further assess their performance under conditions representative of real-world operation, a custom evaluation printed circuit board (PCB) was developed. This on-jig measurement setup enables testing the MMICs in an operational environment closely resembling their deployment within a fully assembled system.

A. Measurement Setup

On-wafer measurements were conducted on over 130 samples across three different wafers using RF probes directly on the semiconductor wafer. These tests were carried out by the foundry service in pulsed-wave (PW) mode (30-μs pulses at a 10% duty cycle) to limit self-heating, as active cooling is not possible during this type of testing. In contrast, on-jig measurements allow for proper thermal control and were performed under CW excitation.

A photograph of the test PCB used for on-jig characterization is presented in Fig. 13(a). The MMIC sample was first mounted onto a nickel-plated copper (Cu) carrier employing AuSn eutectic solder. A Cu carrier was chosen over other options for its higher thermal conductivity and the possibility of X-ray inspection of the solder joints. This metallic carrier acts as an effective heat sink, which is essential to mitigate thermal performance degradation when the MMIC is operated under CW conditions. After the die attachment, the evaluation board was affixed on top of the carrier using conductive epoxy.

The PCB includes RF traces to route the MMIC's RF ports to the PCB coaxial connectors, as well as an external biasing network incorporating appropriate decoupling and filtering components to suppress low-frequency noise and prevent the risk of bias oscillations. Electrical connections between the PCB and the bare–die—both dc and RF—were implemented

[1]There are uncertainties in the simulated nonlinear behavior of the LNA, as the nonlinear device models in the PDK are not validated for V_{DS} < 20 V.

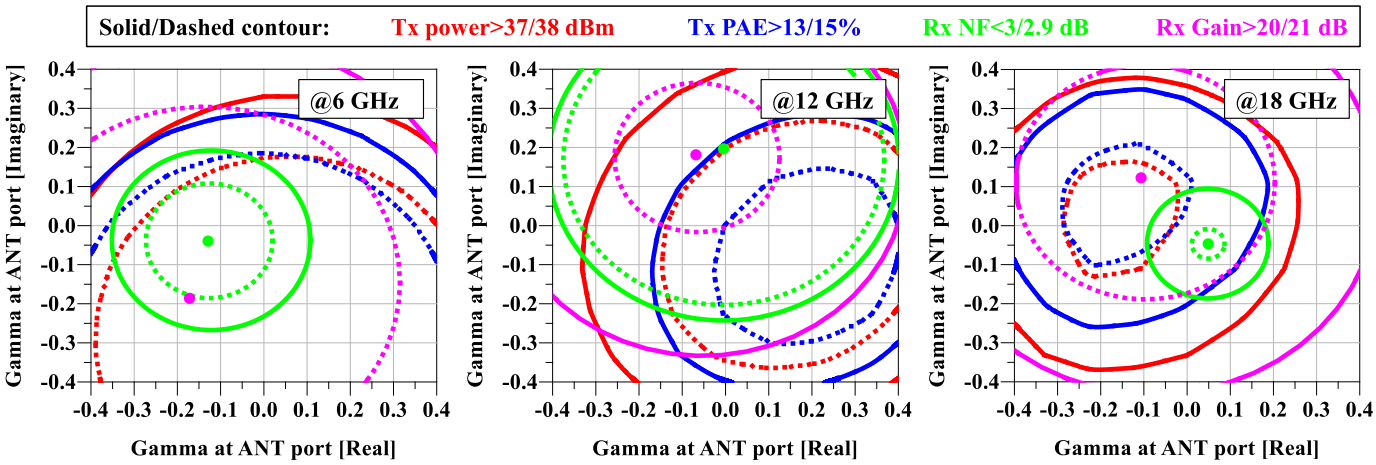

Fig. 10. Simulated load–pull/source–pull contours in Tx and Rx modes for the load at the ANT port of the MMIC. Simulations correspond to Tx mode with 19-dBm input power and Rx mode in the small-signal regime, both with nominal dc biasing. The solid contours represent the SCFE MMIC specifications.

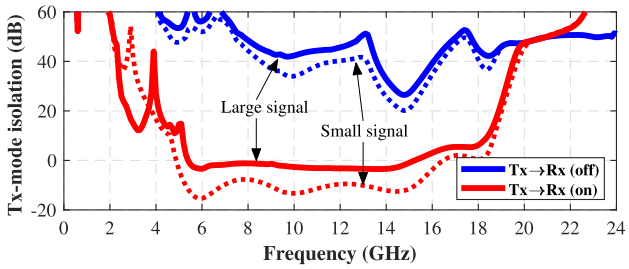

Fig. 11. Simulated Tx-mode isolation from the TX_{IN} port to the RX_{OUT} port. Simulations are shown for the small-signal regime (dashed) and the large-signal regime (solid) with 19-dBm input power at TX_{IN}.

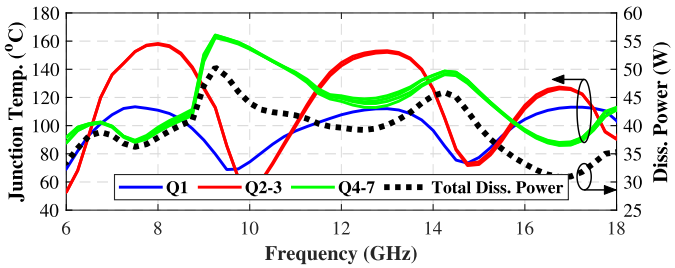

Fig. 12. Simulated junction temperatures of the HPA devices in Tx mode with 19-dBm input power at TX_{IN} port and nominal dc biasing.

using gold wire bondings. In addition, a thru-reflect-line (TRL) calibration fixture was designed and fabricated to enable accurate de-embedding of the on-jig measurements up to the MMIC interface.

On-jig characterization was carried out under CW excitation to evaluate the MMIC operation in the worst case operational scenario expected for a phased-array system (e.g., jamming mode in electronic warfare applications). In this context, effective thermal management is critical to mitigate self-heating effects, which could otherwise lead to excessive junction temperatures compromising both performance and device reliability. Thus, for testing, the carrier was mounted on an actively cooled base plate (cold plate), capable of maintaining a constant temperature of approximately 20 °C

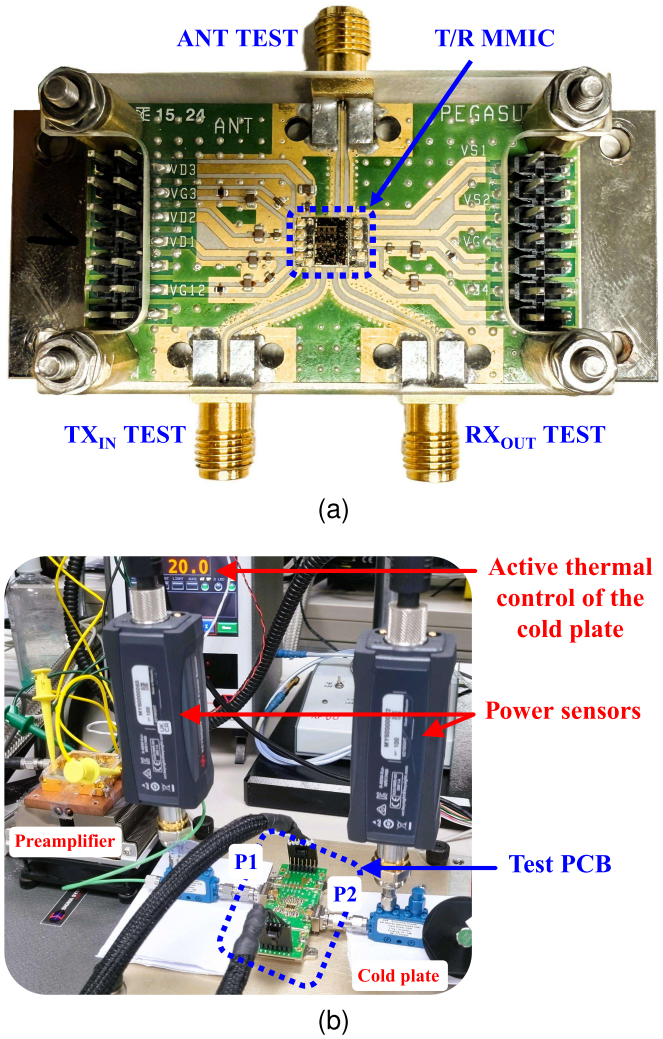

Fig. 13. Photographs of the test setup for on-jig characterization. (a) PCB assembly. (b) Test setup for large-signal characterization.

at the topside of the carrier, thereby ensuring thermal stability throughout the measurements. Due to imperfect thermal contact, achieving this temperature required operating the cold

plate at a lower temperature. Small-signal characterization was conducted in a vector network analyzer (Keysight M9837A), whereas large-signal measurements involved the use of directional couplers (Pasternack PE2CP1122-20) and power sensors (Keysight U2064XA) to accurately monitor input and output power levels at the PCB ports. A photograph of the large-signal test setup is shown in Fig. 13(b): this setup is driven by a signal generator followed by a wideband preamplifier (Pasternack PE15A4058), which then feeds the required input power level to the PCB; the output path ends with an attenuator and a matched load.

B. Small-Signal Characterization

Figs. 14 and 15 present the small-signal performance of the prototypes under Rx- and Tx-mode operation, respectively. In particular, each figure compares the simulated data with both the average of all on-wafer measurement curves and the measured performance of two representative die samples assembled on a test jig. In addition, the spread of the on-wafer measurements is reported by showing a shaded region including the 5th-to-95th percentile range across frequency. This representation captures the central 90% of the measured data, excluding the influence of extreme outlier samples.

In Rx mode, on-wafer characterization shows a typical linear gain higher than 21 dB, with gain ripple within ±0.4 dB across the target bandwidth from 6 to 18 GHz [see Fig. 14(a)]. The input return loss (IRL) and output return loss (ORL) exceed 8.5 dB and 10.8 dB, respectively [see Fig. 14(b) and (c)]. These curves align closely with the simulated data, except for a noticeable shift in the IRL at high frequency, which slightly reduces the bandwidth compared with the simulation. Fig. 14(a) shows that the linear gain remains nearly the same in the on-jig setup. However, the IRL and ORL curves measured on jig now exhibit a ripple pattern [see Fig. 14(b) and (c)], which is attributable to the parasitic inductance introduced by the bonding wires at the MMIC-to-PCB interfaces—elements not accounted for in the TRL calibration.

Fig. 14(d) presents the Rx NF, including the contribution of the switch. Measured on wafer at room temperature, the prototypes exhibit an average Rx NF of 3 dB across the 6–18-GHz band, with a maximum of 3.3 dB at the lower end of the band. The measured NF is roughly 0.2 dB higher than predicted from the simulation. This small discrepancy is consistent with previous designs [10] using the same technology, suggesting the noise might be underestimated in the foundry's device models. In addition, on-jig measurements indicate a further NF increase of about 0.2 dB compared with on-wafer results.

In Tx mode, as shown in Fig. 15, the MMIC prototypes demonstrate on-wafer linear gain exceeding 23 dB [see Fig. 15(a)] with IRL above 9 dB [see Fig. 15(b)] across the target bandwidth. In this design, the Tx-mode output was not matched, as observed in ORL curves [see Fig. 15(c)]. Similar to the Rx results, the measured S-parameters closely match the simulations, with only minor discrepancies between on-wafer and on-jig measurements.

Fig. 15(d) presents the small-signal isolation for the Ant-to-Rx and Tx-to-Rx leakage paths in Tx mode. The measured Ant-to-Rx isolation is above the noise floor of the VNA, indicating negligible coupling in this path. The Tx-to-Rx isolation is better than 33.6 dB, which is higher than predicted by standalone MMIC simulations—likely due to additional non-de-embedded effects from the test fixture.

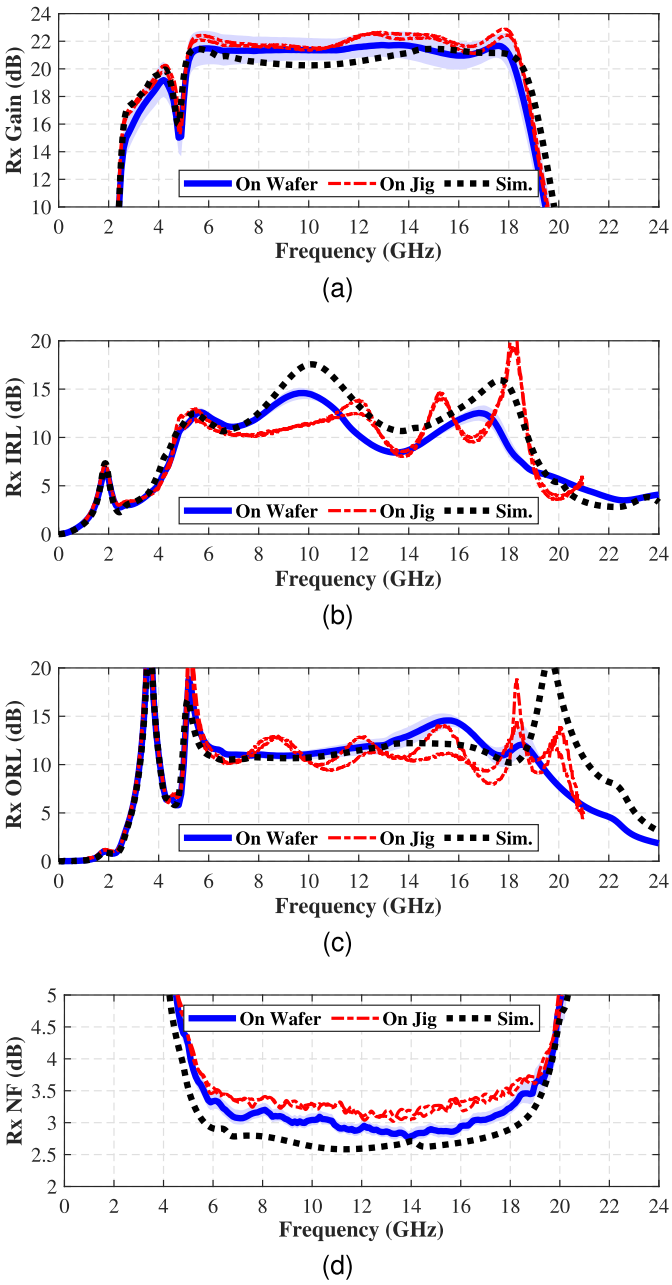

Fig. 14. Small-signal receiver performance comparing simulations, on-wafer measurements (134 samples), and on-jig measurements (two samples). (a) Transducer gain. (b) IRL. (c) ORL. (d) NF. DC bias condition: VD4 = 7.5 V, $ID_{Q.Rx}$ = 195 mA, and VD1 = VD2 = VD3 = 25 V, VG2 = VG3 = −10 V. For on-wafer measurements, the blue solid line represents the mean, and the shaded blue region indicates the 5th–95th percentile range.

C. Large-Signal Characterization

Fig. 16(a) and (b) presents the large-signal Tx performance of the MMIC for an available input power (P_{IN}) of 19 dBm at the TX_{IN} port. It is observed that the on-wafer measurements

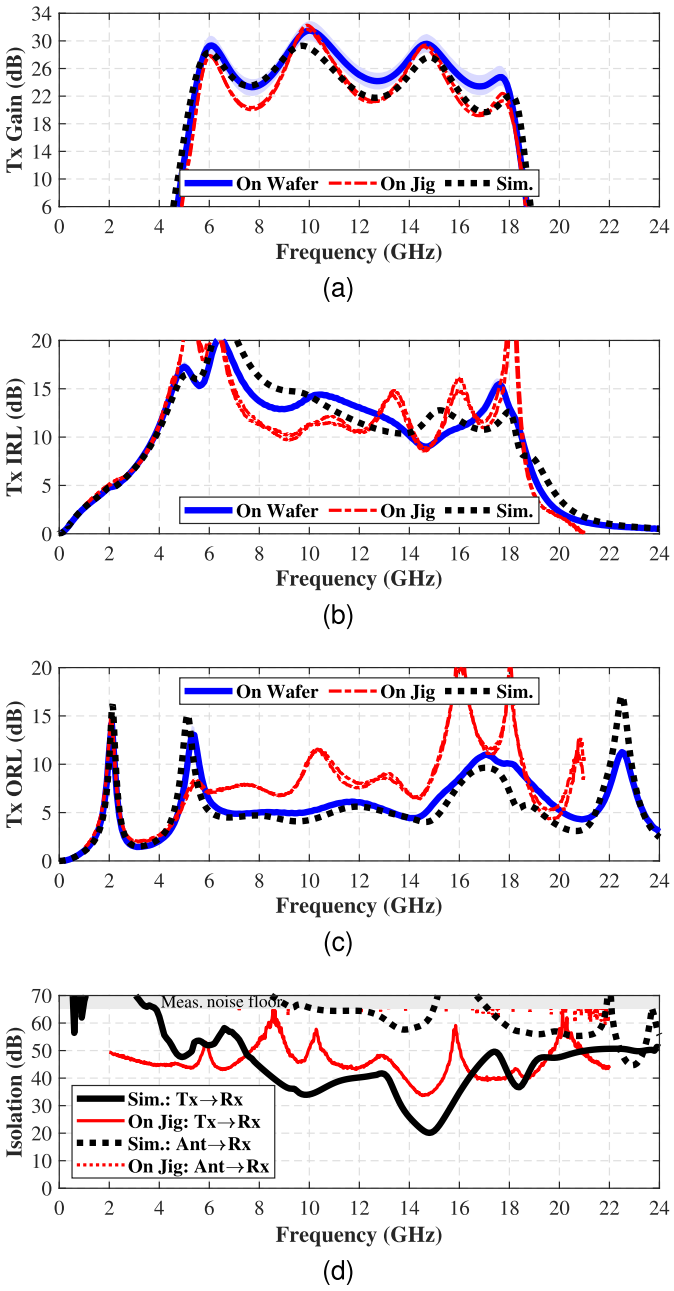

Fig. 15. Small-signal transmitter performance comparing simulations, on-wafer measurements (134 samples), and on-jig measurements (two samples). (a) Transducer gain. (b) IRL. (c) ORL. (d) Tx-mode isolation with LNA bias OFF. DC bias condition: VD1 = VD2 = VD3 = 25 V, $ID_{Q,Tx}$ = 525 mA, and VD4 = 7.5 V, VG4 = −10 V. For on-wafer measurements, the blue solid line represents the mean, and the shaded blue region indicates the 5th–95th percentile range.

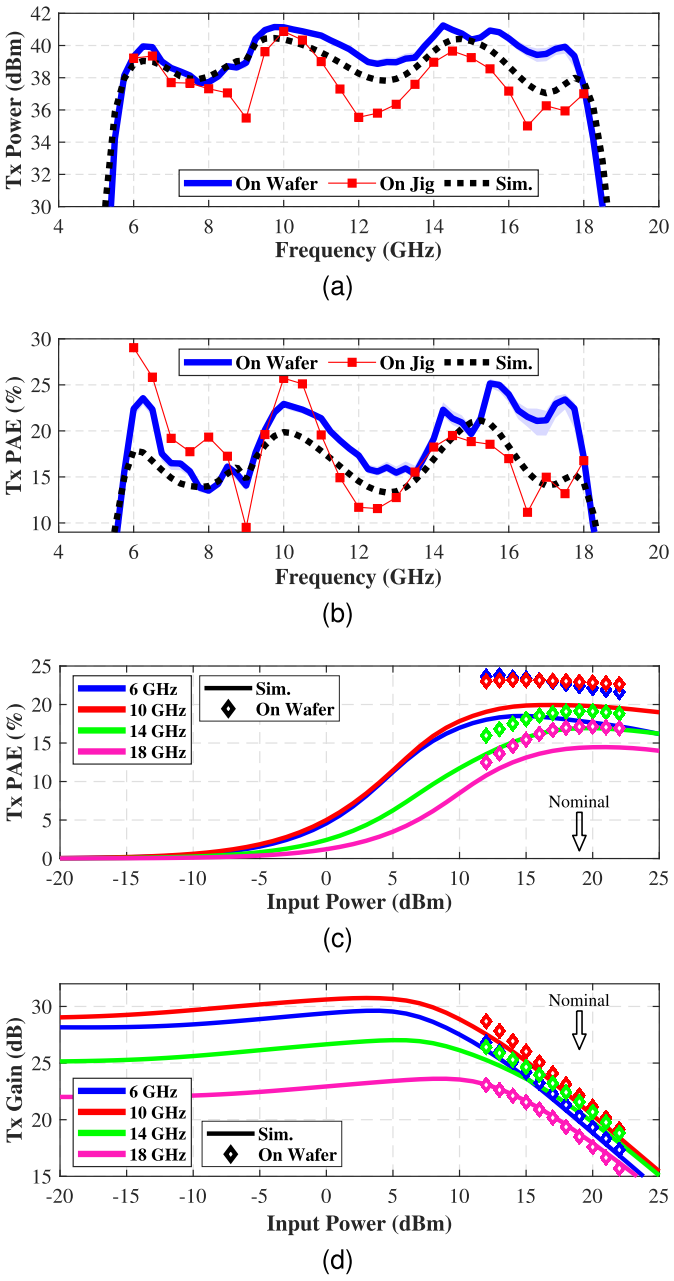

Fig. 16. Large-signal transmitter performance comparing simulations, on-wafer measurements (134 samples), and on-jig measurements (one sample). (a) Output power at nominal input power (P_{IN}) value of 19 dBm. (b) PAE at nominal P_{IN}. (c) PAE as a function of P_{IN}. (d) Transducer gain as a function of P_{IN}. DC bias condition: VD1 = VD2 = VD3 = 25 V, $ID_{Q,Tx}$ = 525 mA, and VD4 = 7.5 V, VG4 = −10 V. For on-wafer measurements in plots (a) and (b), the solid line represents the mean, and the shaded region indicates the 5th–95th percentile range.

outperform the simulation results, especially at the upper end of the frequency band. The average output power measured at the ANT port is 39.8 dBm (9.5 W) across the target 6–18-GHz band, with a minimum of 37.5 dBm (5.6 W) at 18 GHz [see Fig. 16(a)]. This corresponds to a saturated transducer gain above 18.5 dB. The measured dc current consumption under RF operation is 1.95 A, yielding an average PAE of 19.4% across the band, with a minimum of 13.5% at 8 GHz [see Fig. 16(b)].

On-jig measurements replicate the trends observed in the on-wafer characterization. However, they exhibit an average degradation of 1.75 dB in output power and 1.7 percentage points in PAE. This performance drop is attributed to parasitic effects of the bonding wires—consistent with the observations in the small-signal gain [see Fig. 15(a)]—and possible thermal performance degradation due to CW operation, which imposes greater thermal stress on the HPA devices compared with the PW conditions used during on-wafer testing.

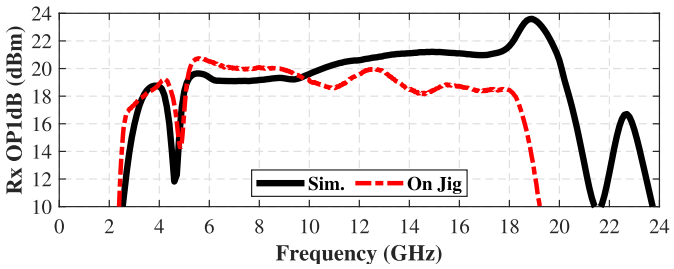

Fig. 17. Large-signal receiver performance comparing simulations and on-jig measurements: OP1dB. DC bias condition: VD4 = 7.5 V, $ID_{Q,Rx}$ = 195 mA, and VD1 = VD2 = VD3 = 25 V, VG2 = VG3 = −10 V.

TABLE II
STATISTICAL SPREAD OF KEY PERFORMANCE METRICS FROM ON-WAFER CHARACTERIZATION AT SELECTED FREQUENCIES

Freq. (GHz)	Rx Gain (dB)	Rx NF (dB)	Tx P_{OUT} (dBm)	Tx PAE (%)
6	20.3–22.7	3.2–3.4	39.2–39.4	21.6–22.8
12	20.8–22.5	2.9–3.1	39.2–39.6	16.9–17.8
18	19.8–22.4	3.2–3.4	36-6–38.1	15–18.8

Note: The values represent the 5th and 95th percentiles across 134 samples from 3 wafers. Tx data for an input power of 19 dBm.

Fig. 16(c) and (d) provides an overview of the on-wafer results and simulated performance of MMIC prototypes in Tx mode as a function of the input power. On average, the PAE peaks for P_{IN} values between 19 and 20 dBm [see Fig. 16(c)]. Dynamically optimizing P_{IN} for each frequency point would further increase the average and minimum PAE to 19.7% and 14.2%, respectively. On the other hand, Fig. 16(d) shows that the HPA operates in a high compression regime; in particular, at P_{IN} = 19 dBm, the measured average gain compression is 5.5 dB, which exceeds the simulated value of 4.8 dB. Nonetheless, simulations confirm that the MMIC remains within safe junction temperature limits under such compression. This conclusion is further supported by the previously discussed on-jig measurements, which were performed under CW excitation without any signs of long-term degradation or thermal failure.

To validate the Rx nonlinear performance, the OP1dB was measured on jig (see Fig. 17), showing values above 18 dBm across the band. This assesses the operation of nonlinear PDK devices at V_{DS} = 7.5 V, where they are still not validated by the foundry. Overall, the model agrees well with measurements up to ∼10 GHz, with deviations exceeding 3 dB at the upper edge of the band.

Finally, to provide a concise overview of the measured sample-to-sample variability, Table II summarizes the percentile limits of some key performance metrics of the MMIC prototypes. Overall, the measured sample-to-sample variability is small, as evidenced by the narrow percentile bands in all plots, with the exception of the small-signal gains, which exhibit a wider spread [see Figs. 14(a) and 15(a)]. The variability in Rx gain is attributed to a relatively small dc-blocking capacitor in the LNA, which has been confirmed by Monte Carlo simulations. In Tx mode, gain variability appears only under small-signal conditions, possibly due to the chosen quiescent bias near pinch-off.

TABLE III
LITERATURE ON SINGLE-DIE GAN-BASED T/R FRONTENDS

Parameter [a]	[2]	[4]	[10]	This work [b]
Freq. range (GHz)	5.5 – 18	2 – 18	4 – 18	6 – 18
Tx P_{OUT} (dBm)	∼36 {37.4}	38.2	34 {35.1}	37.5 {39.8}
Tx PAE (%)	∼8 {9.1}	7	16.6 {22.1}	13.5 {19.4}
Tx sat. gain (dB)	10 {11.4}	9.5	21 {22.1}	18.5 {20.8}
Tx P_{DC} (W)	{50}	—	17.4 {14.6}	62 {49}
Rx lin. gain (dB)	-4	∼17 {18}	24 {24.6}	21 {21.4}
Rx NF (dB)	—	3.5	3.5 {3.15}	3.3 {3}
Rx OP1dB (dBm)	—	∼16 {18}	—	18 {19.2}
Tx–Rx Isolation (dB)	5	—	—	36.6 {45.5}
Size (mm×mm)	6.3×4.3	3.2×2.5	5×3.5	4.9×3.4
Technology	250 nm GaN/SiC	100 nm GaN/Si	150 nm GaN/SiC	150 nm GaN/SiC

[a] The parameters listed denote the minimum values within the published bandwidth, with the exception of "Rx NF" and "Tx P_{DC}" which indicate the maximum values. The typical or average values across the band are shown inside curly brackets. Symbol "∼" indicates an estimate from reported graphs.
[b] On-wafer measurements for all metrics, excepting the Rx OP1dB and Tx–Rx isolation which are measured on jig. Tx data for an input power of 19 dBm.

IV. CONCLUSION

A wideband 6–18-GHz GaN-on-SiC MMIC has been presented, integrating high-power and low-noise amplification, along with Tx–Rx switching, within a single-chip solution. Conceived as a fully integrated frontend from the start, the design followed a top-down approach, where the HPA, LNA, and switch were co-designed together, so that critical system-level challenges—such as EM interactions between circuits, non-50-Ω impedance matching at the interfaces, or floorplan design—could be addressed directly at the die level. This methodology led to a successful first-pass implementation, delivering balanced RF performance across all Tx and Rx metrics over the full 3:1 target bandwidth.

On-wafer measurements demonstrate competitive performance compared with the reported literature detailed in Table III. Notably, this work exhibits an average output power of 39.8 dBm (9.5 W), exceeding 37.5 dBm (5.6 W) across the entire target bandwidth. This represents an improvement of 4.7 dB over a previous design reported by the same research group [10]. While the Tx efficiency is lower than in [10], this reduction is attributed to the addition of a protection polymer film for low-cost encapsulation, which also contributes to a slight degradation of the Rx NF. Comparative analysis with other documented works [2], [4] reveals a similar output power in Tx mode, but a significantly higher efficiency and gain in this design. Furthermore, the prototypes exhibit a remarkable sensitivity for the Rx mode, with NF below 3.3 dB over the entire band (average of 3 dB), representing the lowest reported NF value among comparable fully monolithic GaN frontends.

These results confirm the suitability of the proposed T/R MMIC for integration into broadband phased-array systems, offering a well-balanced combination of output power,

efficiency, sensitivity, and compactness. Beyond on-wafer characterization, the MMIC prototypes were also assembled and tested on a custom PCB, enabling CW testing under controlled thermal conditions. The on-jig measurements closely follow the trends observed on-wafer, with moderate performance degradation attributed to assemblage parasitics and thermal stress associated with CW operation. Taken together, the obtained results validate the system-level co-design approach and position this work at the state of the art in broadband SCFE MMIC design, while also highlighting the competitiveness of European GaN technology.

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Views and opinions expressed are those of the authors only and do not necessarily reflect those of the granting authorities.

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